Pin Configuration

Pin Name	Function
A0 - A16	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

FLATPACK
Top View

A16	1		32	VCC
A15	2		31	NC
A12	3		30	$\overline{WE}$
A7	4		29	A14
A6	5		28	A13
NC	6		27	A8
A5	7		26	A9
A4	8		25	A11
A3	9		24	$\overline{OE}$
A2	10		23	A10
A1	11		22	$\overline{CE}$
A0	12		21	I/O7
I/O0	13		20	I/O6
I/O1	14		19	I/O5
I/O2	15		18	I/O4
GND	16		17	I/O3
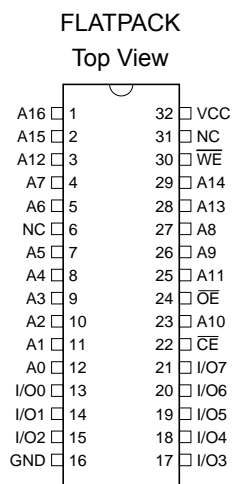
Block Diagram
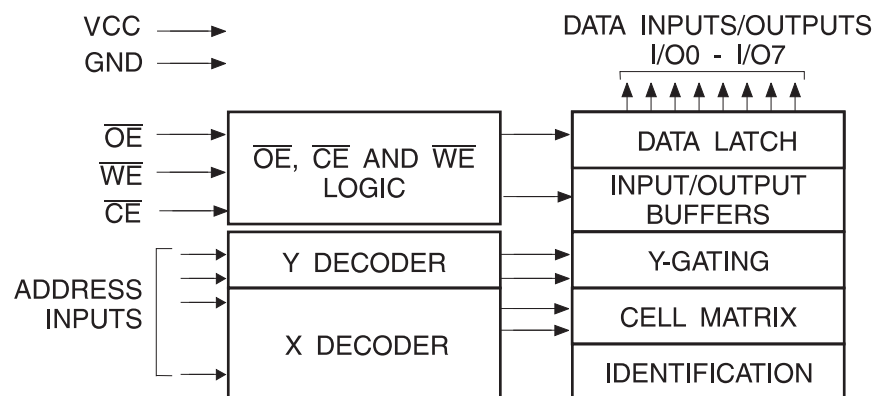
AT28C010-12DK

Device Operation

- **READ:** The AT28C010-12DK is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention in their system.

- **BYTE WRITE:** A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

- **PAGE WRITE:** The page write operation of the AT28C010-12DK allows 1 to 128 bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; the first byte written can then be followed by 1 to 127 additional bytes. Each successive byte must be written within 150 μs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded the AT28C010-12DK will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A7 - A16 inputs. For each $\overline{WE}$ high to low transition during the page write operation, A7 - A16 must be the same.

- The A0 to A6 inputs are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

- **DATA POLLING:** The AT28C010-12DK features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. $\overline{DATA}$ Polling may begin at anytime during the write cycle.

- **TOGGLE BIT:** In addition to $\overline{DATA}$ Polling the AT28C010-12DK provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

- **DATA PROTECTION:** If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Atmel has incorporated both hardware and software features that will protect the memory against inadvertent writes.
  For more information see the application note:
  http://www.atmel.com/dyn/resources/prod_documents/DOC0544.PDF

- **HARDWARE PROTECTION:** Hardware features protect against inadvertent writes to the AT28C010-12DK in the following ways: (a) V_{DD} sense – if V_{DD} is below 3.8V (typical) the write function is inhibited; (b) V_{DD} power-on delay – once V_{DD} has reached 3.8V the device will automatically time out 5 ms (typical) before allowing a write: (c) write inhibit - holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles; (d) noise filter - pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.
  SOFTWARE DATA PROTECTION: A software controlled data protection feature has been implemented on the AT28C010-12DK. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user; the AT28C010-12DK is shipped from Atmel with SDP disabled.

- SDP is enabled by the host system issuing a series of three write commands; three specific bytes of data are written to three specific addresses (refer to Software Data Protection

Algorithm). After writing the 3-byte command sequence and after t_{WC} the entire AT28C010-12DK will be protected against inadvertent write operations. It should be noted, that once protected the host may still perform a byte or page write to the AT28C010-12DK. This is done by preceding the data to be written by the same 3-byte command sequence used to enable SDP.

• Once set, SDP will remain active unless the disable command sequence is issued. Power transitions do not disable SDP and SDP will protect the AT28C010-12DK during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. The data in the enable and disable command sequences is not written to the device and the memory addresses used in the sequence may be written with data in either a byte or page write operation.

• After setting SDP, any attempt to write to the device without the 3-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, read operations will effectively be polling operations.

• **DEVICE IDENTIFICATION:** An extra 128 bytes of EEPROM memory are available to the user for device identification. By raising A9 to 12V $\pm$ 0.5V and using address locations 1FF80H to 1FFFFH the bytes may be written to or read from in the same manner as the regular memory array.

• **OPTIONAL CHIP ERASE MODE:** The entire device can be erased using a 6-byte software code. Please see Software Chip Erase application note for details.

DC and AC Operating Range

	AT28C010-12DK-12
Operating Temperature (Case)	-55°C to +125°C
V_{DD} Power Supply	5V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[1]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby	V_{IH}	X	X	High Z
Write Inhibit	X	X	V_{IH}	D_{OUT} or High Z
Write Inhibit	V_{IH}	X	X	High Z
Write Inhibit	X	V_{IL}	X	D_{OUT} or High Z
Write Inhibit	V_{IL}	V_{IL}	V_{IL}	No operation
Software Chip Clear	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Software Write Protect	V_{IL}	V_{IH}	V_{IL}	D_{IN}
High Voltage Chip Clear	V_{IL}	V_H	V_{IL}	V_{IH}
Output Disable	X	V_{IH}	X	High Z

V_{IH} = High Logic, "1" state, V_{IL} = Low Logic "0" state.

X = logic "don't care" state, High Z = high impedance state.

V_H = Chip clear voltage, D_{OUT} = Data out, and D_{IN} = Data in.

Notes: 1. Refer to AC Programming Waveforms

Electrical Characteristics

Absolute Maximum Ratings*

Temperature Under Bias .... -55°C to +125°C

Storage Temperature .... -65°C to +150°C

All Input Voltages
(including NC Pins)
with Respect to Ground ....-0.6V to +6.25V

All Output Voltages
with Respect to Ground ....-0.6V to V_{DD} + 0.6V

Voltage on $\overline{OE}$ and A9
with Respect to Ground ....-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

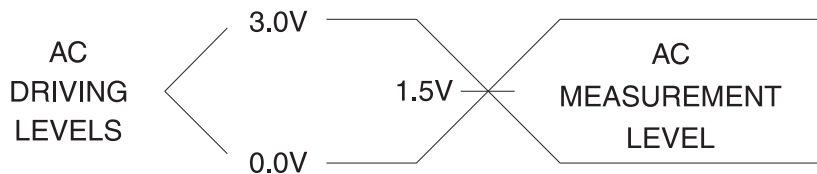| Symbol	Parameter	Condition	Min	Max	Units
I_{IL} , I_{IH}	Low Level Input Current	V_{IN} = 0V to V_{DD} +1V	-10	10	mA
I_{OZL} , I_{OZH}	Output Leakage Current	$V_{I/O}$ = 0V to V_{DD}	-10	10	mA
I_{CC3}	V_{DD} Standby Current CMOS	$\overline{CE}$ = V_{DD} - 0.3V to V_{DD} + 1V		10	mA
I_{CC2}	V_{DD} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{DD} + 1V		10	mA
I_{CC1}	V_{DD} Active Current	f = 5 MHz; I_{OUT} = 0 mA		50	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 mA	2.4		V
V_{OH2}	Output High Voltage CMOS	I_{OH} = -100 mA; V_{DD} = 4.5V	4,2		V

AC Read Characteristics

### AC Read Waveforms[1][2][3][4]
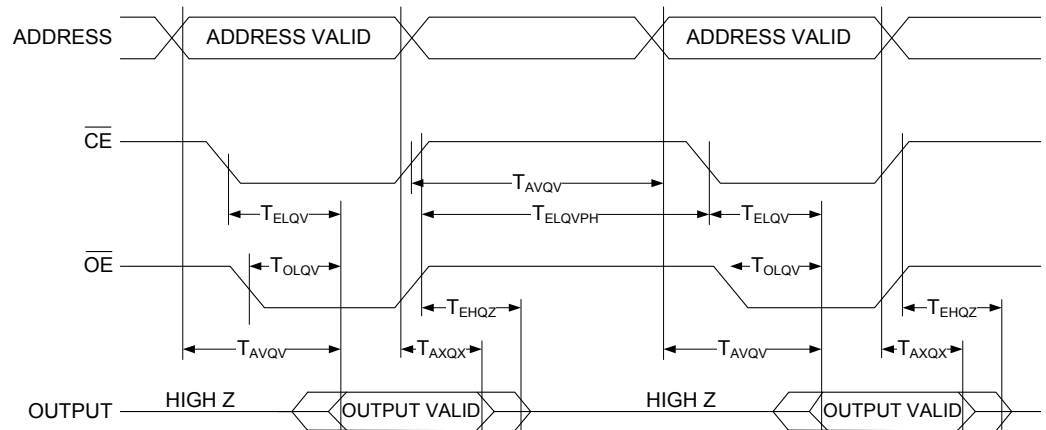
Notes: 1. $\overline{CE}$ may be delayed up to T_{AVQV} - T_{ELQV} after the address transition without impact on T_{AVQV}.

2. $\overline{OE}$ may be delayed up to T_{ELQV} - T_{OLQV} after the falling edge of $\overline{CE}$ without impact on T_{ELQV} or by T_{AVQV} - T_{OLQV} after an address change without impact in T_{AVQV}.

3. T_{EHQZ} is specified from OE or CE wichever occurs first (CL = 5 pF).

4. This parameter is characterized and is not 100% tested.

5. If $\overline{CE}$ is de-asserted, it must remain de-asserted for at least 50ns during read operations otherwise incorrect data may be read.

Input Test Waveforms and Measurement Level

Output Test Load
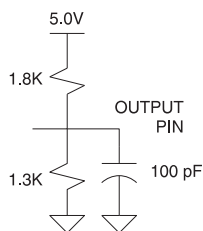
Pin Capacitance

f = 1 MHz, T = 25°C[1]

| Symbol	Typ	Max	Units	Conditions
C_{IN}	4	10	pF	$V_{IN} = 0V$
C_{OUT}	8	12	pF	$V_{OUT} = 0V$

Note: 1. This parameter is 100% characterized and is not 100% tested.
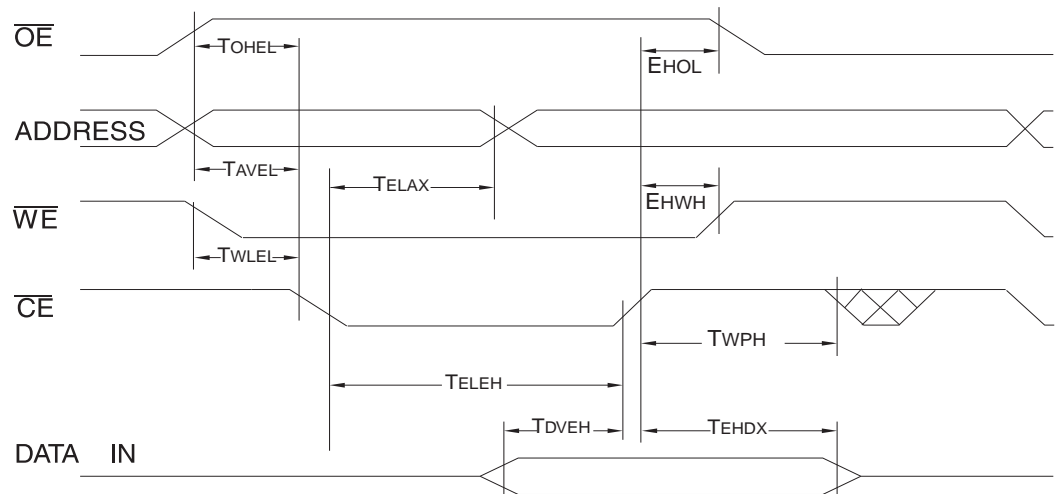
AC Write Characteristics

Symbol	Parameter	Min	Max	Units
T_{AVEL}, T_{AVWL}, T_{OHWL}, T_{OHEL},	Address, $\overline{OE}$ Set-up Time	0		ns
T_{ELAX}, T_{WLAX}	Address Hold Time	50		ns
T_{WLEL}, T_{ELWL}	Chip Select Set-up Time	0		ns
T_{EHWH}, T_{WHEH}	Chip Select Hold Time	0		ns
T_{ELEH}, T_{WLWHI}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100		ns
T_{DVEH}, T_{DVWH}	Data Set-up Time	50		ns
T_{EHDX}, T_{WHDX}, T_{WHOL}, T_{EHOL}	Data, $\overline{OE}$ Hold Time	0		ns
T_{WPH}	Write Pulse Width High	50		ns

AC Write Waveforms

$\overline{WE}$ Controlled
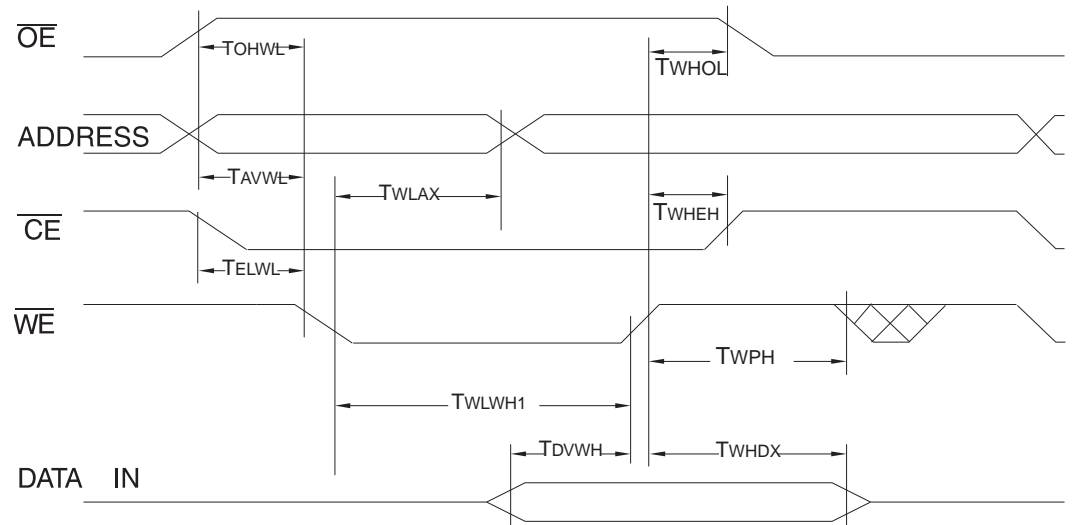
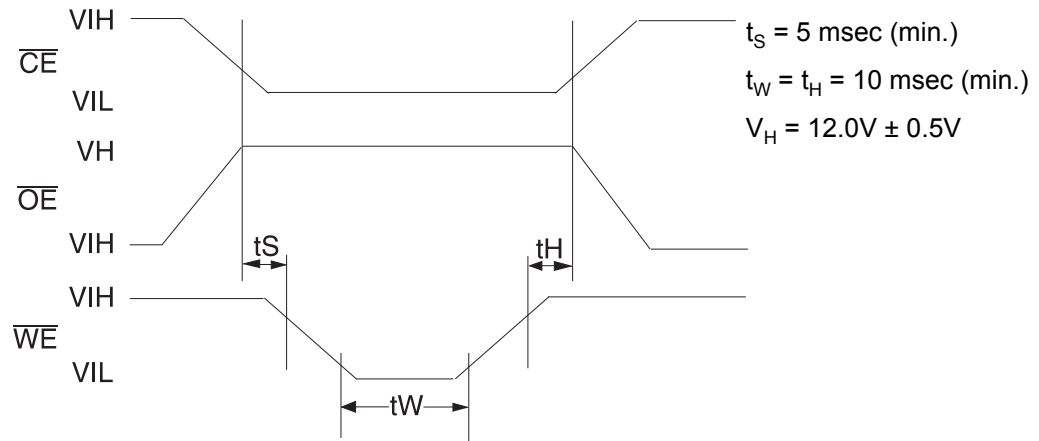### $\overline{CE}$ Controlled

Page Mode Characteristics

Symbol	Parameter	Min	Max	Units
T_{WHWL1}	Write Cycle Time		10	ms
T_{AVWL}, T_{OHWL}	Address Set-up Time, $\overline{OE}$ Set up time	0		ns
T_{WLAX}	Address Hold Time	50		ns
T_{DVWH}	Data Set-up Time	50		ns
T_{WHDX}, T_{WHOL}	Data Hold Time, $\overline{OE}$ Hold time	0		ns
T_{WLWH1}	Write Pulse Width	100		ns
T_{WHWL2}	Byte Load Cycle Time		150	ms
T_{WPH}	Write Pulse Width High	50		ns

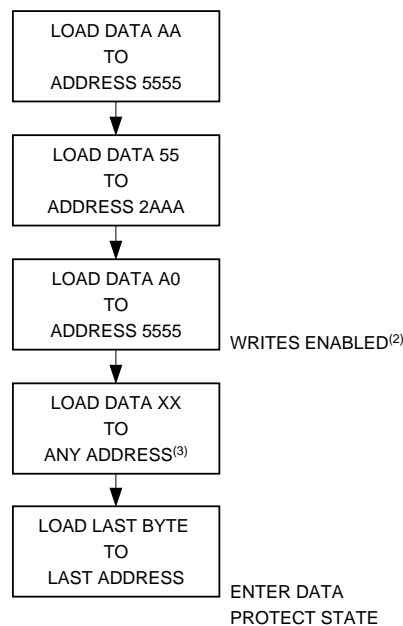## Page Mode Write Waveforms [1][2]
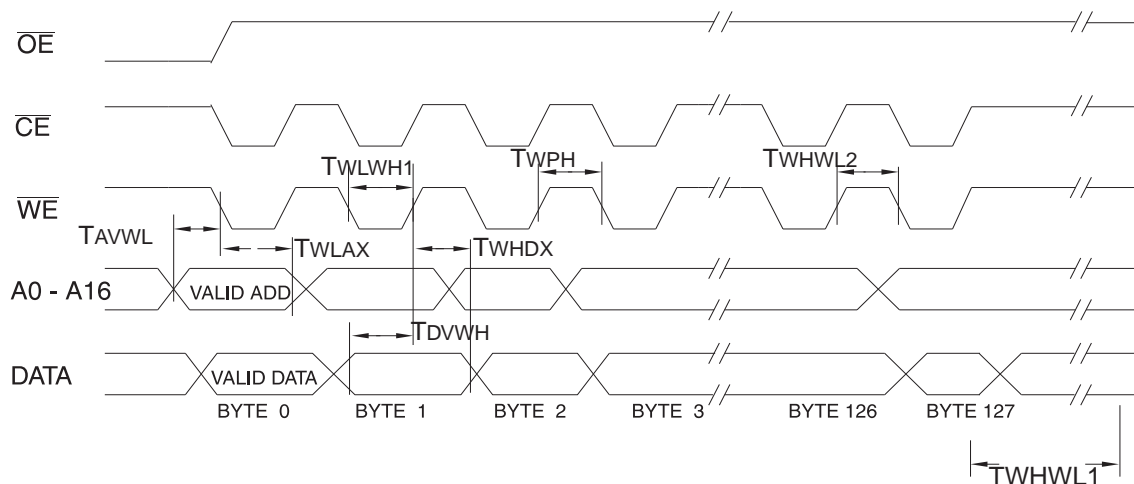
Notes: 1. A7 through A16 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
2. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

AT28C010-12DK
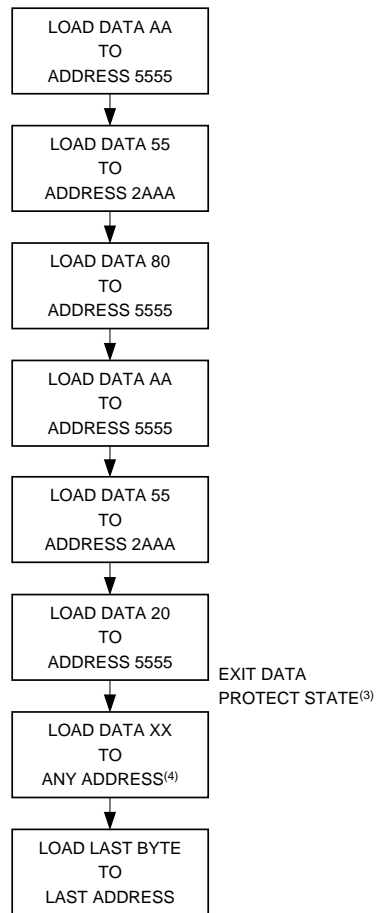
Chip Erase Waveforms

t_S = 5 msec (min.)

t_W = t_H = 10 msec (min.)

V_H = 12.0V ± 0.5V

Software Data

Figure 1. Protection Enable Algorithm[1]

LOAD DATA AA TO ADDRESS 5555

LOAD DATA 55 TO ADDRESS 2AAA

LOAD DATA A0 TO ADDRESS 5555 — WRITES ENABLED[2]

LOAD DATA XX TO ANY ADDRESS[3]

LOAD LAST BYTE TO LAST ADDRESS — ENTER DATA PROTECT STATE

Notes: 1. Data Format: I/O7 - I/O0 (Hex);
Address Format: A14 - A0 (Hex).

2. Write Protect state will be activated at end of write even if no other data is loaded.

3. 1 to 128 bytes of data are loaded.

Figure 2. Protection Disable Algorithm[1]

```
┌─────────────────┐
│   LOAD DATA AA  │
│       TO        │
│  ADDRESS 5555   │
└────────┬────────┘
         ▼
┌─────────────────┐
│   LOAD DATA 55  │
│       TO        │
│  ADDRESS 2AAA   │
└────────┬────────┘
         ▼
┌─────────────────┐
│   LOAD DATA 80  │
│       TO        │
│  ADDRESS 5555   │
└────────┬────────┘
         ▼
┌─────────────────┐
│   LOAD DATA AA  │
│       TO        │
│  ADDRESS 5555   │
└────────┬────────┘
         ▼
┌─────────────────┐
│   LOAD DATA 55  │
│       TO        │
│  ADDRESS 2AAA   │
└────────┬────────┘
         ▼
┌─────────────────┐
│   LOAD DATA 20  │
│       TO        │       EXIT DATA
│  ADDRESS 5555   │       PROTECT STATE[3]
└────────┬────────┘
         ▼
┌─────────────────┐
│   LOAD DATA XX  │
│       TO        │
│ ANY ADDRESS[4]  │
└────────┬────────┘
         ▼
┌─────────────────┐
│ LOAD LAST BYTE  │
│       TO        │
│  LAST ADDRESS   │
└─────────────────┘
```

Notes: 1. Data Format: I/O7 - I/O0 (Hex);
          Address Format: A14 - A0 (Hex).

          2. Write Protect state will be activated at end of write even if no other data is loaded.

          3. Write Protect state will be deactivated at end of write period even if no other data if loaded.

          4. 1 to 128 bytes of data are loaded.

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Software Protected Program Cycle Waveform[(1)(2)(3)]
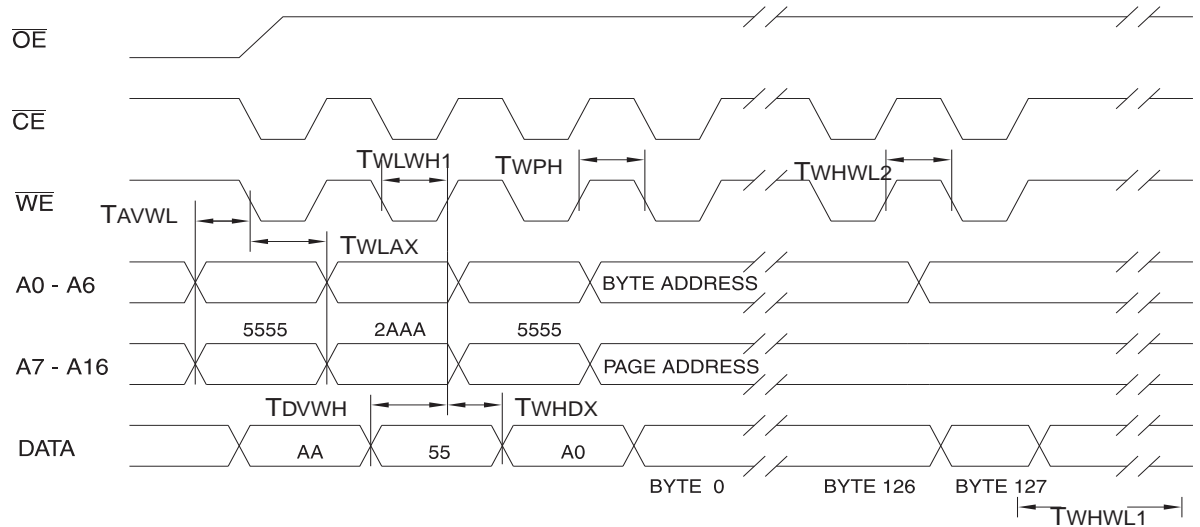
Notes: 1. A0 - A14 must conform to the addressing sequence for the first 3 bytes as shown above.
2. After the command sequence has been issued and a page write operation follows, the page address inputs (A7 - A16) must be the same for each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
3. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Data Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
T_{WHDX}	Data Hold Time	10			ns
T_{WHOL}	$\overline{OE}$ Hold Time	10			ns
T_{OLQV}	$\overline{OE}$ Access Time[2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See AC Read Characteristics.

Data Polling Waveforms
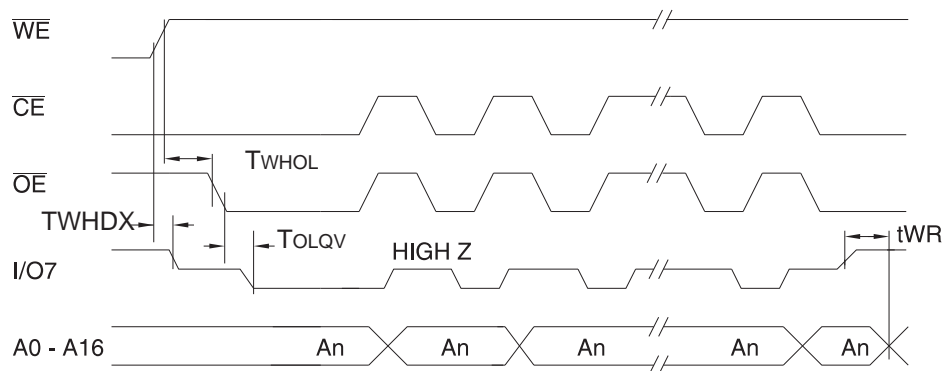
Toggle Bit Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
T_{WHDX}	Data Hold Time	10			ns
T_{WHOL}	$\overline{OE}$ Hold Time	10			ns
T_{OLQV}	$\overline{OE}$ Access Time[2]				ns
T_{OEHP}	$\overline{OE}$ High Pulse	150			ns
T_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See AC Read Characteristics.

Toggle Bit Waveforms[1][2][3]
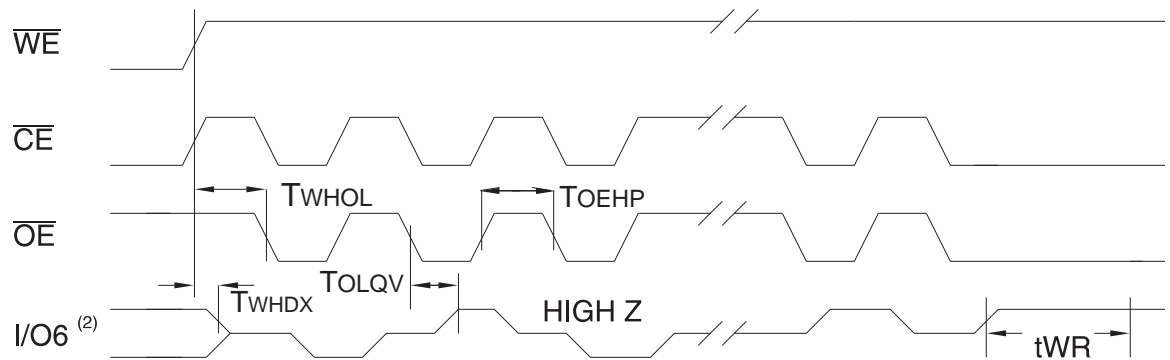
Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any addres location may be used but the address should not vary.

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Ordering Information

t$_{ACC}$ (ns)	I$_{CC}$ (mA)		Ordering Code	Package	Packing
	Active	**Standby**			
120	50	10	AT28C010-12DK-E	FP32.4	Engineering Samples
			AT28C010-12DK-MQ		Military Level B
			AT28C010-12DK-SV		Space Level B

Packaging Information

FP32.435   32F, 32-Lead, Non-Windowed, Ceramic Bottom
Brazed Flat Package (Flatpack)
Dimensions in Inches and Millimeters
MIL-STD-1835 F-18 CONFIG B
JEDEC OUTLINE MO-115
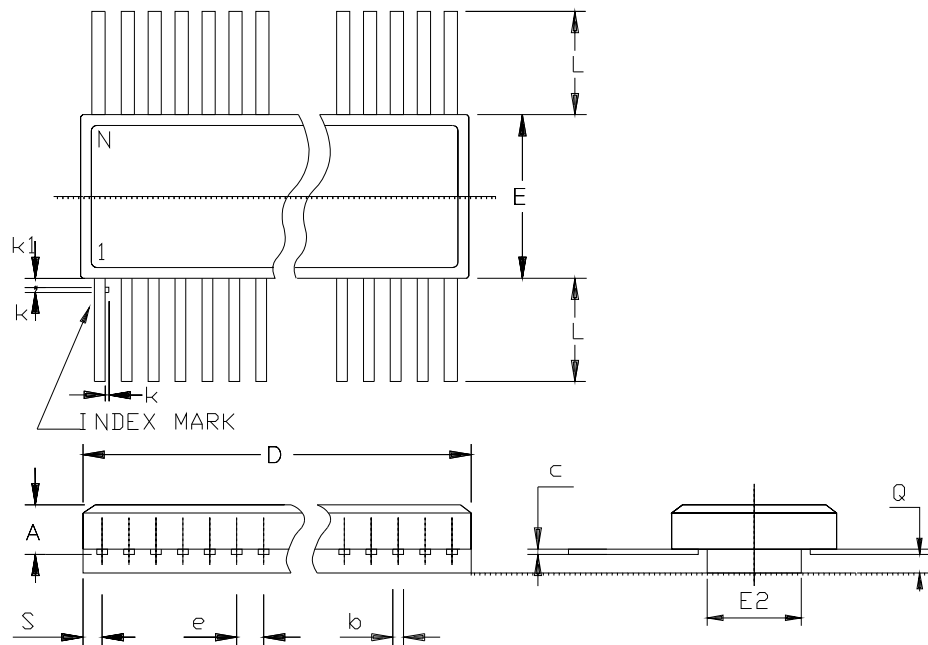
	MM Min	MM Max	INCH Min	INCH Max
A	1.78	2.72	.070	.107
b	0.38	0.48	.015	.019
c	0.076	0.15	.003	.007
D	20.62	21.03	.812	.828
E	10.92	11.18	.430	.440
E2	8.46	8.82	.333	.347
k	0.20	0.38	.008	.015
k1	0.63 BSC		.025 BSC	
e	1.27 BSC		.050 BSC	
L	6.65	8.20	.262	.323
Q	0.66	----	.026	----
S	0.13	----	.005	.045
N	32		32	

Document Revision History

Changes from Rev. C to Rev. D

Page 7 : updated to be in compliance with military version of the datasheet which implements a condition on the CE Pulse High Time to avoid bad output data when a very fast read enable is used by application.

Changes from Rev. D to Rev. E

Page 1 :
- "Preliminary" status suppressed
- Endurance : Read Cycles replaced by Read/Modify Write Cycles @ Ground Level

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