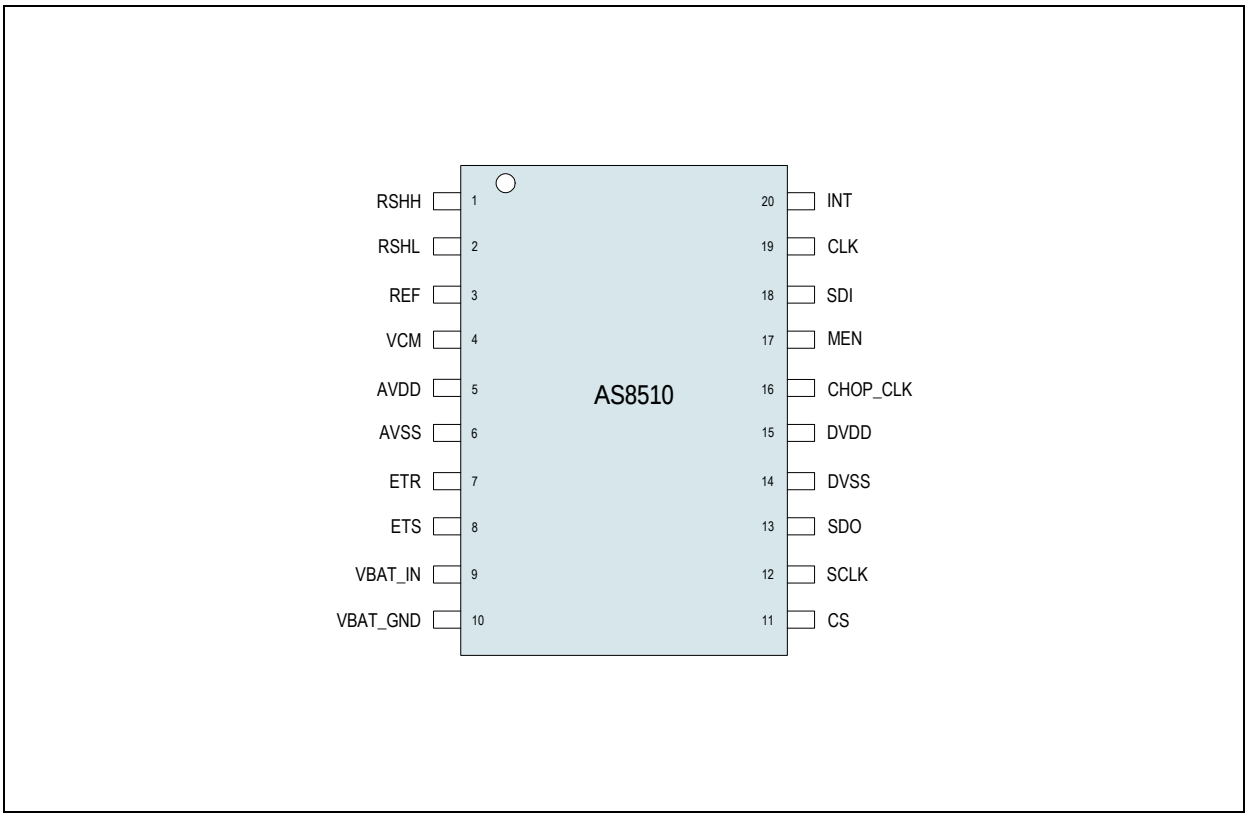
Contents

4 Pin Assignments

Figure 2. Pin Assignments (Top View)



4.1 Pin Descriptions

Table 1. Pin Descriptions

Pin Number	Pin Name	Pin Type	Description
1	RSHH	Analog input	Positive Differential input for current channel
2	RSHL		Negative differential input for current channel
3	REF	Analog output	Internal reference voltage to sigma-delta ADC; connect 100nF to AVSS from this pin.
4	VCM		Common Mode voltage to the internal measurement path; connect 100nF to AVSS from this pin.
5	AVDD	Supply pad	+3.3V Analog Power-supply
6	AVSS		0V Power-supply analog
7	ETR	Analog input	Voltage channel single ended input
8	ETS		
9	VBAT_IN		Battery voltage (high) input
10	VBAT_GND		Battery voltage (low) input
11	CS	Digital input with pull-up	Chip select with an internal pull-up resistor (SPI Interface)
12	SCLK	Digital input	Clock signal (SPI Interface)
13	SDO	Digital output	Serial Data Input (SPI Interface)

Table 1. Pin Descriptions

Pin Number	Pin Name	Pin Type	Description
14	DVSS	Supply pad	0V Digital Ground
15	DVDD		+3.3V Digital Supply
16	CHOP_CLK	Digital output	Chop Clock used in High side measurements to synchronize external chopper. (As an example, when AS8525 is used to condition the input signal to the input range of AS8510, the chop clock is used by AS8525.)
17	MEN		Digital output issued during the Standby Mode (SBM) to signal the short duration of data sampling. This signal is useful in the case of a High Side Measurement application. (For example: This signal is used by AS8525 device to wake-up and enable the measurement path.)
18	SDI	Digital input	Data signal (SPI Interface)
19	CLK	Digital I/O	By default this pin is the internal clock output which can be used by a Microcontroller. The internal clock may also be disabled as an output by programming Register 08. To use an external Clock, Register 08 has to be programmed.
20	INT	Digital output	Active High Interrupt to indicate data is ready

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 7 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Notes
Electrical Parameters				
DC supply voltage (AVDD and DVDD)	-0.3	5	V	
Input voltage (V_{IN})	-0.3	AVDD + 0.3 DVDD + 0.3	V	
Input current (latchup immunity) (I_{SCR})	-100	100	mA	AEC - Q100 - 004
Electrostatic Discharge				
Electrostatic discharge (ESD) all pins		±2	kV	AEC - Q100 - 002
Continuous Power Dissipation				
Total power dissipation (all supplies and outputs) (P_t)		50	mW	SSOP20 in still air, soldered on JEDEC standard board @ 125º ambient, static operation with no time limit
Temperature Ranges and Storage Conditions				
Storage temperature (T_{STRG})	-50	125	ºC	
Junction temperature (T_J)		130	ºC	
Thermal resistance (R_{thJC})		80	K/W	JEDEC standard test board, 0 air velocity
Package body temperature (T_{BODY})		260	ºC	Norm: IPC/JEDEC J-STD-020[1]
Moisture Sensitive level (MSL)	3			
Humidity non-condensing	5	85	%	

1. The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices”.

6 Electrical Characteristics

6.1 Operating Conditions

Table 3. Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Units
AVDD	Positive analog supply voltage		3.0	3.6	V
AVSS	0V Ground		0	0	V
A - D	Difference in analog and digital supplies			0.1	V
DVDD	Positive digital supply		2.97	3.63	V
DVSS	0V Digital Ground		0	0	V
T_{AMB}	Ambient temperature		-40	125	ºC
I_{SUPP}	Supply current			5.5	mA
f_{CLK}	System clock frequency[1]			4.096	MHz

1. Nominal clock frequency from external or internal oscillator.

6.2 DC/AC Characteristics for Digital Inputs and Outputs

All pull-up and pull-down have been implemented with active devices. SDO has been measured with 10pF load.

Table 4. INT

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LEAK}	Tri-state leakage current		-1		+1	µA
V_{OH}	High level output voltage		2.5			V
V_{OL}	Low level output voltage				0.4	V
I_O	Output Current				4	mA

Table 5. CS Input

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High level input voltage		2.0			V
V_{IL}	Low level input voltage				0.8	V
I_{LEAK}	Input leakage current		-1		+1	µA
Ipu	Pull up current	CS pulled to DV_{DD} = 3.3V	-150		-15	µA

Table 6. SDI

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High level input voltage		2.0			V
V_{IL}	Low level input voltage				0.8	V
I_{LEAK}	Input leakage current		-1		+1	µA

Table 7. SDO Output

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	High level output voltage	Isource = 8mA	2.5			V
V_{OL}	Low level output voltage	Isink = 8mA			0.4	V
I_O	Output Current				8	mA

Table 8. CHOP_CLK Output

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	High level output voltage		2.5			V
V_{OL}	Low level output voltage				0.4	V
I_O	Output Current				4	mA

Table 9. CLK I/O with Input Schmitt Trigger and Output Buffer

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High level input voltage	DV_{DD} = 3.3V	2.4			V
V_{IL}	Low level input voltage	DV_{DD} = 3.3V			1.0	V
I_{LEAK}	Input leakage current		-1		+1	µA
I_{PD}	Pull down current	CLK pulled to DVSS	10		100	µA
I_O	Output Current				4	mA
V_{OH}	High level output voltage		2.5			V
V_{OL}	Low level output voltage				0.4	V

Table 10. SCLK with Input Schmitt Trigger

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High level input voltage	DV_{DD} = 3.3V	2.4			V
V_{IL}	Low level input voltage	DV_{DD} = 3.3V			1.0	V
I_{LEAK}	Input leakage current		-1		+1	µA

Table 11. MEN Output

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	High level output voltage		2.5			V
V_{OL}	Low level output voltage				0.4	V
I_O	Output Current				2	mA

6.3 Detailed System and Block Specifications

6.3.1 Electrical System Specifications

Table 12. Electrical System Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes
IDD_{NOM}	Current consumption normal mode		3	5.5	mA	
IDD_{SBM}	Current consumption standby mode		40		µA	Average of NORMAL Mode Power consumption over a period of 10sec when the device is in STANDBY Mode

6.4 Current Measurement Ranges (across 100µOhm shunt resistor)

Table 13. Current Measurement Ranges

Symbol	Parameter	I_{max} [A]	V_{sh} [mV]	PGA Gain Nominal	Data Rate (f_{OUT})	V_{INADC} [1] [mV]	PSR [2] [dB]
I70	Input current range of 70A in NOM	±77	±8.1	100	@ 1 kHz	890	60
I200	Input current range of 200A in NOM	±235	±24.7	40	@ 1 kHz	1088	60
I400	Input current range of 400A in NOM	±400	±42	25	@ 1 kHz	1137	60
I1500	Input current range of 1500A in NOM	+2076/-1523	+218/-160	5	@ 1 kHz	1204	60

1. $V_{INADC} = V_{sh} * Gain$, gain deviations to be considered according to Table 15 and Table 16.
2. AVDD, DVDD of 3.3V with ±5% variation.

The maximum current range can be calculated by the equation:

$I_{max} = (VREF_{min} – V_{OSDRIFT}*Gn*e)/(Gn *e*R_{SHUNT})$

Where

$VREF_{min}$ is minimum ADC reference voltage for the anticipated temperature range e.g.1220mV

$V_{OSDRIFT}$ is the maximum input referred PGA offset (e.g. 3 mV)

Gn is the nominal gain as selected (G1 to G4)

e is maximum gain tolerance (1,1)

R_{SHUNT} is the maximum shunt resistance

Exceeding this maximum current range will lead first to non-linearity and finally to clamping.

Note: The Data Rate at the output can be calculated according to the formula:

fsout=2*fchop /R2 (R2 is down sampling ratio taking values 1, 2, 4 up to 32768 as powers of 2)

Table 14. Valid Combinations of the Chopper Clock, Oversampling Clock and Decimation Ratios

Over Sampling Frequency	Chopper Frequency	Decimation Ratio
1.024MHz	2kHz	64
2.048MHz	2kHz	64
2.048MHz	2kHz	128
2.048MHz	4kHz	64

6.4.1 Differential Input Amplifier for Current Channel

Table 15. Differential Input Amplifier for Current Channel

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IN_AMP}	Input voltage range	RSHH and RSHL	-160		+160	mV
I_{IN_AMP}	Input current [1, 11]	RSHH and RSHL@ +160mV input voltage at 125ºC with PGA	-50	2	50	nA
ICM	Absolute input voltage range [2]			-160 +300		mV
G = G1	Gain1 [3, 4, 9]	I10		100		
G = G2	Gain2 [3, 4, 9]	I200		40		
G = G3	Gain3 [3, 4, 9]	I400		25		
G = G4	Gain4 [3, 4, 9]	I1500		5		
e	Gain deviation	i = 1, 2, 3, 4	0.9 * Gi		1.1 * Gi	
f_{P_AMP}	Pole frequency [4, 5]		15			kHz
εT1	Gain drift with temperature [6]	-20ºC to +65ºC Gain 5, 25, referenced to room temperature			±0.3	%
V_{os}	Input referred offset [7, 10]	@65ºC		350	2700	µV
		After trim at -20ºC			420	µV
V_{os_ch}	Measurement path offset [7, 10]	Chopping enabled		0		LSB
V_{Ndin}	Noise density [4, 8]			25		nV/√Hz
THD	Total harmonic distortion	For 150 Hz input signal		70		dB

Notes:

1. Leakage test accuracy is limited by tester resource accuracy and tester hardware.
2. For gain 100 PGA input common mode is 0V and the minimum supply is 3.15V.
3. The measurement ranges are referred only by the gain of input amplifier, while other parameters such as bandwidth etc. are programmed independently.
4. This parameter is not measured directly in production. It is measured indirectly via gain measurements of the whole path. It is guaranteed by design.
5. Pole frequency of input amplifier changes with GAIN. The number is valid for the gain at G1, while the bandwidth will be higher for other ranges. This parameter is not measured in production.
6. Based on device evaluation. Not tested.
7. These offsets are cancelled if chopping enabled (default).
8. Noise density calculated by taking system bandwidth as 150Hz.
9. Refer to Measurement Ranges shown in Table 13.
10. No impact on the measurement path. If the chopping is enabled, both the offset and offset drift will be eliminated.
11. For negative input voltages up to -160mV below ground, Input leakage is typically -20nA @ 65ºC due to forward conductance of protection diode.

6.4.2 Differential Input Amplifier for Voltage Channel

Table 16. Differential Input Amplifier for Voltage Channel

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IN_AMP}	Input voltage range [1, 10]		-160		+160	mV
I_{IN_AMP}	Input current [2, 10]	VBAT_IN, ETR, ETS @ +160mV input voltage at 125ºC with PGA	-50	2	50	nA
ICM	Absolute input voltage range [3]			-160 +300		mV
G = G1	Gain1 [4, 5]			100		
G = G2	Gain2 [4, 5]			40		
G = G3	Gain3 [4, 5]			25		
G = G4	Gain4 [4, 5]			5		
e	Gain deviation	i = 1, 2, 3, 4	0.9 * Gi		1.1 * Gi	
f_{P_AMP}	Pole frequency [5, 6]		15			kHz
V_{NDIN}	Noise density [5, 7]			25		nV/√Hz
THD	Total harmonic distortion	For 150Hz input signal		70		dB
$\varepsilon T1$	Gain drift with temperature [8]	-20ºC to +65ºC Gain 5, 25, referenced to room temperature			±0.3	%
V_{OS}	Input referred offset [9]	After trim at @ -20ºC			420	µV
		@ 65ºC		350	2700	µV
V_{os_ch}	Measurement path offset [9]	Chopping enabled		0		LSB

Notes:

1. Input for the voltage channel can be as high as 1220mV, in this high input case PGA will be bypassed.
2. Leakage test accuracy is limited by tester resource accuracy and tester hardware, especially at low temperatures due to condensing moisture.
3. For gain 100 PGA input common mode is 0V and the minimum supply is 3.15V.
4. The measurement ranges are referred only by the gain of input amplifier, while other parameters such as bandwidth etc. are programmed independently.
5. This parameter is not measured directly in production. It is measured indirectly via gain measurements of the whole path. It is guaranteed by design.
6. Pole frequency of input amplifier changes with changing the GAIN. The number is valid for the gain at G1, while the bandwidth will be higher for other ranges. This parameter is not measured in production.
7. Noise density calculated by taking system bandwidth as 150Hz.
8. Based on device evaluation. Not tested.
9. No impact on the measurement path. If the chopping is enabled, both the offset and offset drift will be eliminated.
10. For negative input voltages up to -160mV below ground, Input leakage is typically -20nA @ 65ºC due to forward conductance of protection diode.

6.4.3 Sigma Delta Analog to Digital Converter

Table 17. Sigma Delta Analog to Digital Converter

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VREF	Reference voltage [6]			1.225		V
V_{INADC}	Input range [1]	At V_{ref} = 1.22V	0		±1.22	V
R1	Oversampling ratio/Decimation Ratio [2]		64	128	128	
f_{ovs}	Oversampling frequency [3]			1024/ 2048		kHz
RES	Number of bits				16	bits
BW	Bandwidth [4]		1		500	Hz
S/N	Signal to noise ratio [5]			90		dB

Notes:

1. Production test at ±800mV. Maximum VIN can be 1.22V with VREF=1.225V.
2. Programmable. It is defined with respect to the first decimator in the ΣΔ ADC.
3. Programmable: Internal clock is 1024/2048 kHz; external clock max is 8192 kHz.
4. Dependent on fovs, R1 and R2. The bandwidth is calculated according to the formula: BW=fovs/(2*R1*R2); the sampling frequency at the output of the A/D converter is 2*BW.
5. Defined at maximum input signal, BW=500 Hz (1Hz to 500 Hz), fovs=1024 kHz, R1=64, fchop=2 kHz and R2=2.
6. Reference voltage might be forced from external.

6.4.4 Bandgap Reference Voltage

Table 18. Bandgap Reference Voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{REFTRIM}$	Reference Voltage after trim [1, 2]	Trim at 65ºC		1.225		V
V_{REFACC}	Reference Voltage Initial Accuracy [1, 2]	At 65ºC			±3.5	mV
$V_{REFDRIFT}$	Reference Voltage Temperature drift	Temperature range -20 to 65 ºC			±0.4	%
		Temperature range -40 to 125 ºC		+0.4/ -0.6		%
$PSRR_{REF}$	PSR @ dc			80		dB
SUT_{AVDD}	Start Up Time with supply ramp [3]			5		ms
SUT_{PD}	Start Up Time from power down [3]				1	ms
R_{NDVREF}	Output resistance of band gap			500	1000	Ω
V_{NDVREF}	Bandgap reference thermal noise density [3]				300	nV/√Hz
CL_{VREF}	Output Capacitor (Ceramic)			100		nF
ESR_{VREF}			0.02		1	Ω

Notes:

1. Accuracy at 65ºC.
2. No DC current is allowed from this pin.
3. This is a design parameter and not production tested.

6.4.5 Internal (Programmable) Current Source for External Temperature Measurement

Table 19. External Temperature Measurement

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CURON}	5-bit current source enabled [1]	5-bit programmable current source	0	270	320	µA
I_{CUROFF}	5-bit current source disabled	Limited by leakage		10		nA
T_{K_CS}	Temperature coefficient of current source [2]			1000		ppm / °K
V_{MAXETR}	Voltage on pin ETR [3]				1000/G	mV
$V_{MAXETRMOD}$	Max voltage on pin ETR when PGA is bypassed [4]				1.22	V
V_{MAXETS}	Voltage on pin ETS for resistor sensor [3]				1000/G	V
$V_{MAXETSMOD}$	Max. Voltage on pin ETS when PGA is bypassed [5]				1.22	V

Notes:

1. Current value can be programmed in steps of 8µA from 0 to 256µA with a process error of 30%.
2. Temperature coefficient is not important since external temperature measurement is a 2 step measurement. The value specified is guaranteed by design and will not be tested in production.
3. Maximum voltage on pin ETR (reference) can be calculated by given formula, where G is the gain of PGA (G=100).
4. Maximum voltage on pin ETR, if PGA is bypassed.
5. Maximum voltage on pin ETS, if PGA is bypassed.

6.4.6 CMREF Circuit (VCM)

Table 20. CMREF Circuit

Symbol	Parameter	Min	Typ	Max	Units
V_{VCM}	Output voltage	1.6	1.7	1.8	V
C_L	Load capacitance		100		nF

6.4.7 Internal AVDD Power-on Reset

Table 21. Internal AVDD Power-on Reset

Symbol	Parameter	Min	Typ	Max	Units
V_{PORHIA}	Power On Reset Threshold	2.2	2.4	2.6	V
t_{PORA}	POR time - The duration from Power ON till the time, internal Power On Reset signal goes HIGH[1]	1			µs
I_{PORA}	Current consumption in POR block[2]		1.5		µA

1. POR pulse is always longer than t_{PORA} whatever the slope of the supply.
2. I_{PORA} can not be switched off.

6.4.8 Internal DVDD Power-on Reset

Table 22. Internal DVDD Power-on Reset

Symbol	Parameter	Min	Typ	Max	Units
V_{PORHID}	Power On Reset Threshold	2.2	2.4	2.7	V
V_{HYST}	Hysteresis[1]	0.2	0.25	0.4	V
t_{PORD}	POR time - The duration from Power ON till the time, internal Power On Reset signal goes HIGH[2]	1			µs
I_{PORD}	Current[3]		1.5		µA

1. $V_{PORLO} = V_{PORHI} - V_{HYST}$ where V_{PORLO} is the lower threshold of POR.
2. $V_{PORLO} = V_{PORHI} - V_{HYST}$ where V_{PORLO} is the lower threshold of POR.
3. I_{PORD} can not be switched off.

6.4.9 Low Speed Oscillator

Table 23. Low Speed Oscillator

Symbol	Parameter	Min	Typ	Max	Units
f_{LS}	Frequency		262.144		kHz
f_{LS_ACC}	Accuracy		± 7		%
I_{LS}	Supply current		5		µA

6.4.10 High Speed Oscillator

Table 24. High Speed Oscillator

Symbol	Parameter	Min	Typ	Max	Units
f_{HS}	Frequency		4.096		MHz
f_{HSACC}	Accuracy [1, 2]		±4		%
I_{HS}	Supply current		300		µA

Notes:

1. Accuracy after trimming.
2. Accuracy for limited temperature range of -20 to 65 °C.

6.4.11 External Clock

Table 25. External Clock

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{CLKEXT}	Clock frequency			2048/ 4096/ 8192		kHz
DIV_{CLKEXT}	Clock division factor	to be programmed in Register 08 CLK_REG through the serial bus SPI.		2/4/8		
DC_{CLKEXT}	Duty Cycle of external clock		40		60	%

6.4.12 Internal Temperature Sensor

Table 26. Internal Temperature Sensor

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{INTRNG}	Temperature sensor range		-40		125	°C
ΔT_{IN}	Temperature measurement accuracy			3		°C
T_{INTSLP}	Temperature sensor slope	Guaranteed by design; at PGA gain 5 which is the recommended Gain for internal temperature measurement.		27		Digits/C
TINT65G5	Temperature sensor output at gain 5		40660	41807	43012	Digits

6.5 System Specifications

Table 27. System Specifications

Symbol	Parameter	Min	Typ	Max	Units
I_S	Channel to channel isolation [1]			-90	dB
At	Difference in channel to channel attenuation @600Hz [1, 2]			3	dB
Ph	Difference in phase shift between the two channels @600Hz [1, 2]			5	Deg

System Measurement Error Budget for Voltage and Current Channel.

Temperature Range: -20ºC to +65ºC; Output data rate is 1kHz, V_{CC} = 3.3V, chopping enabled.

Table 28. System Measurement Error Budget for Gains 5 and 25

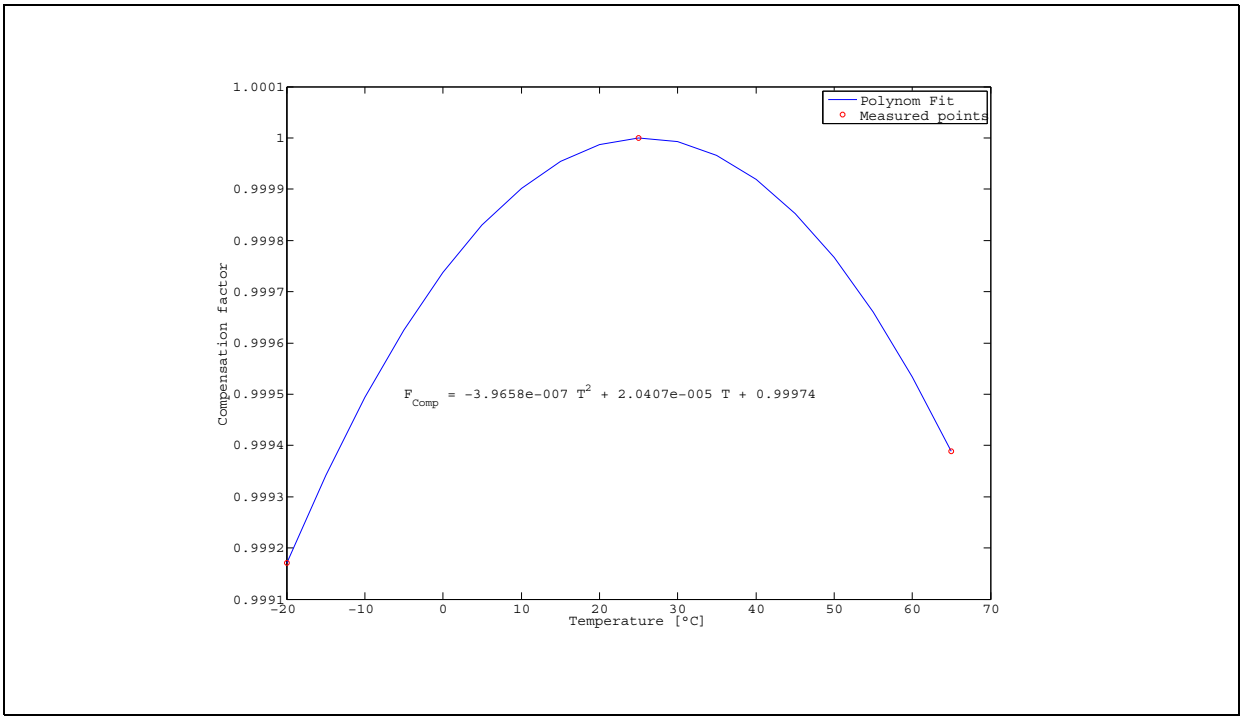
Symbol	Parameter	Conditions	Min	Typ	Max	Units
Err	System measurement error [3, 4]			±0.5	±0.8	%
	Voltage channel signal path measurement error [5]				±0.5	
	Measurement error due to PGA gain drift	From device evaluation			±0.3	%
	Measurement error due to V_{REF} drift				±0.4	%
	Measurement error due to non-linearity of PGA	Tested by distortion measurements			±0.025	%

Notes:

1. These specifications are defined by taking one channel as reference and measured on the other channel.
2. Guaranteed by design.
3. System measurement error due to noise, individual block parameter drifts and non linearity. Based on evaluation, not tested.
4. System error due to offset is neglected because of chopper architecture.
5. PGA is by-passed.

System Error Compensation Function: For battery voltage measurement it is recommended to by-pass the PGA. This eliminates PGA gain drift as an error source, thus error for the VBAT/VBAT_GND differential signal path is determined by VREF drift with temperature. The typical characteristic of VREF versus temperature extracted from 3 production lots is shown in Figure 3. This function could be used to improve accuracy by an error correction method utilizing the internal temperature sensor. In this case ADC raw data readings need to be corrected with a temperature dependent factor by the software in the external micro controller. This factor is given by a generic compensation function and can be applied to all IC's because VREF is production trimmed to minimize linear coefficient of VREF over temperature.

Figure 3. Reference Error Compensation Function



Generic compensation factor the ADC output need to be multiplied with:

F_{comp} = (A*T^2 + B*T + C)

Where:

F_{comp} is the compensation factor for VREF drift over temperature normalized to 1 at 25°C

T is Temperature reading from calibrated internal temperature sensor in [°C]

A: -4E-7

B: 2E-5

C: 0,9997

The compensated ADC value = raw ADC value * F_{comp}

If PGA is by-passed and an external precision reference is applied, the signal path measurement error is basically determined by the drift due to temperature and ageing of the external reference.

Current channel error contributions for a single temperature end of line calibrated system are shunt resistance, PGA gain and VREF changes with temperature. The drift of a shunt resistor made from Manganin alloy and VREF drift with temperature are non-linear and show 2nd order curvature in same direction and similar relative magnitude. Thus shunt error is already reduced by the generic VREF(T) curvature (see Figure 3) if thermally coupled to the AS8510. Over all error can be further reduced by an error correction method in external micro controller by matching typical VREF(T) curvature to R_{shunt} (T) curvature with the help of the internal temperature sensor.

Temperature sensor system considerations: Internal temperature sensor can be used to measure the ambient temperature because there is just 13 mW of AS8510 power dissipation in normal mode. This results in internal self-heating of less than 1°C.

7 Detailed Description

The AS8510 consists of two independent high resolution 16-bit SD analog to digital conversion channels. The measurement path of these two channels integrates a programmable gain amplifier, chopper and de-chopper, sigma-delta modulator, decimator and a digital filter for simultaneous measurement of Current and Voltage/Temperature.

The two measurement channels, namely the Current and Voltage/Temperature measurement channels have identical data path.

The input signal is amplified in the Programmable Gain Amplifier (PGA) with any of the selected gains of 1, 5, 25, 40 and 100 facilitating measurement of a wide range of Current, voltage and temperature levels. Gain Settings for different input ranges and any associated restrictions are explained in the Table 13.

Offset in the measurement path is minimized with the use of a chopper and a de-chopper at appropriate stages in the data path. By default the chopper/de-chopper is ON in the measurement path. It may be disabled by programming the appropriate register.

The amplified input signal is converted into a single-bit pulse-density modulated stream by the Σ-Δ Modulator. A decimator acting as a low-pass filter filters out the quantization noise and generates 16-bit data corresponding to the input signal. The decimation ratios of 64, 128 may be selected in the first filter stage. For reducing data rate further, the second stage decimation can be used.

An optional FIR Filter is provided to offer matched low pass filter response typically required in lead acid battery sensor systems.

7.1 Current Measurement Channel

The voltage across a Shunt Resistor, connected in series with the Battery negative terminal, forms the input signal to the Current Measurement channel. RSHH and RSHL are the Current measurement input pins. Offset in the input signal is nullified with the use of a chopper and a de-chopper at appropriate stages in the data path. The programmable gain amplifier in the data path with programmable settings of 1, 5, 25, 40 and 100 enables measurement of current ranges from ±1A to ±1500A. The sampled input signal is converted into a single-bit pulse-density modulated stream by the Σ-Δ Modulator. A decimator acting as a low-pass filter filters out the quantization noise and generates 16-bit data equivalent to the input current signal. The programmable input sampling rate and the decimation ratio determine the output data rates. The data path can be programmed to provide 1Hz to 2 kHz rates in the various modes available. An optional FIR filter is provided to offer matched low pass filter response typically required in lead acid battery sensor systems.

After enabling the current measurement channel, the delay for the availability of the first sample is two conversion cycles.

7.2 Voltage/Temperature Measurement Channel

The other two parameters of the Battery for measurement are Voltage and its Temperature. The second channel accepts signals from four independent sources through a Multiplexer as listed below:

- An attenuated battery voltage obtained through appropriate external resistor divider, (or)
- A signal from the external temperature sensor, (or)
- A signal from external reference, (or)
- A signal from the internal temperature sensor.

Apart from this difference in the multiplexing of four input signals, the rest of the data path is identical to the Current measurement channel. RSHH and RSHL are the Current measurement input pins

The Battery Voltage which can go up to 18V is attenuated through a Resistor Divider externally and is applied to the Voltage Channel. For Automotive Battery measurement, the Gain of the PGA should be restricted to 5 and 25. The latency for the first result from the voltage measurement channel is two conversion cycles.

A second option on this measurement channel is to measure Temperature. Internally generated constant current is pumped through the Temperature Sensor with positive temperature coefficient, and, a high- precision resistor. The voltages across the sensor and the resistor form the inputs to the measurement channel one at a time. The difference between the two voltages which is independent of the magnitude of the current is used to determine the temperature accurately. The Voltage across the sensor is applied between the ETS and VSS pins and, the voltage across the high-precision resistor is applied between ETR and VSS. External Temperature measurement involves the acquisition of two signals one after the other using the same constant current source. The latency for the first result from the temperature measurement channel is two conversion cycles.

A third option on the measurement channel is to measure the internal temperature. Hence, one of the three options for measurement of Battery Voltage, External Temperature and, internal temperature may be carried out by selection of appropriate inputs through the internal multiplexer selection.

7.3 Digital Implementation of Measurement Path

Figure 4. Block Diagram of Digital Implementation

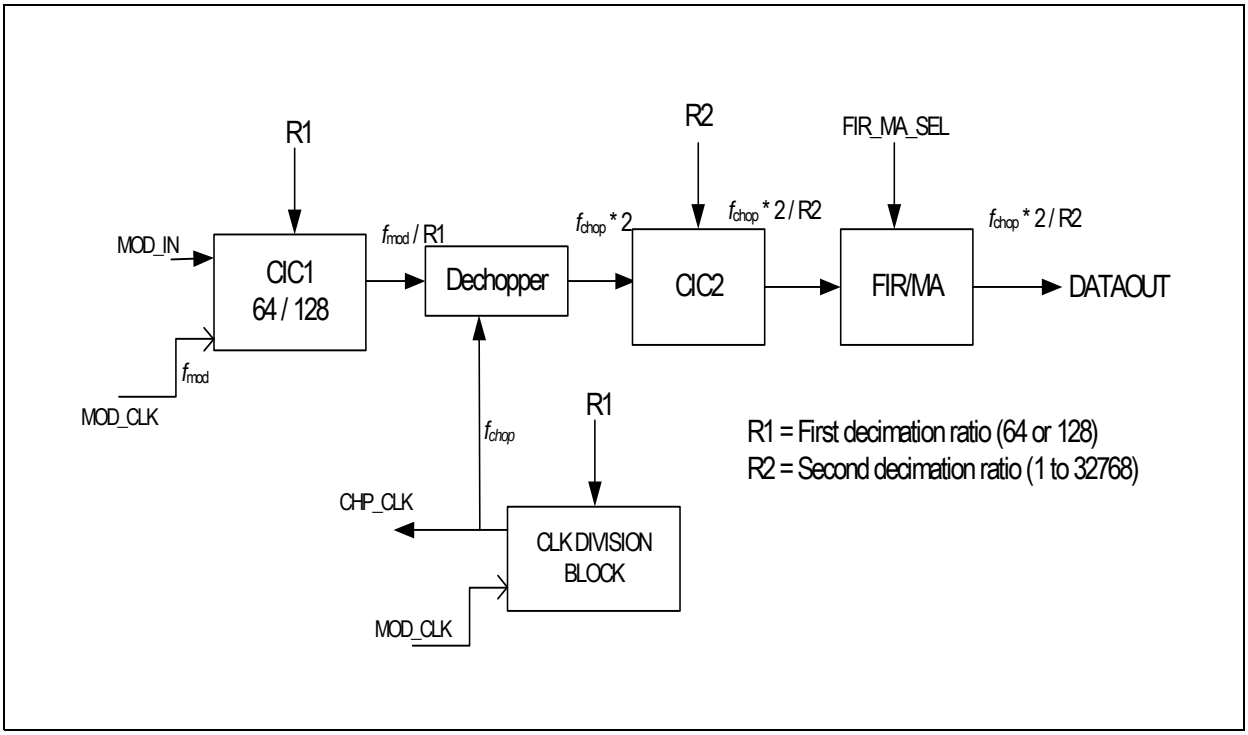


Figure 4 shows the digital implementation of the decimator and filter to process the 1-bit output of the Modulator. This block receives a 1-bit pulse density modulated output (MOD_IN) from the second order sigma delta modulator along with the oversampling frequency clock (MOD_CLK). The MOD_CLK directly goes to a clock division block, which generates chopper clock (CHOP_CLK). The CHOP_CLK can be one of 2kHz or 4kHz selected by Register CLK_REG in Table 33. The MOD_CLK can be either 1MHz or 2MHz. The Decimation is a two phase process. In the first phase, the R1 down sampling rate can be obtained by selecting either 64 or 128 in Registers DECREG_R1_I, DECREG_R1_V in Table 33. The 16-bit CIC1 output is dechopped with respect to CHOP_CLK. The output of Dechopper is passed through the CIC2 filter with a decimation ratio of 1to 32768 in steps of power of 2. This output is then processed through a FIR or Moving Average (MA) filter. FIR Filter is provided to offer matched low pass filter response typically required in lead acid battery sensor systems. MA filter is used to provide averaged output and the number of samples for averaging can be any integer value from 1, 3, 7 or 15.

7.4 Modes of Operation

The device operates in four different modes, namely,

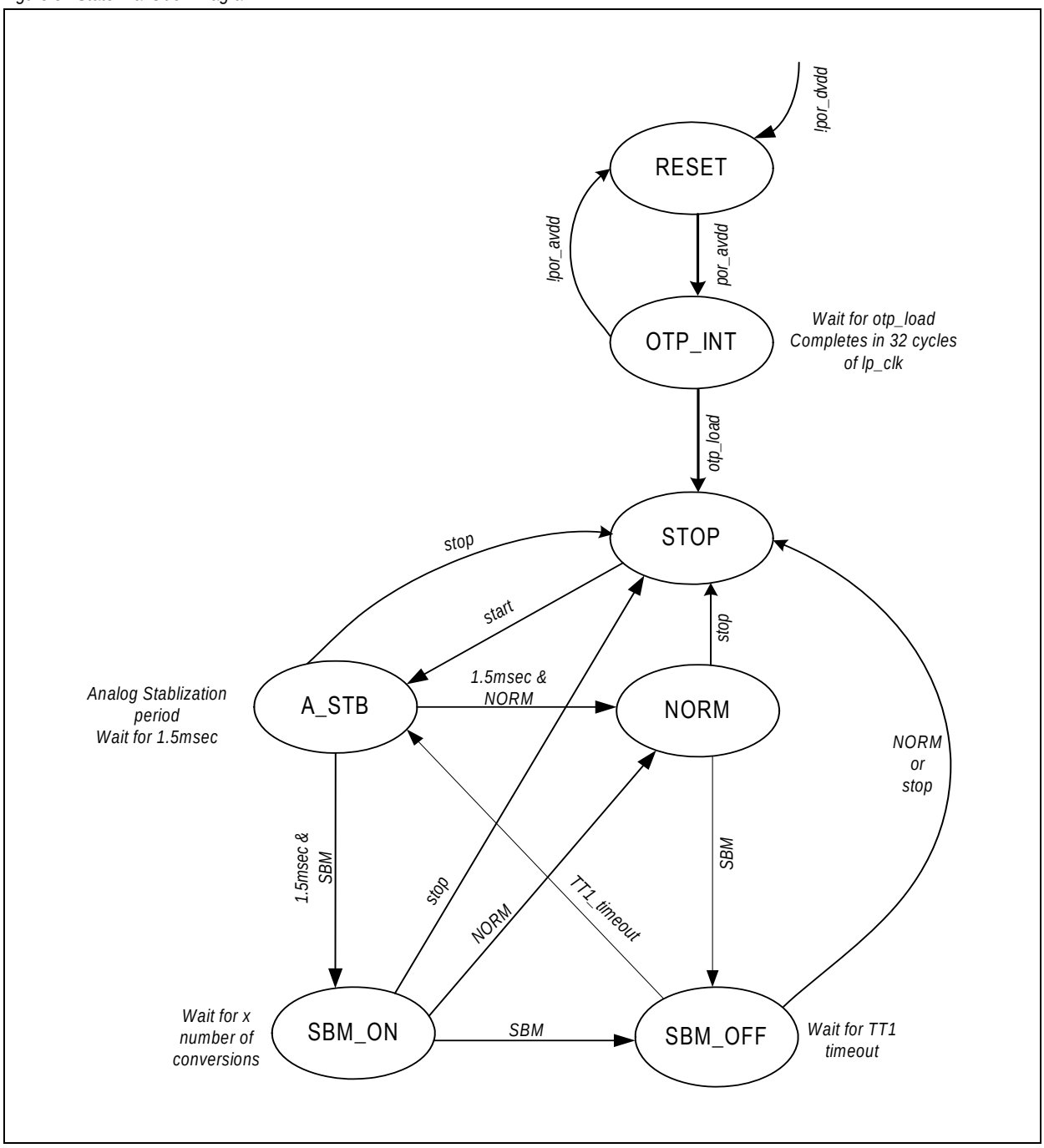
- Normal Mode 1 (NOM1),
- Normal Mode 2 (NOM2),
- Standby Mode 1 (SBY1), and,
- Standby Mode 2 (SBY2).

The Normal Modes are full-power modes with the exception that in Normal Mode 2, sampling is normally at a programmed lower frequency and is increased to a higher rate only when a measured input signal level crosses the programmed threshold in the current measurement channel.

The Standby Modes are lower power modes. Sampling is normally at a very low frequency interval. In Standby Mode 2, data sampling can be carried out only when the internal comparator detects the input current to be greater than the programmed threshold and it generates interrupt on the INT pin.

The device enters into the “Stop” state on Power On. This is a state where in the data path is inactive and can be entered into from any of the four Modes. The State transition Diagram involving the state of Stop and the four Modes is illustrated in the Figure 5.

Figure 5. State Transition Diagram



Note:

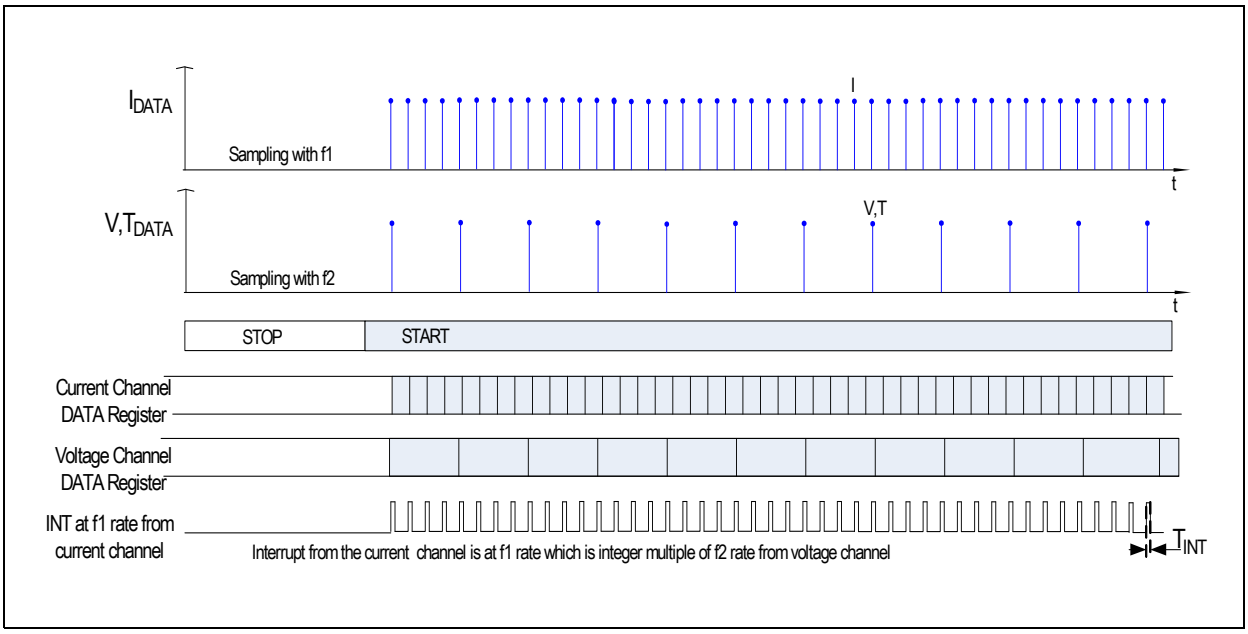
1. Device soft reset can be written in any of the following states STOP, A_STB, SBM_ON, SBM_OFF by writing “0” into D[7] of the RESET _REG (Address 0X09).
2. Measurement path of soft reset should be written in any the states, STOP, SBM_OFF by writing “0” into D[6] of the RESET _REG (Address 0X09).
3. When soft reset is used for the measurement path or for the device, external clock needs to be disabled if the system clock is external clock in the application.

7.4.1 Normal Mode 1 (NOM1)

On Power-on-reset of the device, AS8510 goes into STOP State.

Transition to Normal mode1 (NOM1) occurs when the “START BIT” D0 of Mode Control Register MOD_CTL_REG in Table 33 is set to “1” through the serial port SPI. Data Rate of voltage and current channels can be independently programmed and both the channels generate interrupts for every output available from ADC. The interrupt signal is generated on the INT pin. The width of the interrupt pulse is eight cycles of I_{p_clk}. The data is stable up to the next interrupt. If the data rate is different for the two channels, the interrupt rate would follow the higher rate among the two channels. Data update can be known by reading the status register. The functionality is explained in the waveform shown in Figure 6. When the device is configured to NORMAL Mode1 from any mode the configuration should be through the STOP state only.

Figure 6. Normal Mode 1

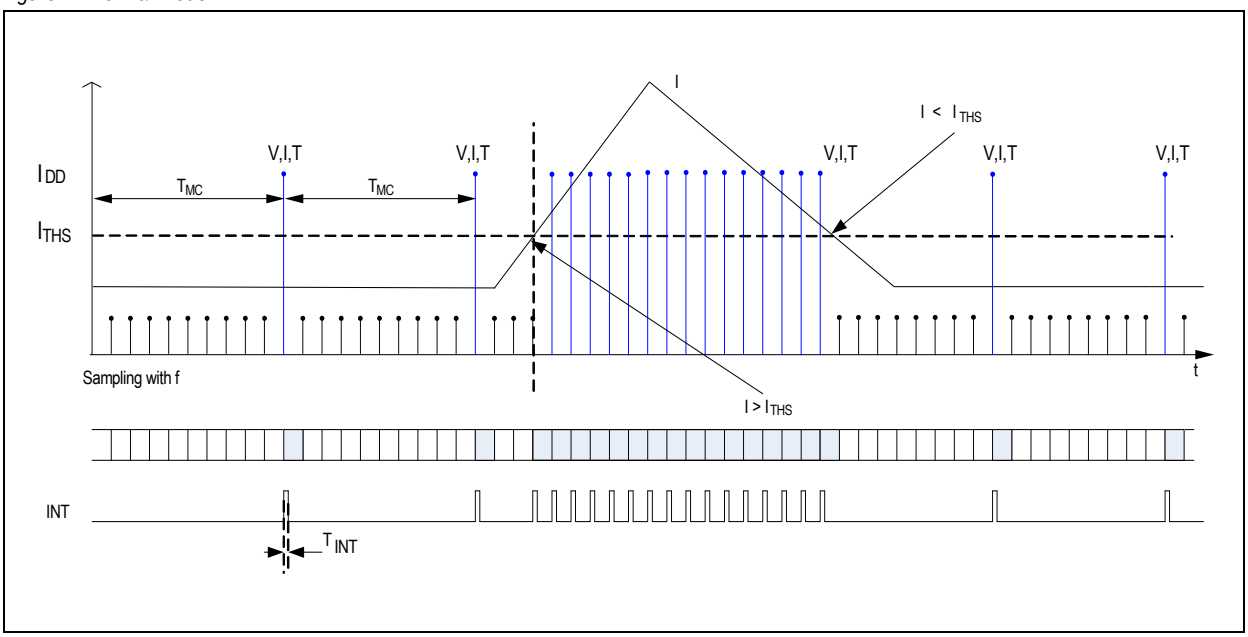


7.4.2 Normal Mode 2 (NOM2)

NOM2 differs from NOM1 in such a way that it allows for a relaxed data rate at a period of T_{MC} by programming the corresponding register as long as the amplitude of current is less than a programmed threshold I_{THC}. However, when, the measured input signal exceeds the programmed threshold, the data rate is changed to the rate of NOM1 mode.

Transition to NOM2 occurs when the “START BIT” D0 of Mode Control register MOD_CTL_REG in Table 33 is set to 1 and mode control bits to 01 through SPI. In this mode the data rate should be programmed with the time of T_{MC}. An interrupt signal is generated on INT at the rate of T_{MC} secs with a pulse width of eight cycles of I_{p_clk}. The data is stable up to the next interrupt. The data sample is compared against the programmed threshold and when it is exceeded, the data sampling rate is changed to provide data at the data rate of NOM1 mode. However, as soon as the data sample amplitude falls below the programmed threshold, the sampling rate is restored to provide data at the rate of T_{MC}. The functionality is illustrated in the waveform Figure 7.

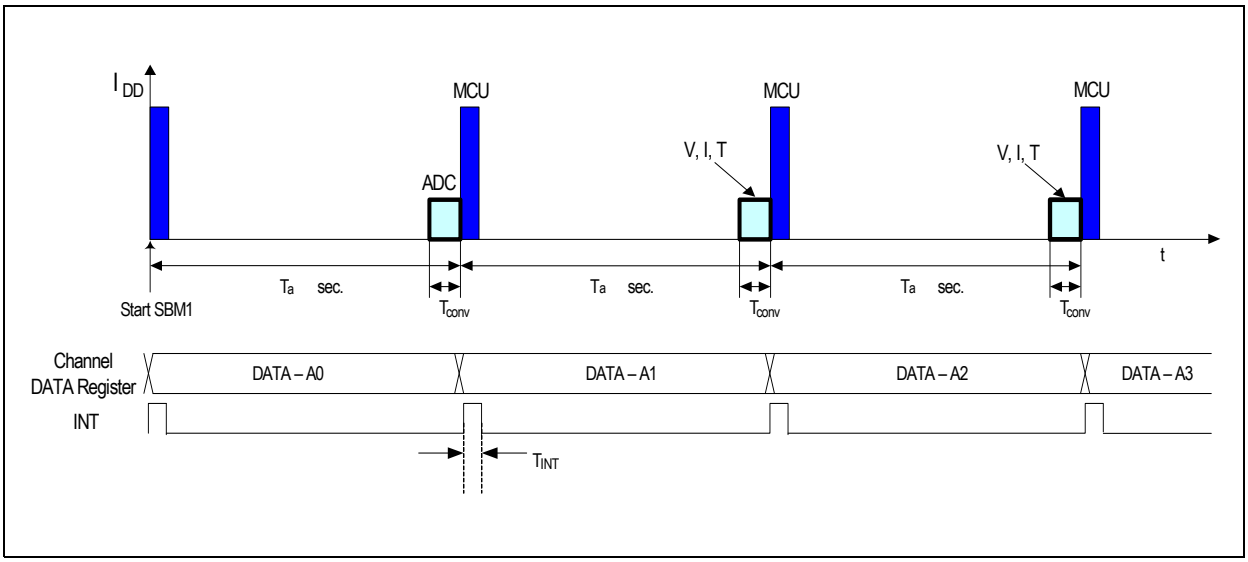
Figure 7. Normal Mode 2



7.4.3 Standby Mode1 (SBM1)

The low-power Standby Mode can be entered only through the STOP state. Transition to SBM1 mode occurs when the “START BIT” D0 of Mode Control register MOD_CTL_REG in Table 33 is set to “1” and Mode Control Bits to “10” through SPI. In this mode the date rate is programmable with the time of Ta. An interrupt signal is generated on INT at the rate of Ta secs., and with a pulse width of eight cycles of I_{p_clk}. The data is stable up to the next interrupt. The functionality is illustrated in Figure. During the period of Ta, only one data sample is made available and, during the rest of the period, the device is maintained in STOP state to reduce power consumption. The microcontroller which receives the data on the Interrupt, is also expected to be processing the data for a short time as shown clearly in the Figure 8 to ensure the overall low-power consumption of the data acquisition and processing system.

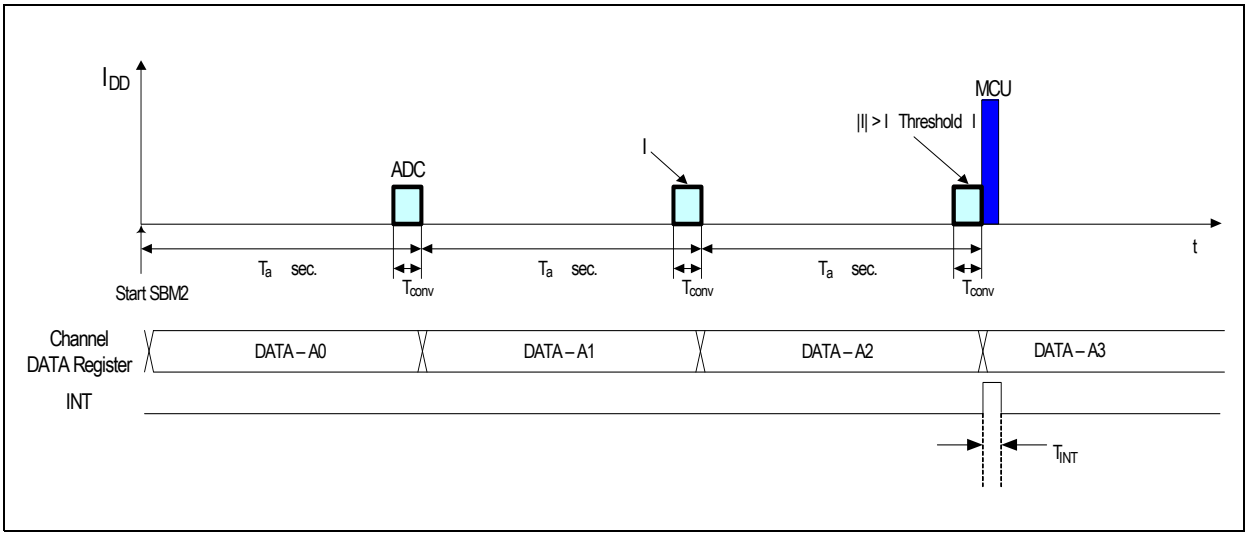
Figure 8. Standby Mode 1



7.4.4 Standby Mode2 (SBM2)

Standby Mode 2 is an extension of the Standby Mode1 to achieve even a lower power in the data acquisition system by providing interrupt to the microcontroller only when the data sample exceeds the set current threshold. The Standby Mode can be entered only through the STOP state. Transition to SBM2 mode occurs when the “START BIT” D0 of Mode Control register MOD_CTL_REG in Table 33 is set to “1” and Mode Control Bits D7,D6 to “1,1” through SPI. In this mode the date rate is programmable with the time of Ta in the Ta control registers B, C. The data sample is made available and an interrupt signal is generated on INT pin only when the input signal exceeds the threshold set in Current Threshold Registers D,E. It should be noted here that the data is stable for Ta secs. The functionality is illustrated in Figure 9.

Figure 9. Standby Mode 2



7.5 Reference-Voltage

Band gap-reference voltage is used for the ADC as a reference and for the generation of the current for external temperature measurement.

7.6 Oscillators

A High-speed oscillator (HS) generates the oversampling clock. For internal state machine and Interrupt generation, a low-speed Oscillator (LS) is also available.

7.7 Power-On Reset

The AS8510 has PORs, APOR and DPOR on analog and digital power supplies respectively. On PORs of both supplies, initialization sequence happens and the system status is shown in state diagram (see Figure 5).

As shown in the state diagram, the system is in RESET state until DPOR output goes to logic HIGH and subsequently until APOR output goes to logic HIGH. Once analog power supply is available, the system goes into OTP_INT state and loads the default values into the control and data registers and goes into STOP state. If analog POR, APOR goes low at any time, the system goes into RESET state. In the STOP state, the AS8510 can be programmed and by giving start command it starts working following the state machine.

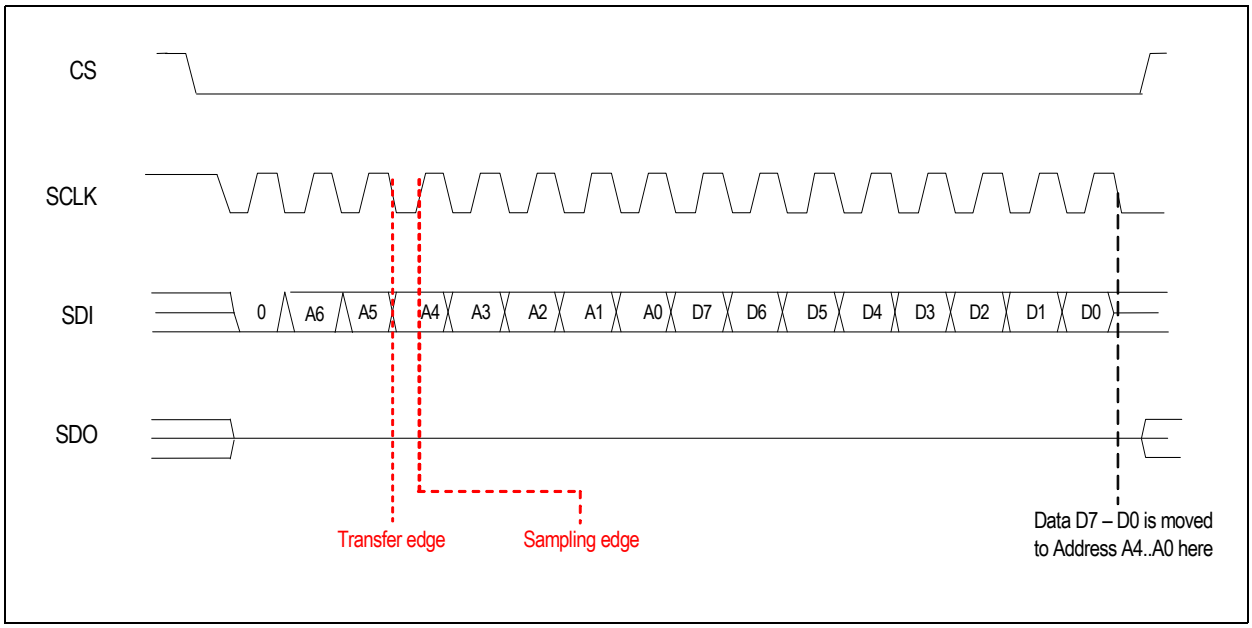
7.8 4-Wire Serial Port Interface

The SPI interface is used as interface between the AS8510 and an external micro-controller to configure the device and access the status information. The micro-controller begins communication with the SPI which is configured as a slave. The SPI protocol is simple and the length of each frame is an integer multiple of bytes except when a transmission is started. Each frame has 1 command bit, 7 address/configuration bits, and one or more data bytes. The edge of CS and the level of SCLK during the start of a SPI transaction, determine the edge on which the data is transferred from the SPI and the edge on which the data is sampled by the slave. Table 29 describes the setting of the transfer and sampling edges of SCLK. Figure 10 shows the falling edge and rising edge for data transfer and data sampling respectively, when SCLK is HIGH on the falling edge of CS.

Table 29. CS and SCLK

CS	SCLK	Description
FALL	LOW	Serial data transferred on rising edge of SPI clock. Sampled at falling edge of SPI clock.
FALL	HIGH	Serial data transferred on falling edge of SPI clock. Sampled at rising edge of SPI clock.
ANY	ANY	Serial data transfer edge is unchanged.

Figure 10. Protocol for Serial Data Write with Length = 1



7.8.1 SPI Frame

A frame is formed by a first byte for command and address/configuration and a following bit stream that can be formed by an integer number of bytes. Command is coded on the 1 first bit, while address is given on LSB 7 bits (see Table 30).

Table 30. Command Bits

Command Bits	Register Address or Transmission Configuration						
C0	A6	A5	A4	A3	A2	A1	A0

Table 31. Command Bits

C0	Command	<A6:A0>	Description
0	WRITE	ADDRESS	Writes data byte on the given starting address.
1	READ	ADDRESS	Read data byte from the given starting address.

If the command is read or write, one or more bytes follow. When the micro-controller sends more bytes (keeping CS LOW and SCLK toggling), the SPI interface increments the address of the previous data byte and writes/reads data to/from consecutive addresses.

7.8.2 Write Command

For write command, C0=0. After the command code C0 is transferred, the address of register to be written is provided from MSB to LSB. Subsequently one or more data bytes can be transferred from MSB to LSB. For each data byte following the first one, used address is the incremented value of the previously written address. Each bit of the frame has to be driven by the SPI master on the SPI clock transfer edge. The SPI slave samples it on the next clock edge. These edges are determined by the level of SCLK as shown in Table 29. Figure 11 and Figure 12 are examples of write command without and with address self-increment.

Figure 11. Protocol for Serial Data Write with Length = 1

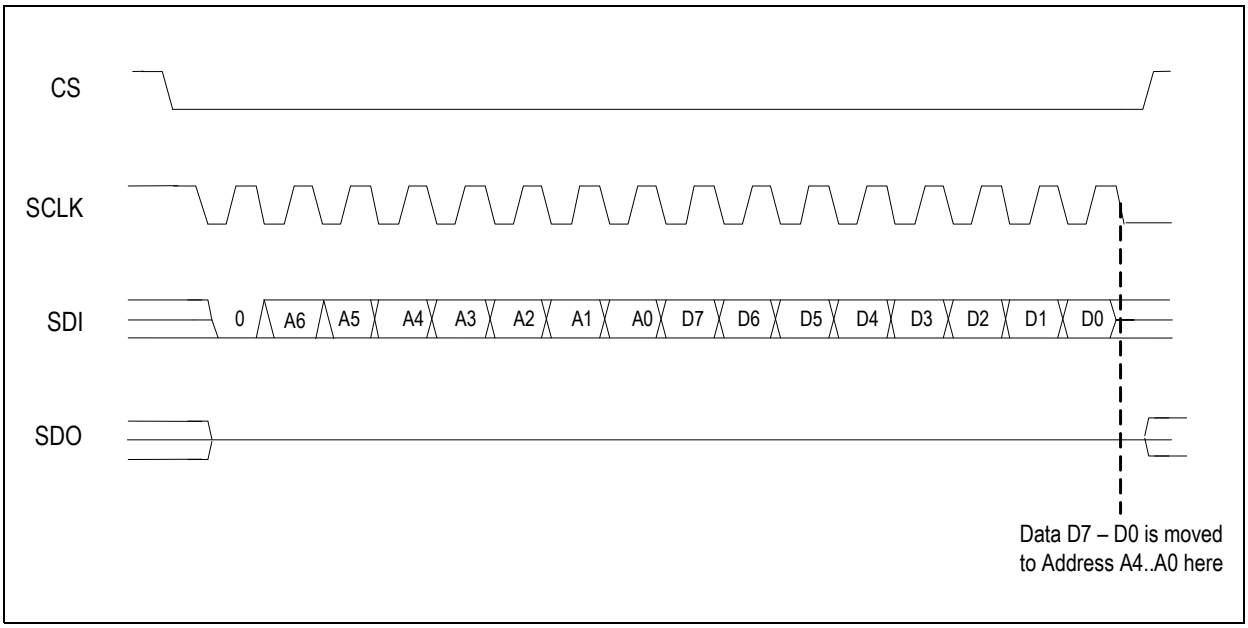
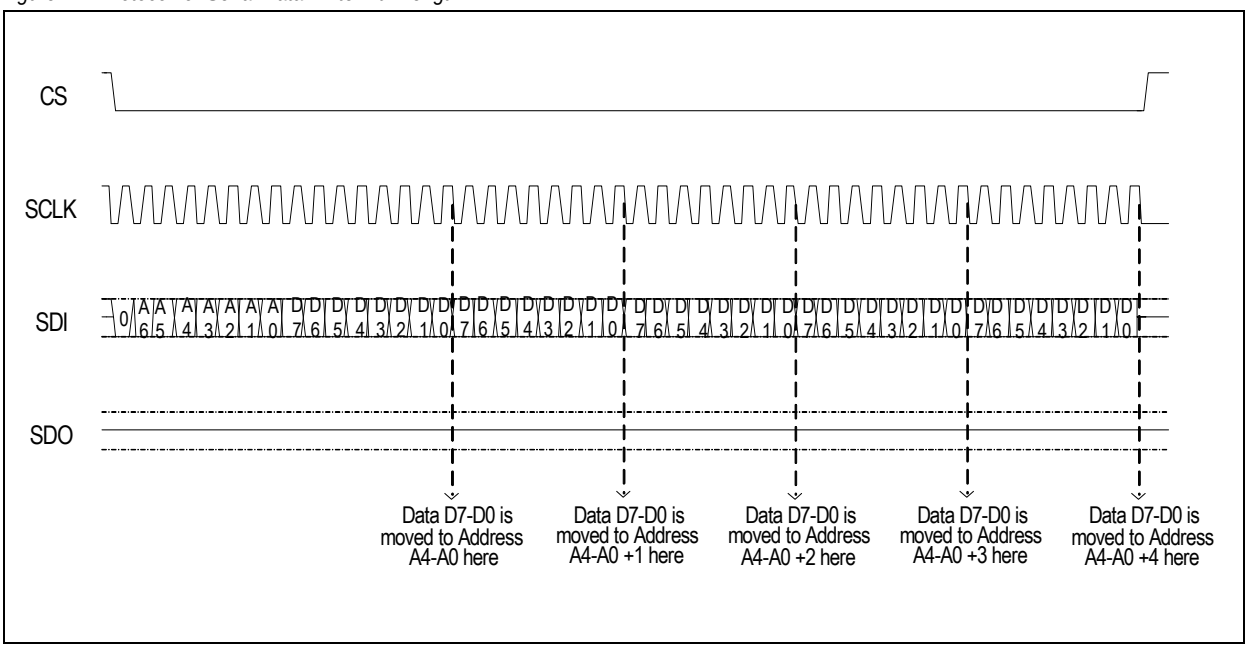


Figure 12. Protocol for Serial Data Write with Length = 4



7.8.3 Read Command

For Read command C0=1. After the command code C0, the address of register to be read is provided from MSB to LSB. Then one or more data bytes can be transferred from the SPI slave to the master, always from MSB to LSB. To transfer more bytes from consecutive addresses, SPI master keeps CS signal LOW and SPI clock active as long as it desires to read data from the slave. Each bit of the command and address of the frame is to be driven by the SPI master on the SPI clock transfer edge where SPI slave samples it on the next SPI clock edge.

Each bit of the data section of the frame is driven by the SPI slave on the SPI clock transfer edge and SPI master samples it on the next SPI clock edge. These edges are determined as per Table 29 and examples of read command without and with address self-increment.

Figure 13. Protocol for Serial Data Read with Length = 1

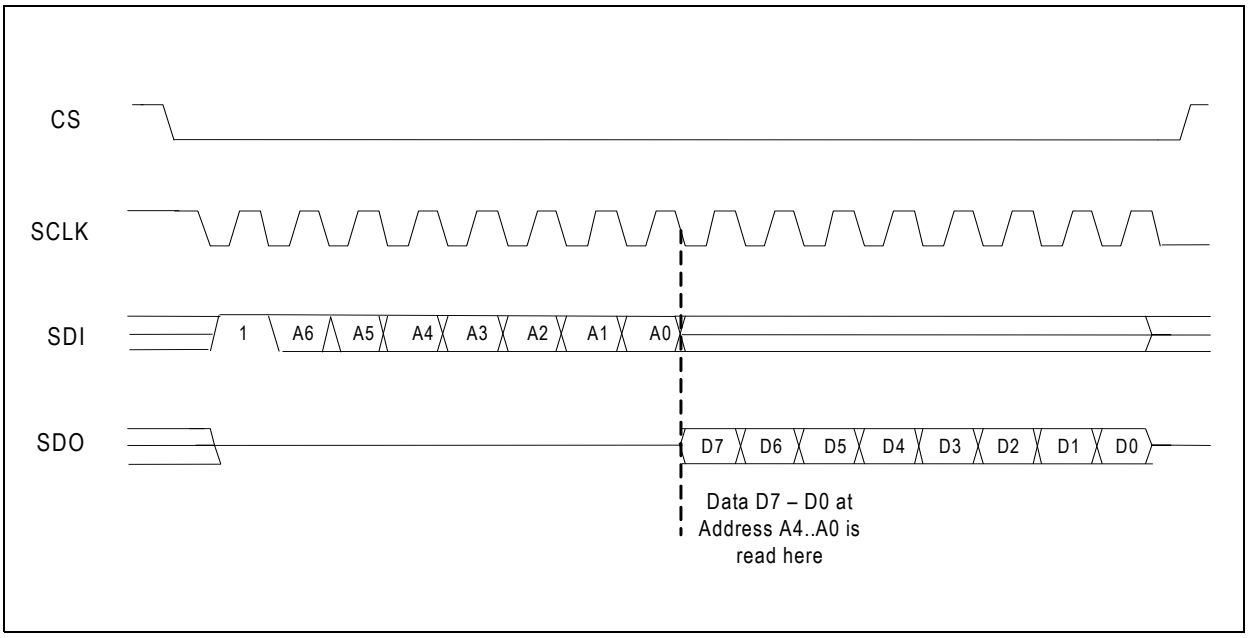
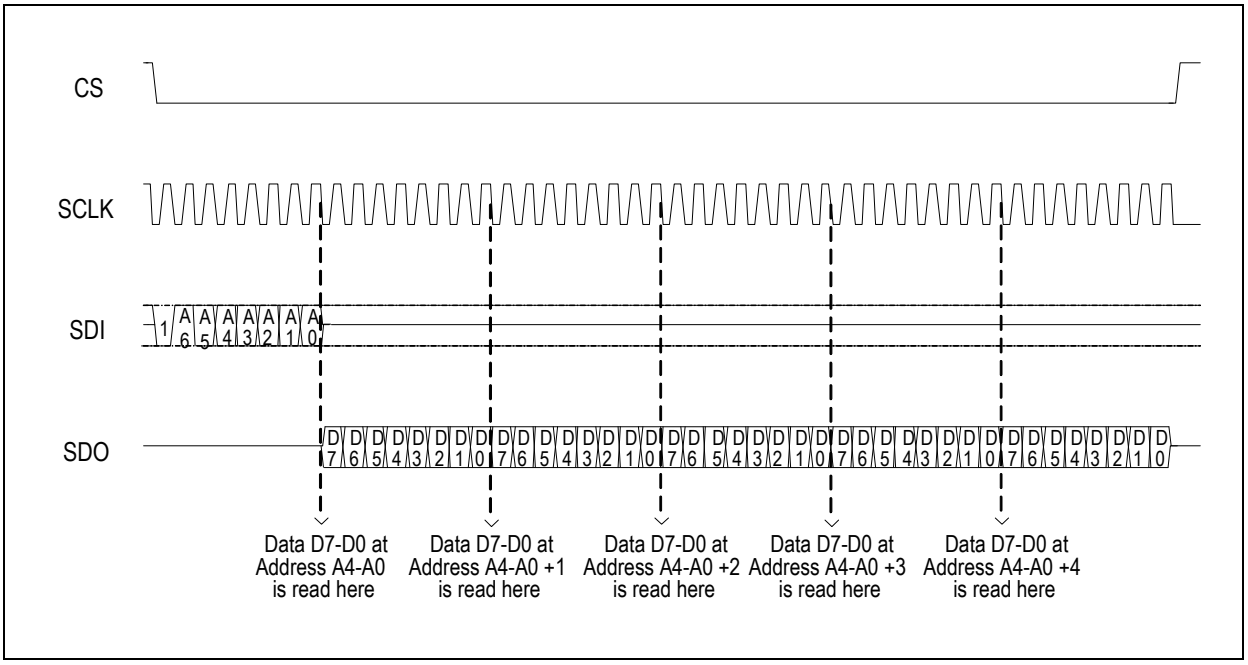


Figure 14. Protocol for Serial Data Read with Length = 4



7.8.4 Timing

In the following timing waveforms and parameters are exposed.

Figure 15. Write Timing for Writing

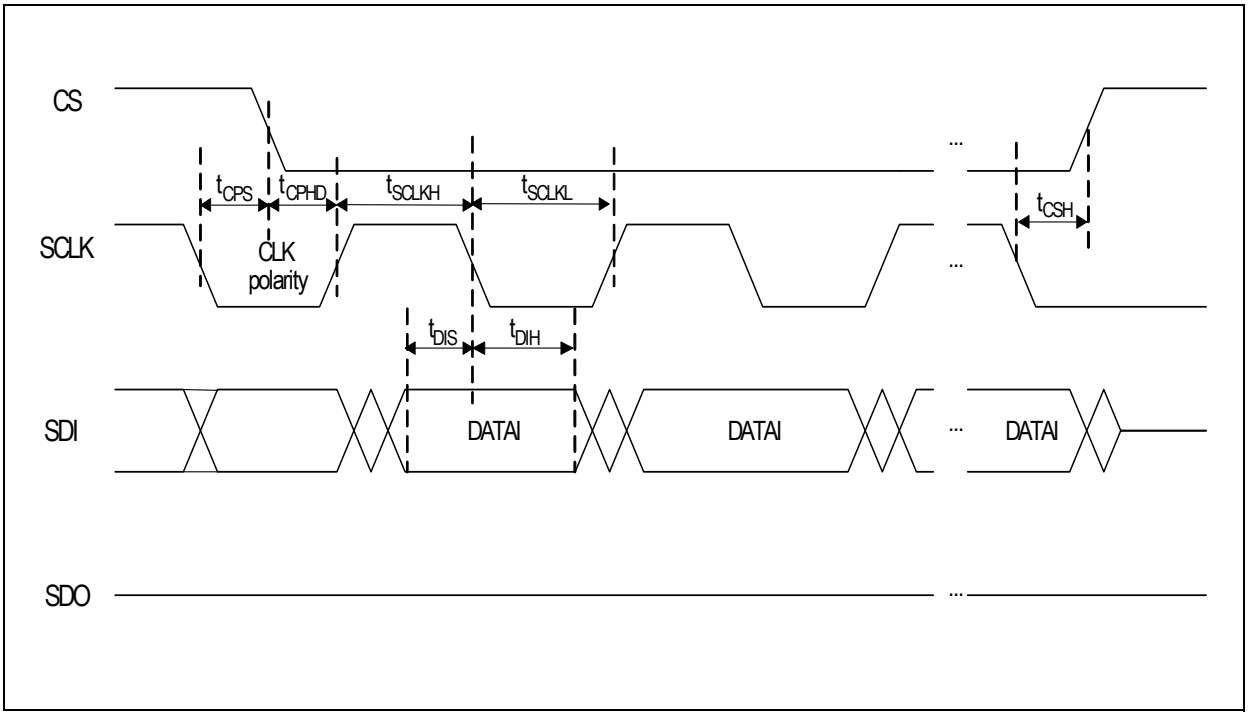
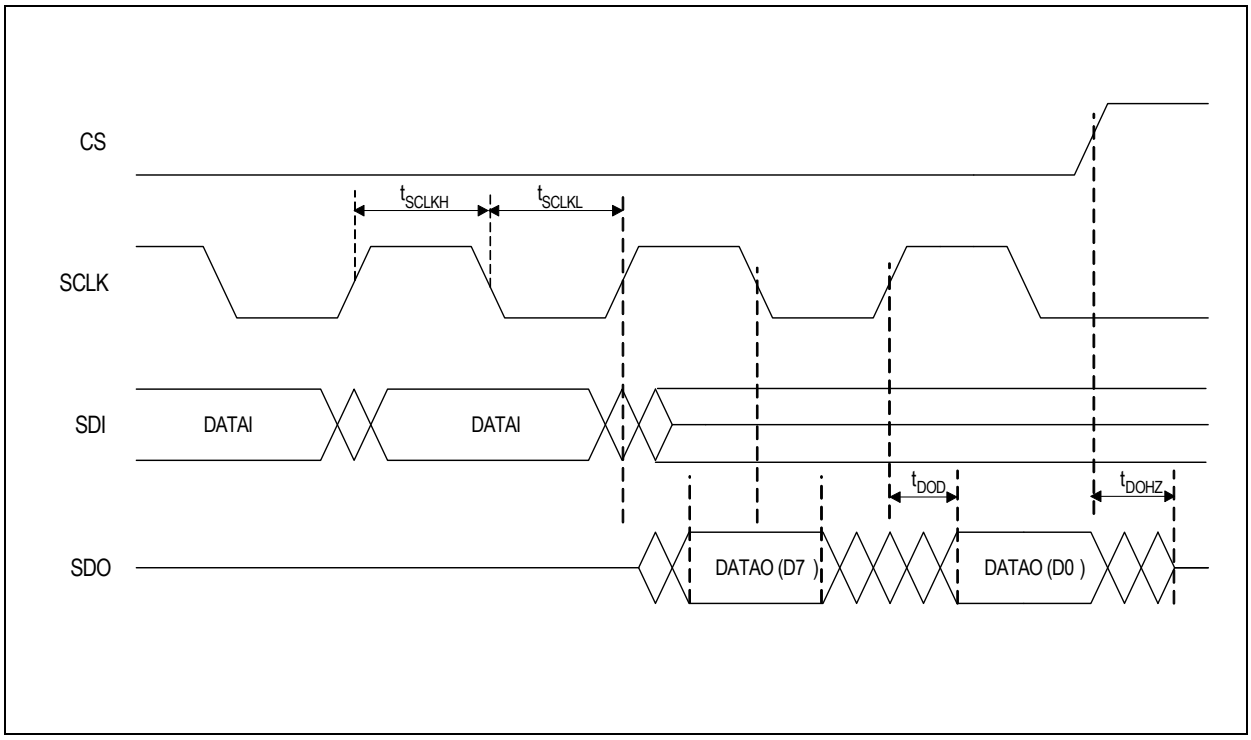


Figure 16. Read Timing for Reading



7.8.5 SPI Interface Timing

Table 32. SPI Interface Timing

Symbol	Parameter	Conditions	Min	Typ	Max	Units
General						
BR_{SPI}	Bit rate				1	Mbps
T_{SCLKH}	Clock high time		400			ns
T_{SCLKL}	Clock low time		400			ns
Write timing						
t_{DIS}	Data in setup time		20			ns
t_{DIH}	Data in hold time		20			ns
T_{CSH}	CS hold time		20			ns
Read timing						
t_{DOD}	Data out delay				80	ns
t_{DOHZ}	Data out to high impedance delay	Time for the SPI to release the SDO bus			80	ns
Timing parameters when entering 4-Wire SPI mode (for determination of CLK polarity)						
t_{CPS}	Clock setup time (CLK polarity)	Setup time of SCLK with respect to CS falling edge	20			ns
t_{CPHD}	Clock hold time (CLK polarity)	Hold time of SCLK with respect to CS falling edge	20			ns

7.9 Control Register

This section describes the control registers used in AS8510. Registers can be broadly classified into the following categories.

- Data access registers
- Status Registers
- Digital signal path control registers
- Digital Control registers
- Analog Control Registers

Table 33. Control Registers

Addr in HEX	Register Name	POR Value	R/W	8-bit Control / Status Data	
Data Access Registers					
00	DREG_I1 (ADC Data Register for Current)	0000_0000	R	D[7:0]	Denotes the Current ADC MSB Byte (ADC_I[15:8])
01	DREG_I2 (ADC Data Register for Current)	0000_0000	R	D[7:0]	Denotes the Current ADC LSB Byte (ADC_I[7:0])
02	DREG_V1 (ADC Data Register for Voltage)	0000_0000	R	D[7:0]	Denotes the Voltage ADC MSB Byte (ADC_V[15:8])
03	DREG_V2 (ADC Data Register for Voltage)	0000_0000	R	D[7:0]	Denotes the Voltage ADC LSB Byte (ADC_V[7:0])
Status Registers					
04	STATUS_REG	0000_0000	R	D[7]	NOM1/NOM2 Data Ready
				D[6]	NOM2 Threshold Crossover
				D[5]	SBM1 Data Ready
				D[4]	SBM2 Threshold Crossover
				D[3]	APOR status
				D[2]	Data from current channel updated
				D[1]	Data from voltage channel updated
				D[0]	Reserved

Table 33. Control Registers

Addr in HEX	Register Name	POR Value	R/W	8-bit Control / Status Data	
Digital Signal Path Control Registers for Current Channel					
05	DEC_REG_R1_I	0100_ 0101	R/W	D[7]	This bit selects decimation rate is used for current channel. Default is 0 (Down Sampling Rate is 64)
					0 — Down Sampling Rate is 64
					1 — Down Sampling Rate is 128
				D[6:5]	These two bits select division ratio of oversampling frequency clock MOD_CLK to be used as chopper clock, CHOP_CLK. Default is “10” (divide by 512)
					00 — Chopper Clock Always High
					01 — Divide by 256
					10 — Divide by 512
					11 — Divide by 1024
				D[4:1]	These four bits select the decimation ratio of second CIC stage. Default is “0010” (equal to 4)
					0000 — 1
					0001 — 2
					0010 — 4
					0011 — 8
					0100 — 16
					0101 — 32
					0110 — 64
					0111 — 128
					1000 — 256
					1001 — 512
					1010 — 1024
					1011 — 2048
					1100 — 4096
					1101 — 8192
					1110 — 16384
					1111 — 32768
				D[0]	CIC1 Saturation Interrupt Mask Control. Default is 1
					0 — Unmask
					1 — Mask

Table 33. Control Registers

Addr in HEX	Register Name	POR Value	R/W	8-bit Control / Status Data		
06	DEC_REG_R2_I	1100_0101	R/W	D[7]	I-Channel Enable, Default 1=enable	
				D[6]	V-Channel Enable, Default 1=enable	
				D[5]	Interrupt polarity	
					0	Active high
					1	Active low
				D[4]	. Interrupt Mask Control for Current Channel Data Ready Interrupt on INT pin (Default is 0)	
					0	Unmasked
					1	Masked
				D[3:2]	These two bits select the source of output 16-bit data in Normal mode from Current channel. Default is 01	
					00	FIR / MA Output
					01	CIC2 Output
					10	Dechop/Demod Output
					11	CIC1 Output
				D[1:0]	These two bits select the source of output 16-bit data in SBM mode from Current channel. Default is 01	
					00	FIR / MA Output
					01	CIC2 Output
					10	Dechop/Demod Output
					11	CIC1 Output

Table 33. Control Registers

Addr in HEX	Register Name	POR Value	R/W	8-bit Control / Status Data		
07	FIR CTL_REG_I	0000_0100	R/W	D[7]	This bit selects FIR / MA Filter in Current channel. Default is 0 (FIR)	
					0	FIR
					1	MA Filter
				D[6:3]	These bits select the number of data samples for averaging in MA filter in Current channel. Default is 0000 (bypass)	
					0000	bypass
					0001	1
					0011	3
					0111	7
					1111	15
				D[2:1]	These two bits select the Measurement Path architecture in both Current and Voltage channels. Default is 10 (Dechopper after CIC)	
					00	Demodulator after CIC1
					01	Demodulator before CIC1
					10	Dechopper after CIC1 (preferred and suggested)
					11	Demodulator before CIC1 with settled sample
				D[0]	Reserved. Default 0. Do not change	

Table 33. Control Registers

Addr in HEX	Register Name	POR Value	R/W	8-bit Control / Status Data		
Digital Control Registers						
08	CLK_REG (Clock Control Register)	0010_0000	R/W	D[7:6]	Oversampling frequency clock selection. Default is 00 (high speed (HS) internal Clock)	
					00	Internal HS Clock with No Clock Output
					01	Internal HS Clock with Clock Output
					10	External Clock
				D[5:4]	These two bits select the division ratio for HS clock/ external clock. Default is 10 (division by 4)	
					00	No division
					01	Divide by 2
					10	Divide by 4
					11	Divide by 8
				D[3:2]	These two bits select the division ratio of HS clock, by which it should be divided before providing it on CLK pin. Default is 00 (No Division)	
					00	No Division
					01	Divide by 2
					10	Divide by 4
					11	Divide by 8
				D[1]	This bit selects the division ratio of LS clock	
					0	LS _CLK undivided (Low Speed clock)
					1	LS _CLK divide by 2
				D[0]	Reserved	
09	RESET_REG (Reset Control Register)	1100_0000	R/W	D[7]	Entire device can be soft reset by writing “0” into this register bit. This bit will take a default 1 value on coming out of Reset	
				D[6]	Measurement Path can be soft reset by writing “0” into this register bit. This bit will take a default 1 value after Measurement Path is reset.	
				D[5:0]	Reserved	

Table 33. Control Registers

Addr in HEX	Register Name	POR Value	R/W	8-bit Control / Status Data		
0A	MOD_CTL_REG (Mode Control Registers)	0000_0000	R/W	D[7:6]	These two bits select the operating mode of the Device. Default is 00 (Normal Mode 1)	
					00	Normal Mode 1
					01	Normal Mode 2
					10	Standby Mode 1
					11	Standby Mode 2
				D[5:3]	These three bits select the number of cycles to be ignored before comparison with the set threshold in Standy Mode. Default is 000 (3 cycles of data)	
					000	3 cycles of data
					001	4 cycles of data
					010	5 cycles of data
					011	6cycles of data
					100	7 cycles of data
					101	8 cycles of data
					110	9 cycles of data
					111	10 cycles of data
				D[2]	This bit controls the CHOP_CLK availability on CHOP_CLK pin. Default is 0	
					0	Disabled
					1	Enabled
				D[1]	Enabling the MEN pin to indicate transition from Standby to Normal Mode.	
					0	Disabled
					1	Enabled
				D[0]	This bit is used to take the device from STOP state to any of the Modes based on D[7:6] selection of this register.	
					0	Retain in STOP state
					1	Enables transition to Normal or Standby Modes.
0B	MOD_Ta_REG1 (Ta Control Register)	1000_0000		D[7]	Unit of Ta in SBM1/SBM2. Default is 1	
					0	Unit is in milliseconds
					1	Unit is in seconds
				D[6:0]	MSB value of Ta	
0C	MOD_Ta_REG2 (Ta Control Register)	0000_0000	R/W	D[7:0]	Unit of Ta in SBM1/SBM2 LSB value of Ta	
0D	MOD_ITH_REG1 (Current Threshold Register)	0000_0000	R/W	D[7:0]	MSB bits of 16 bits SBM2 threshold register	
0E	MOD_ITH_REG2 (Current Threshold Register)	0000_0000	R/W	D[7:0]	LSB bits of 16 bits SBM2 threshold register	

Table 33. Control Registers

Addr in HEX	Register Name	POR Value	R/W	8-bit Control / Status Data		
0F	MOD_TMC_REG1 (T_{MC} Control Registers)	0000_0000	R/W	D[7:0]	MSB value of number of data samples to be dropped from ADC before sending Interrupt in NOM2	
10	MOD_TMC_REG2 (T_{MC} Control Register)	0000_0000	R/W	D[7:0]	LSB value of number of data samples to be dropped from ADC before sending Interrupt in NOM2	
11	NOM_ITH_REG1	0000_0000	R/W	D[7:0]	Eight MSB bits of NOM2 current threshold register	
12	NOM_ITH_REG2	0000_0000	R/W	D[7:0]	Eight LSB bits of NOM2 current threshold register	
Analog Control Registers						
13	PGA_CTL_REG (PGA Control Registers)	0101_0000	R/W	D[7:6]	Setting of Gain G of Current Channel PGA. Default is 01 (G = 25)	
					00	5
					01	25
					10	40
					11	100
				D[5:4]	Setting of Gain G in Voltage channel. Default is 01 (G = 25)	
					00	5
					01	25
					10	40
					11	100
				D[3:0]	Reserved	
14	PD_CTL_REG_1 (Power Down Control Register)	1100_1111	R/W			
				D[7]	0	Disable Chopper clock to Current channel
					1	Enable Chopper clock to Current channel
				D[6]	0	Disable Chopper clock to Voltage channel
					1	Enable Chopper clock to Voltage channel
				D[5]	Reserved	
				D[4]	Reserved	
				D[3]	0	Disable Current channel PGA
					1	Enable Current channel PGA
				D[2]	0	Disable Current channel ΣΔ Modulator
					1	Enable Current channel ΣΔ Modulator
				D[1]	0	Disable Voltage channel PGA
					1	Enable Voltage channel PGA
				D[0]	0	Disable Voltage channel ΣΔ Modulator
					1	Enable Voltage channel ΣΔ Modulator

Table 33. Control Registers

Addr in HEX	Register Name	POR Value	R/W	8-bit Control / Status Data		
15	PD_CTL_REG_2 (Power Down Control Register)	1111_0011	R/W	D[7]	0	Disable CIC1 of both channels
					1	Enable CIC1 of both channels
				D[6]	0	Disable CIC2 of both channels
					1	Enable CIC2 of both channels
				D[5]	0	Disable Dechopper in both channels
					1	Enable Dechopper in both channels
				D[4]	0	Disable FIR in both channels
					1	Enable FIR in both channels
				D[3]	0	Do not bypass PGA in Current Channel Default 0
					1	Bypass PGA in Current Channel
				D[2]	0	Do not bypass PGA in Voltage Channel Default 0
					1	Bypass PGA in Voltage Channel
				D[1]	0	Disable Current Channel Chopper
					1	Enable Current Channel Chopper
				D[0]	0	Disable Voltage Channel Chopper
					1	Enable Voltage Channel Chopper
16	PD_CTL_REG_3 (Power Down Control Register)	1111_1000		D[7]	0	Disable Common Mode Reference
					1	Enable Common Mode Reference
				D[6]	0	Disable Internal Current Source
					1	Enable Internal Current Source
				D[5]	0	Disable Internal temperature sensor
					1	Enable Internal temperature sensor
				D[4]	Reserved. (Default 1) Do not change	
				D[3]	Reserved. (Default 1) Do not change	
				D[2]	0	Data Output in binary numbering system
					1	Data Output in 2's complement numbering system
				D[1]	Reserved. (Default 0) Do not change	
				D[0]	Reserved	

Table 33. Control Registers

Addr in HEX	Register Name	POR Value	R/W	8-bit Control / Status Data		
17	ACH_CTL_REG (Analog Channel Selection Register)	0000_0000	R/W	D[7:6]	These bits specify the selection of voltage/temperature in Voltage Channel Default is 00 (Voltage Channel)	
					00	Voltage Channel
					01	External Temperature Channel ETR
					10	External Temperature Channel ETS
					11	Internal Temperature Channel
				D[5]	Reserved. (Default 0) Do not change	
				D[4]	Internal current source switch enable. Default is 0 **Note:** D4 bit is used for Enabling current source to the channel selected by bits D[7,6] of this register.	
					0	Disabled
					1	Enabled
				D[3]	Enable/disable Internal current source to RSHH pin of Current channel	
					0	Disabled
					1	Enabled
				D[2]	Enable/disable current source switch to RSHL pin of Current channel	
					0	Disabled
					1	Enabled
				D[1:0]	Reserved	
18	ISC_CTL_REG (Current Source Setting Register)	0000_0000	R/W	D[7:3]	These three bits specify the selection of magnitude of current from the Internal current source. Default is 00000 (0µA).	
					00000	0µA
					00001	8.5µA
					00010	17µA
					00100	34.5µA
					01000	68µA
					10000	135µA
					11111	270µA
				D[2:0]	Reserved	
19	OTP_EN_REG	0000_0000	R/W	D[7]	1	Reserved (default = 1) Do not change
				D[6:0]	Reserved	
44	STATUS_REG_2	0000_0000	R	D[7]	Status indicating data saturation in Current channel	
				D[6]	Status indicating data saturation in Voltage channel	
				D[5:0]	Reserved	

Table 33. Control Registers

Addr in HEX	Register Name	POR Value	R/W	8-bit Control / Status Data		
Digital Signal path control registers for Voltage Channel						
45	DEC_REG_R1_V	0100_ 0101	R/W	D[7]	Selection of Decimation ratio for Voltage/Temperature channel. Default is 0 (Down Sampling Rate is 64)	
					0	Down Sampling Rate is 64
					1	Down Sampling Rate is 128
				D[6:5]	Division of oversampling clock, which is used as Chopper Clock. Default is 10 (divide by 512)	
					00	Chopper Clock Always High
					01	Divide by 256
					10	Divide by 512
					11	Divide by 1024
				D[4:1]	Decimation ratio of CIC2. Default is 0010 (4)	
					0000	1
					0001	2
					0010	4
					0011	8
					0100	16
					0101	32
					0110	64
					0111	128
					1000	256
					1001	512
					1010	1024
					1011	2048
					1100	4096
					1101	8192
					1110	16384
					1111	32768
				D[0]	CIC1 Saturation Interrupt Mask Control. Default is 1	
					0	Unmasked
					1	Masked

Table 33. Control Registers

Addr in HEX	Register Name	POR Value	R/W	8-bit Control / Status Data		
46	DEC_REG_R2_V	0000_0100	R/W	D[7:5]	Reserved	
				D[4]	Interrupt Mask Control for Voltage channel data Ready Interrupt on INT pin (Default is 0)	
					0	Unmasked
					1	Masked
				D[3:2]	These two bits select the source of output 16-bit data in Normal mode from Voltage channel. Default is 01	
					00	FIR / MA Output
					01	CIC2 Output
					10	Dechop/Demod Output
					11	CIC Output
				D[1:0]	Reserved	
47	FIR CTL_REG_V	0000_0000	R/W	D[7]	This bit selects FIR / MA Filter in Voltage channel. Default is 0 (FIR)	
					0	FIR
					1	MA Filter
				D[6:3]	These bits select the number of data samples for averaging in MA filter in Voltage channel. Default is 0000 (bypass)	
					0000	bypass
					0001	1
					0011	3
					0111	7
					1111	15
				D[2:0]	Reserved	

Note: All the registers from address 0x19 to 0x2C are read-only.

There is an OTP test lock bit set by factory which locks the write access to all the test registers from 0x1A to 0x2C.

7.9.1 Standby Mode - Power Consumption

In Standby Mode 1 there is a timer based accurate measurement every Ta seconds. The device itself stays in idle-mode as long as it does not get a different command from the SPI interface. Internal oscillator frequency is typically foscint=262 kHz to reduce power consumption as long as the timer runs. After every time out of Ta secs, it performs accurate measurement of current, voltage/ temperature. Data ready is signaled to microcontroller through an interrupt signal on INT and goes into STOP state.

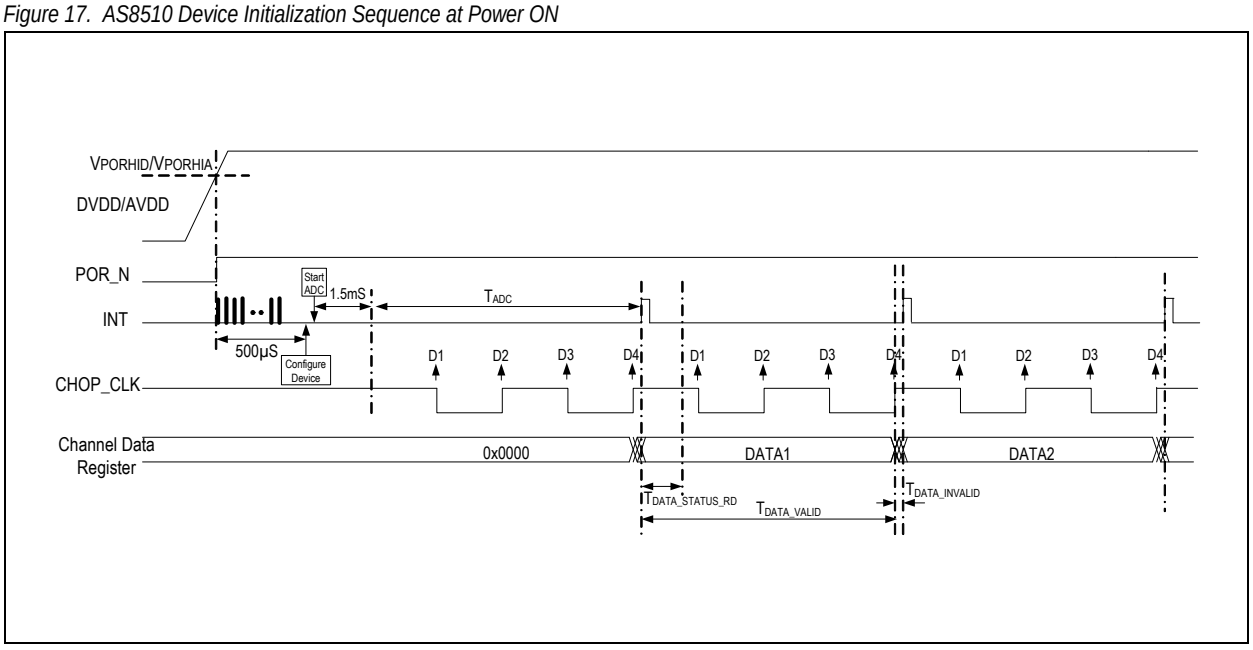
In the SBM the following equations hold:

- T_{sbm1} = Ta= 10s (default value is 10secs); the power consumption is valid for this setting. This is the period of the repetition rate in SBM 1 and SBM2.
- $T_{sett} \approx$ 2ms (depending on external capacitors). This is the time required by the analog part to settle when the new measuring period is started. Any measurements performed during T_{sett} produce invalid results.
- T1 = 3ms (by default setting, every third measurement is sent to microcontroller in the SBM mode 1) is the time needed to perform the first measurement.
- $T_{meas} = T_{sett} + T1$ is the total active time needed to get a valid result.
- $DR_{SBM} = T_{meas}/T_{sbm} \approx$ 5ms/10s. This is the ratio of repetition time versus the active time (Device in NOM mode).

Power consumption = (DR_{SBM}*NOM mode power consumption) + ((10s-5ms)/10s)*Stop mode power consumption)

7.9.2 Initialization Sequence at Power ON

Figure 17. AS8510 Device Initialization Sequence at Power ON



Device initialization starts if the DVDD and AVDD supplies are switched ON and DVDD > V_{PORHID}. The duration period of Initialization is 500µsec and during this period, INT pin toggles at the rate of internal low power oscillator. Toggling on INT during the period of initialization should be ignored in the system. Device configuration and activation should be carried out only after the initialization period.

On ADC start, device enters into analog stabilization state and takes 1.5msec for oscillator and Reference to settle. After this 1.5msec period, the first interrupt will occur after a time period of T_{ADC}.

$T_{DATA\_STATUS\_RD}$ is the time period during which the micro-controller should complete reading of data and status from the device. If reading is carried out beyond this time period, then, ADC performance will degrade for next sample generation. Status register gets cleared automatically only when micro-controller reads this register. Data in the channel registers is changed after T_{DATA_VALID} duration. Ensure that data channel registers and status registers are not read during the $T_{DATA\_INVALID}$ duration.

Example:

Configuration registers are set as follows:

CLK_REG = 8'b0010_0000

DEC_REG_R1_I = 0100_0101

DEC_REG_R2_I = 1100_0101

FIR_CTL_REG_I = 0000_0100

ADC is configured to a data rate of 1KHz, CHOP_CLK to 2KHz, and Modulator clock to 1MHz, Decimation ratio of CIC1 = 64, and Decimation ratio of CIC2 = 4. With these settings the various time periods as shown in the Figure 17 are as follows:

$T_{DATA\_STATUS\_RD}$ = 100 µsec

($T_{DATA\_STATUS\_RD}$ = (1/mod_clk) * R1 * [((mod_clk/(2*chop_clk))*(1/R1)) - 2.5)

$T_{DATA\_INVALID}$ = 8 µsec

T_{ADC} = 1msec

$T_{DATA\_VALID} = T_{ADC} - T_{DATA\_INVALID}$ = 1msec - 8 µsec

CHOP_CLK and POR_N are internal signals of the device.

Table 34 provides valid combinations of Modulator clock, Chopper clock and Decimation R1 and the corresponding values of $T_{DATA\_STATUS\_RD}$ and T_{ADC}.

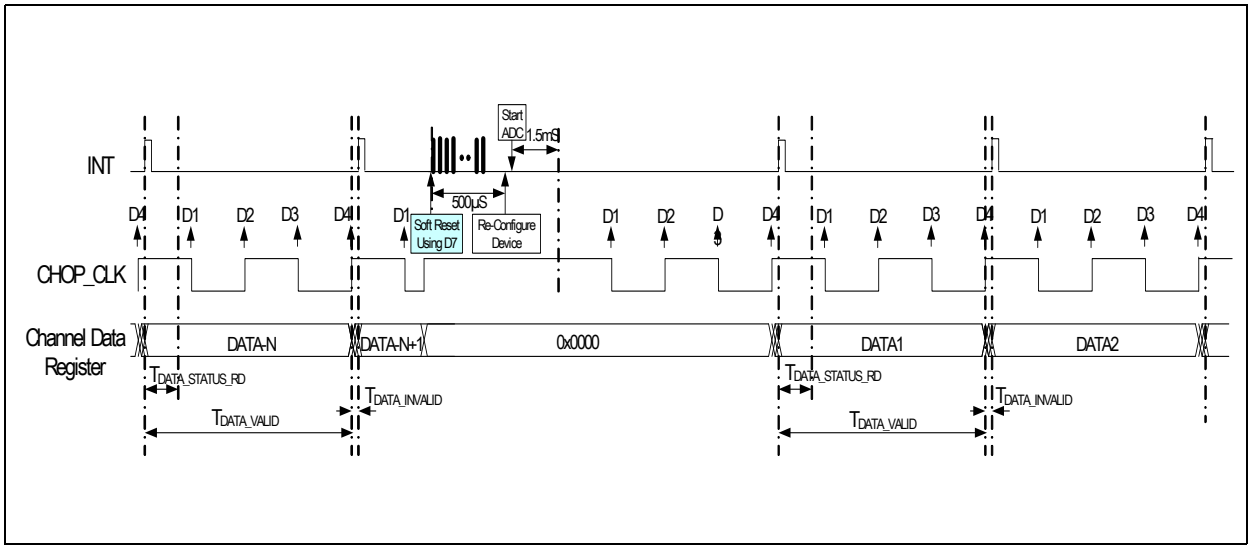
Table 34. Valid Combinations of Modulator Clock, Chopper Clock and Decimation Ratio R1

Modulator Clock	Chopper Frequency CHOP_CLK	Decimation Ratio R1	$T_{DATA\_STATUS\_RD}$	T_{ADC} R2/(2*CHOP_CLK) for R2=4
1.024MHz	2KHz	64	1usec * 64 * [4 - 2.5] = 96usec	1mSec
2.048MHz	2KHz	64	0.5usec * 64 * [8 - 2.5] = 176usec	1mSec
2.048MHz	2KHz	128	0.5usec * 128 * [4 - 2.5] = 96usec	1mSec
2.048MHz	4KHz	64	0.5usec * 64 * [4 - 2.5] = 48usec	0.5mSec

7.9.3 Soft-reset of Device Using Bit D[7] of Reset Register 0x09

It is possible to soft-reset the device by writing "0" into D[7] bit of Reset Register at 0x09. On applying soft-reset, the device enters into initialization state and D[6] bit changes back to "1". The duration period of Initialization is 500µsec, and, during this period, INT pin toggles at the rate of internal low power oscillator. Toggling on INT during the period of initialization should be ignored in the system. Device configuration and activation should be carried out only after the initialization period. See Figure 18 for the timing details of the sequence of device initialization on soft-reset.

Figure 18. AS8510 Device Initialization Sequence at Soft-reset



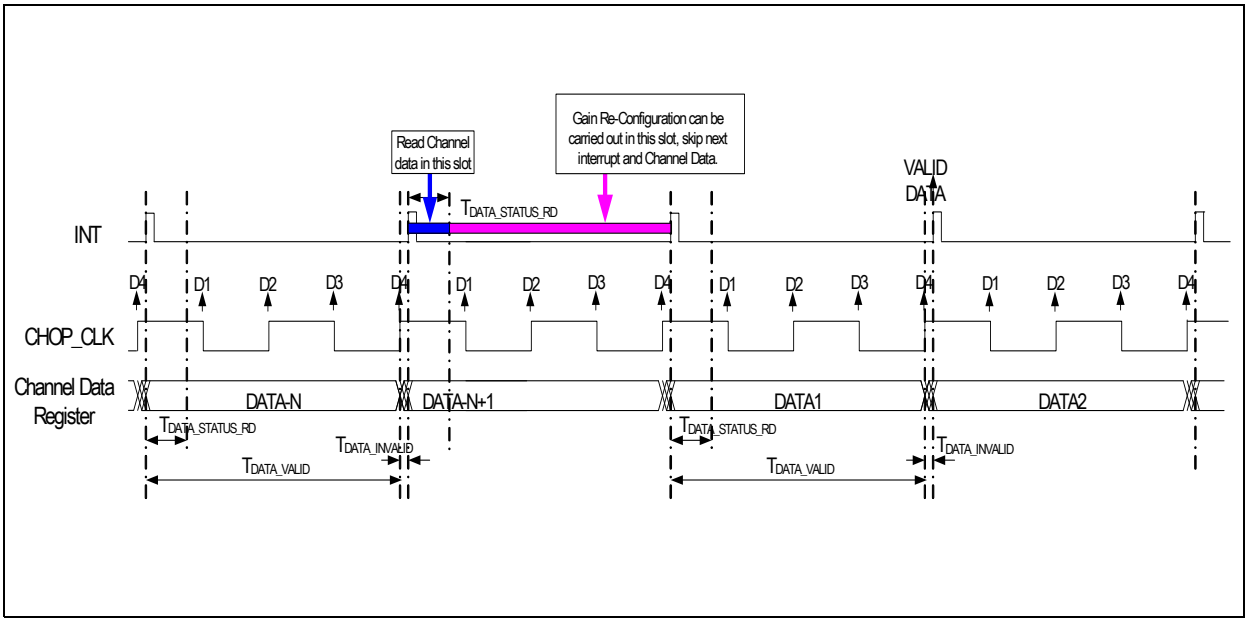
7.9.4 Soft-reset of the Measurement Path Using Bit D[7] of Reset Register 0x09

Measurement path also can be reset by using D[6] bit of Reset Register at 0x09. On applying soft-reset only signal measurement path registers will be reset. For applying this reset, device should be in STOP state. If the device is working with external clock, at the time of soft-reset the clock needs to be disabled.

7.9.5 Reconfiguring Gain Setting of PGA

Only PGA gain settings can be changed dynamically while ADC conversions are in progress. When PGA gain settings are changed, the first sample from the ADC is invalid. Ignore the first interrupt after the gain re-configuration. Valid data starts from the second interrupt onwards.

Figure 19. AS8510 - Re-configuration of Gain Setting of PGA



7.9.6 Configuring the Device During Normal Mode

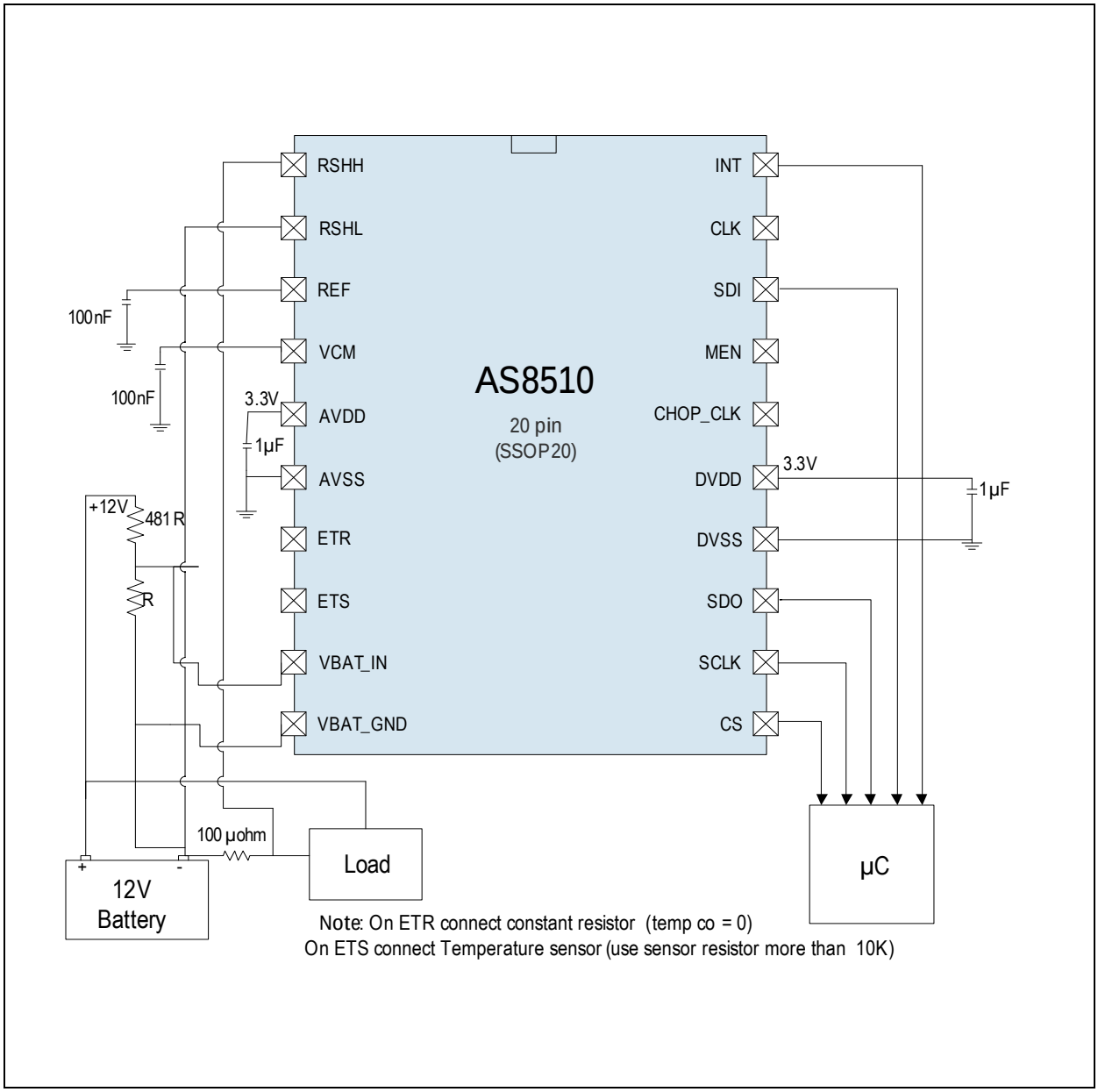
Following registers can be programmed dynamically when the device is in operational mode (Normal mode).

- ACH_CTL_REG address is 0x17 for channel selection on the voltage measurement path
- PGA_CTL_REG address is 0x13 for gain setting
- PD_CTL_REG2 address is 0x15 for PGA Bypass
- ISC_CTL_REG address is 0x18 for current source programmability

During the operation (Normal mode) of the device, if any of the registers need to be programmed or changed other than the above mentioned registers, then it is required to STOP the device by writing into MOD_CTL_REG “STOP” bit and configure the device as per the requirements and start the device.

7.10 Low Side Current Measurement Application

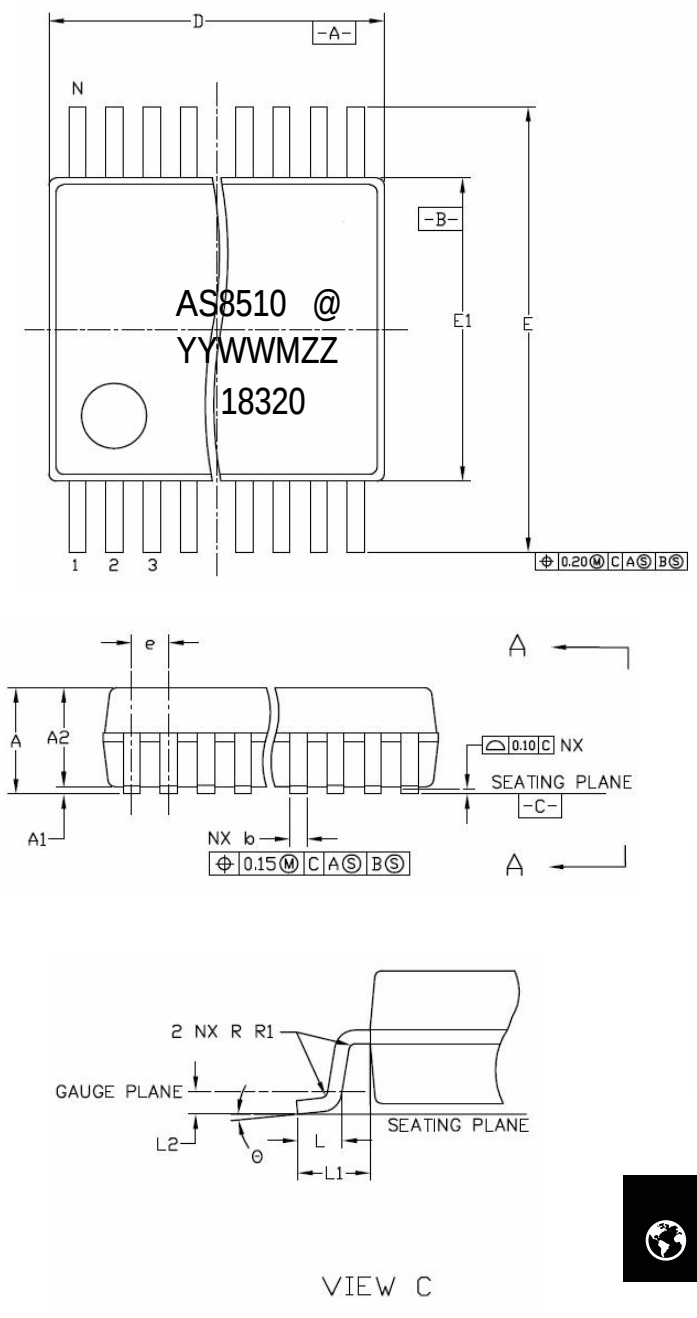
Figure 20. Application Diagram



8 Package Drawings and Markings

The product is available in a 20-pin SSOP package.

Figure 21. Drawings and Dimensions



Symbol	Min	Nom	Max
A	-	-	2.00
A1	0.05	-	-
A2	1.65	1.75	1.85
b	0.22	-	0.38
c	0.09	-	0.25
D	6.90	7.20	7.50
E	7.40	7.80	8.20
E1	5.00	5.30	5.60
e	-	0.65 BSC	-
L	0.55	0.75	0.95
L1	-	1.25 REF	-
L2	-	0.25 BSC	-
R	0.09	-	-
θ	0°	4°	8°
N	20		

Notes:

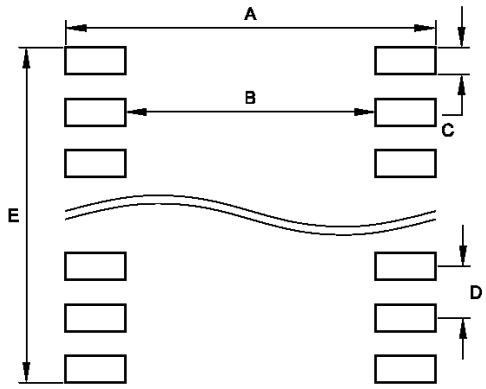
1. Dimensions & tolerancing conform to *ASME Y14.5M-1994*.
2. All dimensions are in millimeters. Angles are in degrees.

Marking: @YYWWMZZ.

@	YY	WW	M	ZZ
Sublot Identifier	Last two digits of the current year	Manufacturing Week	Assembly Plant Identifier	Letters of free choice

8.1 Recommended PCB Footprint

Figure 22. PCB Footprint



Recommended Footprint Data	
Symbol	mm
A	9.02
B	6.16
C	0.46
D	0.65
E	6.31

Revision History

Revision	Date	Description
1.1	Jun 22, 2009	Initial version
1.2	Dec 02, 2009	Updated the datasheet according to 1.8 specification
	Dec 08, 2009	Following modifications carried out in Table 27: 1) Deleted Max value for parameter 'Temperature upper limit' 2) Added Footnote 2 3) Added new parameter 'Temperature Sensor Output (without gain calibration)
1.3	Feb 19, 2010	Updated Table 15 with PGA information
		Updated Voltage Measurement
		Updated VREFand VIN values in Table 17 and VREF in Table 18
		Inserted new Table 28 - System Measurement Error Budget
2.0	June 01, 2010	Changed the pin name AGND to VCM
		Current source added in the block diagram
		Added application diagram
		Updated Electrical Characteristics on page 7
		Updated Detailed System and Block Specifications on page 9
		Updated Standby Mode - Power Consumption on page 40
3.0	Oct 29, 2010	Updates carried out across the datasheet
3.1	Nov 02, 2010	Updated Ref Voltage Offset in Table 18
3.2	Nov 14, 2010	Added sections 7.9.2, 7.9.3, 7.9.5
3.3	Nov 26, 2010	Formatted figures 17, 18 in portrait mode. Index modified from page 39
	Dec 03, 2010	Added Configuring the Device During Normal Mode on page 43
3.4	Mar 01, 2011	Updated General Description, Key Features, Applications, Pin Descriptions, Current Measurement Ranges, Differential Input Amplifier for Current Channel, Differential Input Amplifier for Voltage Channel, Sigma Delta Analog to Digital Converter, Bandgap Reference Voltage, System Measurement Error Budget for Gains 5 and 25, Package Drawings and Markings. Deleted Voltage Measurement.
3.5	Aug 05, 2011	Updated Table 14, Figure 5, Table 19, Table 18, Section 7.9.6, Figure 20. Added Section 7.9.4
	Dec 31, 2012	Updated ordering table
3.6	Feb 07, 2013	Additional information added to System Specifications section.
3.7	Feb 27, 2014	Updated Table 13, Table 15, description of Figure 4, note of Table 33, Figure 21, Figure 3 and its description.
3.8	Apr 24, 2014	Updated description above and below Figure 3 on page 17. Updated Table 2.
	May 08, 2014	Updated Table 15 & Table 16.

Note: Typos may not be explicitly mentioned under revision history.

9 Ordering Information

The devices are available as the standard products shown in Table 35.

Table 35. Ordering Information

Ordering Code	Description	Delivery Form	Package
AS8510-ASSP	Data Acquisition Device for Battery Sensors	Tape and Reel (2000 pcs)	20-pin SSOP
AS8510-ASSM	Data Acquisition Device for Battery Sensors	Tape and Reel (500 pcs)	20-pin SSOP

Note: All products are RoHS compliant and ams green.
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Contact Information:

Headquarters
ams AG
Tobelbaderstrasse 30
8141 Unterpremstaetten
Austria, Europe

Tel: +43 (0) 3136 500 0

Website: www.ams.com