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12/12—Rev. B to Rev. C

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6/10—Rev. A to Rev. B

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1/04—Rev. 0 to Rev. A

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Added LFCSP Layout Considerations Section ... 11
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SPECIFICATIONS

All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC) methods. Ambient temperature of 85°C corresponds to a junction temperature of 125°C under pulsed full-load test conditions. Application stable with no load. V_{IN} = 6.0 V, C_{IN} = C_{OUT} = 1.0 µF, T_A = −40°C to +85°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OUTPUT						
Voltage Accuracy[1]	V_{OUT}	V_{IN} = $V_{OUT(NOM)}$ + 0.4 V to 12 V	−0.9		+0.9	%
		I_L = 0.1 mA to 500 mA				
		T_A = 25°C				
		V_{IN} = $V_{OUT(NOM)}$ + 0.4 V to 12 V	−1.8		+1.8	%
		I_L = 0.1 mA to 500 mA				
		T_A = 85°C				
		V_{IN} = $V_{OUT(NOM)}$ + 0.4 V to 12 V	−2.3		+2.3	%
		I_L = 0.1 mA to 500 mA				
		T_J = 150°C				
Line Regulation[1]		V_{IN} = $V_{OUT(NOM)}$ + 0.4 V to 12 V		0.04		mV/V
		I_L = 0.1 mA				
		T_A = 25°C				
Load Regulation		I_L = 0.1 mA to 500 mA		0.04		mV/mA
		T_A = 25°C				
Dropout Voltage	V_{DROP}	V_{OUT} = 98% of $V_{OUT(NOM)}$				
		I_L = 500 mA		200	370	mV
		I_L = 300 mA		140	230	mV
		I_L = 50 mA		30	110	mV
		I_L = 0.1 mA		10	40	mV
Peak Load Current	I_{LDPK}	V_{IN} = $V_{OUT(NOM)}$ + 1 V		800		mA
Output Noise	V_{NOISE}	f = 10 Hz to 100 kHz, C_L = 10 µF		47		µV rms
		I_L = 500 mA, C_{NR} = 10 nF				
		f = 10 Hz to 100 kHz, C_L = 10 µF		95		µV rms
		I_L = 500 mA, C_{NR} = 0 nF				
GROUND CURRENT						
In Regulation	I_{GND}	I_L = 500 mA		4.5	10	mA
		I_L = 300 mA		2.6	6	mA
		I_L = 50 mA		0.5	2.5	mA
		I_L = 0.1 mA		80	110	µA
In Dropout	I_{GND}	V_{IN} = $V_{OUT(NOM)}$ − 100 mV		120	400	µA
		I_L = 0.1 mA				
In Shutdown	$I_{\overline{GNDSD}}$	$\overline{SD}$ = 0 V, V_{IN} = 12 V		0.01	1	µA
SHUTDOWN						
Threshold Voltage	$V_{\overline{THSD}}$	ON	2.0			V
		OFF			0.4	V
$\overline{SD}$ Input Current	$I_{\overline{SD}}$	0 ≤ $\overline{SD}$ ≤ 5 V		1.2	3	µA
Output Current in Shutdown	$I_{\overline{OSD}}$	V_{IN} = 12 V, V_{OUT} = 0 V		0.01	5	µA

[1] V_{IN} = 2.6 V to 12 V for models with $V_{OUT(NOM)}$ ≤ 2.2 V.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Input Supply Voltage	−0.3 V to +16 V
Shutdown Input Voltage	−0.3 V to +16 V
Power Dissipation	Internally Limited
Operating Ambient Temperature Range	−40°C to +85°C
Operating Junction Temperature Range	−40°C to +150°C
θ_{JA}, 2-layer MSOP-8	220°C/W
θ_{JA}, 4-layer MSOP-8	158°C/W
θ_{JA}, 2-layer LFCSP-8	62°C/W
θ_{JA}, 4-layer LFCSP-8	48°C/W
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering 10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

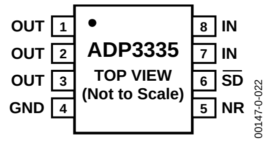
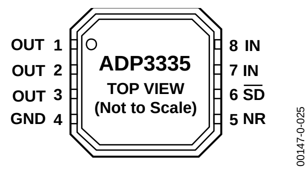


Figure 3. 8-Lead MSOP



NOTES
1. THE EXPOSED PAD ON THE BOTTOM OF THE PACKAGE ENHANCES THE THERMAL PERFORMANCE AND IS ELECTRICALLY CONNECTED TO DIE SUBSTRATE. THERMAL VIAS MUST BE ISOLATED OR CONNECTED TO IN. DO NOT CONNECT THE THERMAL PAD TO GROUND.

Figure 4. 8-Lead LFCSP

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Function
1, 2, 3	OUT	Output of the Regulator. Bypass to ground with a 1.0 µF or larger capacitor. All pins must be connected together for proper operation.
4	GND	Ground Pin.
5	NR	Noise Reduction Pin. Used for further reduction of output noise (see the Noise Reduction section for further details).
6	$\overline{\text{SD}}$	Active Low Shutdown Pin. Connect to ground to disable the regulator output. When shutdown is not used, this pin should be connected to the input pin.
7, 8	IN	Regulator Input. All pins must be connected together for proper operation.
EP	Exposed Pad	The exposed pad on the bottom of the LFCSP package enhances thermal performance and is electrically connected to the die substrate, which is electrically common with the input pins, IN (Pin 7 and Pin 8), inside the package.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

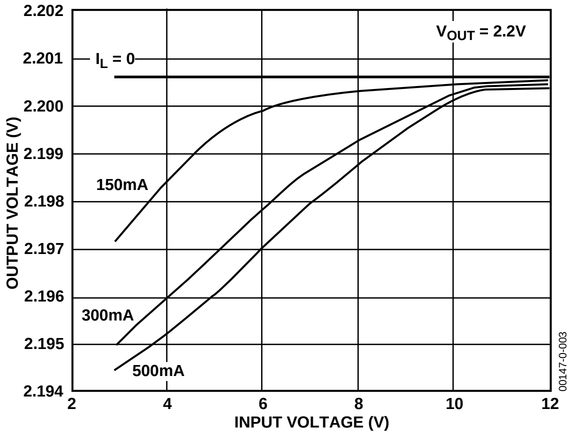


Figure 5. Line Regulation Output Voltage vs. Supply Voltage

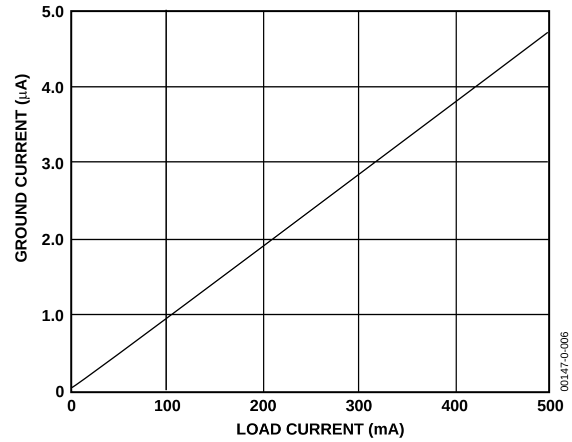


Figure 8. Ground Current vs. Load Current

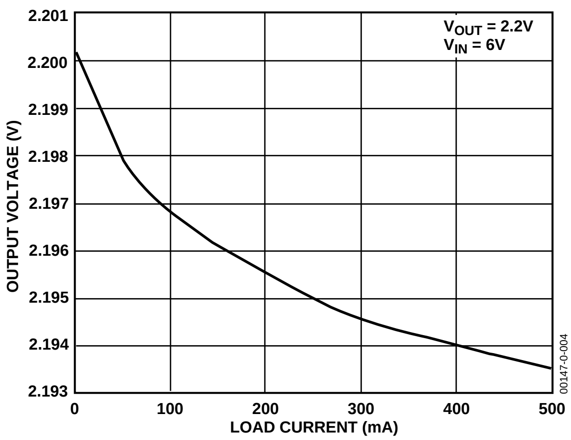


Figure 6. Output Voltage vs. Load Current

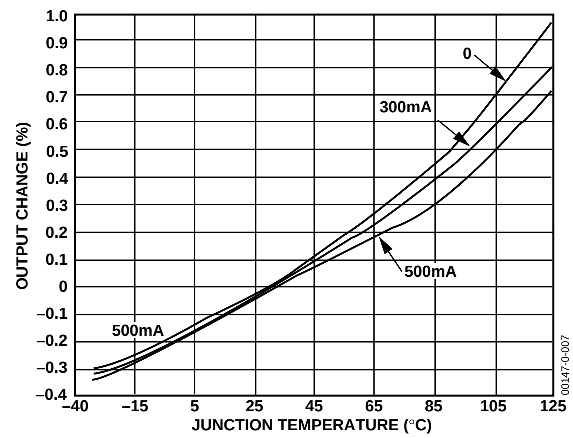


Figure 9. Output Voltage Variation vs. Junction Temperature

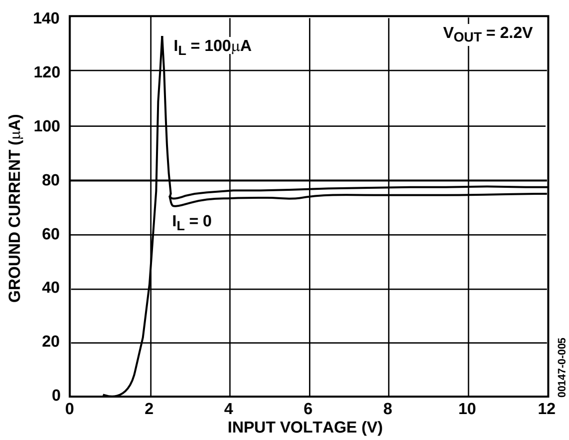


Figure 7. Ground Current vs. Supply Voltage

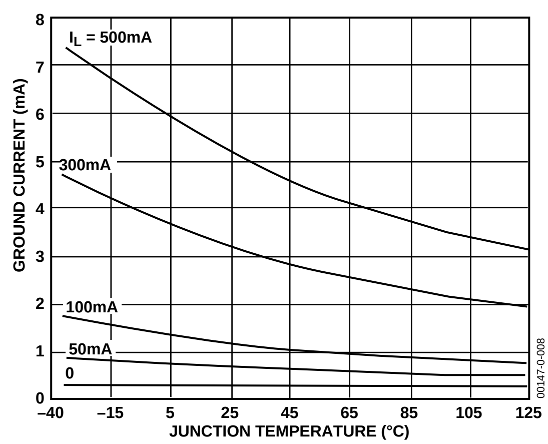


Figure 10. Ground Current vs. Junction Temperature

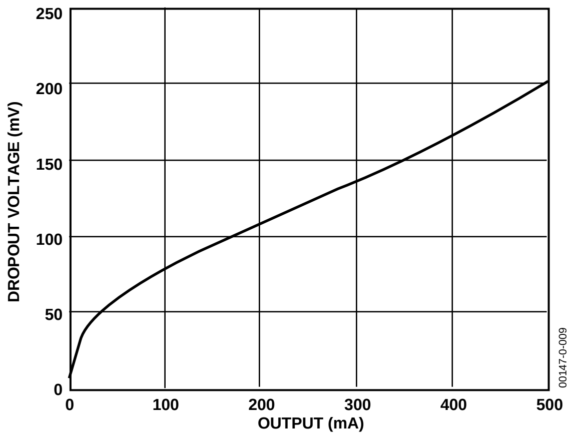


Figure 11. Dropout Voltage vs. Output Current

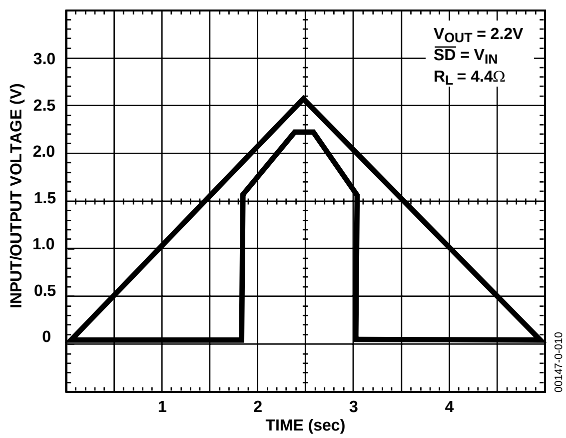


Figure 12. Power-Up/Power-Down

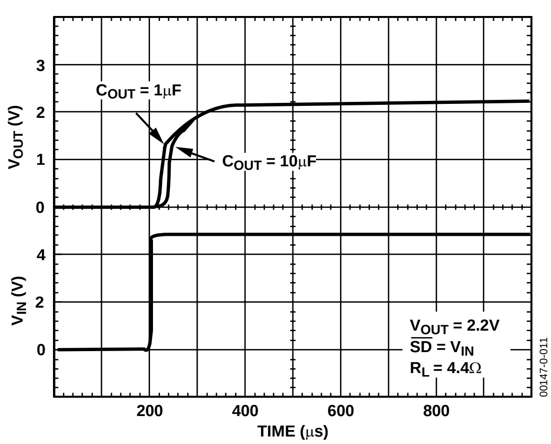


Figure 13. Power-Up Response

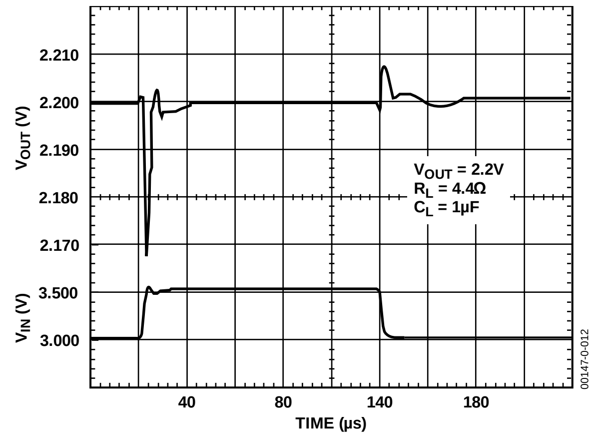


Figure 14. Line Transient Response

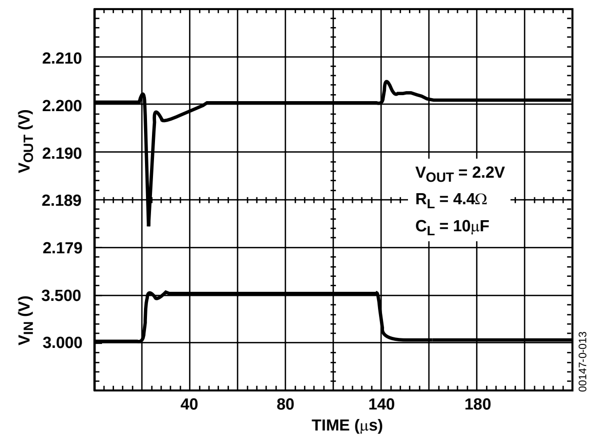


Figure 15. Line Transient Response

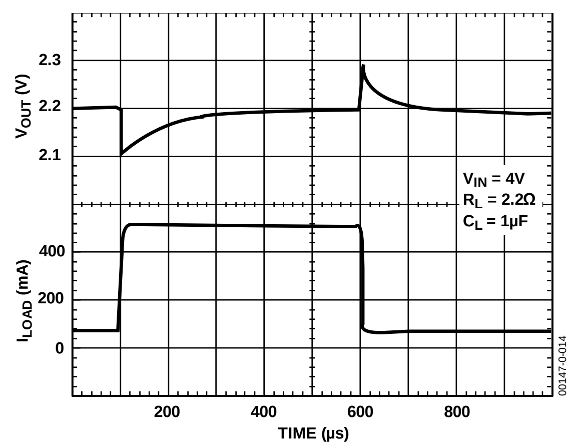


Figure 16. Load Transient Response

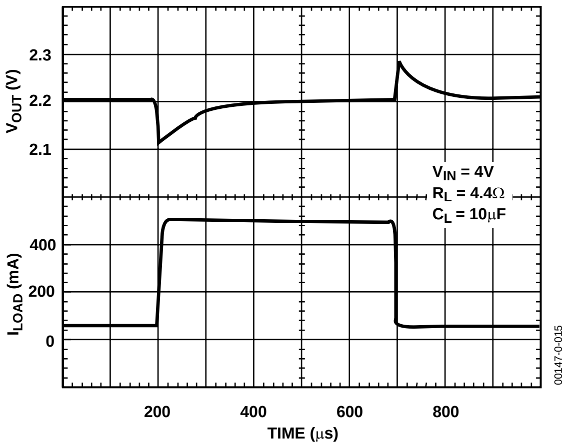


Figure 17. Load Transient Response

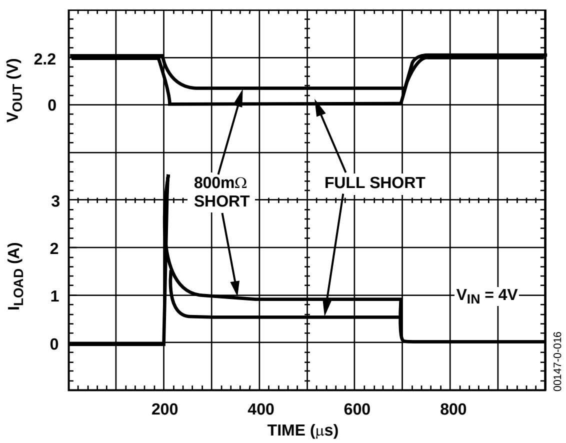


Figure 18. Short-Circuit Current

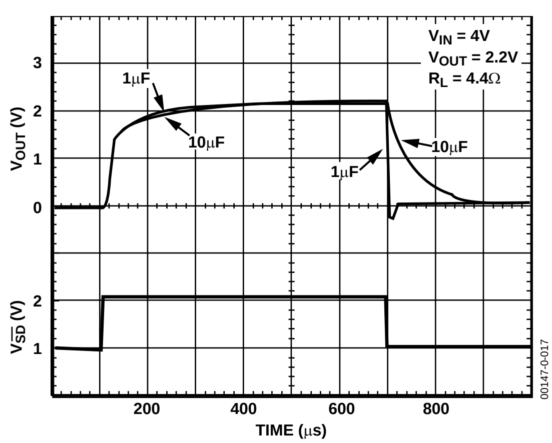


Figure 19. Turn On/Turn Off Response

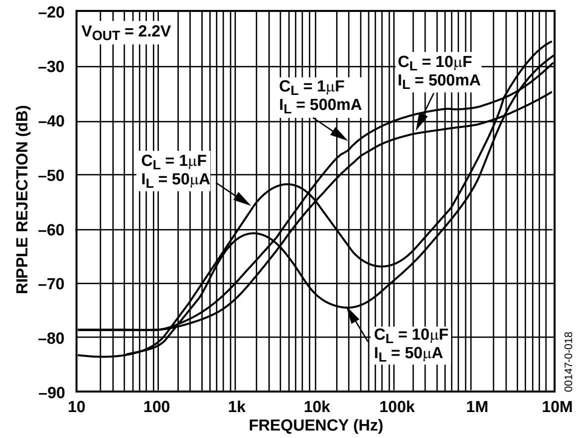


Figure 20. Power Supply Ripple Rejection

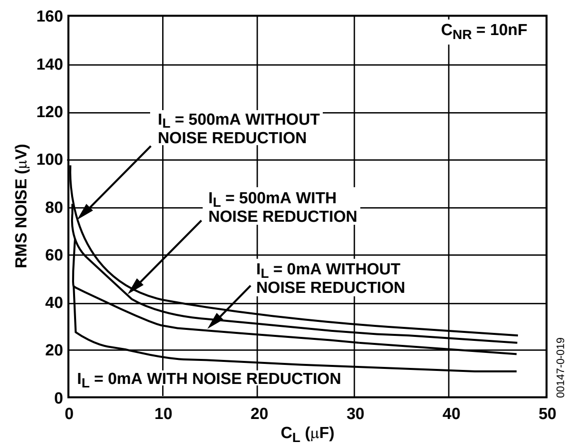


Figure 21. RMS Noise versus C_L (10 Hz to 100 kHz)

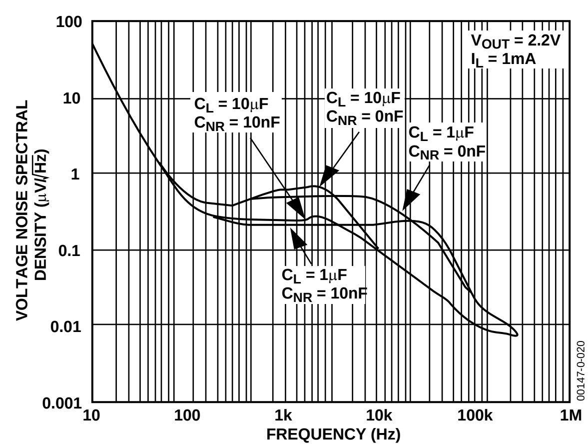


Figure 22. Output Noise Density

THEORY OF OPERATION

The ADP3335 uses a single control loop for regulation and reference functions. The output voltage is sensed by a resistive voltage divider, R1 and R2, which is varied to provide the available output voltage option. Feedback is taken from this network by way of a series diode, D1, and a second resistor divider, R3 and R4, to the input of an amplifier.

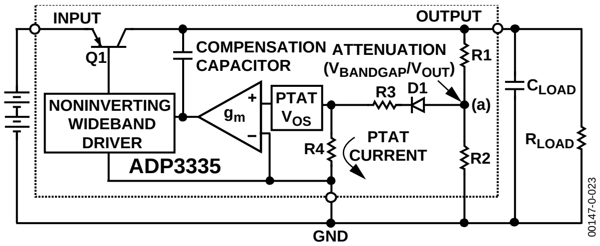


Figure 23. Functional Block Diagram

A very high gain error amplifier is used to control this loop. The amplifier is constructed in such a way that equilibrium produces a large, temperature proportional input offset voltage that is repeatable and very well controlled. The temperature proportional offset voltage combines with the complementary diode voltage to form a virtual band gap voltage implicit in the network, although it never appears explicitly in the circuit.

This patented design makes it possible to control the loop with only one amplifier. This technique also improves the noise characteristics of the amplifier by providing more flexibility in the trade-off of noise sources that leads to a low noise design.

The R1 and R2 divider is chosen in the same ratio as the band gap voltage to the output voltage. Although the R1 and R2 resistor divider is loaded by the D1 diode and a second divider—R3 and R4, the values can be chosen to produce a temperature stable output. This unique arrangement specifically corrects for the loading of the divider, thus avoiding the error resulting from base current loading in conventional circuits.

The patented amplifier controls a new and unique noninverting driver that drives the pass transistor, Q1. This special noninverting driver enables the frequency compensation to include the load capacitor in a pole-splitting arrangement to achieve reduced sensitivity to the value, type, and ESR of the load capacitance.

Most LDOs place very strict requirements on the range of ESR values for the output capacitor, because they are difficult to stabilize due to the uncertainty of load capacitance and resistance. The ESR value required to keep conventional LDOs stable, moreover, changes depending on load and temperature. These ESR limitations make designing with LDOs more difficult because of their unclear specifications and extreme variations over temperature.

With the ADP3335, ESR limitations are no longer a source of design constraints. The ADP3335 can be used with virtually any good quality capacitor and with no constraint on the minimum ESR. This innovative design allows the circuit to be stable with just a small 1 µF capacitor on the output. Additional advantages of the pole-splitting scheme include superior line noise rejection and very high regulator gain, which lead to excellent line and load regulation. Impressive ±1.8% accuracy is guaranteed over line, load, and temperature.

Additional features of the circuit include current limit, thermal shutdown, and noise reduction.

APPLICATIONS INFORMATION

OUTPUT CAPACITOR SELECTION

As with any micropower device, output transient response is a function of the output capacitance. The ADP3335 is stable over a wide range of capacitor values, types, and ESR (anyCAP). A capacitor as low as 1 µF is all that is needed for stability; larger capacitors can be used if high output current surges are anticipated. The ADP3335 is stable with extremely low ESR capacitors (ESR ≈ 0), such as multilayer ceramic capacitors (MLCC) or organic semiconductor electrolytic capacitors (OSCON). Note that the effective capacitance of some capacitor types may fall below the minimum at extreme temperatures. Ensure that the capacitor provides more than 1 µF over the entire temperature range.

INPUT BYPASS CAPACITOR

An input bypass capacitor is not strictly required, but is advisable in any application involving long input wires or high source impedance. Connecting a 1 µF capacitor from IN to ground reduces the circuit's sensitivity to PC board layout. If a larger value output capacitor is used, then a larger value input capacitor is also recommended.

NOISE REDUCTION

A noise reduction capacitor (C_{NR}) can be used, as shown in Figure 24, to further reduce the noise by 6 dB to 10 dB (Figure 22). Low leakage capacitors in the 100 pF to 1 nF range provide the best performance. Since the noise reduction pin, NR, is internally connected to a high impedance node, any connection to this node should be made carefully to avoid noise pickup from external sources. The pad connected to this pin should be as small as possible, and long PC board traces are not recommended.

When adding a noise reduction capacitor, maintain a minimum load current of 1 mA when not in shutdown.

It is important to note that as C_{NR} increases, the turn-on time will be delayed. With NR values greater than 1 nF, this delay may be on the order of several milliseconds.

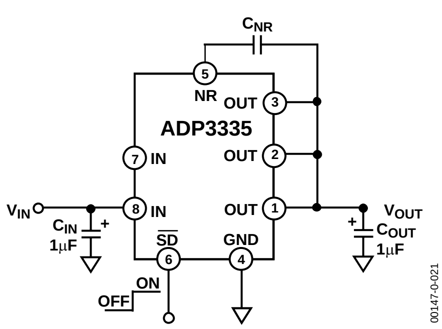


Figure 24. Typical Application Circuit

THERMAL OVERLOAD PROTECTION

The ADP3335 is protected against damage from excessive power dissipation by its thermal overload protection circuit, which limits the die temperature to a maximum of 165°C. Under extreme conditions (i.e., high ambient temperature and power dissipation) where die temperature starts to rise above 165°C, the output current is reduced until the die temperature has dropped to a safe level. The output current is restored when the die temperature is reduced.

Current and thermal limit protections are intended to protect the device against accidental overload conditions. For normal operation, device power dissipation should be externally limited so that junction temperatures will not exceed 150°C.

CALCULATING JUNCTION TEMPERATURE

Device power dissipation is calculated as follows:

$$P_D = (V_{IN} - V_{OUT})I_{LOAD} + (V_{IN})I_{GND}$$

Where I_{LOAD} and I_{GND} are load current and ground current, and V_{IN} and V_{OUT} are input and output voltages, respectively. Assuming I_{LOAD} = 400 mA, I_{GND} = 4 mA, V_{IN} = 5.0 V, and V_{OUT} = 3.3 V, device power dissipation is

$$P_D = (5\text{ V} - 3.3\text{ V})400\text{ mA} + 5.0\text{ V}(4\text{ mA}) = 700\text{ mW}$$

The junction temperature can be calculated from the power dissipation, ambient temperature, and package thermal resistance. The thermal resistance is a function not only of the package, but also of the circuit board layout. Standard test conditions are used to determine the values published in this data sheet, but actual performance will vary. For an LFCSP-8 package mounted on a standard 4-layer board, θ_{JA} is 48°C/W. In the above example, where the power dissipation is 700 mW, the temperature rise above ambient will be approximately equal to

$$\Delta T_{JA} = 0.700\text{ W} \times 48°\text{C/W} = 33.6°\text{C}$$

To limit the maximum junction temperature to 150°C, the maximum allowable ambient temperature will be

$$T_{AMAX} = 150°\text{C} - 33.6°\text{C} = 116.4°\text{C}$$

In this case, the resulting ambient temperature limitation is above the maximum allowable ambient temperature of 85°C.

PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

All surface-mount packages rely on the traces of the PC board to conduct heat away from the package. Use the following general guidelines when designing printed circuit boards to improve both electrical and thermal performance.

1. Keep the output capacitor as close as possible to the output and ground pins.
2. Keep the input capacitor as close as possible to the input and ground pins.
3. PC board traces with larger cross sectional areas will remove more heat from the ADP3335. For optimum heat transfer, specify thick copper and use wide traces.
4. It is not recommended to use solder mask or silkscreen on the PCB traces adjacent to the ADP3335's pins, since doing so will increase the junction-to-ambient thermal resistance of the package.
5. Use additional copper layers or planes to reduce the thermal resistance. When connecting to other layers, use multiple vias, if possible.

LFCSP LAYOUT CONSIDERATIONS

The LFCSP package has an exposed die paddle on the bottom, which efficiently conducts heat to the PCB. In order to achieve the optimum performance from the LFCSP package, special consideration must be given to the layout of the PCB. Use the following layout guidelines for the LFCSP package.

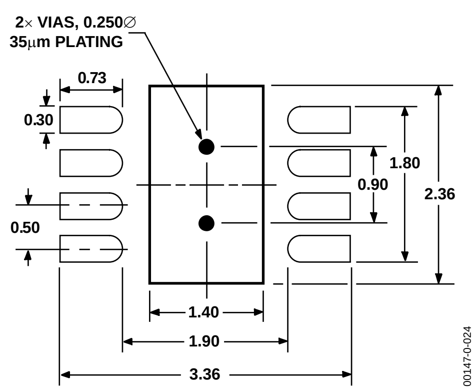


Figure 25. 3 mm × 3 mm LFCSP Pad Pattern (Dimensions shown in millimeters)

1. The pad pattern is given in Figure 25. The pad dimension should be followed closely for reliable solder joints, while maintaining reasonable clearances to prevent solder bridging.
2. The thermal pad of the LFCSP package provides a low thermal impedance path (approximately 20°C/W) to the PCB. Therefore, the PCB must be properly designed to effectively conduct heat away from the package. This is achieved by adding thermal vias to the PCB, which provide a thermal path to the inner or bottom layers. See Figure 25 for the recommended via pattern. Note that the via diameter is small to prevent the solder from flowing through the via and leaving voids in the thermal pad solder joint.

   Also, note that the thermal pad is attached to the die substrate, so the thermal planes to which the thermal vias connect must be electrically isolated or tied to V_{IN}. Do NOT connect the thermal pad to ground.
3. The solder mask opening should be about 120 µ (4.7 mils) larger than the pad size, resulting in a minimum 60 µm (2.4 mils) clearance between the pad and the solder mask.
4. The paste mask opening is typically designed to match the pad size used on the peripheral pads of the LFCSP package. This should provide a reliable solder joint as long as the stencil thickness is about 0.125 mm. The paste mask for the thermal pad needs to be designed for the maximum coverage to effectively remove the heat from the package. However, due to the presence of thermal vias and the size of the thermal pad, eliminating voids may not be possible.
5. The recommended paste mask stencil thickness is 0.125 mm. A laser cut stainless steel stencil with trapezoidal walls should be used. A "No Clean" Type 3 solder paste should be used for mounting the LFCSP package. Also, a nitrogen purge during the reflow process is recommended.
6. The package manufacturer recommends that the reflow temperature should not exceed 220°C and the time above liquidus is less than 75 seconds. The preheat ramp should be 3°C/second or lower. The actual temperature profile depends on the board density and must be determined by the assembly house as to what works best.

SHUTDOWN MODE

Applying a TTL high signal to the shutdown ($\overline{SD}$) pin or tying it to the input pin, turns the output ON. Pulling $\overline{SD}$ down to 0.4 V or below, or tying it to ground, turns the output OFF. In shutdown mode, quiescent current is reduced to a typical value of 10 nA.

OUTLINE DIMENSIONS

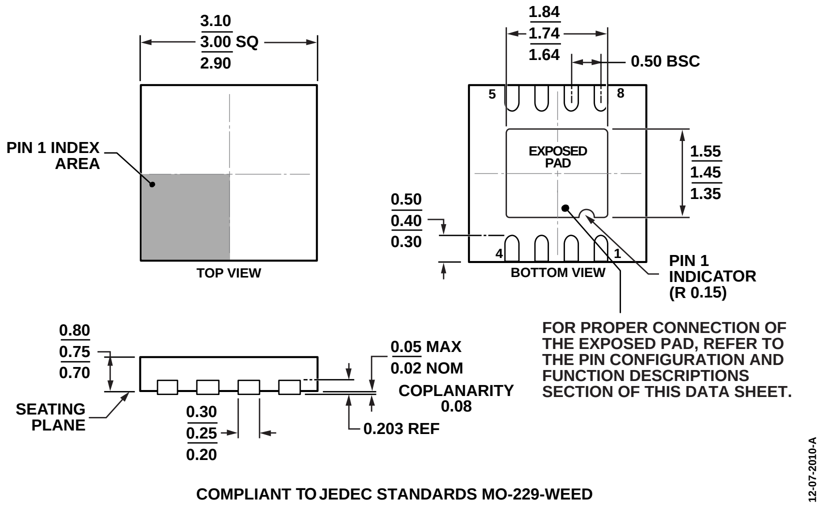


Figure 26. 8-Lead Lead Frame Chip Scale Package [LFCSP_WD]
3 mm × 3 mm Body, Very Very Thin, Dual Lead
(CP-8-13)
Dimensions shown in millimeters

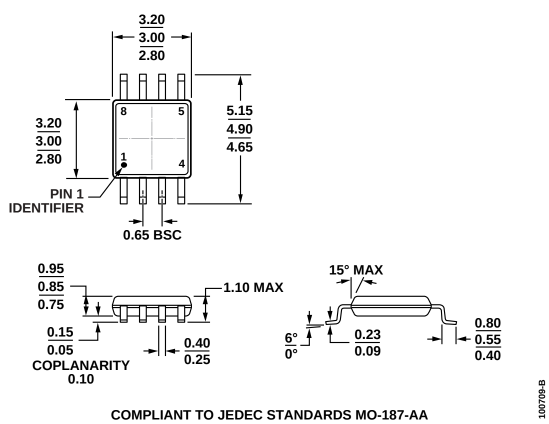


Figure 27. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Output Voltage (V)[2]	Temperature Range	Package Description	Package Option	Branding[3]
ADP3335ACPZ-1.8-R7	1.8	−40°C to +85°C	8-Lead LFCSP_WD	CP-8-13	L1G
ADP3335ACPZ-2.5-R7	2.5	−40°C to +85°C	8-Lead LFCSP_WD	CP-8-13	L1H
ADP3335ACPZ-2.85R7	2.85	−40°C to +85°C	8-Lead LFCSP_WD	CP-8-13	L1J
ADP3335ACPZ-3.3-R7	3.3	−40°C to +85°C	8-Lead LFCSP_WD	CP-8-13	L1K
ADP3335ACPZ-3.3-RL	3.3	−40°C to +85°C	8-Lead LFCSP_WD	CP-8-13	L1K
ADP3335ACPZ-5-R7	5	−40°C to +85°C	8-Lead LFCSP_WD	CP-8-13	L1L
ADP3335ARMZ-1.8-R7	1.8	−40°C to +85°C	8-Lead MSOP	RM-8	LFA
ADP3335ARMZ-1.8-RL	1.8	−40°C to +85°C	8-Lead MSOP	RM-8	LFA
ADP3335ARMZ-2.5-RL	2.5	−40°C to +85°C	8-Lead MSOP	RM-8	LFC
ADP3335ARMZ-2.5RL7	2.5	−40°C to +85°C	8-Lead MSOP	RM-8	LFC
ADP3335ARMZ-2.85R7	2.85	−40°C to +85°C	8-Lead MSOP	RM-8	LFD
ADP3335ARMZ-2.85RL	2.85	−40°C to +85°C	8-Lead MSOP	RM-8	LFD
ADP3335ARMZ-3.3-RL	3.3	−40°C to +85°C	8-Lead MSOP	RM-8	LFE
ADP3335ARMZ-3.3RL7	3.3	−40°C to +85°C	8-Lead MSOP	RM-8	LFE
ADP3335ARMZ-5-R7	5	−40°C to +85°C	8-Lead MSOP	RM-8	LFF
ADP3335ARMZ-5-REEL	5	−40°C to +85°C	8-Lead MSOP	RM-8	LFF

[1] Z = RoHS Compliant Part.
[2] For additional voltage options, contact a local sales or distribution representative.
[3] Z = RoHS Compliant Parts have a "#" marked on the device preceding the date code.

NOTES

NOTES

NOTES

D00147-0-10/13(D)

ANALOG DEVICES

www.analog.com