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REVISION HISTORY

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SPECIFICATIONS

5 V SINGLE SUPPLY

V_{DD} = 5 V ± 10%, V_{SS} = 0 V, and GND = 0 V, unless otherwise noted. Temperature range is −40°C to +85°C.

Table 1.

Parameter	+25°C	−40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On Resistance, R_{ON}	2.5		Ω typ	V_S = 0 V to V_{DD}, I_S = 10 mA
	4.5	5	Ω max	
On Resistance Match Between Channels, ΔR_{ON}		0.4	Ω typ	
		0.8	Ω max	V_S = 0 V to V_{DD}, I_S = 10 mA
On Resistance Flatness, $R_{FLAT(ON)}$	0.6		Ω typ	V_S = 0 V to V_{DD}, I_S = 10 mA
		1.2	Ω max	
LEAKAGE CURRENTS				V_{DD} = 5.5 V
Source Off Leakage, $I_{S (OFF)}$	±0.01		nA typ	V_D = 4.5 V/1 V, V_S = 1 V/4.5 V
	±0.1	±0.3	nA max	
Drain Off Leakage, $I_{D (OFF)}$	±0.01		nA typ	V_D = 4.5 V/1 V, V_S = 1 V/4.5 V
	±0.1	±0.3	nA max	
Channel On Leakage, $I_{D (ON)}$, $I_{S (ON)}$	±0.01		nA typ	V_D = V_S = 1 V or 4.5 V
	±0.1	±0.3	nA max	
DIGITAL INPUTS				
Input Voltage				
High, V_{INH}		2.4	V min	
Low, V_{INL}		0.8	V max	
High or Low Input Current, I_{INH} or I_{INL}	0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	μA max	
Digital Input Capacitance, C_{IN}	3		pF typ	
DIGITAL OUTPUT, ADG714, DOUT				
Output Voltage Low, V_{OL}		0.4	V max	I_{SINK} = 6 mA
Digital Output Capacitance, C_{OUT}	4		pF typ	
DIGITAL INPUTS, SCL, SDA				
Input Voltage				
High, V_{INH}		0.7 × V_{DD}	V min	
		V_{DD} + 0.3	V max	
High, V_{INH}		−0.3	V min	
		0.3 × V_{DD}	V max	
Input Leakage Current, I_{IN}	0.005		μA typ	V_{IN} = 0 V to V_{DD}
		±1	μA max	
Input Hysteresis, V_{HYST}	0.05 × V_{DD}		V min	
Input Capacitance, C_{IN}	6		pF typ	
LOGIC OUTPUT, SDA				
Output Voltage Low, V_{OL}		0.4	V max	I_{SINK} = 3 mA
		0.6	V max	I_{SINK} = 6 mA
DYNAMIC CHARACTERISTICS				
On Time, t_{ON}				
ADG714	20		ns typ	V_S = 3 V, R_L = 300 Ω, C_L = 35 pF
		32	ns max	
ADG715	95		ns typ	V_S = 3 V, R_L = 300 Ω, C_L = 35 pF
		140	ns max	

Parameter	+25°C	−40°C to +85°C	Unit	Test Conditions/Comments
Off Time, t_{OFF}				
ADG714	8		ns typ	V_S = 3 V, R_L = 300 Ω, C_L = 35 pF
		15	ns max	
ADG715	85		ns typ	V_S = 3 V, R_L = 300 Ω, C_L = 35 pF
		130	ns max	
Break-Before-Make Time Delay, t_D	8		ns typ	V_S = 3 V, R_L = 300 Ω, C_L = 35 pF
		1	ns min	
Charge Injection, Q_{INJ}	±3		pC typ	V_S = 2 V, R_S = 0 Ω, C_L = 1 nF
Off Isolation	−60		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz
	−80		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz
Channel to Channel Crosstalk	−70		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz
	−90		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz
−3 dB Bandwidth	155		MHz typ	R_L = 50 Ω, C_L = 5 pF
Insertion Loss	−0.3		dB typ	
Off Switch Source Capacitance, $C_{S\ (OFF)}$	11		pF typ	
Off Switch Drain Capacitance, $C_{D\ (OFF)}$	11		pF typ	
On Switch Capacitance, $C_{D\ (ON)}$, $C_{S\ (ON)}$	22		pF typ	
POWER REQUIREMENTS				V_{DD} = 5.5 V
Positive Power Supply Current, I_{DD}	10		μA typ	Digital inputs = 0 V or 5.5 V
		20	μA max	

3 V SINGLE SUPPLY

V_{DD} = 3 V ± 10%, V_{SS} = 0 V, and GND = 0 V, unless otherwise noted. Temperature range is −40°C to +85°C.

Table 2.

Parameter	+25°C	−40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On Resistance, R_{ON}	6		Ω typ	V_S = 0 V to V_{DD}, I_S = 10 mA
	11	12	Ω max	
On Resistance Match Between Channels, ΔR_{ON}		0.4	Ω typ	V_S = 0 V to V_{DD}, I_S = 10 mA
		1.2	Ω max	
On Resistance Flatness, $R_{FLAT(ON)}$		3.5	Ω typ	V_S = 0 V to V_{DD}, I_S = 10 mA
LEAKAGE CURRENTS				V_{DD} = 3.3 V
Source OFF Leakage, $I_{S\ (OFF)}$	±0.01		nA typ	V_S = 3 V/1 V, V_D = 1 V/3 V
	±0.1	±0.3	nA max	
Drain OFF Leakage, $I_{D\ (OFF)}$	±0.01		nA typ	V_S = 1 V/3 V, V_D = 3 V/1 V
	±0.1	±0.3	nA max	
Channel ON Leakage, $I_{D\ (ON)}$, $I_{S\ (ON)}$	±0.01		nA typ	V_S = V_D = 1 V or 3 V
	±0.1	±0.3	nA max	
DIGITAL INPUTS				
Input Voltage				
High, V_{INH}		2.0	V min	
Low, V_{INL}		0.8	V max	
High or Low Input Current, I_{INH} or I_{INL}	0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	μA max	
Digital Input Capacitance, C_{IN}	3		pF typ	
DIGITAL OUTPUT, ADG714, DOUT				
Output Voltage Low, V_{OL}		0.4	V max	I_{SINK} = 6 mA
Digital Output Capacitance, C_{OUT}	4		pF typ	

Parameter	+25°C	−40°C to +85°C	Unit	Test Conditions/Comments
DIGITAL INPUTS, SCL, SDA				
Input Voltage				
High, V_{INH}		0.7 × V_{DD}	V min	
		V_{DD} + 0.3	V max	
Low, V_{INL}		−0.3	V min	
		0.3 × V_{DD}	V max	
Input Leakage Current, I_{IN}	0.005		μA typ	V_{IN} = 0 V to V_{DD}
		±1	μA max	
Input Hysteresis, V_{HYST}	0.05 × V_{DD}		V min	
Input Capacitance, C_{IN}	6		pF typ	
LOGIC OUTPUT, (SDA)				
Output Voltage Low, V_{OL}		0.4	V max	I_{SINK} = 3 mA
		0.6	V max	I_{SINK} = 6 mA
DYNAMIC CHARACTERISTICS				
On Time, t_{ON}				
ADG714	35		ns typ	V_S = 2 V, R_L = 300 Ω, C_L = 35 pF
		65	ns max	
ADG715	130		ns typ	V_S = 2 V, R_L = 300 Ω, C_L = 35 pF
		200	ns max	
Off Time, t_{OFF}				
ADG714	11		ns typ	V_S = 2 V, R_L = 300 Ω, C_L = 35 pF
		20	ns max	
ADG715	115		ns typ	V_S = 2 V, R_L = 300 Ω, C_L = 35 pF
		180	ns max	
Break-Before-Make Time Delay, t_D	8		ns typ	V_S = 2 V, R_L = 300 Ω, C_L = 35 pF
		1	ns min	
Charge Injection, Q_{INJ}	±2		pC typ	V_S = 1.5 V, R_S = 0 Ω, C_L = 1 nF
Off Isolation	−60		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz
	−80		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz
Channel to Channel Crosstalk	−70		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz
	−90		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz
−3 dB Bandwidth	155		MHz typ	R_L = 50 Ω, C_L = 5 pF
Insertion Loss	−0.4		dB typ	
Off Switch Source Capacitance, $C_{S (OFF)}$	11		pF typ	
Off Switch Drain Capacitance, $C_{D (OFF)}$	11		pF typ	
On Switch Capacitance, $C_{D (ON)}$, $C_{S (ON)}$	22		pF typ	
POWER REQUIREMENTS				V_{DD} = 3.3 V
Positive Power Supply Current, I_{DD}	10		μA typ	Digital inputs = 0 V or 3.3 V
		20	μA max	

±2.5 V DUAL SUPPLY

V_{DD} = +2.5 V ± 10%, V_{SS} = −2.5 V ± 10%, and GND = 0 V, unless otherwise noted. Temperature range is −40°C to +85°C.

Table 3.

Parameter	+25°C	−40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		V_{SS} to V_{DD}	V	
On Resistance, R_{ON}	2.5		Ω typ	V_S = V_{SS} to V_{DD}, I_{DS} = 10 mA
	4.5	5	Ω max	
On Resistance Match Between Channels, ΔR_{ON}		0.4	Ω typ	V_S = V_{SS} to V_{DD}, I_{DS} = 10 mA
		0.8	Ω max	
On Resistance Flatness, $R_{FLAT(ON)}$	0.6		Ω typ	V_S = V_{SS} to V_{DD}, I_{DS} = 10 mA
		1	Ω max	

Parameter	+25°C	−40°C to +85°C	Unit	Test Conditions/Comments
LEAKAGE CURRENTS				V_{DD} = +2.75 V, V_{SS} = −2.75 V
Source Off Leakage, $I_{S\ (OFF)}$	±0.01		nA typ	V_S = +2.25 V/−1.25 V, V_D = −1.25 V/+2.25 V
	±0.1	±0.3	nA max	
Drain Off Leakage, $I_{D\ (OFF)}$	±0.01		nA typ	V_S = +2.25 V/−1.25 V, V_D = −1.25 V/+2.25 V
	±0.1	±0.3	nA max	
Channel On Leakage, $I_{D\ (ON)}$, $I_{S\ (ON)}$	±0.01		nA typ	V_S = V_D = +2.25 V/−1.25 V
	±0.1	±0.3	nA max	
DIGITAL INPUTS				
Input Voltage				
High, V_{INH}		1.7	V min	
Low, V_{INL}		0.7	V max	
High or Low Input Current, I_{INH} or I_{INL}	0.005		µA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	µA max	
Digital Input Capacitance, C_{IN}	3		pF typ	
DIGITAL OUTPUT, ADG714, DOUT				
Output Voltage Low, V_{OL}		0.4	V max	I_{SINK} = 6 mA
Digital Output Capacitance, C_{OUT}	4		pF typ	
DIGITAL INPUTS, SCL, SDA				
Input Voltage				
High, V_{INH}		0.7 × V_{DD}	V min	
		V_{DD} + 0.3	V max	
High, V_{INH}		−0.3	V min	
		0.3 × V_{DD}	V max	
Input Leakage Current, I_{IN}	0.005		µA typ	V_{IN} = 0 V to V_{DD}
		±1	µA max	
Input Hysteresis, V_{HYST}	0.05 × V_{DD}		V min	
Input Capacitance, C_{IN}	6		pF typ	
LOGIC OUTPUT, SDA				
Output Voltage				
Low, V_{OL}		0.4	V max	I_{SINK} = 3 mA
		0.6	V max	I_{SINK} = 6 mA
DYNAMIC CHARACTERISTICS				
On Time, t_{ON}				
ADG714	20		ns typ	V_S = 1.5 V, R_L = 300 Ω, C_L = 35 pF
		32	ns max	
ADG715	133		ns typ	V_S = 1.5 V, R_L = 300 Ω, C_L = 35 pF
		200	ns max	
Off Time, t_{OFF}				
ADG714	8		ns typ	V_S = 1.5 V, R_L = 300 Ω, C_L = 35 pF
		18	ns max	
ADG715	124		ns typ	V_S = 1.5 V, R_L = 300 Ω, C_L = 35 pF
		190	ns max	
Break-Before-Make Time Delay, t_D	8		ns typ	V_S = 1.5 V, R_L = 300 Ω, C_L = 35 pF
		1	ns min	
Charge Injection, Q_{INJ}	±3		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF
Off Isolation	−60		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz
	−80		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz
Channel to Channel Crosstalk	−70		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz
	−90		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz
−3 dB Bandwidth	155		MHz typ	R_L = 50 Ω, C_L = 5 pF
Insertion Loss	−0.3		dB typ	

Parameter	+25°C	−40°C to +85°C	Unit	Test Conditions/Comments
Off Switch Source Capacitance, $C_{S\ (OFF)}$	11		pF typ	
Off Switch Drain Capacitance, $C_{D\ (OFF)}$	11		pF typ	
On Switch Capacitance, $C_{D\ (ON)}$, $C_{S\ (ON)}$	22		pF typ	
POWER REQUIREMENTS				V_{DD} = +2.75 V, V_{SS} = −2.75 V
Positive Power Supply Current, I_{DD}	15		µA typ	Digital inputs = 0 V or V_{DD}
		25	µA max	
Negative Power Supply Current, I_{SS}	15		µA typ	
		25	µA max	

TIMING CHARACTERISTICS

ADG714

V_{DD} = 2.7 V to 5.5 V. All specifications are from −40°C to +85°C, unless otherwise noted. See Figure 3. All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.

Table 4.

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Conditions/Comments
f_{SCLK}	30	MHz max	SCLK cycle frequency
t_1	33	ns min	SCLK cycle time
t_2	13	ns min	SCLK high time
t_3	13	ns min	SCLK low time
t_4	0	ns min	$\overline{SYNC}$ to SCLK rising edge setup time
t_5	5	ns min	Data setup time
t_6	4.5	ns min	Data hold time
t_7	0	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge
t_8	33	ns min	Minimum $\overline{SYNC}$ high time
t_9[1]	20	ns max	SCLK rising edge to DOUT valid
t_{10}	0	ns min	SCLK falling edge to $\overline{SYNC}$ falling edge
t_{11}	6	ns max	$\overline{SYNC}$ rising edge to SCLK rising edge

[1] C_L = 20 pF, R_L = 1 kΩ.

ADG715

V_{DD} = 2.7 V to 5.5 V. All specifications are from −40°C to +85°C, unless otherwise noted. See Figure 4.

Table 5.

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Conditions/Comments
f_{SCL}	400	kHz max	SCL clock frequency
t_1	2.5	µs min	SCL cycle time
t_2	0.6	µs min	SCL high time, t_{HIGH}
t_3	1.3	µs min	SCL low time, t_{LOW}
t_4	0.6	µs min	Start/repeated start condition hold time, $t_{HD, STA}$
t_5	100	ns min	Data setup time, $t_{SU, DAT}$
t_6[1]	0.9	µs max	Data hold time, $t_{HD, DAT}$
	0	µs min	
t_7	0.6	µs min	Setup time for repeated start, $t_{SU, STA}$
t_8	0.6	µs min	Stop condition setup time, $t_{SU, STO}$
t_9	1.3	µs min	Bus free time between a stop condition and a start condition, t_{BUF}
t_{10}	300	ns max	Rise time of both SCL and SDA when receiving, t_R
	$20 + 0.1C_b$[2]	ns min	
t_{11}	250	ns max	Fall time of SDA when receiving, t_F
t_{11}	300	ns max	Fall time of SDA when transmitting, t_F
	$0.1C_b$[2]	ns min	

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Conditions/Comments
C_b	400	pF max	Capacitive load for each bus line
t_{SP}[3]	50	ns max	Pulse width of spike suppressed

[1] A master device must provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IH} min of the SCL signal) to bridge the undefined region of the falling edge of SCL.
[2] C_b is the total capacitance of one bus line in pF. t_R and t_F measured between 0.3 × V_{DD} and 0.7 × V_{DD}.
[3] Input filtering on both the SCL and SDA inputs suppress noise spikes that are less than 50 ns.

Timing Diagrams

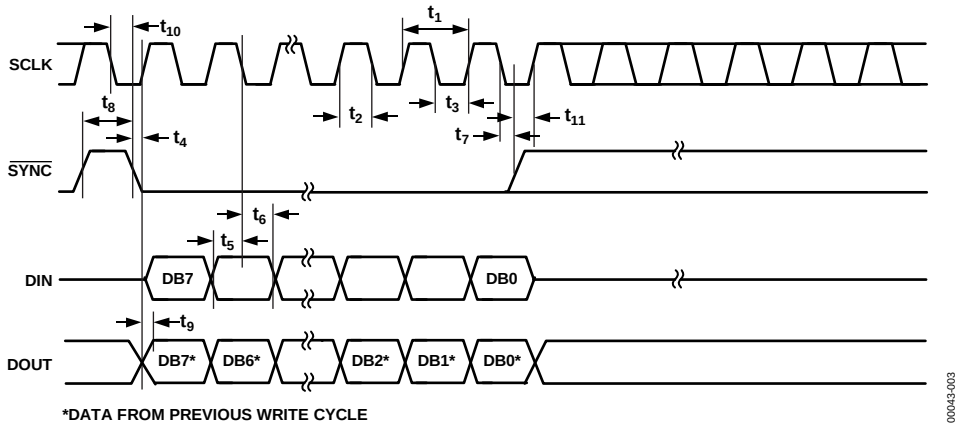


Figure 3. 3-Wire Serial Interface Timing Diagram

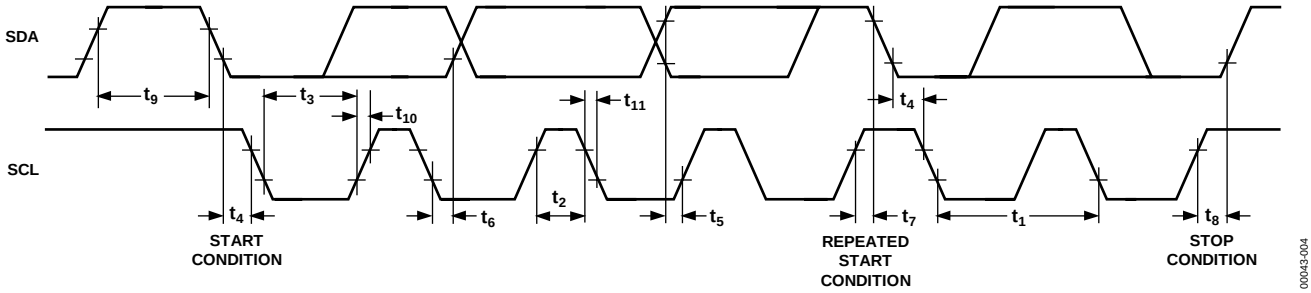


Figure 4. 2-Wire Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
V_{DD} to V_{SS}	7 V
V_{DD} to GND	−0.3 V to +7 V
V_{SS} to GND	+0.3 V to −3.5 V
Analog Inputs[1]	V_{SS} −0.3 V to V_{DD} +0.3 V or 30 mA, whichever occurs first
Digital Inputs[1]	−0.3 V to V_{DD} +0.3 V or 30 mA, whichever occurs first
Peak Current, Sx or Dx	100 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, Sx or Dx	30 mA
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Lead Temperature, Soldering (10 sec)	300°C
Infrared Reflow (20 sec)	235°C

[1] Overvoltages at the DIN pin, Sx, or Dx are clamped by internal diodes. Limit current to the given maximum ratings.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment.

Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection, junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
RU-24	128	42	°C/W
CP-24-10	127.99[1]	15.38[2]	°C/W

[1] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board. See JEDEC JESD-51.
[2] Thermal impedance simulated values are based on a cool plate location at the top of the package and measured at the bottom of the exposed paddle of the LFCSP.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

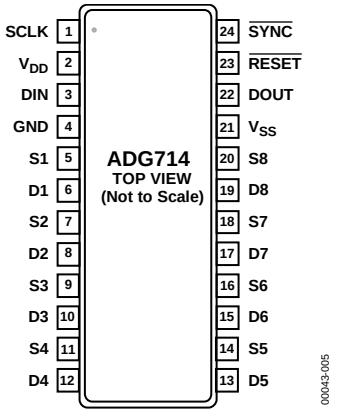


Figure 5. ADG714 TSSOP Pin Configuration

Table 8. ADG714 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. These devices accommodate serial input rates of up to 30 MHz.
2	V_{DD}	Positive Analog Supply Voltage.
3	DIN	Serial Data Input. Data is clocked into the 8-bit input register on the falling edge of the serial clock input.
4	GND	Ground Reference.
5, 7, 9, 11, 14, 16, 18, 20	Sx	Source. These pins may be an input or an output.
6, 8, 10, 12, 13, 15, 17, 19	Dx	Drain. These pins may be an input or an output.
21	V_{SS}	Negative Analog Supply Voltage. For single-supply operation, tie this pin to ground.
22	DOUT	Serial Data Output. This pin allows a number of devices to be daisy-chained. Data is clocked out of the input shift register on the rising edge of SCLK. DOUT is an open-drain output that is pulled to the supply with an external pull-up resistor.
23	$\overline{\text{RESET}}$	Active Low Control Input. This pin clears the input register and turns all switches to the off condition.
24	$\overline{\text{SYNC}}$	Active Low Control Input. This pin is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, this pin powers on the SCLK and DIN buffers and the input shift register is enabled. Data is transferred on the falling edges of the following clock cycle. Taking $\overline{\text{SYNC}}$ high updates the switches.

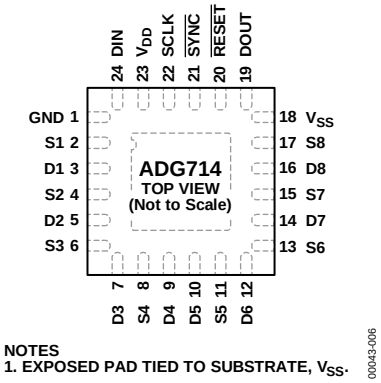


Figure 6. ADG714 LFCSP Pin Configuration

Table 9. ADG714 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	GND	Ground (0 V) Reference.
2, 4, 6, 8, 11, 13, 15, 17	Sx	Source. These pins may be an input or an output.
3, 5, 7, 9, 10, 12, 14, 16	Dx	Drain. These pins may be an input or an output.
18	V_{SS}	Most Negative Power Supply Potential. In single-supply applications, V_{SS} is connected to ground.
19	DOUT	Serial Data Output. This pin is used for daisy-chaining a number of these devices together or for reading back data in the shift register for diagnostic purposes. The serial data is transferred on the rising edge of SCLK and is valid on the falling edge of the clock. Pull this open-drain output to the supply with an external resistor.
20	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$. Under normal operation, drive the $\overline{\text{RESET}}$ pin with a 2.7 V to 5 V supply. Pull the pin low (<0.8 V) for a short period (15 ns is sufficient) to complete a hardware reset. All switches are opened and the appropriate registers are cleared to 0. When using the $\overline{\text{RESET}}$ pin to complete a hardware reset, all other SPI pins ($\overline{\text{SYNC}}$, SCLK, and DIN) must be driven low.
21	$\overline{\text{SYNC}}$	Active Low Control Input. This pin is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, this pin powers on the SCLK and DIN buffers and enables the input shift register. Data is transferred in on the falling edges of the following clock cycle. Taking $\overline{\text{SYNC}}$ high updates the switch condition.
22	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data is transferred at rates of up to 50 MHz.
23	V_{DD}	Most Positive Power Supply Potential.
24	DIN	Serial Data Input. This device has an 8-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
EP	EP	Exposed Pad. Exposed pad tied to the substrate, V_{SS}.

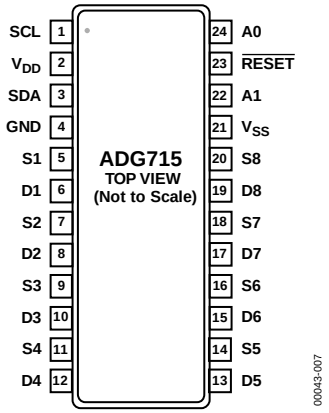


Figure 7. ADG715 Pin Configuration

Table 10. ADG715 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SCL	Serial Clock Line. This pin is used in conjunction with the SDA line to clock data into the 8-bit input shift register. Clock rates of up to 400 kbps are accommodated with this 2-wire serial interface.
2	V_{DD}	Positive Analog Supply Voltage.
3	SDA	Serial Data Line. This pin is used in conjunction with the SCL line to clock data into the 8-bit input shift register during the write cycle and used to read back one byte of data during the read cycle. SDA is a bidirectional open-drain data line that is pulled to the supply with an external pull-up resistor.
4	GND	Ground Reference.
5, 7, 9, 11, 14, 16, 18, 20	Sx	Source. These pins may be an input or an output.
6, 8, 10, 12, 13, 15, 17, 19	Dx	Drain. These pins may be an input or an output.
21	V_{SS}	Negative Analog Supply Voltage. For single-supply operation, tie this pin to ground.
22	A1	Address Input. This pin sets the second LSB of the 7-bit slave address.
23	$\overline{\text{RESET}}$	Active Low Control Input. This pin clears the input register and turns all switches to the off condition.
24	A0	Address Input. This pin sets the LSB of the 7-bit slave address.

TYPICAL PERFORMANCE CHARACTERISTICS

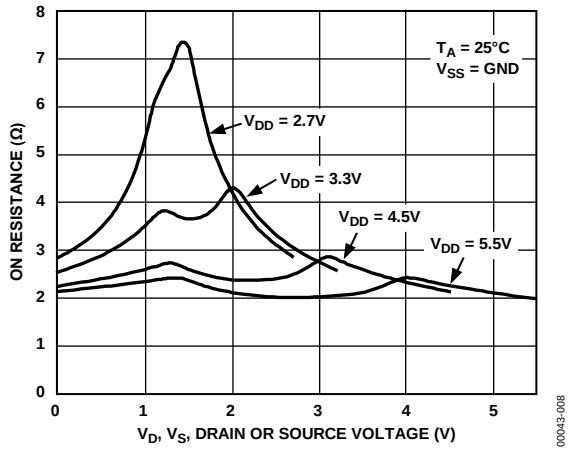


Figure 8. On Resistance as a Function of V_D (V_S), Single Supply

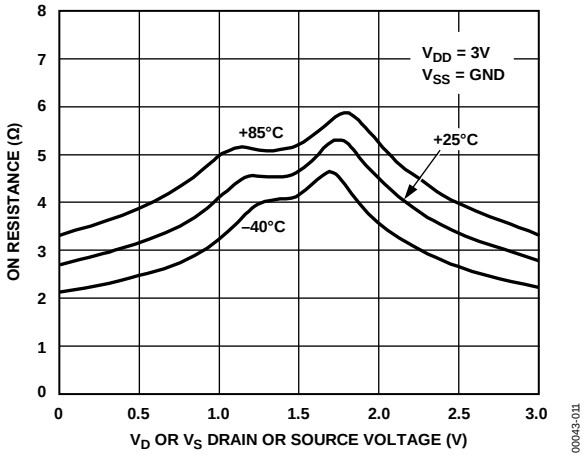


Figure 11. On Resistance as a Function of V_D (V_S) for Different Temperatures, V_{DD} = 3 V

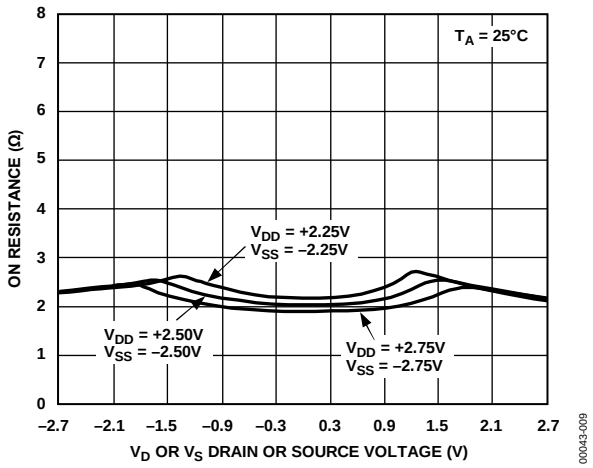


Figure 9. On Resistance as a Function of V_D (V_S), Dual Supply

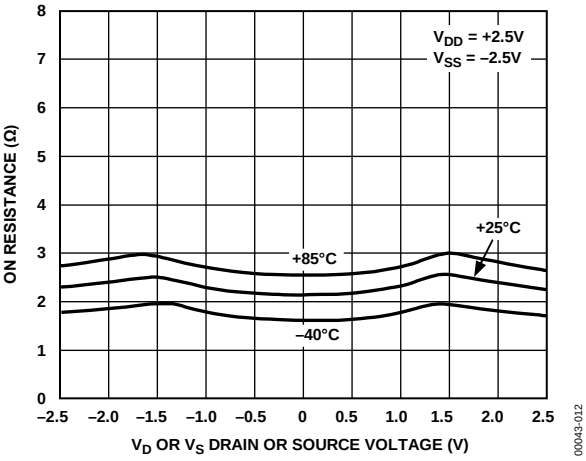


Figure 12. On Resistance as a Function of V_D (V_S) for Different Temperatures, Dual Supply

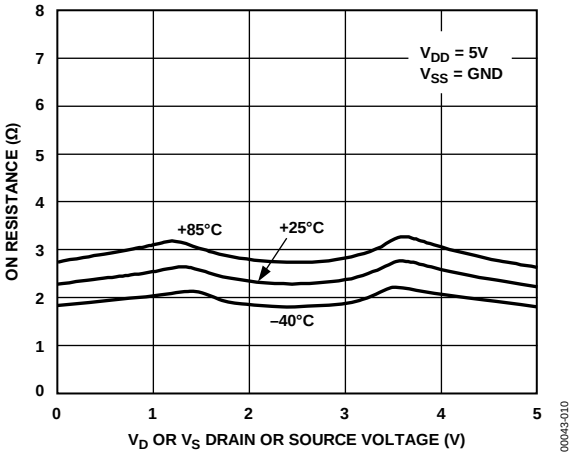


Figure 10. On Resistance as a Function of V_D (V_S) for Different Temperatures, V_{DD} = 5 V

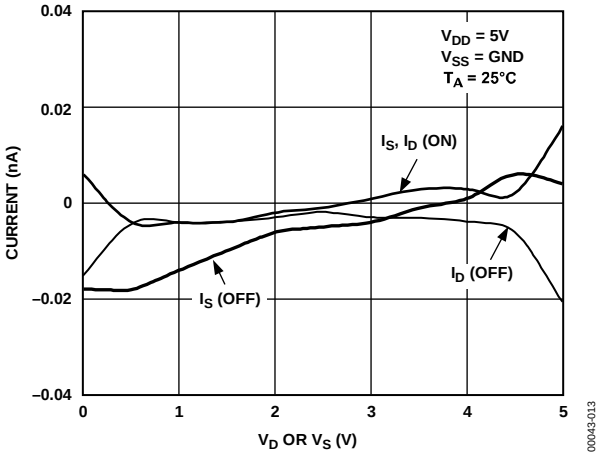


Figure 13. Leakage Currents as a Function of V_D (V_S)

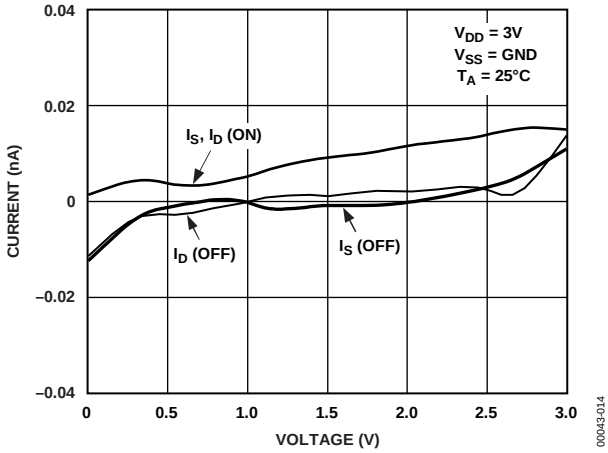


Figure 14. Leakage Currents as a Function of V_D (V_S), Single Supply

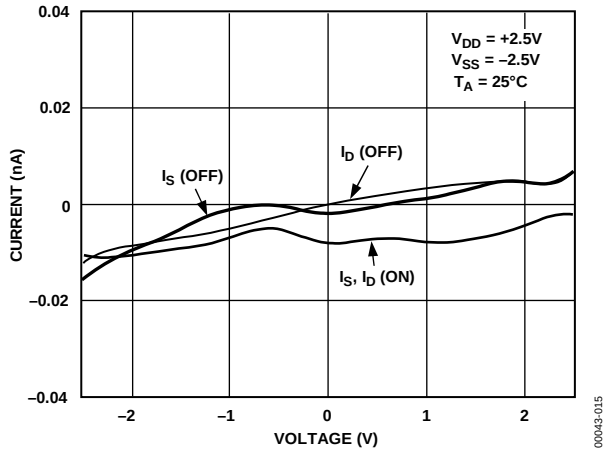


Figure 15. Leakage Currents as a Function of V_D (V_S), Dual Supply

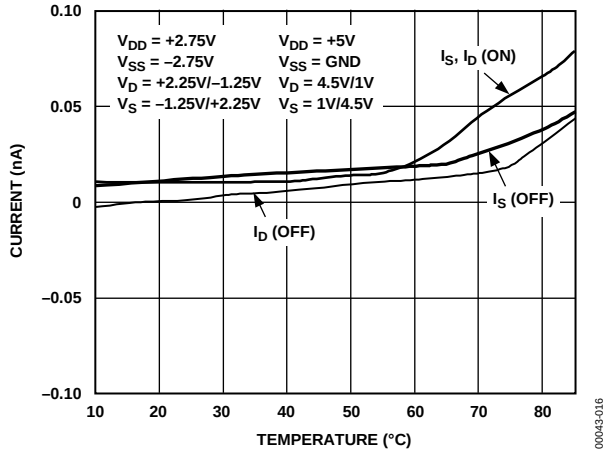


Figure 16. Leakage Currents as a Function of Temperature at ±2.75 V Dual Supply and +5 V Single Supply

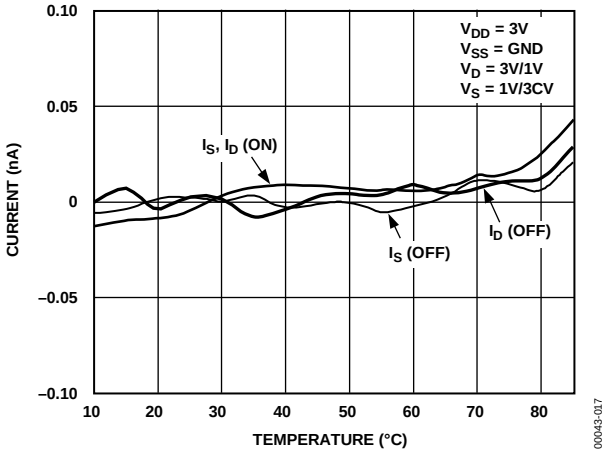


Figure 17. Leakage Currents as a Function of Temperature at 3 V Single Supply

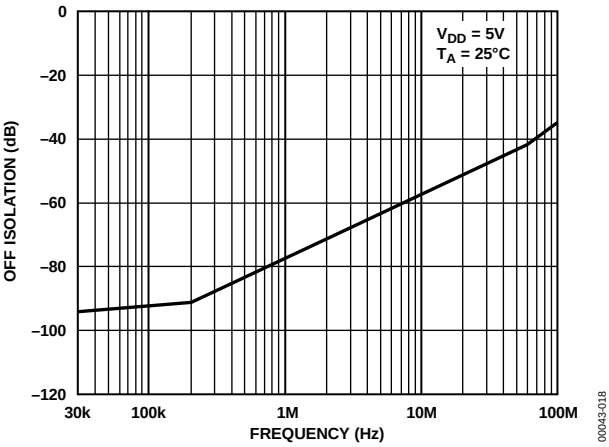


Figure 18. Off Isolation vs. Frequency

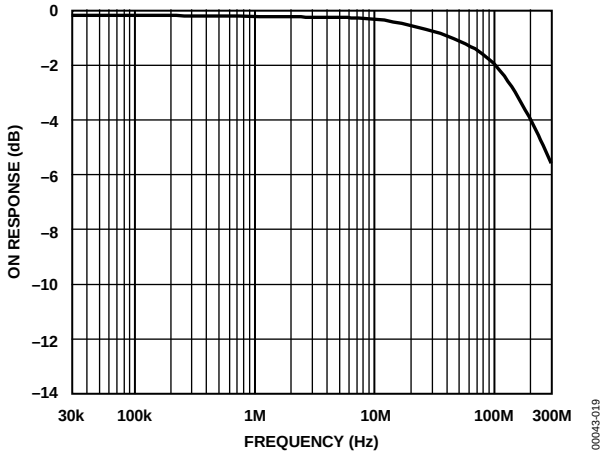


Figure 19. On Response vs. Frequency

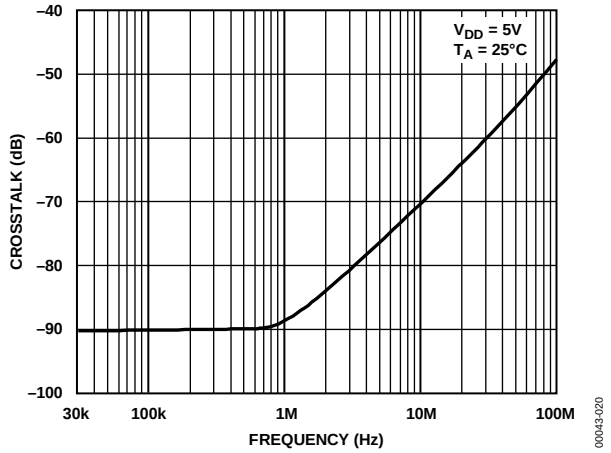


Figure 20. Crosstalk vs. Frequency

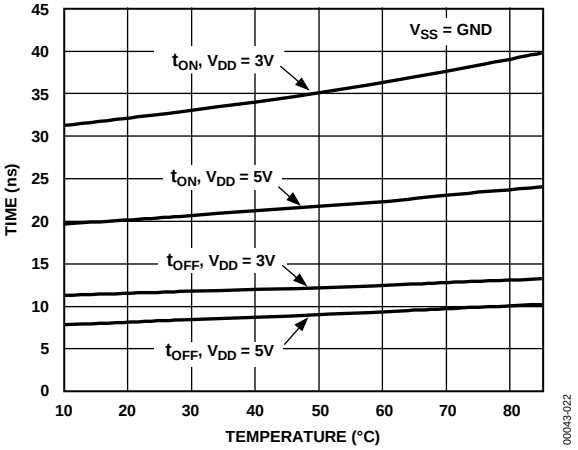


Figure 22. t_{ON}/t_{OFF} Times vs. Temperature for the ADG714

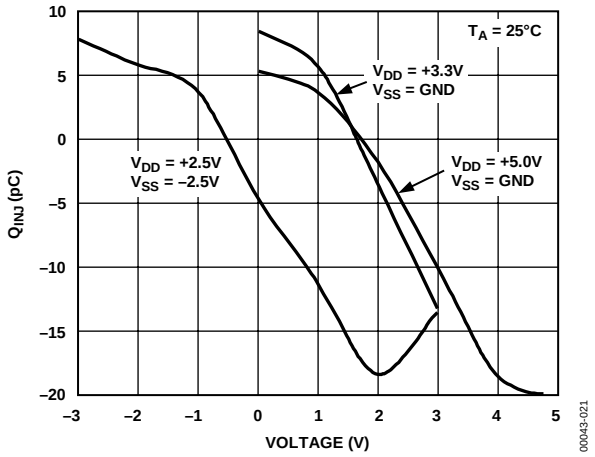


Figure 21. Q_{INJ} vs. Source/Drain Voltage

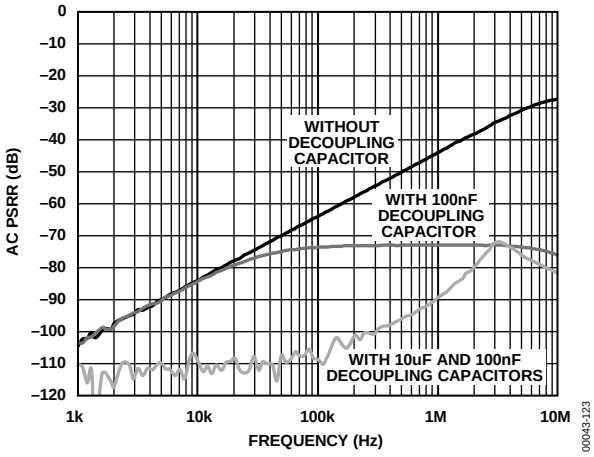


Figure 23. AC Power Supply Rejection Ratio (AC PSRR) vs. Frequency, 5 V Single Supply

TERMINOLOGY

V_{DD}
Most positive power supply potential.

V_{SS}
Most negative power supply in a dual-supply application. In single-supply applications, tie this pin to ground.

I_{DD}
Positive supply current.

I_{SS}
Negative supply current.

GND
Ground (0 V) reference.

Sx
Source terminal. May be an input or an output.

Dx
Drain terminal. May be an input or an output.

R_{ON}
Ohmic resistance between Dx and Sx.

ΔR_{ON}
On resistance match between any two channels, for example, R_{ON} max − R_{ON} min.

$R_{FLAT(ON)}$
Flatness is defined as the difference between the maximum and minimum values of on resistance as measured over the specified analog signal range.

$I_{S (OFF)}$
Source leakage current with the off switch.

$I_{D (OFF)}$
Drain leakage current with the off switch.

$I_{D (ON)}$, $I_{S (ON)}$
Channel leakage current with the on switch.

V_D, V_S
Analog voltage on the Dx and Sx terminals.

$C_{S (OFF)}$
Off switch source capacitance. $C_{S (OFF)}$ is measured with reference to ground.

$C_{D (OFF)}$
Off switch drain capacitance. $C_{D (OFF)}$ is measured with reference to ground.

$C_{D (ON)}$, $C_{S (ON)}$
On switch capacitance. $C_{D (ON)}$, $C_{S (ON)}$ is measured with reference to ground.

C_{IN}
Digital input capacitance.

t_{ON}
Delay time between loading new data to the shift register and selected switches switching on.

t_{OFF}
Delay time between loading new data to the shift register and selected switches switching off.

Off Isolation
A measure of unwanted signal coupling through an off switch.

Crosstalk
A measure of unwanted signal that is coupled through from one channel to another because of parasitic capacitance.

Charge Injection
A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Bandwidth
The frequency at which the output is attenuated by −3 dB.

On Response
The frequency response of the on switch.

Insertion Loss
The loss due to the on resistance of the switch. Insertion loss = 20 $\log_{10}$ (V_{OUT} with switch and V_{OUT} without switch).

V_{INL}
Maximum input voltage for Logic 0.

V_{INH}
Minimum input voltage for Logic 1.

I_{INL}, I_{INH}

Input current of the digital input.

I_{DD}
Positive supply current.

THEORY OF OPERATION

The ADG714 and ADG715 are serially controlled, octal SPST switches, controlled by either a 2- or 3-wire interface. Each bit of the 8-bit serial word corresponds to one switch of the device. A Logic 1 in the bit position turns the switch on, and a Logic 0 turns the switch off. Each switch is independently controlled by an individual bit, which provides the option of having any, all, or none of the switches on.

When changing the switch conditions, a new 8-bit word is written to the input shift register. Some of the bits may be the same as the previous write cycle because the user may not change the state of some switches. To minimize glitches on the output of these switches, the devices compare the state of switches from the previous write cycle. When the switches are already in the on condition and are required to stay on, there are minimal glitches on the output of the switch.

POWER-ON RESET

On power-up of the device, all switches are in the off condition, the internal shift register is filled with zeros, and the register remains so until a valid write takes place.

SERIAL INTERFACE

3-Wire Serial Interface

The ADG714 has a 3-wire serial interface ($\overline{\text{SYNC}}$, SCLK, and DIN), that is compatible with SPI, QSPI, MICROWIRE interface standards, and most DSP interface standards. Figure 3 shows the timing diagram of a typical write sequence.

Data is written to the 8-bit shift register via DIN under the control of the $\overline{\text{SYNC}}$ and SCLK signals. Data may be written to the shift register in more or less than eight bits. In each case, the shift register retains the last eight written bits.

When $\overline{\text{SYNC}}$ goes low, the input shift register is enabled. Data from DIN is clocked into the shift register on the falling edge of SCLK. Each bit of the 8-bit word corresponds to one of the eight switches. Figure 24 shows the contents of the input shift register. Data appears on the DOUT pin on the rising edge of SCLK suitable for daisy chaining, delayed by eight bits. When all eight bits have been written into the shift register, the $\overline{\text{SYNC}}$ line is brought high again. The switches are updated with the new configuration, and the input shift register is disabled. With $\overline{\text{SYNC}}$ held high, the input shift register is disabled so that further data or noise on the DIN line has no effect on the shift register.

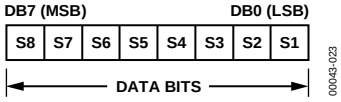


Figure 24. Input Shift Register Contents

2-Wire Serial Interface

The ADG715 is controlled via an I²C-compatible serial bus. This device is connected to the bus as a slave device (no clock is generated by the switch).

The ADG715 has a 7-bit slave address. The five MSBs are 10010 and the two LSBs are determined by the state of the A0 and A1 pins.

The 2-wire serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a start condition, which is when a high to low transition on the SDA line occurs while SCL is high. The following byte is the address byte, which consists of a 7-bit slave address followed by an R/$\overline{\text{W}}$ bit (this bit determines whether data is read from or written to the slave device).
   The slave whose address corresponds to the transmitted address responds by pulling the SDA line low during the ninth clock pulse (the pulling of SDA line is termed the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its serial register. If the R/$\overline{\text{W}}$ bit is high, the master reads from the slave device. If the R/$\overline{\text{W}}$ bit is low, the master writes to the slave device.
2. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL.
3. When all data bits are read or written, a stop condition is established by the master. A stop condition is defined as a low to high transition on the SDA line while SCL is high. In write mode, the master pulls the SDA line high during the tenth clock pulse to establish a stop condition. In read mode, the master issues a no acknowledge for the ninth clock pulse, and the SDA line remains high. The master brings the SDA line low before the tenth clock pulse and then high during the tenth clock pulse to establish a stop condition.

See Figure 25 for an ADG715 write sequence.

A repeated write function gives the user the flexibility to update the matrix switch a number of times after addressing the device only once. During the write cycle, each data byte updates the configuration of the switches. For example, after the matrix switch acknowledges its address byte and receives one data byte, the switches update after the data byte. If another data byte is written to the matrix switch while still in the same addressed slave device, this data byte also causes a switch configuration update. Repeating the read of the matrix switch is also allowed.

Input Shift Register

The input shift register is eight bits wide. Figure 24 illustrates the contents of the input shift register. Data is loaded into the device as an 8-bit word under the control of a serial clock input, SCL. The timing diagram for this operation is shown in Figure 4. The 8-bit word consists of eight data bits, each controlling one switch. MSB (Bit 7) is loaded first.

Write Operation

When writing to the ADG715, the user begins with an address byte and an R/$\overline{W}$ bit, after which the switch acknowledges that it is prepared to receive data by pulling SDA low. This address byte is followed by the 8-bit word. The write operation for the switch is shown in Figure 25.

Read Operation

When reading data back from the ADG715, the user begins with an address byte and an R/$\overline{W}$ bit, after which the switch acknowledges that it is prepared to transmit data by pulling SDA low. The readback operation is a single byte that consists of the eight data bits in the input register. The read operation for the switch is shown in Figure 26.

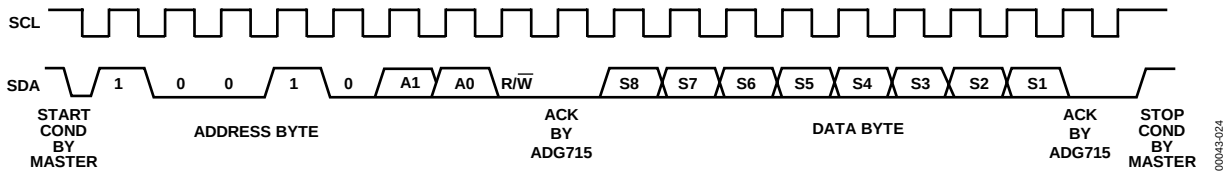


Figure 25. ADG715 Write Sequence

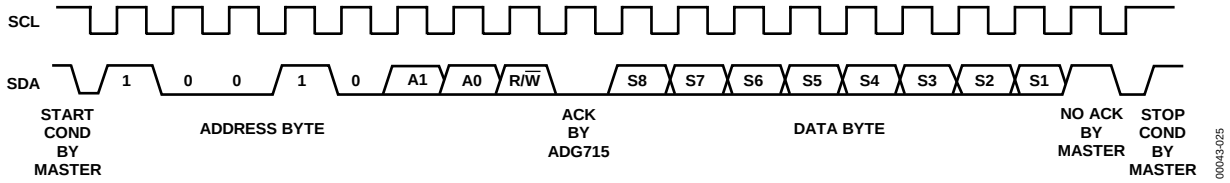


Figure 26. ADG715 Readback Sequence

APPLICATIONS INFORMATION

MULTIPLE DEVICES ON ONE BUS

Figure 27 shows four ADG715 devices on the same serial bus. Each has a different slave address because the state of the A0 and A1 pins is different. This difference allows each switch to be written to or read from independently.

DAISY-CHAINING MULTIPLE ADG714 DEVICES

A number of ADG714 switches can be daisy-chained simply by using the DOUT pin. Figure 28 shows a typical implementation. The $\overline{\text{SYNC}}$ pin of all three devices in the example are tied together. When $\overline{\text{SYNC}}$ is brought low, the input shift registers of all devices are enabled, data is written to the devices via DIN and clocked through the shift registers. When the transfer is complete, $\overline{\text{SYNC}}$ is brought high, and all switches are updated simultaneously. Further shift registers may be added in a series.

POWER SUPPLY SEQUENCING

When using CMOS devices, take care to ensure correct power supply sequencing. Incorrect power supply sequencing can result in the devices being subjected to stresses beyond the absolute maximum ratings listed in Table 6. Digital and analog inputs are always applied after power supplies and ground. In dual-supply applications, if digital or analog inputs are applied to the devices prior to the V_{DD} and V_{SS} supplies, the addition of a Schottky diode connected between V_{SS} and GND ensures that the devices power on correctly. For single-supply operation, V_{SS} is tied to GND as close to the devices as possible.

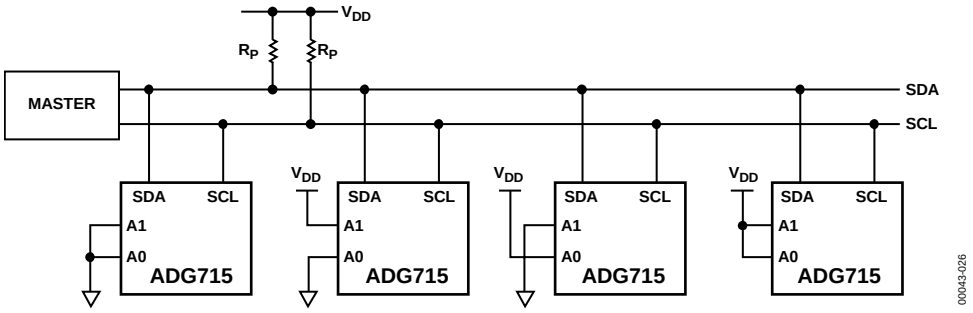


Figure 27. Multiple ADG715 Devices on One Bus

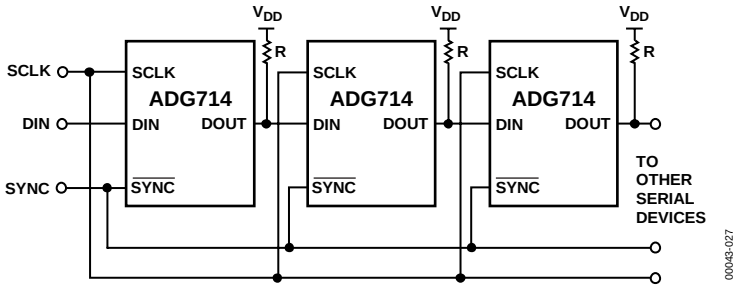


Figure 28. Multiple ADG714 Devices in a Daisy-Chained Configuration

DECODING MULTIPLE ADG714 DEVICES USING THE ADG739

Use the dual 4-channel ADG739 multiplexer to multiplex a single chip select line to provide chip selects for up to four devices on the SPI bus. Figure 29 illustrates the ADG739 and multiple ADG714 devices in such a typical configuration. All devices receive the same serial clock and serial data, but only one device receives the $\overline{\text{SYNC}}$ signal at any one time. The ADG739 is also a serially controlled device. One bit programmable pin of the microcontroller is used to enable the ADG739 via $\overline{\text{SYNC2}}$, while another bit programmable pin is used as the chip select for the other serial devices, $\overline{\text{SYNC1}}$. Driving $\overline{\text{SYNC2}}$ low enables changes to be made to the addressed serial devices. By bringing $\overline{\text{SYNC1}}$ low, the selected serial device hanging from the SPI bus is enabled, and data is clocked into the shift register on the falling edges of SCLK. The design of the matrix switch allows for different combinations of the four serial devices to be addressed at any one time. If more devices must be addressed via one chip select line, the ADG738, an 8-channel device, allows further expansion of the chip select scheme. Note that there is digital feedthrough from the digital input lines because SCLK and DIN are permanently connected to each device. Using a burst clock minimizes the effects of this digital feedthrough on the analog channels.

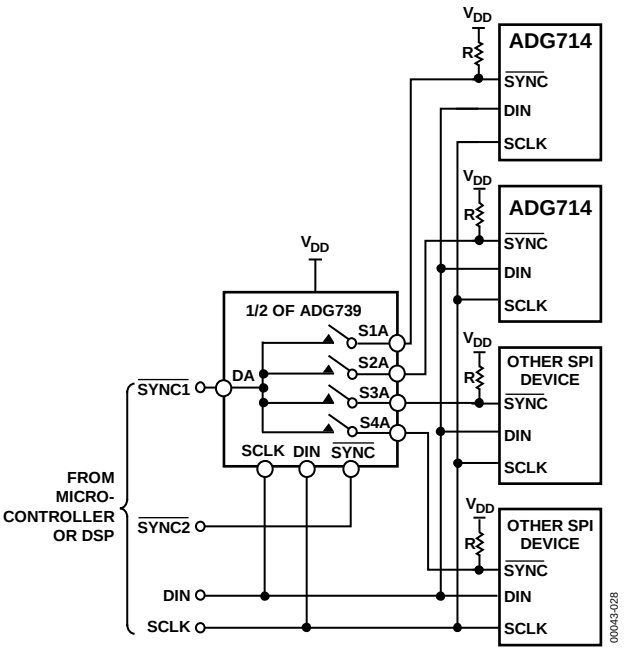
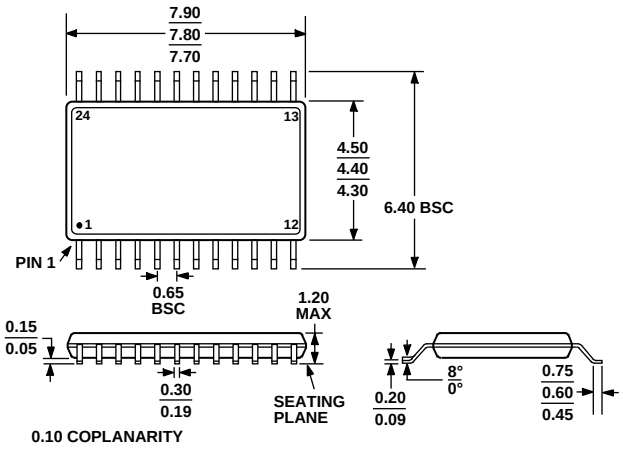


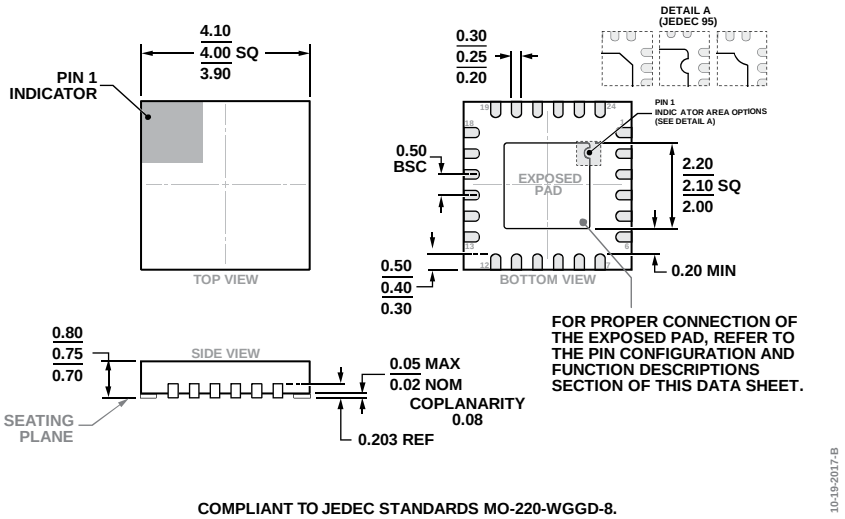
Figure 29. Addressing Multiple ADG714 Devices Using an ADG739

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AD

Figure 30. 24-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-24)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD-8.

Figure 31. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-24-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADG714BRUZ	−40°C to +85°C	24-Lead Thin Shrink Small Outline Package [TSSOP]	RU-24
ADG714BRUZ-REEL	−40°C to +85°C	24-Lead Thin Shrink Small Outline Package [TSSOP]	RU-24
ADG714BRUZ-REEL7	−40°C to +85°C	24-Lead Thin Shrink Small Outline Package [TSSOP]	RU-24
ADG714BCPZ-REEL7	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-10
ADG715BRUZ	−40°C to +85°C	24-Lead Thin Shrink Small Outline Package [TSSOP]	RU-24
ADG715BRUZ-REEL	−40°C to +85°C	24-Lead Thin Shrink Small Outline Package [TSSOP]	RU-24
ADG715BRUZ-REEL7	−40°C to +85°C	24-Lead Thin Shrink Small Outline Package [TSSOP]	RU-24

[1] Z = RoHS Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

D00043-0-6/18(E)