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REVISION HISTORY

Revision 0: Initial Version

Rev. A-082203

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ANALOG SPECIFICATIONS

(Analog and digital supplies = 3.3 V; F_{CLKIN} = 32 MHz;
TxDAC settings: F_{DAC} = 32 MSPS; 8x interpolation; R_{SET} = 4.02 kΩ; differential load resistance of 100 Ω[1];
RxADC settings: F_{ADC} = 32 MSPS; No Decimation, INT ref; differential analog inputs; unless otherwise noted)

Table 1. Tx Path Specifications

Parameter		Temp	Test Level	Min	Typ	Max	
Tx PATH GENERAL	Resolution	Full			12		Bits
	Maximum DAC Update Rate	Full		32			MHz
	Maximum Full Scale Output Current	Full		20			mA
	Gain Mismatch Error				TBD		% FS
	Offset Mismatch Error				TBD		% FS
	Reference Voltage				1.23		V
	Output Capacitance				5		pF
	Output Voltage Compliance Range			–1.0		+1.0	V
Tx PATH DC ACCURACY	Integral Nonlinearity (INL)						Lsb
	Differential Nonlinearity (DNL)						Lsb
	TxPGA Gain Range				12		dB
	TxPGA Step Size				6		dB
Tx PATH DYNAMIC PERFORMANCE (Ioutfs = 20mA; Fout = 1 MHz)	SNR				73		dBFS
	SINAD				TBD		dB
	THD				TBD		dBc
	SFDR, Wideband (dc to Nyquist)				TBD		dBc

Table 2. Rx Path Specifications

Parameter		Temp	Test Level	Min	Typ	Max	Unit
Rx PATH GENERAL	Resolution	Full			14		Bits
	Maximum I/Q Channel Sample Rate	Full		32			MSPS
	Gain Mismatch Error				TBD		% FS
	Offset Mismatch Error				TBD		% FS
	Reference Voltage				TBD		V
	Reference Voltage (REFT-REFB) Error				TBD		mV
	Input Capacitance				TBD		pF
	Input Bandwidth				TBD		MHz
	Differential Analog Input Voltage Range				3		V
Rx PATH DC ACCURACY	Integral Nonlinearity (INL)				TBD		LSB
	Differential Nonlinearity (DNL)				TBD		LSB
	Aperature Delay				TBD		ns
	Aperature Uncertainty (Jitter)				TBD		ps rms
	Input Refered Noise				TBD		
Rx PATH DYNAMIC PERFORMANCE (Vin = -0.5 dBFS; Fin = 1 MHz)	SNR				76		dBc
	SINAD				TBD		dBc
	THD (2nd to 9th harmonic)				TBD		dBc
	SFDR, Wideband (dc to Nyquist)				TBD		dBc
	Crosstalk between ADC inputs				TBD		dB

[1] See Figure ## for description of TxDAC termination scheme

Table 3. Power Specifications

Parameter		Temp	Test Level	Min	Typ	Max	Unit
POWER SUPPLY RANGE	ADC Supply Voltage (ADCVDD)	Full		3.0	3.3	3.6	V
	DAC Supply Voltage (DACVDD)			3.0	3.3	3.6	
	Auxilary Supply Voltage (AUXVDD)			3.0	3.3	3.6	
	Clock Supply Voltage (CLKVDD)	Full		3.0	3.3	3.6	
	Digital Supply Voltage (DVDD)	Full		2.7	3.3	3.6	V
	Driver Supply Voltage (DRVDD)	Full		2.7	3.3	3.6	V
ANALOG SUPPLY CURRENTS	ADCVDD (nominal bias)	Full			100		mA
	DACVDD (20 mA full scale outputs)	Full			74		mA
	DACVDD (2 mA full scale outputs)	Full			TBD		mA
	AUXVDD				2		mA
	CLKVDD				3		mA
DIGITAL SUPPLY CURRENTS[1]	DVDD (Tx Mode)				116		mA
	DVDD (Rx Mode)				107		mA
	DRVDD (Tx Mode)				6.5		
	DRVDD (Rx Mode)				19.5		

DIGITAL SPECIFICATIONS

Conditions: AVDD=3.3 V ± 5%, DVDD = CLKVDD = DRVDD = 3.3 V ± 10%; R_{SET} = 2 kΩ, unless otherwise noted

Table 4. Digital Logic Levels

Parameter	Temp	Test Level	Min	Typ	Max	Unit
CMOS LOGIC INPUTS						
High Level Input Voltage	Full	VI	DRVDD – 0.7			V
Low Level Input Voltage	Full	VI			0.4	V
Input Leakage Current					12	µA
Input Capacitance	Full	VI		3		pF
CMOS LOGIC OUTPUTS (C_{LOAD} = 5 pF)						
High Level Output Voltage (I_{OH} = 1 mA)	Full	VI	DRVDD – 0.7			V
Low Level Output Voltage (I_{OH} = 1 mA)	Full	VI			0.4	V
Output Rise/Fall Time (High Strength Mode and C_{LOAD} = 5 pF)	Full	VI		0.7/0.7		ns
Output Rise/Fall Time (Low Strength Mode and C_{LOAD} = 5 pF)	Full	VI		1.0/1.0		ns
RESET						
Minimum Low Pulse Width (Relative to f_{ADC})			1			Clock cycles

Table 5. CLKIN Timing Specifications

Parameter		Temp	Test Level	Min	Typ	Max	Unit
INPUT CLOCK	CLKIN Clock Rate w/ 2X CLK Multiplier			16		32	MHz
	CLKIN Clock Rate w/o 2X CLK Multiplier			4		64	
	CLKIN Pulse Width High						ns
	CLKIN Pulse Width Low						ns

[1] Rx digital path configured for 4X decimation with FIR, Tx Path configured for 16X interpolation

Table 6. ADIO Port Timing Specifications

Parameter	Temp	Test Level	Min	Typ	Max	Unit
READ OPERATION[1] (See **Error! Reference source not found.**)						
Output Data Rate	Full	II	20		80	MSPS
Three-State Output Enable Time (t_{PZL})	Full	II			3	ns
Three-State Output Disable Time (t_{PLZ})	Full	II			3	ns
Rx Data Valid Time (t_{VT})	Full	II	1.5			ns
Rx Data Output Delay (t_{OD})	Full	II			4	ns
WRITE OPERATION (See **Error! Reference source not found.**)						
Tx Data Setup Time (t_{DS})	Full	II	1			ns
Tx Data Hold Time (t_{DH})	Full	II	2.5			ns
Latch Enable Time (t_{EN})	Full	II			3	ns
Latch Disable Time (t_{DIS})	Full	II			3	ns

Table 7. Serial Port Timing Specifications

Parameter	Temp	Test Level	Min	Typ	Max	Unit
WRITE OPERATION (See **Error! Reference source not found.**)						
SCLK Clock Rate (f_{SCLK})	Full	IV			32	MHz
SCLK Clock High (t_{HI})	Full	IV	14			ns
SCLK Clock Low (t_{LOW})	Full	IV	14			ns
SDIO to SCLK Setup Time (t_{DS})	Full	IV	14			ns
SCLK to SDIO Hold Time (t_{DH})	Full	IV	0			ns
$\overline{SEN}$ to SCLK Setup Time (t_S)	Full	IV	14			ns
SCLK to $\overline{SEN}$ Hold Time (t_H)	Full	IV	0			ns
READ OPERATION (See **Error! Reference source not found.** and **Error! Reference source not found.**)						
SCLK Clock Rate (f_{SCLK})	Full	IV			32	MHz
SCLK Clock High (t_{HI})	Full	IV	14			ns
SCLK Clock Low (t_{LOW})	Full	IV	14			ns
SDIO to SCLK Setup Time (t_{DS})	Full	IV	14			ns
SCLK to SDIO Hold Time (t_{DH})	Full	IV	0			ns
SCLK to SDIO (or SDO) Data Valid Time (t_{DV})	Full	IV			14	ns
$\overline{SEN}$ to SDIO Output Valid to Hi-Z (t_{EZ})	Full	IV		2		ns

Table 5. Explanation of Test Levels

Level	Description
I	100% production tested.
II	100% production tested at +25°C and guaranteed by design and characterization at specified temperatures.
III	Sample tested only.
IV	Parameter is guaranteed by design and characterization testing.
V	Parameter is a typical value only.
VI	100% production tested at +25°C and guaranteed by design and characterization for industrial temperature range.

[1] C_{LOAD}=5 pF for Digital Data Outputs

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
ELECTRICAL	
AVDD, CLKVDD Voltage	3.9 V max
DVDD, DRVDD Voltage	3.9 V max
RX1+, RX1−, RX2+, RX2−,	???
REFT, REFB	−0.3 V to AVDD + 0.3 V
IOUTP+, IOUTP−	−1.5 V to AVDD + 0.3 V
CLKIN	−0.3 V to CLVDD + 0.3 V
REFIO, REFADJ	−0.3 V to AVDD + 0.3 V
Digital Input and Output Voltage	−0.3 V to DRVDD + 0.3 V
Digital Output Current	5 mA max
ENVIRONMENTAL	
Operating Temperature Range (Ambient)	−40°C to +85°C
Maximum Junction Temperature	125°C
Lead Temperature (Soldering, 10 s)	150°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses above those listed under the Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

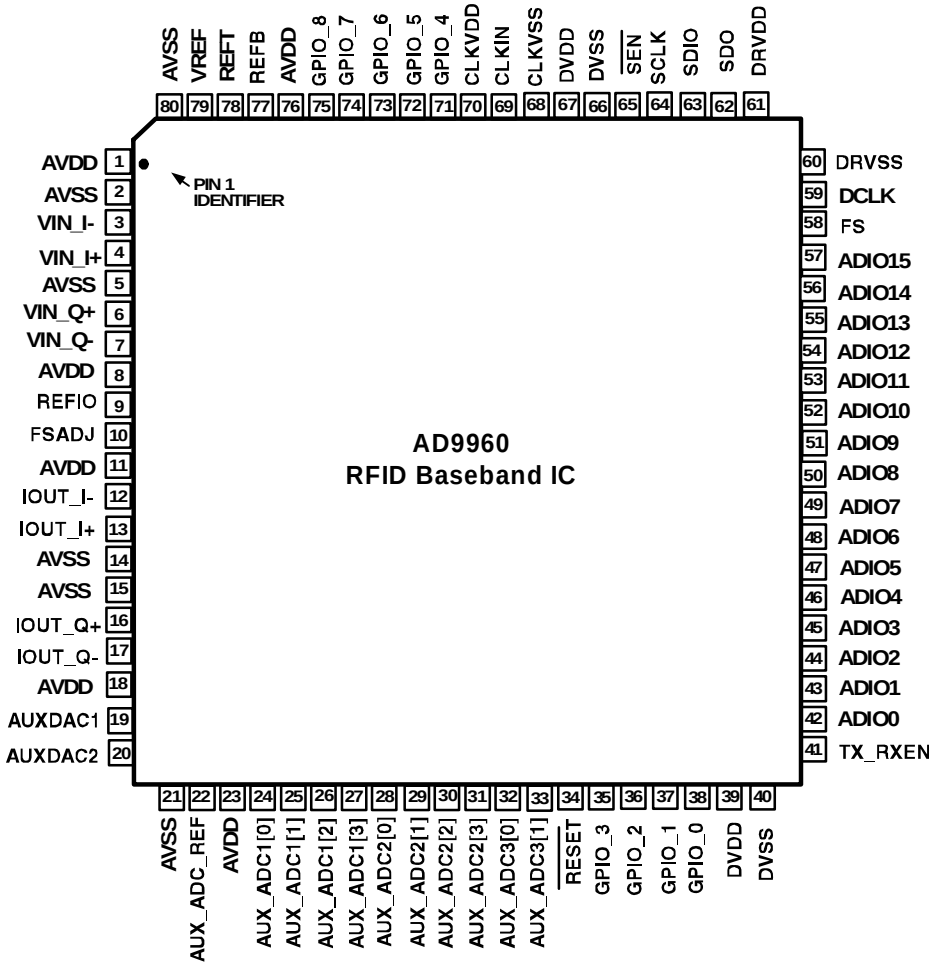

Figure 2. Pin Configuration

PIN CONFIGURATION AND PIN FUNCTION DESCRIPTIONS

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Pin Function
1, 8, 11, 18, 23, 76	AVDD	Analog Supply Input
2, 5,14, 15, 21, 80	AVSS	Analog Supply Return
3,4	VIN_I-, VIN_I+	I Channel Differential Voltage Rx input
6,7	VIN_Q+, VIN_Q-	Q Channel Differential Voltage Rx input
9	REFIO	I and Q TxDAC's Reference Input/Output
10	FSADJ	I and Q TxDAC's Full-Scale Current Adjust
12, 13	IOUT_I-, IOUT_I+,	I TxDAC Differential Current Output
16, 17	IOUT_Q+, IOUT_Q-,	Q TxDAC Differential Current Output
19, 20	AUXDAC1, AUXDAC2	Voltage Output of Auxilary DAC's
22	AUX_REG	Regulator Output that sets full-scale span for all Auxilary ADC's and DAC's
24-27	AUXADC1[0-3]	Voltage Inputs to Auxilary 4 Channel Muxed ADC1
28-31	AUXADC2[0-3]	Voltage Inputs to Auxilary 4 Channel Muxed ADC2
32-33	AUXADC3[0-1]	Voltage Inputs to Auxilary 2 Channel Muxed ADC3
34	RESET	Reset Input (Active Low)
35	GPIO_3	General Purpose Input/Output (or Single-Bit Tx Mode Data Input)
36	GPIO_2	General Purpose Input/Output (or Single-Bit Tx Mode Clock Output)
37	GPIO_1	General Purpose Input/Output (or TI DSP Interface Control Output)
38	GPIO_0	General Purpose Input/Output (or TI DSP Interface Control Output)
39, 67	DVDD	Digital Supply Input
40, 66	DVSS	Digital Supply Return
41	TX_RXEN	Half-Duplex Tx/Rx Digital Bus Control Input
42	ADIO0	Bit 0 (LSB) of 16-bit bi-directional ADIO buffer
43-56	ADIO1-ADIO14	Bits 1-14 of 16-bit bi-directional ADIO buffer
57	ADIO15	Bit 15 (MSB) of 16-bit bi-directional ADIO buffer
58	FS	Frame Sync Pulse Outut (Indicates start of when valid I/Q is placed on bus for DSP)
59	DCLK	Digital Clock Output to DSP (equal to ADIO data rate)
60	DRVSS	Digital I/0 Supply Return
61	DRVDD	Digital I/0 Supply Input
62	SDO	Serial Port Data Output
63	SDIO	Serial Port Data Input/Output
64	SCLK	Serial Port Clock Input
65	SEN	Serial Port Enable Input (Active Low)
68	CLKVSS	Clock Supply Return
69	CLKIN	Clock Input
70	CLKVDD	Clock Supply Input
71	GPIO_4	General Purpose Input/Output (or ADC Overload Output)
72-75	GPIO_5-GPIO_8	General Purpose Input/Outputs
77,78	REFB, REFTT	ADC Reference Decoupling
79	VREF	ADC Reference Input/Output

REGISTER MAP DESCRIPTION

The AD9960 contains a set of programmable registers described in Table 1 that can be used to optimize its numerous features, interface options, and performance parameters from its default register settings. Registers pertaining to similar functions have been grouped together and assigned adjacent addresses to minimize the update time when using the multi-byte serial port interface (SPI) read/write feature. Registers pertaining to the digital operation of the AD9960 are located between Reg. 0x00 and 0x1F while registers pertaining to the mixed-signal sections are located at 0x20 and above. Bits that are undefined within a register should be assigned a 0 when writing to that register.

Table 1. Register Map—Registers 0x00 to 0x3A

Name	*Address*	*7*	*6*	*5*	*4*	*3*	*2*	*1*	*0*	*Default*	*Notes*
RESET	0x00	3 wire/ not 4 wire	Force DCLK tri-state	tx path reset	rx path reset	full sync reset	-	-	S/W reset	0x70	S/W reset forces a reset of SPI registers pertain to digital section only.
HOST DSP I/F	0x01	-	-	-	-	Address Generation	TI compatible mode*	Real onlyTX	-	0x00	Default Interface is for ADI Backfin DSP *Also Supports TI DSP's
	0x02	-	-	-	-	-	-	-	-	0x00	Reserved Register
TX MODE	0x03	-	-	-	-	-	-	-	-	0x10	Used for TI DSP Only Contact Factory
RX MODE	0x04	-	-	-	-	-	-	-	-	0x10	
DETAIL MODE	0x05	-	-	-	DCLK clk detail mode	txfir detail mode	txcci detail mode	rxcic detail mode	rxfir detail mode	0x00	Enables user to set Tx interp. and Rx dec. factors as well internal clocks to support these factors
TXFIR CONFIG	0x06	txfir bypass	-	-	txfir int factor	txfir clkin sel <3:0>				0x00	Sets interp. factor of Tx FIR and CIC as well as input clock rates to FIR and CIC
TXCCI CONFIG	0x07	txcci bypass	txcci int factor <2:0>			txcci clkin sel <3:0>				0x00	
RXCIC CONFIG	0x08	rxcic bypass	rxcic dec factor <2:0>			rxcic clkout sel <3:0>				0x00	Sets dec. factor of Rx FIR and CIC as well as input clock rates to FIR and CIC
RXFIR CONFIG	0x09	rxfir bypass	-	-	rxfir dec factor	rxfir clkout sel <3:0>				0x00	
DCLK CONFIG	0x0A	DCLK tx clk sel <3:0>				DCLK rx clk sel <3:0>				0x00	Sets DCLK for ADIO port for Tx and Rx
FIR LENGTH	0x0B	-	-	TXFIR length<2:0>			RXFIR length<2:0>			0x00	Selects length of Tx and Rx FIR filters
	0x0C	-	-	-	-	-	-	-	-	0x00	Reserved Registers
	0x0D										
	0x0E										
	0x0F										
GPIO DIREC-TION	0x10	GPIO dir<8:1>								0xFF	Set GPIO bit to 1 for input (default setting) or 0 for output.
	0x11	GPIO dir<0>	-	-	-	-	-	-	-	0x80	
GPIO READ/ WRITE	0x12	GPIO<8:1>								N/A	Read and Write Values of GPIO pins
	0x13	GPIO<0>	-	-	-	-	-	-	-	N/A	
GPIO control	0x14	-	ADC OVR enable	-	CLK enable	CLK out divide<3:0>				0x00	
TI Host Address	0x15	TX Address[19:12]								0x00	Contact Factory for Support
	0x16	TX Address[11:4]								0x00	
	0x17	TX Address[3:0]				-	-	-	-	0x00	

	0x18	RX Address[19:12]								0x00	
	0x19	RX Address[11:4]								0x00	
	0x1A	RX Address[3:0]				-	-	-	-	0x00	
TX Hold	0x1B	Count[7:0]								0x00	Delay which TxDAC input latches disabled
	0x1C	-	-	-	-	-	-	-	-	0x00	Reserved Registers
	0x1D										
RAM ADDRESS	0x1E	address<7:0>								0x00	Use these registers to load coefficients into Tx and Rx FIR
RAM DATA	0x1F	data<7:0>								N/A	
Power Down	0x20	Rx ADC	VREF ADC	VREF ADC BUF.	CLK	CLK MULT.	AUX_ DAC1	AUX_ DAC2	AUX DAC REG.	0x06	Set Bit to 1 to power-up
	0x21	Tx DAC	Tx DAC_I Sleep	Tx DAC_Q Sleep	VREF DAC	-	-	-	-	0x00	
RxADC	0x22	ADC Span 3 or 2 Vp.p.	Duty Cycle Res. Enable	2's Comp. Enable	ADC BIAS <2>	ADC BIAS <1>	ADC BIAS <0>	-	-	0x20	RxADC set to 3 Vp.p. Span, 2's comp., and full bias.
	0x23	-	-	-	-	-	-	-	-	0x13	Reserved Registers
	0x24	-	-	-	-	-	-	-	-	0x00	
AUX ADCs	0x25	Aux ADC1 start	Aux ADC2 start	Aux ADC2 start	Aux ADC1 ref_sel.	Aux ADC2 ref_sel	Aux ADC3 ref_sel	Aux_Reg_ sel[1:0]		0x00	Input Span of Aux. ADC's is Regulator Output or AVDD.
	0x26	Aux ADC1 Channel Select [1:0]		Aux ADC2 Channel Select [1:0]		Aux ADC3 Ch. Sel.	clk div-by-2	-	-	0x00	Channel Select for Aux ADC's
	0x27	aux_adc_1_data[9:2]									Aux ADC1 10-bit Data Output
	0x28	aux_adc_1_data [1:0]		-	-	-	-	-	-		
	0x29	aux_adc_2_data[9:2]									Aux ADC2 10-bit Data Output
	0x2A	aux_adc_2_data [1:0]		-	-	-	-	-	-		
	0x2B	aux_adc_3_data[9:2]									Aux ADC3 10-bit Data Output
	0x2C	aux_adc_3_data [1:0]		-	-	-	-	-	-		
AUX DACs	0x2D	aux_dac_1_data[9:2]								0x00	Aux DAC1 10-bit Input Data, Output Span set to Regulator or AVDD, Invert Out.
	0x2E	aux_dac_1_data [1:0]		aux_dac_1_ref_sel	aux_dac_1_inv_d	-	-	-	-	0x00	
	0x2F	aux_dac_2_data[9:2]								0x00	Aux DAC2 10-bit Input Data, Output Span set to Regulator or AVDD, Invert Out
	0x30	aux_dac_2_data [1:0]		aux_dac_2_ref_sel	aux_dac_2_inv_d	-	-	-	-	0x00	
CLOCKS	0x31	gate_clk_mult	clk_mult_by_pass	gate_tx_dac_clk	dac_clk_div_2	-	-	-	-	0x0F	CLK Multiplier and TxDAC Clock Control
	0x32	-	-	-	-	-	-	-	-	0x00	Reserved

DIGITAL REGISTER DESCRIPTIONS

Register 0x00: RESET

bit 7: 3 wire/not 4 wire

This bit sets the mode of operation of the SPI interface. The default value of 0 sets the 4 wire mode. This is the only bit in register map that is not cleared by a software reset.

bit 6: Force ADIO tri-state

This bit is set by default and is used to force the ADIO bus to a tri-state value until the DSP has had time to initialize the rest of the system. This bit must be cleared to enable normal operation.

bits 5, 4: Tx/Rx path reset

These bits are used to force the data paths into a reset state. The CIC filters are reset by clearing their internal registers and the FIR filters are flushed by forcing zeros at their inputs. The DAC driver block is forced to 0, and the DSP interface is also held in reset. Note, the DSP interface block receives the OR of these two signals, so it is not possible to reset one data path while processing with the other.

bit 3: Full Synchronous reset

This bit is forces a full synchronous reset of the state machines within the control path, this includes the clock generation block. Holding this at 1 will stop the digital clocks and can be used in a stand-by mode. The data paths are unaffected.

bit 0: Software Reset

This bit is used to clear the register map to hardware reset defaults. Setting this bit to 1 initiates a reset. This bit automatically clears itself and is not readable. The only register not affected by this reset is the 3wire/not 4wire bit.

Register 0x01: HOST I/F

bit 3: Address Generation

Enables the automatic address initialization of the address over the ADIO bus in host interface mode.

bit 2: Host Interface mode

Enables the TI compatible Host Interface mode of the ADIO bus.

bit 1: Real Only TX

Enables the real only data path support of the ADIO interface. In this mode, both the I and Q paths receive the same data. When using this mode, the DCLK interface TX clock needs to be set to half the speed of the clock during the complex transmissions.

Register 0x03, 0x04: TX/RX MODE

This register is required for the current Host Interface mode of operation. Please contact factory for support with this mode.

Register 0x05: DETAIL MODE

bit 5, 4, 3, 2, 1, 0: Detail mode enable

Enables the detailed programming mode of each of the data path blocks. All of these bits should be set to 1 for the Blackfin compatible ADIO interface mode. Please refer to the mode selection tables to ensure proper programming of the data path configuration registers.

Register 0x06: TXFIR CONFIGURATION

bit 7: TXFIR bypass

Setting this to 1 bypasses the TXFIR filter. In this case, the input clock (bits 3:0) must match the TXCIC input clock.

bit 4: TXFIR mode

Selects the interpolation rate of the TXFIR filter. Setting to 0 puts the filter in the 4x 64-tap mode, and 1 selects the 5x 60-tap mode.

bits 3, 2, 1, 0: TXFIR input clock select

These bits select the input clock rate to the TXFIR based on the clock selection table. This clock needs to be set based on the input clock rate of the TXCIC and TXFIR mode.

Register 0x07: TXCIC CONFIGURATION

bit 7: TXCIC bypass

Setting this to 1 bypasses the TXCIC filter. In this case, the input clock (bits 3:0) must match the DAC input clock (32MHz or 0xE).

bits 6, 5, 4: TXCIC mode selection

These bits set the TXCIC interpolation mode. 0 = 2x, 1 = 4x, 2 = 5x, 3 = 8x, 4 = 16x.

bits 3, 2, 1, 0: TXCIC input clock select

These bits select the input clock rate to the TXCIC based on the clock selection table. This clock needs to be set based on the DAC clock rate and the TXCIC mode.

Register 0x08: RXCIC CONFIGURATION

bit 7: RXCIC bypass

Setting this to 1 bypasses the RXCIC filter. In this case, the input clock (bits 3:0) must match the ADC input clock (32MHz or 0xE).

bits 6, 5, 4: RXCIC mode selection

These bits set the RXCIC decimation mode. 0 = 2x, 1 = 4x, 2 = 5x, 3 = 8x, 4 = 16x.

bits 3, 2, 1, 0: RXCIC input clock select

These bits select the input clock rate to the RXCIC based on the clock selection table. This clock needs to be set based on the ADC clock rate and the RXCIC mode.

Register 0x09: RXFIR CONFIGURATION

bit 7: RXFIR bypass

Setting this to 1 bypasses the RXFIR filter. In this case, the output clock (bits 3:0) must match the RXCIC output clock.

bit 4: RXFIR mode

Selects the interpolation rate of the RXFIR filter. Setting to 0 puts the filter in the 4x 64-tap mode, and 1 selects the 5x 80-tap mode.

Register 0x0A: DCLK Configuration

bits 7, 6, 5, 4: DCLK TX mode clock select

Selects the clock rate of the DCLK interface during transmit mode. This needs to be twice the rate of the TXFIR input clock for complex data, and equal to the TXFIR input clock when the Real Only mode is enabled.

bits 3, 2, 1, 0: DCLK RX mode clock select

Selects the clock rate of the DCLK interface during the receive mode. This always needs to be twice the rate of the RXFIR output clock.

Register 0x0B: FIR LENGTH

bits 5, 4, 3: TXFIR length

Selects the length of the TXFIR filter. The lengths listed are for 4x/5x mode of operation: 0x0 = 64/60, 0x1 = 56/50, 0x2 = 48/40, 0x3 = 40/30, 0x4 = 32/20, 0x5 = 24/10, 0x6 = 16/x, 0x7 = 8/x.

bits 2, 1, 0: RXFIR length

Selects the length of the RXFIR filter. The lengths listed are for 4x/5x mode of operation: 0x0 = 64/80, 0x1 = 56/70, 0x2 = 48/60, 0x3 = 40/50, 0x4 = 32/40, 0x5 = 24/30, 0x6 = 16/20, 0x7 = 8/10.

Register 0x10: GPIO DIRECTION MSB

Sets the direction of the GPIO pins 8:1. The default sets the pins as inputs, and writing a 0 to the corresponding bit sets it as an output. The direction register must be set correctly when using the special modes, as the special modes select the behavior of the pin but not the direction.

Register 0x11: GPIO DIRECTION LSB

Sets the direction of the GPIO pin 0. The default sets the pins as inputs, and writing a 0 to the corresponding bit sets it as an output. The direction register must be set correctly when using the special modes, as the special modes select the behavior of the pin but not the direction.

Register 0x12: GPIO READ/WRITE MSB

Used to read or write the value of the GPIO pins 8:1. Reading from pins selected as outputs reads back 0. Writing to inputs will hold the value, and set it as an output if the pin changes direction. All GPIO inputs are synchronized with SCLK.

Register 0x13: GPIO READ/WRITE LSB

Used to read or write the value of the GPIO pin 0. Reading from pins selected as outputs reads back 0. Writing to inputs will hold the value, and set it as an output if the pin changes direction. All GPIO inputs are synchronized with SCLK.

Register 0x14: GPIO CONTROL

bit 6: ADC overrange enable

Setting to 1 enables the output of the ADC overrange bit on GPIO4. Reg 0x10, Bit 3 must be cleared to enable this output.

bit 4: Clock output enable

Enables the clock functionality on GPIO8. Reg 0x10, bit 7 must be cleared to enable this functionality. The use of this clock output can impact the performance of the ADC

bits 3, 2, 1, 0: Clock output select

Selects the output clock frequency based on the values in the clock selection table.

Register 0x1B: TX HOLD

Sets the delay of the DAC driver latch used to hold a constant DC value into the TxDACs during RX mode. This value specifies the number of 2MHz periods to wait before holding the output of the TXCIC filter. The default value of 0x00 disables this functionality. The programmed length should be long enough to allow the TX filters to settle before latching.

SERIAL PORT INTERFACE (SPI)

The serial port of the AD9960 has 4-wire or 3-wire SPI capability, allowing read/write access to all registers that configure the device's internal parameters. The default 4-wire serial communication port consists of a serial port enable (SEN), a clock (SCLK), a bidirectional data (SDIO) signal, and an output data (SDO) signal. A 3-wire SPI interface can be enabled by setting the MSB (bit 7) of Reg 0x00 resulting on data appearing on the SDIO pin during a read operation while SDO remains three-stated.

$\overline{\text{SEN}}$ is an active low control gating read and write cycles. When $\overline{\text{SEN}}$ is high, SDO and SDIO are three-stated. SCLK is used to synchronize SPI read and write operations at a maximum bit rate of 32 MHz with input data being registered on the *rising* edge and output data on the *falling* edge. The inputs to SCLK, $\overline{\text{SEN}}$, and SDIO contain a Schmitt trigger with a nominal hysteresis of 0.4 V centered about VDDH/2.

An 8-bit instruction header must accompany each read and write SPI operation. Both the write and read operation supports an auto increment mode, allowing a series of registers to be configured in a single write (or read) operation. The exception to using this auto increment mode behavior is when either the RAM ADDR or RAM DATA address registers (Reg 0x1E and 0x1F) has been reached.

Loading these registers is covered at the end of this section. The instruction header is shown in Table II. It includes a read/not-write indicator bit and seven address bits. The data bits immediately follow the instruction header for both read and write operations. Note that the address and data are always given MSB first.

Table 7. Instruction Header Information

MSB							**LSB**
17	16	15	14	13	12	11	10
R/$\overline{\text{W}}$	A6	A5	A4	A3	A2	A1	A0

Figure 1a illustrates the timing requirements for a 4- or 3-write operation to the SPI port. After the serial port enable ($\overline{\text{SEN}}$) signal goes low, data (SDIO) pertaining to the instruction header is read on the rising edges of the clock (SCLK). To initiate a write operation, the read/not-write bit is set low. After the instruction header is read, the eight data bits pertaining to the specified register are shifted into the data pin (SDIO) on the rising edge of the next eight clock cycles. SEN stays low during the operation and goes high at the end of the transfer. If SEN rises before the eight clock cycles have passed, the operation is aborted.

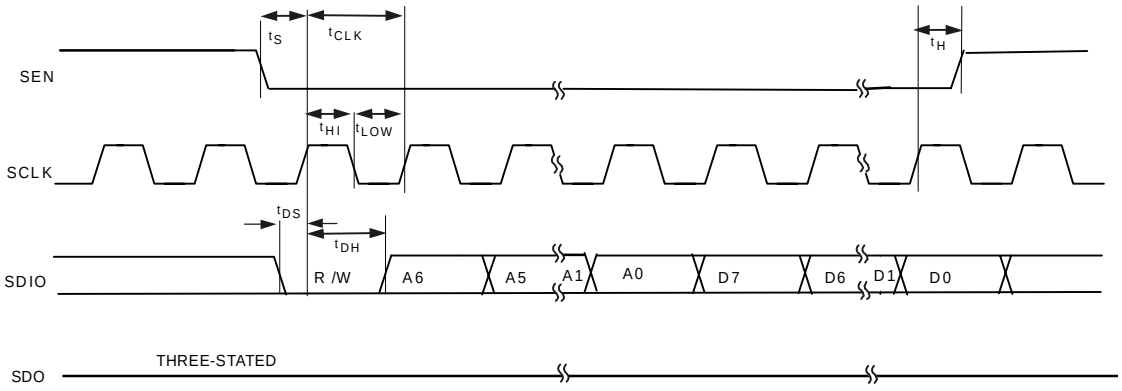

Figure 1a. Timing Diagram for a 4- or 3- wire SPI write operation

If SEN stays low for an additional eight clock cycles, the destination address is incremented and another eight bits of data are shifted in. Again, should SEN rise early, the current byte is ignored. By using this implicit addressing mode, the multiple registers can be configured with a single write operation. Registers identified as being subject to frequent updates have been assigned adjacent addresses to minimize the time required to update them. Note that multibyte registers are big-endian (the

most significant byte has the lower address) and are updated when a write to the least significant byte occurs.

Figure 2a and 2b illustrates the timing for a 4-wire and 3-wire read operation to the SPI port. Read operations are required to access the auxiliary ADC data but can also be used in the product development phase for system authentication. After the serial port enable ($\overline{SEN}$) signal goes low, input data (SDIO) pertaining to the instruction header is read on the rising edges of the clock (SCLK). A read operation occurs if the read/not-write indicator is set high. After the address bits of the instruction header are read, the eight data bits pertaining to the specified register are shifted out of the data output pin (SDO) on the falling edges of the next eight clock cycles. If the 3-wire SPI interface is enabled, the eight data bits will only appear on the SDIO pin (with the same timing relationship as SDO) but with SDO remaining three-stated. After the last data bit is shifted out, the user should return SEN high, causing SDIO to become three-stated and return to its normal status as an input pin.

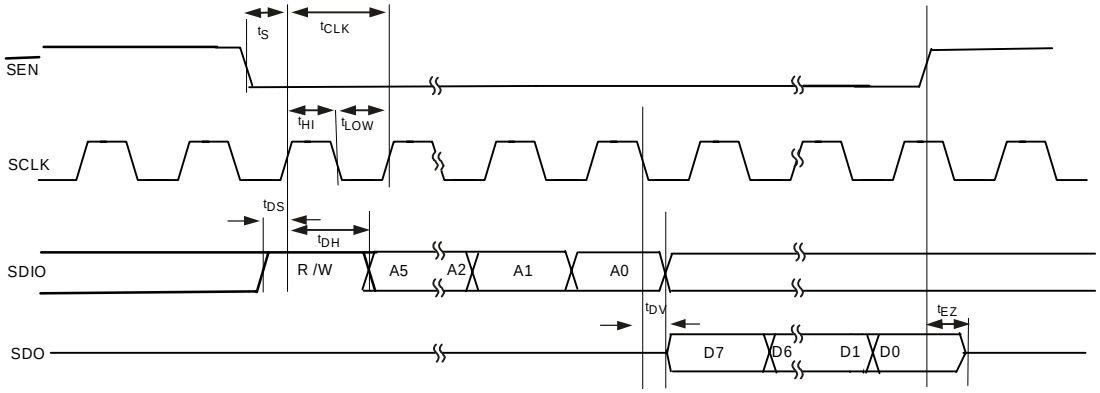

Figure 2a. Timing diagram for 4-wire read operation

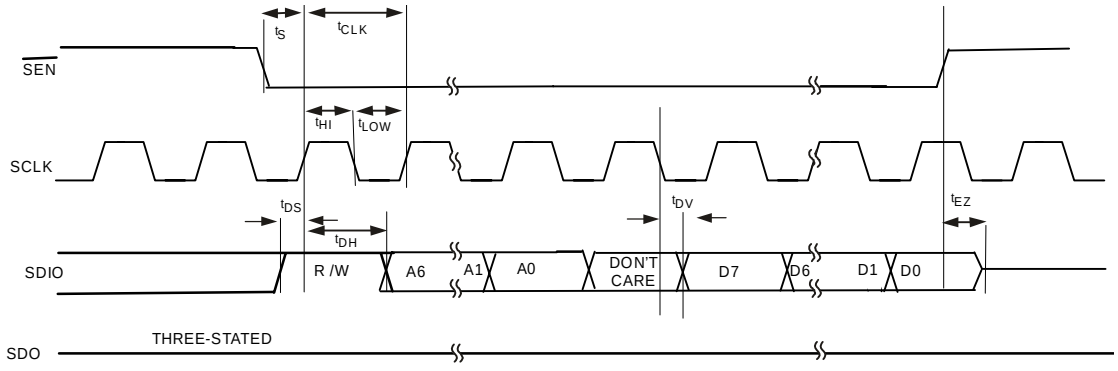

Figure 2b. Timing diagram for 4-wire read operation

As previously mentioned, the SPI registers (i.e. Reg 0x1E and 0x01F) that access the Tx and Rx path RAM filters must be accessed separately. As a result, it will take four write operations to configure the AD9960 for system initialization. In this case, the first write operation could load SPI registers 0x00 to 0x1D while a second write operation loads SPI registers 0x20 to 0x39. The third and fourth write operations are required to program the Tx and Rx FIR coefficients into a 144-byte RAM.

In RAM access mode, the two registers RAM ADDRESS and RAM DATA (i.e. Reg 0x1E and 0x01F) provide access to an 8-bit indexed address space to read and write the RAM coeffi-

cients. The RX FIR is located in the lower portion of the 8-bit address space while the Tx FIR is located in the upper space. The RAM allocation for the Rx FIR is 64 registers for 4X decimation and 80 registers for 5X decimation. The RAM allocation for the Tx FIR is 64 registers (i.e. 32 unique taps) for 4X interpolation and 60 registers (i.e. 30 unique taps) for 5X

An auto increment feature (similar to the SPI auto increment described above) allows multi-byte transfer to the FIR RAM memory space to speed up data transfer. To use this functionality, first the RAM ADDRESS register must be written with the start address. A write to the RAM DATA register will update the RAM location pointed to by the value in RAM ADDRESS. At the end of the 8 SCLKs in the data cycle, the RAM ADDRESS is incremented and another eight bits of data are shifted if SCLK continues to be strobed and SEN remains low. This process will continue until SEN rises at which point the operation is aborted. While the physical method for doing the multi-byte transfers is the same as in the auto-increment mode previously discussed, the internal SPI address value is not incremented during accesses to RAM DATA.

interpolation. Table ?? shows how the memory space is allocated. Although the Tx and Rx FIR filters support reduced length filters in decrements of 8 or 10 taps, zero-padding of unused registers is still required so that the filter remains symmetric in its assigned memory space.

The following example serves to illustrate how to perform a multi-byte write (or read) operation to the FIR RAM. If the user has selected 5X decimation for the Rx FIR filter and 4x interpolation, then 80 registers must be updated for the Rx FIR and 64 registers for the Tx FIR filter. To update the Rx FIR filter coefficients, the user would first write to RAM ADDRESS register (0x1E) and specify 0x00 as the first address of the RAM to written (or read). With SEN low and SCLK continuously being strobed, the SPI address will automatically be incremented to the RAM DATA register (0x1F) such that all subsequent 80 bytes of data will pertain to the Rx RAM coefficients. Upon accessing the last RAM address register, SEN can return high to end this write (or read) operation. A similar procedure exists for writing (or reading) the Tx FIR filter coefficients with the exception that the starting RAM address is 0x080 with 64 bytes of data to follow.

DIGITAL SIGNAL PATH DESCRIPTION

The Tx and Rx digital signal path of the AD9960 are shown in figure abc. Both the Rx and Tx signal paths are considered to be complex or I/Q 16-bit data paths although the Tx signal path can support a real data format also. The AD9960 supports a half-duplex communication protocols via a bidirectional data bus (ADIO) that interfaces to the parallel port of a DSP or FPGA. Note, a future revision to the AD9960 will support a full-duplex interface where the ADIO bus can be dedicated to the Rx data path and a 4-wire serial path can be used for the Tx signal path.

Both the Tx and Rx digital signal paths are highly configurable with programmable RAM FIR and selectable CIC filters allowing it to be optimized for the target communication application. The signal processing capabilities of the AD9960 were designed to offload the host DSP from performing standard Tx and Rx filtering functions that would otherwise consume excessive DSP resources or require an external FPGA.

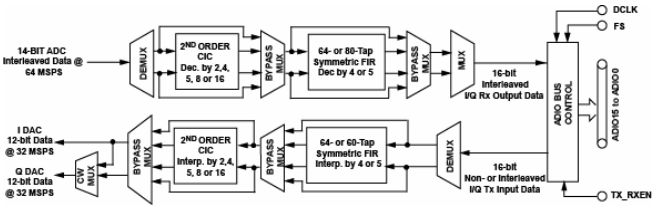

Figure abc. AD9960's Tx and Rx digital signal path

TX PATH OVERVIEW

Referring to figure abc. , 16-bit data originating from a DSP or FPGA is directed into the AD9960's ADIO port when TX_RXEN is brought high. This data can be either real or complex (interleaved) Tx data. A de-multiplexer is used to de-interleave complex data or re-direct real input data such that the input to the programmable Tx FIR input is always I and Q data pairs representing a real or complex sample. This Tx data pair is then be directed to a FIR filter for interpolation by a factor of 4 or 5. A 2nd order CIC interpolation filter follows the FIR filter to up sample the Tx data to its final data rate required by the I and Q TxDAC's (i.e. equal to CLKIN). Note, Tx digital signal path can support an interpolation factor as high as 80 or can be completely bypassed.

TX FIR

The programmable FIR can be configured as a symmetrical 4x or 5x interpolation filter as well as simply bypassed via Reg 0x06. Its maximum non-bypassed output data rate is 8 MSPS thus limiting its maximum input data rate to 1.25 and 2.0 MSPS for 5x and 4x interpolation respectively (assuming CLKIN=32 MHz). Since the coefficient RAM supports 32 unique FIR coefficients, the standard coefficient configuration is for a 64-or 60-tap symmetric FIR for 4x and 5x interpolation respectively.

Figure x.x shows the RAM address space for the Tx FIR filters' coefficients occupying address 0x80 through 0xBF. The coefficients have 16-bit resolution thus occupying two address spaces. Note, to prevent digital clipping, consideration should be given to the coefficient values and/or limiting the peak data input vales into the digital FIR . Programming the FIR filter requires the use of the RAM ADDRESS and RAM DATA SPI Registers as previously discussed. Note, due to the filter implementation, the filter coefficients must be written to the RAM *after* the filter mode is selected via 0x06.

Table 8. Tx FIR RAM Address Space

Address (Hex)	Coefficient and Byte
0x80	0 MSB
0x81	0 LSB
0x82	1 MSB
0x83	1 MSB
…	
0xBA	29 MSB
0xBB	29 LSB
0xBC	30 MSB
0xBD	30 LSB
0xBE	31 MSB
0xBF	31 LSB

The length of the FIR can be altered to support reduced length symmetric operation. The reduced length mode can be considered for symmetric FIR' filters that require lower group delay. For 4x interpolation, the number of taps can be reduced from 64 to 8 taps in increments of 8 (i.e. #of Taps=8*(N+1) where N=0-7). For 5x interpolation, the number of taps can be reduced from 60 to 10 taps in increments of 10 (i.e. #of Taps=10*(N+1) where N=0-5). In these reduced length modes, the filter coefficients must be zero-padded to keep the non-zero coefficients centered on tap 32/33 or tap 30/31.

TX CIC

The TX CIC filter is a standard 2nd order interpolating cascaded-integrator-comb filter with selectable interpolation rates of 2, 4, 5, 8, and 16.

The transfer function of the CIC with respect to the output sampling rate of the CIC is, where L is the selected interpolation rate:

$$CIC(z) = \left(\frac{1 - z^{-L}}{1 - z^{-1}}\right)^2$$

For all interpolation rates except for the 5x case, the CIC filter is a unity gain filter. For the 5x case, the filter exhibits a gain of xxx. This gain could be compensated for in the TxFIR if the total gain of the TX path needs to be closer to unity.

TX Data Path Latch

There is a latch after the TXCIC filter that can be used to latch the output of the TX datapath. This functionality is needed is cases that the chosen TXFIR filter does not have a zero at the images of the DC signal being transmitted during an RX operation.

Register 0x1B is used to specify the time from TX->RX transition to the holding of the value out of the TXCIC. This latch time is specified in 2MHz periods, and should be long enough to allow the held DC value at the input of the TX Data path to settle. When the TX Hold register is set to 0x00, then the latch functionality is disabled, and the output of the TXCIC is always pushed to the DAC.

Table 9. SPI Registers for TX path configuration

Address (Hex)	Bit	Description
0x05	(4:2)	Detailed programming mode enables
0x06	(7)	TX FIR bypass
	(4)	TX FIR mode selection
	(3:0)	TX FIR input clock selection
0x07	(7)	TX CIC bypass
	(6:4)	TX CIC mode selection
	(3:0)	TX CIC input clock selection
0x10	(7:4)	DCLK TX mode clock selection
0x11	(7)	TX FIR non-symmetric mode
	(5:3)	TX FIR length selection
0x12	(7:0)	TX modulation maximum (15:8)
0x13	(7:0)	TX modulation maximum (7:0)
0x14	(7:0)	TX modulation minimum (15:8)
0x15	(7:0)	TX modulation minimum (7:0)
0x1E	(7:0)	RAM Coef Address register
0x1F	(7:0)	RAM Coef Data register

RX PATH

Referring again to Figure xx, the Rx digital signal I/Q path consists of an input data de-interleaver, a CIC filter and a RAM FIR filter. The de-interleaver separates the interleaved samples from the ADC before entering the Rx digital filter path. A 2nd order CIC decimation filter follows the de-interleaver to provide initial decimation of the complex Rx data. The output of the CIC filter is then directed to a FIR filter for further decimation by a 4 or 5. Note, Rx digital signal path can also support a decimation factor as high as 80 or can be completely bypassed.

RX CIC

The RX CIC filter is a standard 2nd order decimating CIC filter with selectable decimation rates of 2, 4, 5, 8 and 16.

The transfer function of the CIC with respect to the input sampling rate of the CIC is, where L is the selected interpolation rate:

$$CIC(z) = \left(\frac{1 - z^{-L}}{1 - z^{-1}} \right)^2$$

For all decimation rates except for the 5x case, the CIC filter is a unity gain filter. For the 5x case, the filter exhibits a gain of xxx. This gain could be compensated for in the RxFIR if the total gain of the RX path needs to be closer to unity.

RX FIR

The programmable FIR can be configured as a symmetrical or asymmetrical 4x or 5x interpolation filter as well as simply bypassed via Reg 0x06. Its maximum non-bypassed input data rate is 32 MSPS thus limiting its maximum output data rate to 6.4 and 8.0 MSPS for 5x and 4x interpolation respectively. Since the coefficient RAM supports 32 unique 16-bit FIR coefficients, the standard coefficient configuration is for a 64-or 60-tap symmetric FIR for 4x and 5x interpolation respectively. Figure x.x shows the RAM address space for Rx FIR filters occupying address 0x00 through 0x4F. Programming the FIR filter requires the use of the RAM ADDRESS and RAM DATA SPI Registers previously discussed. Note, due to the filter implementation, the filter coefficients must be written to the RAM *after* the filter mode is selected via 0x06

Table 10. . Rx FIR RAM Address Space

Address (Hex)	Coefficient and Byte
0x00	0 MSB
0x01	0 LSB
0x02	1 MSB
0x03	1 LSB
.....	….
0x3C	30 MSB
0x3D	30 LSB
0x3E	31 MSB
0x3F	31 LSB
…	…
0x4E	39 MSB
0x4F	39 LSB

Table 11. SPI Registers for RX path configuration

Address (Hex)	Bit	Description
0x05	(4)	Detailed programming mode enables for the DCLK
	(1:0)	Detailed programming mode enabled for the RX path filters
0x08	(7)	RX CIC bypass
	(6:4)	RX CIC mode selection

	(3:0)	RX CIC input clock selection
0x09	(7)	RX FIR bypass
	(4)	RX FIR mode selection
	(3:0)	RX FIR input clock selection
0x10	(3:0)	DCLK RX mode clock selection
0x11	(6)	RX FIR non-symmetric mode
	(2:0)	RX FIR length selection
0x1E	(7:0)	RAM Coef Address register
0x1F	(7:0)	RAM Coef Data register

ADIO BUS CONTROL DESCRIPTION

The bidirectional ADIO port is typically shared in burst fashion between the transmit path and receive path. It provides a 16-bit wide data bus in a 2's complement format only. Internally, the ADIO port consists of an input latch for the Tx path in parallel with an output latch with three-state output capability for the Rx path. Note, the ADIO port is three-stated upon power-up and must be disabled via SPI Reg 0x00, bit 6. Also, its output drive strength can be reduced by a half by setting bit 0 of Reg 0x21.

Once enabled, the DSP controls the bus direction via a TX_RXEN signal. The ADIO bus turn around occurs immediately upon receipt of this signal. Note, at the end of a Tx burst, the last sample registered into the Tx path is held and continuously re-sampled by the Tx digital interpolation filters such that the dc values are presented to the I and Q TxDACs. This feature allows the DSP to control the transmit CW power level during a receive (i.e. tag-to-reader) operation and eliminates any transient when going back into transmit operation (i.e. reader-to-tag) provided that the 1st sample is equal to the last sample of the previous Tx burst.

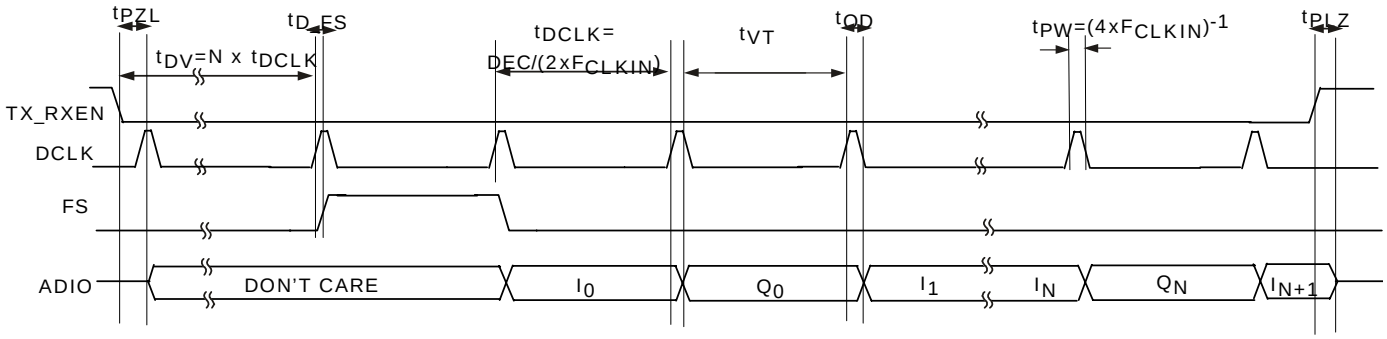

Figure ?a. Timing Diagram of ADIO bus in Rx mode.

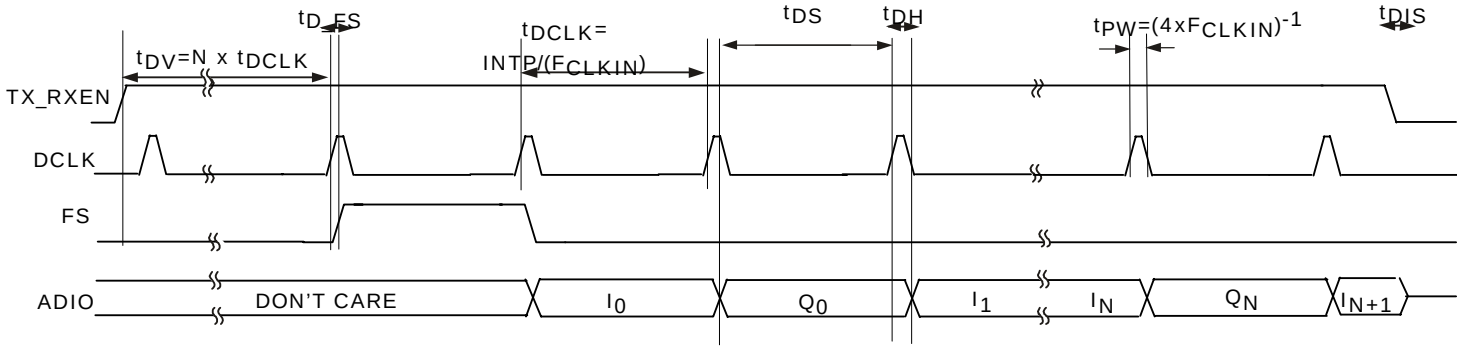

Figure ?a. Timing Diagram of ADIO bus in Tx mode.

Timing diagrams for the ADIO port in Tx and Rx mode are shown in figures ?a and ?b. The AD9960 always serves as the master of the bus providing a clock signal (DCLK) and frame sync pulse (FS) that is equal to one DCLK period . The falling edge of FS indicates when valid data is being placed on the data bus by the AD9960 in Rx mode or can be placed on the bus by the host in Tx mode.

Output data from the ADIO port transitions on the *rising* edge of DCLK while input data is also registered on the *rising* edge. Since the falling edge of FS trails the rising edge of DCLK, it is the next rising edge of DCLK upon which the 1st *valid* output data transitions or input data sample gets latched. The host DSP must also use the FS pulse to maintain proper I/Q pairing in Rx mode (and Tx mode with complex data with the 1st *valid* data on the bus being the I sample.

DCLK is a divided down version of the AD9960's master reference clock, CLKIN, with a constant pulse-width. Its frequency can vary between Tx and Rx modes since the divide-by-N factor depends on the Tx interpolation factor (INTP) and Rx decimation factor (DEC) filter settings. In Rx mode, the DCLK is equal to twice the complex data rate (i.e. 2 x F_{CLKIN}/DEC) since data is always provided as complex interleaved I/Q pairs. In Tx mode, the input data can be real or complex (default setting) hence DCLK will be equal to F_{CLKIN}/INTP or 2 X F_{CLKIN}/INTP. The pulse width of DCLK remains fixed at 1/(4 X F_{CLKIN}).

Interfacing to DSP's

The ADIO bus has been designed to provide a seamless interface to ADI's family of Blackfin DSP's via its DCLK port as shown in figure x.. The Blackfin's DCLK port supports bi-directional data rates up 65 MSPS. It contains a dedicated SPI port allowing easy programming of the AD9960 as well as up to 6 other IC's. The bus turn around of the Blackfin depends mostly on its internal core and system clock frequency as described in application note EE-236.

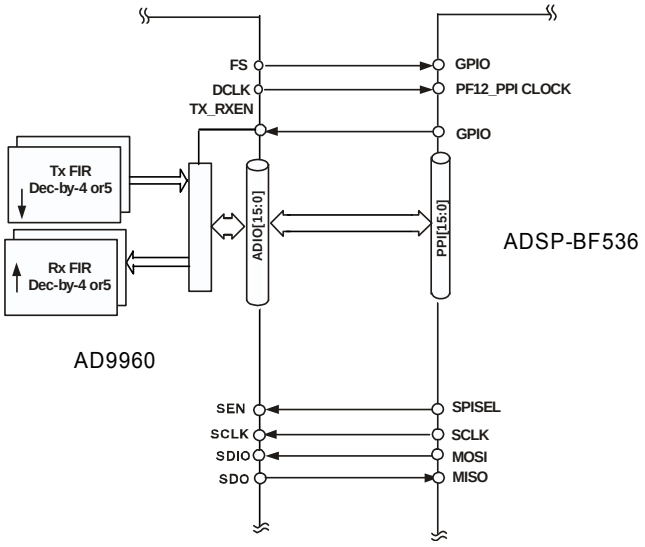

Figure x.x. Digital Interface to ADI BlackFin DSP

The AD9960 can also be interfaced to TI DSP's. The AD9960 can be configured to support TI DSP's requiring the peripheral device to specify the DMA address prior to a DMA operation, By setting bit 2 of Reg 0x01, GPIO_0 and GPIO_1 pins will function as the HCNTL pins to auto-increment the DSP's address regiser. The first 4 cycles during any Rx (Read) or Tx (Write) operation will require the AD9960 to place the 19-bit address register onto the ADIO bus. These addresses are specified in the SPI registers 0x15 through 0x1A. After the DMA has clocked through the full 16-bit address range, an additional 4 cycles of address setup must occur before continuing with the 'write data' cycles.

Table 12. SPI Registers for ADIO Bus

Address (Hex)	Bit	Description
0x00	(6)	ADIO Tri-state Enable
0x01	(3)	Address Generation???
	(2)	TI DSP Interface Mode
	(1)	Real only Tx Data
0x15	(7:0)	TX Address[19:12]
0x16	(7:0)	TX Address[11:4]
0x17	(3:0)	TX Address[3:0]
0x18	(7:0)	RX Address[19:14]
0x19	(7:0)	RX Address[11:4]
0x1A	(3:0)	RX Address[3:0]
0x21	(0)	Low digital drive strength

Alternative 2-wire Tx Data Interface

Applications employing a ASK or PR-ASK modulation scheme may be able to take advantage of an alternative 2-wire Tx data interface. Figure x.x shows such an interface along with a timing diagram to a DSP's serial port. In this interface, the AD9960 provides a data clock via its GPIO_0 pin equal to the baud rate while accepting input data on its GPIO_1 pin relative to the rising edge of this clock. This clock is similar to the DCLK discussed above with its clock rate being equal to F_{CLKIN}/INTP.

ASK or PR-ASK modulation is implemented by the serial data input controlling a multiplexer that places a maximum or minimum value onto the data bus that feeds the Tx digital filter path. These 16-bit values can be loaded into SPI registers 0x0C through 0x0F in a 2's complement format. By appropriate selection of these values, the user can control the digital power level as well as modulation index for ASK. Note, spectral band limiting of this resulting waveform must be performed in the Tx digital filter path.

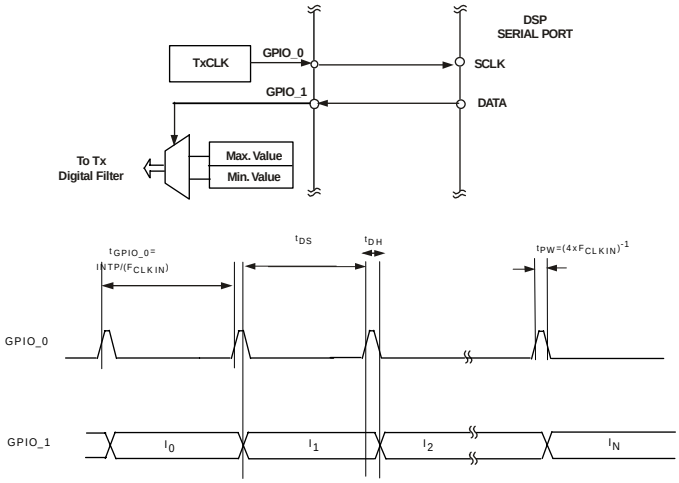

Table 13. SPI Registers for 2-Wire Tx Data Interface

Address (Hex)	Bit	Description
0x01	(0)	Enable GPIO Tx Data Path
0x0C	(7:0)	Max. Modulation Value<15:8>
0x0D	(4)	Max. Modulation Value<7:0>
0x0E	(1)	Max. Modulation Value<15:8>
0x0F	(0)	Min. Modulation Value<7:0>

GPIO FUNCTIONALITY

The AD9960 provides the user with 9 GPIO pins that can be used as general purpose I/Os in addition to sharing functionality with several special purpose modes.

To add greater flexibility to the GPIO pins, pins 0-3 are on the DVDD supply and pins 4-8 are on the ADCVDD supply, giving the system designer access both analog and digital pins. Care must be taken when sourcing or sinking high frequency signals on the analog supplied pins as this can impact the performance of the ADC.

During read back, each of the GPIO pins is synchronized to and latched in the SCLK domain before output on the SPI bus. Read back of pins selected as outputs will always result in a 0 value.

Special Modes

Clock Output Mode

The clock output mode uses GPIO8 to output a clock signal that is a fraction of the system clock. The output options are the same as the clocks that can be selected for the internal data path. See the register map or programming model sections for more information regarding the internal clock selection. This mode is enabled by setting GPIO8 as an output and setting the clock divide ratio.

This mode is intended to supply a clock to DSPs that cannot use the 32MHz TCXO. This may need to be a dedicated output pin since the DSP needs to have its clock before it can communicate over the SPI interface to configure the AD9960.

Address	Value	Description
0x10	0x7F	Set GPIO8 to an output
0x14	0x1?	Enable the clock output mode, replace "?" with the clock selection value from the "Clock Selection" table in "Programming Model" section

Table 14: Register writes to enable the GPIO clock out mode

ADC Overload Mode

In this mode, GPIO4 can be used as an output to indicate an ADC overload condition. The direction bit for this pin must set as an output for this to work. The Overload bit in the SPI must also be set.

Address	Value	Description
0x10	0xF7	Set GPIO4 to an output
0x14	0x40	Enable the ADC overrange mode

Table 15: Register writes to enable the ADC overrange functionality

Rev. A-082203

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.326.8703

RX SIGNAL PATH

DESCRIPTION

The AD9960'S Rx signal path is shown in figure x. It consists of a dual input sample-and-hold (SHA) , a 14-bit analog-to-digital converter (ADC), followed by a de-multiplexer. The SHA simultaneously samples the I and Q inputs at one-half the ADC sample rate and presents the interleaved pair of samples to the ADC for conversion. The switched capacitor, pipelined ADC digitizes the continuous stream of interleaved I and Q samples to 14-bits of resolutions. These digitized samples are then de-interleaved by a demultiplexer before being passed on to the digital filters for further post processing.

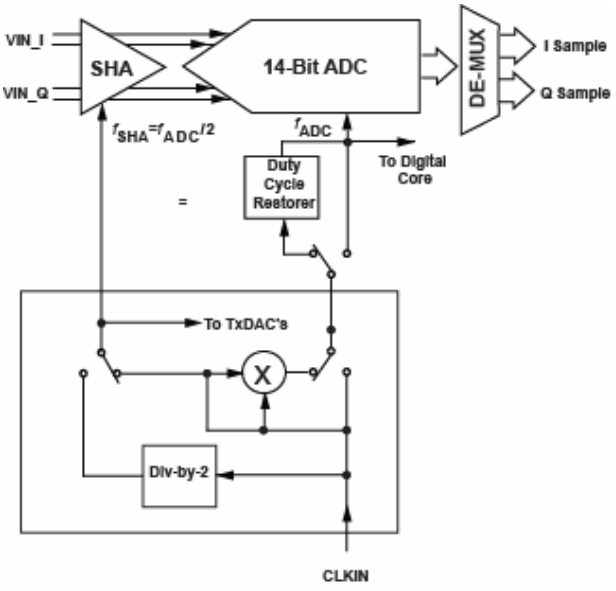

Figure x.x Rx Signal Path and Clock Generation Block Diagram

The ADC always operates at twice the SHA sample rate since it must digitize I and Q interleaved samples. The CLKIN input which serves as the AD9960's master system clock can operate at either the lower SHA sample rate or higher ADC conversion rate. In the former case, an on-chip 2x clock multiplier can be used to generate the higher ADC clock rate for CLKIN frequencies between 16-32 MHz. In this mode, an optional duty cycle restorer can be enabled to ensure that the ADC's sampling clock is approximately 50%. In the latter case, a buffered version of CLKIN is used for the ADC clock rate while a divide-by-2 version of this clock is used for the SHA sampling clock. Note, sampling of the analog inputs occur on the positive edge.

Several parameters and features pertaining to the Rx signal path and clock generator can be adjusted or enabled via the SPI. Table X.X below shows the various SPI registers pertaining to these sections of the IC.

Table 16. SPI Registers for Rx Path and Clock Generator

Address (Hex)	Bit	Description
0x20	(7)	Power Down ADC
	(6)	Power Down VREF
	(5)	Power Down Ref Buffer
	(4)	Power Down CLK and Aux Bias
	(3)	Power Down CLK Multiplier
0x22	(7)	ADC Input Span (3 Vp.p.=0)
	(6)	Enable Duty Cycle Restorer
	(5)	Rx Path 2's Complement
	(4:2)	SHA_ADC Bias Control

POWER BIAS SCALING

The power bias of the AD9960 's ADC (including SHA) can be adjusted over a wide range via SPI register 0x22, bits 4:2. This feature enables the Rx path's power bias to be optimized based on a particular applications performance and sample rate requirements[1]. Figure x.a shows how the current consumption scales with ADC clock rates of 64 and 32 MSPS for the eight possible SPI power scaling settings. Figure x.b shows how the THD and SFDR performance for a full-scale 1 MHz sine wave while figure x.c shows how the SNR varies under the same conditions. These figures indicate that over a 60% savings in current consumtion can be realized when operating the ADC at sample rates at 32 MSPS or less.

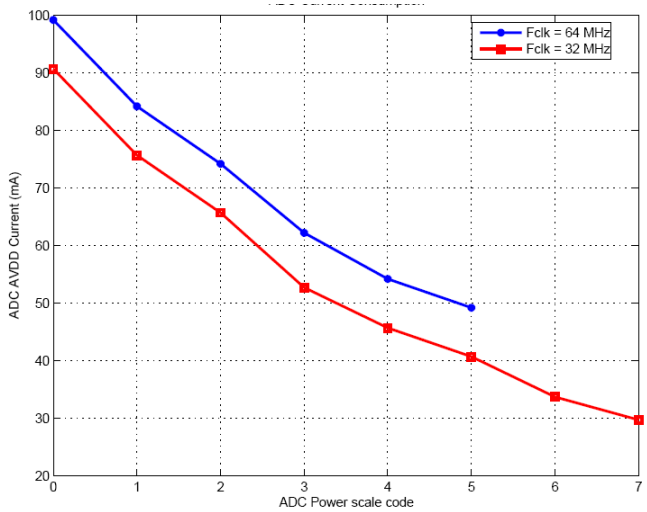

Figure x.a ADC power consumption vs SPI register scaling code.

[1] The current consumption of the digital circuitry that follows the ADC scales proportionally to the ADC sample rate.

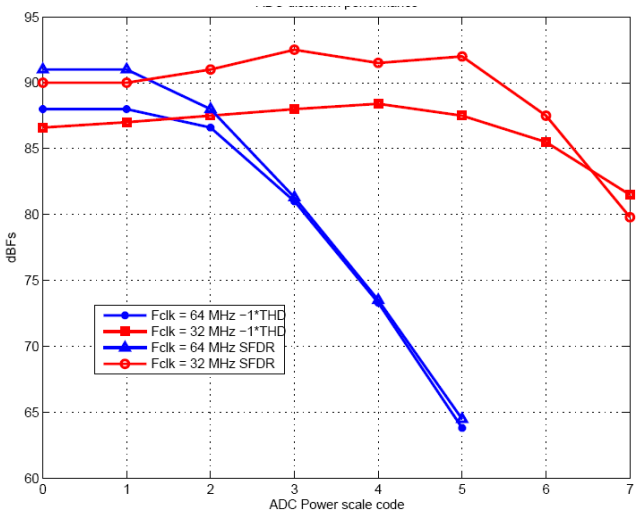

Figure x.x THD and SFDR performance for a 1 MHz, -0.5 dBFS sine wave as a function of power scaling setting.

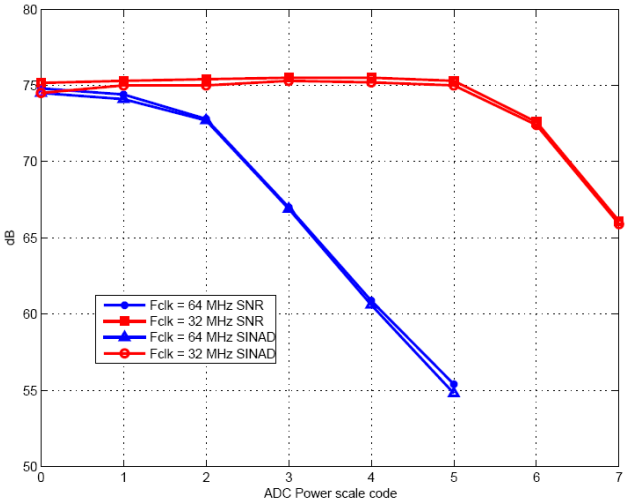

Figure x.x. SNR performance for a 1 MHz, -0.5 dBFS sine wave as a function of power scaling setting

ANALOG INPUT

The two analog input to the AD9960 consists of a differential, switched-capacitor SHA that has been designed for optimum performance while processing differential input signals that can configured for 3 or 2 Vp.p. (depending on the voltage reference setting). The SHA inputs can operate over a wide common-mode range of 0.75 to 2.25 V however a common-mode voltage around mid-supply typically results in optimum linearity performance.

The differential sampling capacitors of the SHA are approximately 5 pF. These capacitors are alternatively switched between the input source during sample mode and an internal bias voltage during hold mode. When the SHA is switched into sample mode, the signal source must charge these sample capacitors such that the voltage across these capacitors accurately track the signal sources input voltage prior to going into hold mode. Referring to figure x.x., a small resistor in series with each input (i.e. 50 Ω) can help reduce the peak transient current required from the output stage of the driving source. Also, a small shunt capacitor can be placed across the inputs to provide dynamic charging currents.

This passive network also creates a 1st order low-pass filter at the ADC input; therefore, the precise values are application dependent. This network in combination with the driving source impedance and effective differential input capacitance of the ADC (i.e. 5 pF) limits the input bandwidth to the ADC. It serves to filter any out-of-band signals and wideband noise from the driving source. For baseband applications, the pole formed by this low pass filter can also be used in conjunction with other filters to realize an overall desired transfer function.

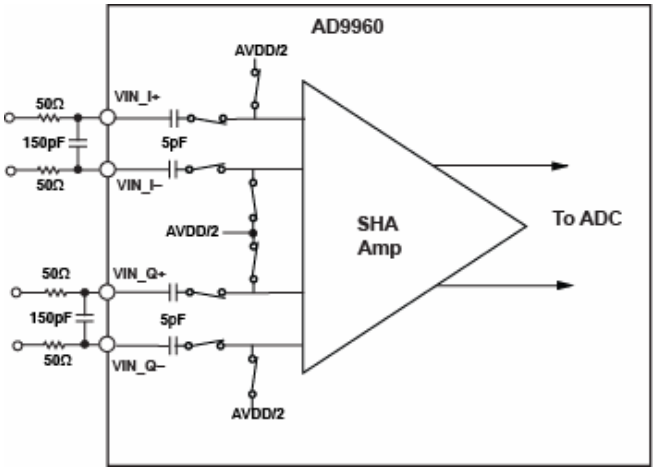

Figure 31. Switched-Capacitor Input

ADC VOLTAGE REFERENCES

The AD9960 's ADC uses an internal references that is designed to support a 3 or 2 V p-p differential input span. The input span is selected via bit 7 of SPI Register 0x22 . Maximum SNR performance is achieved with the reference set to its default setting of 3 V p-p. The relative SNR degradation is approximately 3 dB when the input span is reduced to 2 V p-p.

Figure x.x shows a block diagram of the AD9260's voltage referance and buffer amplifier. The internal band gap reference generates a stable 0.5 V reference voltage. This temperature stable voltage then gets amplified to produce a 1.5 (or 1.0 V) at the VREF pin. REFT and REFB are the differential references generated based on the voltage level of VREF.

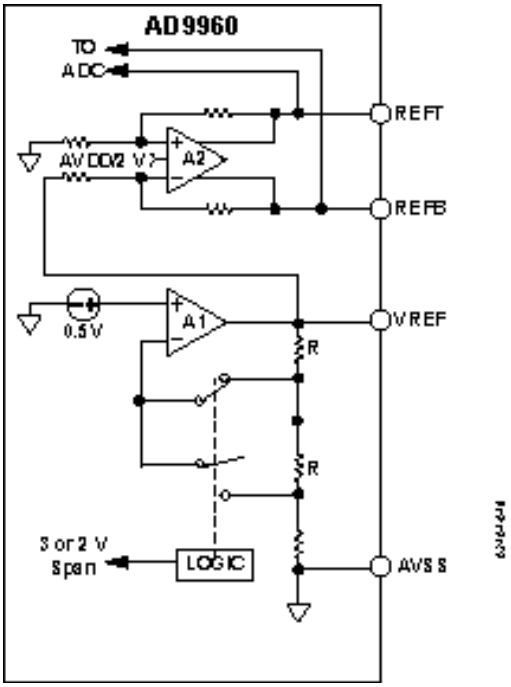

Figure ##. ADC Reference and Reference Buffer

REFT and REFB will be centered at AVDD/2 with a differential voltage equal to the voltage at VREF (by default 1.5 V) allowing a peak to peak differential voltage swing of 2 times VREF. For example, the default 1.5 V VREF reference accepts a 3 V p-p differential input swing and the offset voltage should be:

REFT: AVDD/2 + 0.75 V,
REFB: AVDD/2 – 0.75 V

Figure ## shows the proper decoupling of the reference pins VREF, REFT and REFB. The 0.01 uF differerential capacitor should be placed as close as possible to the REFT and REFT pins (i.e. 402 size) while the other 0.1 uF caps can be placed in proximity to this capacitor. Refer to the AD9960's evaluation board layout documentation for recommended component placements.

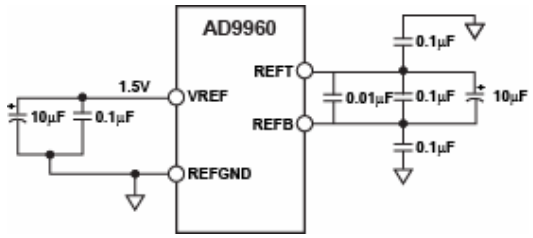

Figure ##. Reference and Reference Buffer Decoupling

CLOCK INPUT AND CONSIDERATIONS

The CLKIN input of the AD9960' provides the master system clock from which all other internal clocks are generated. As shown in figure x.x., the TxDAC's operate off of a buffered version of the SHA sampling clock while a buffered version of the ADC clock is passed to the digital core. As previously mentioned, the ADC clock rate is twice the sample rate of the SHA. Consequencely, the frequency appearing at this CMOS compatible input can be equal to or twice the sample rate of the dual input SHA.

The ADC use both clock edges to generate a variety of internal timing signals and as a result may be sensitive to clock duty cycle at the higher clock rates (i.e**. > 32 MHz**) . A duty cycle restorer can be enabled via bit 6 of Reg 0x22 to ensure that the ADC sampling clock gets approximately a 50% duty cycle from the on-chip 2X clock multiplier or the external direct clock. The duty cycle restorer is specified to operate between 32-64 Mhz and consists of a delay-locked loop circuit that retimes the non-sampling edge, providing an internal clock to the ADC with a nominal 50% duty cycle . Note, the low jitter sampling edge is always passed on to the dual input SHA.

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given full-scale input frequency (f_{INPUT}) due only to aperture jitter (t_A) can be calculated with the following equation:

$$SNR\ degradation = 20 \log [(½)\pi F_{IN} t_A)]$$

In the equation, the rms aperture jitter, t_A, represents the root-sum-square of all jitter sources, which includes the clock input, analog input signal, and aperture jitter specification of its SHA.

The clock input is a digital signal that should be treated as an analog signal with CMOS logic level threshold voltages, especially in cases where aperture jitter may affect the dynamic range of the AD9960. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter crystal controlled oscillators make the best clock sources.

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TX SIGNAL PATH

DESCRIPTION

The AD9960 Tx path consisting of dual 12-bit DACs is shown in Figure . The TxDAC core of the AD9960 provides dual, differential, complementary current outputs that can be set from 2-20 mA via an external resistor. The 12-bit dual DACs support update rates up to 64 MSPS. The differential outputs (i.e., IOUT+ and IOUT–) of each dual DAC are complementary, meaning they always sum to the full-scale current output of the DAC, I_{OUTFS}. Optimum ac performance is achieved when the differential current interface drives balanced loads or a transformer.

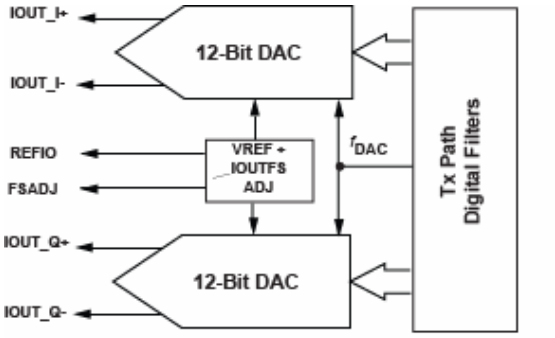

Figure x.x.

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The reference circuitry with the required external components is shown in Figure 3. A 1.2 V internal reference provides a stable voltage to a V-I configured amplifier that converts this voltage to a reference current, I_{REF}, that is then replicated in the I and Q DAC cores.

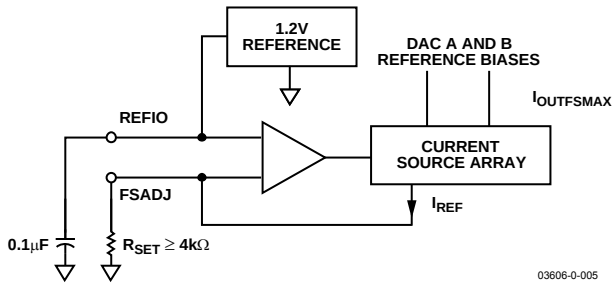


Figure 3.

Referring to the transfer function of the equation below, $I_{OUTFSMAX}$ is the maximum current output of the DAC and is based on a reference current, I_{REF}. I_{REF} is set by the internal 1.2 V reference and the external R_{SET} resistor.

$$I_{OUTFSMAX} = 64 \times (REFIO/R_{SET})$$

Typically, R_{SET} is 4 kΩ, which sets $I_{OUTFSMAX}$ to 20 mA, the optimal dynamic setting for the TxDACs. Increasing R_{SET} by a factor of 2 will proportionally decrease $I_{OUTFSMAX}$ by a factor of 2.

AUXILIARY CONVERTERS

The AD9960 contains three auxiliary analog to digital converters (AuxADC) and two digital to analog converters (AuxDAC) as shown in figure x.x. These auxiliary converters can be used to measure or force system wide control signals. The inputs to the AuxADC's and outputs of the AuxDAC's are single-ended voltages that are ground referenced. The full-scale span of these auxiliary converters can be set to the AVDD supply or to a programmable regulator.

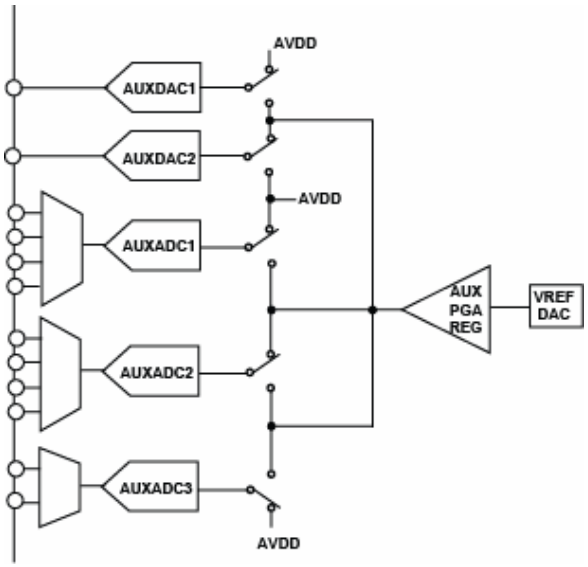
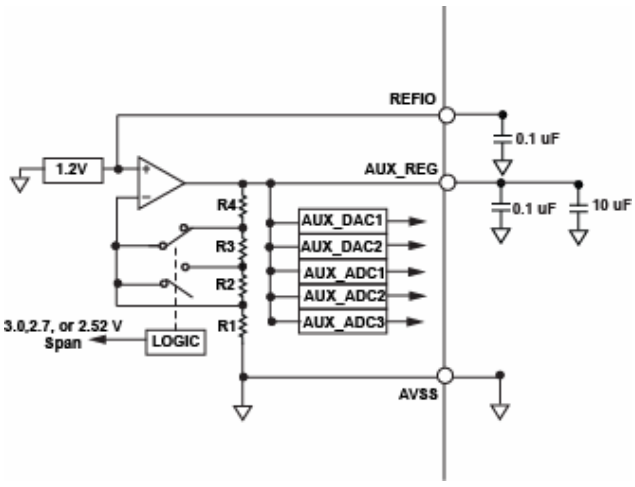


Figure x.x Block diagram of auxiliary ADC's and DAC's.

The programmable regulator is shown in figure x.x. It shares the same 1.2 V reference used by the TxDAC core and can be set to 3 voltage levels via SPI Reg 0x25, bits 1:0. The full-scale span to bits assignment is as follows: 3V[1] for "00", 2.7 V for "01", and 2.52 V for "10". Note, the regulator amplifier output has both low bandwidth and drive capability thus it relies on the external capacitor(s) to provide a low impedance source for the switched capacitor SAR ADC's.



[1] Operation with 3.0 V Span is only recommended for AVDD greater than 3.14 V due to headroom constraints on the regulator.

Figure x.x Auxiliary regulator provides AuxADC's and AuxDAC's with three full-scale span levels.

The auxiliary converters by default are disabled and powered down. Enabling and controlling the auxiliary converters is achieved through the serial programmable registers.

Auxiliary DAC

The AD9960 integrates two 10-bit voltage output auxiliary digital-to-analog converters (AuxDACs), which can be used for setting control voltages. The AuxDACs have programmable options including full scale output voltage, V_{OUTFS} and invert its output.

By default the AuxDAC outputs are powered down and require a serial write to the Power Up registers (Reg 0x29, bit 2-0) to enable them.

The full-scale output of each AuxDAC is independently programmable to full scales of 2.5 V, 2.7 V, 3.0 V or 3.3 V using serial register 0x17. The AuxDAC outputs have an I-to-V driver that produces a voltage output that settles to ±1 LSB within 0.5 µs. The output driver is capable of sinking or sourcing up to 6 mA. Utilizing this feature requires the SPI to be operational.

Power up, pin connections, setting full scale, synchronizing with SPI, synchronizing with Tx Power up signal. to either a single register write or to the TxPwnDwn rising edge. The AuxDACs are based on a resistor divider network.

The AuxDACs output level is proportional to the straight binary input codes from the appropriate SPI registers, Registers 0x24-0x26. By default, the AuxDAC output is updated immediately following the register write, but the update can occur synchronize to a single register write or the TxPwrDwn rising edge.

In slave mode, the AuxDACs update will occur when a logic high is written to the appropriate update registers (Reg0x28, bits 2-0 'Update C, B and A'). Slave mode is enabled by writing a high to the slave mode register bit (Reg0x28, bit 7 'Slave Enable').

Typical settling time for the AuxDAC output is less than 0.5 µs, but is dependent on the load.

Auxiliary ADC

Two auxiliary 10-bit SAR ADCs (AuxADCs) are available for monitoring various external signals throughout the system, such as a receive signal strength indicator (RSSI) function or temperature indicator. The AuxADCs have programmable options including various full scale reference options, conversion rate speed, enabling an auxiliary serial port interface for dedicated data transfers and a sampling average function.

By default the AuxADCs are powered down and automatically powered up when a conversion is initiated.

The two auxiliary ADCs (AuxADC_A and AuxADC_B) can monitor up to three system signals. AuxADC_A has multiplexed inputs that control whether pin AUX_ADC_A1 or pin AUX_ADC_A2 is connected to the input of AuxADC_A. The multiplexer is programmed through **Register xx, SelectA**. By default, the register is low, which connects the AUX_ADCA2 pin to the input.

The full-scale AuxADC reference can be generated from the analog supply (supply dependent), an internal reference, or an external applied reference. Table ## show the proper register setting required to select the AuxADC full scale reference.

By default, an internal reference provides a buffered full-scale reference for both of the auxiliary ADCs that is equal to the supply voltage for the auxiliary ADCs (PLL_AVDD). A supply independent 2.5 V or 3.0 V internal full scale reference can be enabled by writing to register 'Aux ADC Ref Enable' and 'Aux ADC Ref FS' in register 0x17. This internal reference is based on the main Rx path ADC Vref voltage, so it requires that the main Rx path Vref is enabled.

Another AuxADC full scale reference option is an external supplied full-scale reference. The external reference can be applied to either or both of the Aux ADCs by setting the appropriate bit(s) in register 0x22 and 0x17. Setting either or both of these bits high will disconnect the internal reference buffer and enable the externally applied reference from the AuxADC_Ref pin to the respective channel(s).

erence	Aux ADC Ref Enable [Reg0x17, b1]	Aux ADC Ref FS [Reg0x17, b0]	Refsel A/B [Reg0x22, b2/b1]	NOTE
VDD	0	0	0	(2.5xVref)
3xVref)	1	0	1	Decouple at AUXADC_REF pin
	1	1	1	Decouple at AUXADC_REF pin
				Externally forced

	0	Don't Care	1	Force and decouple

Table ##. Configuring AuxADC reference

The AuxADCs can convert at rates up to 5.33 MSPS (0.1875 µs maximum conversion time) and have a bandwidth of around 200 kHz. The conversion time, including setup, requires 16 clock cycles. The maximum clock rate for the auxiliary ADCs is 64 MHz and is generated from a divided down Rx ADC clock. The divide down ratio is controlled by register AuxADC Clock Div [Regter 0x23, b1,0]. By default, the Rx ADC clock is divided by 4. At an Rx ADC rate greater than 64 MHz, the AuxADC Clock Div register must be set to divide by 2 or divide by 4.

On-chip averaging of 2, 4, 8, 16, 32, or 64 samples can be enabled through register 0x18 for AuxADC_A or 0x19 for AuxADC_B. When the averaging option is enabled, the AuxADC will continually convert the number of samples specified and output the average value.

There are three mode of operating the AuxADC: SPI Operation mode (default), SPI with External Start Convert Operation mode, and Aux_SPI Operation mode.

In the default SPI Operation mode, a conversion is initiated by writing a logic high to one or both of the Start register bits, Start A or Start B [Reg0x22, b0 or b3]. If AuxADC is configured as averaging mode, the proper start bit is the Start Average Aux ADC A/B register [Reg 0x18, b7/Reg 0x19, b7].

When the conversion is complete, the straight binary, 10-bit output data of the AuxADC is written to one of three reserved locations in the register map, depending on which auxiliary ADC and which multiplexed input is selected. Because the auxiliary ADCs output 10 bits, two register addresses are needed for each data location.

Rev. A-082203

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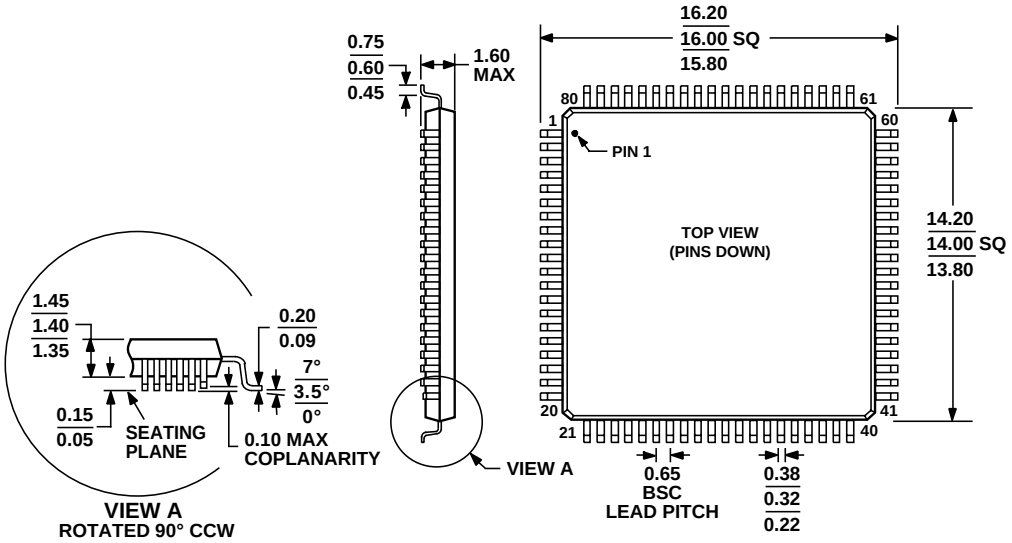
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-BEC

Figure 4.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

Model	Temperature Range	Description	Package Option
AD9960	–40°C to +85°C (Ambient)	80-Pin LFCSP	CP-80
AD9960/PCB	25°C (Ambient)	Evaluation Board	

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