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REVISION HISTORY

4/05—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 2.7 V to 3.6 V or 4.75 V to 5.25 V; GND = 0 V; EXC = 32 kHz; EXC = $\pm V_{DD}/2$; −40°C to +125°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CAPACITIVE INPUT					
Conversion Input Range		±4.096		pF[1]	Factory calibrated
Integral Nonlinearity (INL)[2]			±0.01	% of FSR	
No Missing Codes[2]	24			Bit	Conversion time ≥ 62 ms
Resolution, p-p		16.5		Bit	Conversion time = 62 ms, see Table 5
Resolution Effective		19		Bit	Conversion time = 62 ms, see Table 5
Output Noise, rms		2		aF/√Hz	See Table 5
Absolute Error[3]			±4	fF[1]	25°C, V_{DD} = 5 V, after offset calibration
Offset Error[2, 4]			32	aF[1]	After system offset calibration, Excluding effect of noise[4]
System Offset Calibration Range[2]			±1	pF	
Offset Drift vs. Temperature		−1		aF/°C	
Gain Error[5]		0.02	0.08	% of FS	25°C, V_{DD} = 5 V
Gain Drift vs. Temperature[2]	−28	−26	−24	ppm of FS/°C	
Allowed Capacitance to GND[2]			60	pF	See Figure 9 and Figure 10
Power Supply Rejection		0.3	1	fF/V	
Normal Mode Rejection		65		dB	50 Hz ± 1%, conversion time = 62 ms
		55		dB	60 Hz ± 1%, conversion time = 62 ms
Channel-to-Channel Isolation		70		dB	AD7746 only
CAPDAC					
Full Range	17	21		pF	
Resolution[6]		164		fF	7-bit CAPDAC
Drift vs. Temperature[2]	24	26	28	ppm of FS/°C	
EXCITATION					
Frequency		32		kHz	
Voltage Across Capacitance		$\pm V_{DD}/8$		V	Configurable via digital interface
		$\pm V_{DD}/4$		V	
		$\pm V_{DD} \times 3/8$		V	
		$\pm V_{DD}/2$		V	
Average DC Voltage Across Capacitance			<±40	mV	
Allowed Capacitance to GND[2]			100	pF	See Figure 11
TEMPERATURE SENSOR[7]					V_{REF} internal
Resolution		0.1		°C	
Error[2]		±0.5	±2	°C	Internal temperature sensor
		±2		°C	External sensing diode[8]
VOLTAGE INPUT[7]					V_{REF} internal or V_{REF} = 2.5 V
Differential VIN Voltage Range		$\pm V_{REF}$		V	
Absolute VIN Voltage[2]	GND − 0.03		V_{DD} + 0.03	V	
Integral Nonlinearity (INL)		±3	±15	ppm of FS	
No Missing Codes[2]	24			Bit	Conversion time = 122.1 ms
Resolution, p-p		16		Bits	Conversion time = 62 ms See Table 6 and Table 7
Output Noise		3		µV rms	Conversion time = 62 ms See Table 6 and Table 7
Offset Error		±3		µV	
Offset Drift vs. Temperature		15		nV/°C	
Full-Scale Error[2, 9]		0.025	0.1	% of FS	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Full-Scale Drift vs. Temperature		5		ppm of FS/°C	Internal reference
		0.5		ppm of FS/°C	External reference
Average VIN Input Current		300		nA/V	
Analog VIN Input Current Drift		±50		pA/V/°C	
Power Supply Rejection		80		dB	Internal reference, $V_{IN} = V_{REF}/2$
Power Supply Rejection		90		dB	External reference, $V_{IN} = V_{REF}/2$
Normal Mode Rejection		75		dB	50 Hz ± 1%, conversion time = 122.1 ms
		50		dB	60 Hz ± 1%, conversion time = 122.1 ms
Common-Mode Rejection		95		dB	V_{IN} = 1 V
INTERNAL VOLTAGE REFERENCE					
Voltage	1.169	1.17	1.171	V	T_A = 25°C
Drift vs. Temperature		5		ppm/°C	
EXTERNAL VOLTAGE REFERENCE INPUT					
Differential REFIN Voltage[2]	0.1	2.5	V_{DD}	V	
Absolute REFIN Voltage[2]	GND − 0.03		V_{DD} + 0.03	V	
Average REFIN Input Current		400		nA/V	
Average REFIN Input Current Drift		±50		pA/V/°C	
Common-Mode Rejection		80		dB	
SERIAL INTERFACE LOGIC INPUTS (SCL, SDA)					
V_{IH} Input High Voltage	2.1			V	
V_{IL} Input Low Voltage			0.8	V	
Hysteresis		150		mV	
Input Leakage Current (SCL)		±0.1	±1	µA	
OPEN-DRAIN OUTPUT (SDA)					
V_{OL} Output Low Voltage			0.4	V	I_{SINK} = −6.0 mA
I_{OH} Output High Leakage Current		0.1	1	µA	$V_{OUT} = V_{DD}$
LOGIC OUTPUT ($\overline{RDY}$)					
V_{OL} Output Low Voltage			0.4	V	I_{SINK} = 1.6 mA, V_{DD} = 5 V
V_{OH} Output High Voltage	4.0			V	I_{SOURCE} = 200 µA, V_{DD} = 5 V
V_{OL} Output Low Voltage			0.4	V	I_{SINK} = 100 µA, V_{DD} = 3 V
V_{OH} Output High Voltage	V_{DD} − 0.6			V	I_{SOURCE} = 100 µA, V_{DD} = 3 V
POWER REQUIREMENTS					
V_{DD}-to-GND Voltage	4.75		5.25	V	V_{DD} = 5 V, nominal
	2.7		3.6	V	V_{DD} = 3.3 V, nominal
I_{DD} Current			850	µA	Digital inputs equal to V_{DD} or GND
		750		µA	V_{DD} = 5 V
		700		µA	V_{DD} = 3.3 V
I_{DD} Current Power-Down Mode		0.5	2	µA	Digital inputs equal to V_{DD} or GND

[1] Capacitance units: 1 pF = 10^{-12} F; 1 fF = 10^{-15} F; 1 aF = 10^{-18} F.
[2] Specification is not production tested, but is supported by characterization data at initial product release.
[3] Factory calibrated. The absolute error includes factory gain calibration error, integral nonlinearity error, and offset error after system offset calibration, all at 25°C. At different temperatures, compensation for gain drift over temperature is required.
[4] The capacitive input offset can be eliminated using a system offset calibration. The accuracy of the system offset calibration is limited by the offset calibration register LSB size (32 aF) or by converter + system p-p noise during the system capacitive offset calibration, whichever is greater. To minimize the effect of the converter + system noise, longer conversion times should be used for system capacitive offset calibration. The system capacitance offset calibration range is ±1 pF, the larger offset can be removed using CAPDACs.
[5] The gain error is factory calibrated at 25°C. At different temperatures, compensation for gain drift over temperature is required.
[6] The CAPDAC resolution is seven bits in the actual CAPDAC full range. Using the on-chip offset calibration or adjusting the capacitive offset calibration register can further reduce the CIN offset or the unchanging CIN component.
[7] The VTCHOP bit in the VT SETUP register must be set to 1 for the specified temperature sensor and voltage input performance.
[8] Using an external temperature sensing diode 2N3906, with nonideality factor n_f = 1.008, connected as in Figure 41, with total serial resistance <100 Ω.
[9] Full-scale error applies to both positive and negative full scale.

TIMING SPECIFICATIONS

V_{DD} = 2.7 V to 3.6 V, or 4.75 V to 5.25 V; GND = 0 V; Input Logic 0 = 0 V; Input Logic 1 = V_{DD}; –40°C to +125°C, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SERIAL INTERFACE[1, 2]					See Figure 3
SCL Frequency	0		400	kHz	
SCL High Pulse Width, t_{HIGH}	0.6			µs	
SCL Low Pulse Width, t_{LOW}	1.3			µs	
SCL, SDA Rise Time, t_R			0.3	µs	
SCL, SDA Fall Time, t_F			0.3	µs	
Hold Time (Start Condition), $t_{HD;STA}$	0.6			µs	After this period, the first clock is generated
Set-Up Time (Start Condition), $t_{SU;STA}$	0.6			µs	Relevant for repeated start condition
Data Set-Up Time, $t_{SU;DAT}$	0.25			µs	$V_{DD} \geq 3.0$ V
Data Set-Up Time, $t_{SU;DAT}$	0.35			µs	$V_{DD} < 3.0$ V
Set-Up Time (Stop Condition), $t_{SU;STO}$	0.6			µs	
Data Hold Time, $t_{HD;DAT}$ (Master)	0			µs	
Bus-Free Time (Between Stop and Start Condition, t_{BUF})	1.3			µs	

[1] Sample tested during initial release to ensure compliance.
[2] All input signals are specified with input rise/fall times = 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Output load = 10 pF.

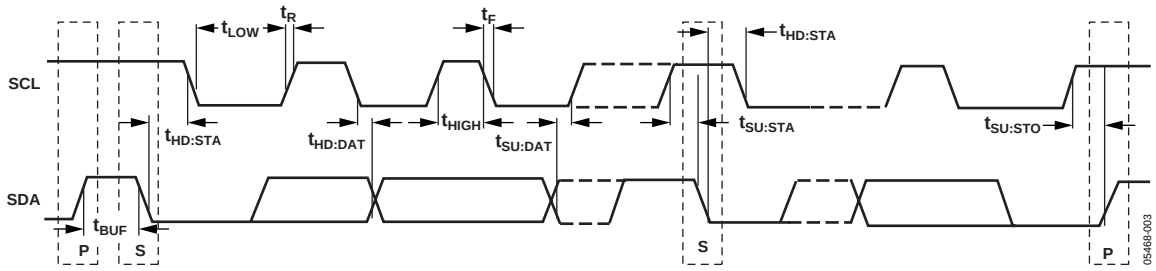


Figure 3. Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
Positive Supply Voltage V_{DD} to GND	−0.3 V to +6.5 V
Voltage on any Input or Output Pin to GND	−0.3 V to V_{DD} + 0.3 V
ESD Rating (ESD Association Human Body Model, S5.1)	2000 V
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
TSSOP Package θ_{JA}, (Thermal Impedance-to-Air)	128°C/W
TSSOP Package θ_{JC}, (Thermal Impedance-to-Case)	14°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

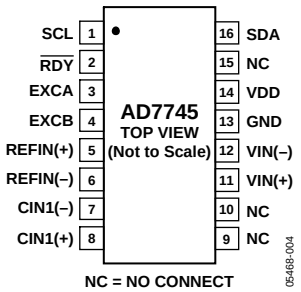


Figure 4. AD7745 Pin Configuration (16-Lead TSSOP)

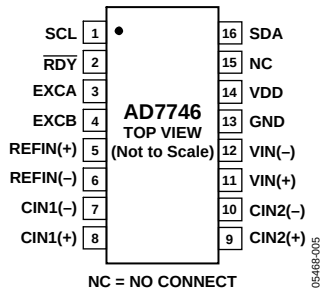


Figure 5. AD7746 Pin Configuration (16-Lead TSSOP)

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SCL	Serial Interface Clock Input. Connects to the master clock line. Requires pull-up resistor if not already provided in the system.
2	$\overline{\text{RDY}}$	Logic Output. A falling edge on this output indicates that a conversion on enabled channel(s) has been finished and the new data is available. Alternatively, the status register can be read via the 2-wire serial interface and the relevant bit(s) decoded to query the finished conversion. If not used, this pin should be left as an open circuit.
3, 4	EXCA, EXCB	CDC Excitation Outputs. The measured capacitance is connected between one of the EXC pins and one of the CIN pins. If not used, these pins should be left as an open circuit.
5, 6	REFIN(+), REFIN(–)	Differential Voltage Reference Input for the Voltage Channel (ADC). Alternatively, the on-chip internal reference can be used for the voltage channel. These reference input pins are not used for conversion on capacitive channel(s) (CDC). If not used, these pins can be left as an open circuit or connected to GND.
7	CIN1(–)	CDC Negative Capacitive Input in Differential Mode. This pin is internally disconnected in single-ended CDC configuration. If not used, this pin can be left as an open circuit or connected to GND.
8	CIN1(+)	CDC Capacitive Input (in Single-Ended Mode) or Positive Capacitive Input (in Differential Mode). The measured capacitance is connected between one of the EXC pins and one of the CIN pins. If not used, this pin can be left as an open circuit or connected to GND.
9, 10 (AD7745)	NC	Not Connected. This pin should be left as an open circuit.
9 (AD7746)	CIN2(+)	CDC Second Capacitive Input (in Single-Ended Mode) or Positive Capacitive Input (in Differential Mode). If not used, this pin can be left open circuit or connected to GND.
10 (AD7746)	CIN2(–)	CDC Negative Capacitive Input in Differential Mode. This pin is internally disconnected in a single-ended CDC configuration. If not used, this pin can be left as an open circuit or connected to GND.
11, 12	VIN(+), VIN(–)	Differential Voltage Input for the Voltage Channel (ADC). These pins are also used to connect an external temperature sensing diode. If not used, these pins can be left as an open circuit or connected to GND.
13	GND	Ground Pin.
14	VDD	Power Supply Voltage. This pin should be decoupled to GND, using a low impedance capacitor, for example in combination with a 10 µF tantalum and a 0.1 µF multilayer ceramic.
15	NC	Not Connected. This pin should be left as an open circuit.
16	SDA	Serial Interface Bidirectional Data. Connects to the master data line. Requires a pull-up resistor if not provided elsewhere in the system.

TYPICAL PERFORMANCE CHARACTERISTICS

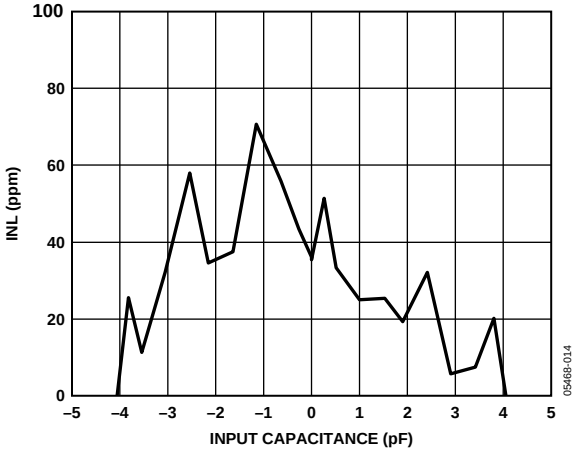


Figure 6. Capacitance Input Integral Nonlinearity, V_{DD} = 5 V, the Same Configuration as in Figure 31

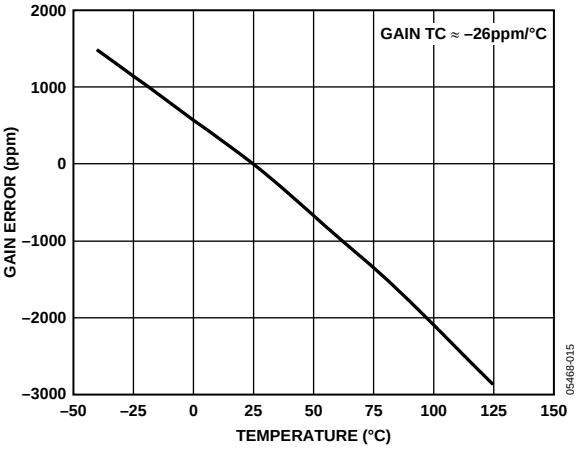


Figure 7. Capacitance Input Offset Drift vs. Temperature, V_{DD} = 5 V, CIN and EXC Pins Open Circuit

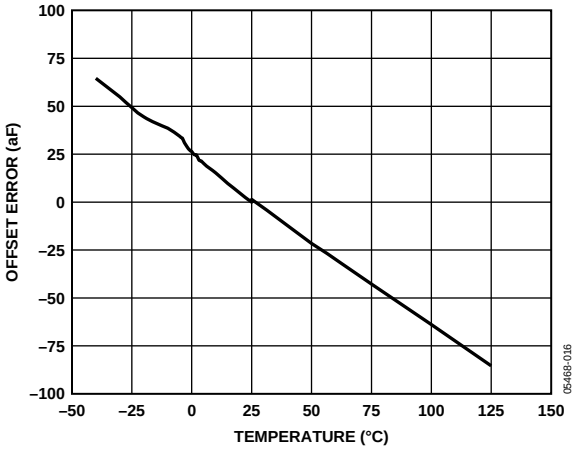


Figure 8. Capacitance Input Gain Drift vs. Temperature, V_{DD} = 5 V, CIN(+) to EXC = 4 pF, the Same Configuration as in Figure 30

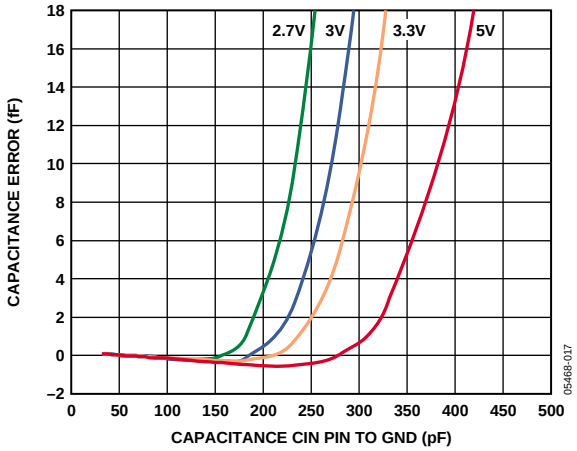


Figure 9. Capacitance Input Error vs. Capacitance between CIN and GND. CIN(+) to EXC = 4 pF, CIN(–) to EXC = 0 pF, V_{DD} = 2.7 V, 3 V, 3.3 V, and 5 V, the Same Configuration as in Figure 33

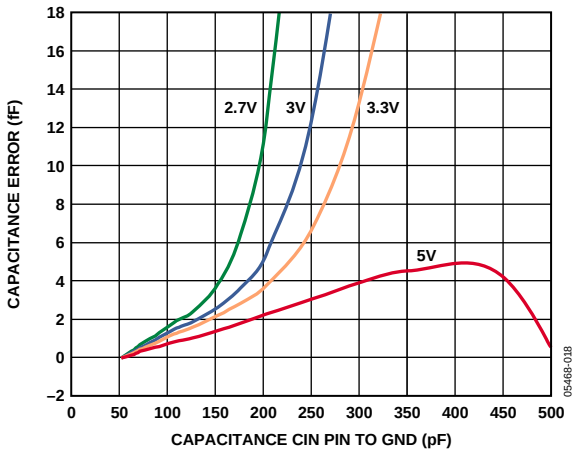


Figure 10. Capacitance Input Error vs. Capacitance between CIN and GND, CIN(+) to EXC = 21 pF, CIN(–) to EXC = 23 pF, V_{DD} = 2.7 V, 3 V, 3.3 V, and 5 V, the Same Configuration as in Figure 34

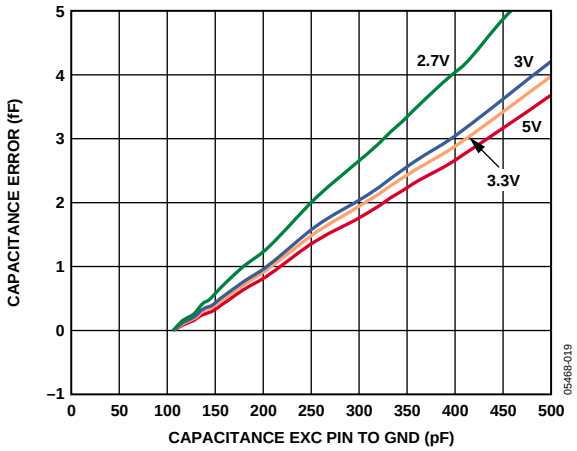


Figure 11. Capacitance Input Error vs. Capacitance between EXC and GND, CIN(+) to EXC = 21 pF, CIN(–) to EXC = 23 pF, V_{DD} = 2.7 V, 3 V, 3.3 V, and 5 V, the Same Configuration as in Figure 34

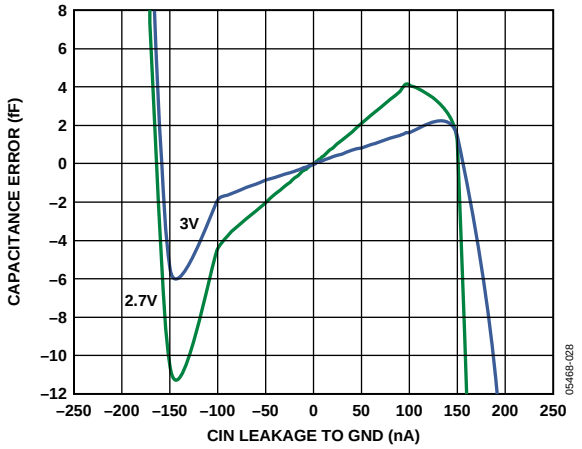


Figure 12. Capacitance Input Error vs. Leakage Current to GND, CIN(+) to EXC = 4 pF, CIN(–) to EXC = 0 pF, V_{DD} = 2.7 V and 3 V

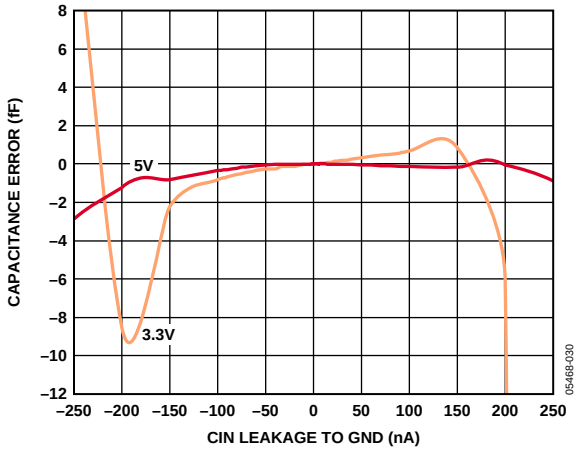


Figure 13. Capacitance Input Error vs. Leakage Current to GND, CIN(+) to EXC =4 pF, CIN(–) to EXC = 0 pF, VDD=3.3 V and 5 V

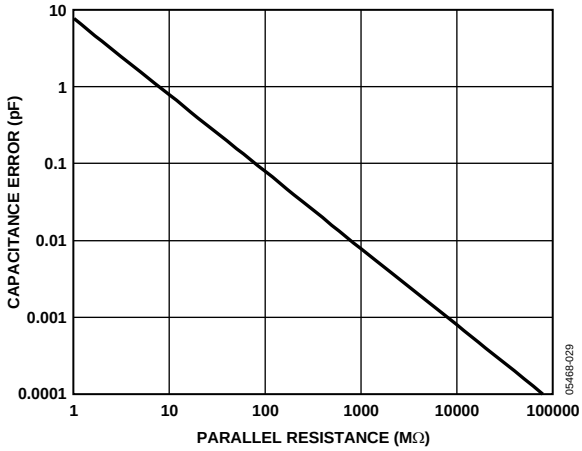


Figure 14. Capacitance Input Error vs. Resistance in Parallel with Measured Capacitance

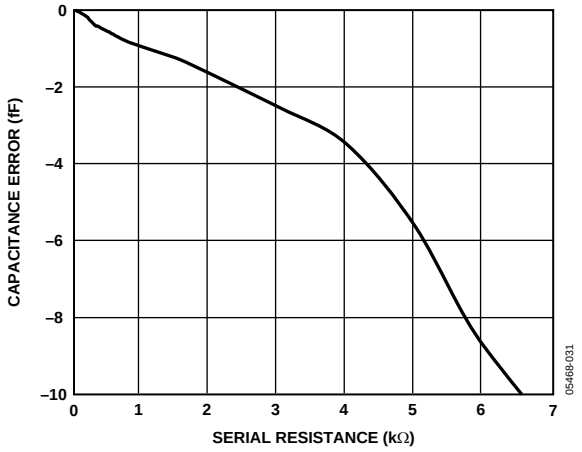


Figure 15. Capacitance Input Error vs. Serial Resistance, CIN(+) to EXC = 21 pF, CIN(–) to EXC = 23 pF, V_{DD} = 5 V, the Same Configuration as in Figure 34.

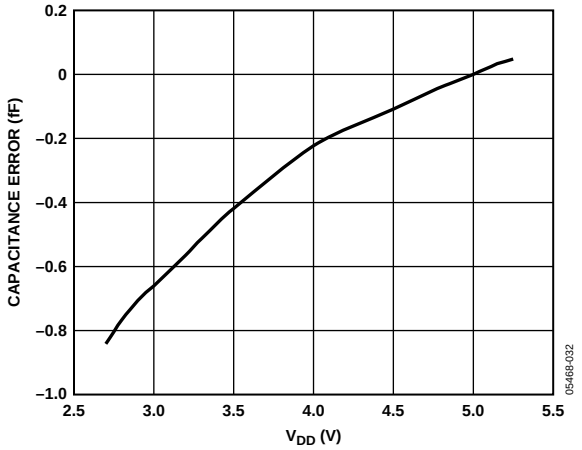


Figure 16. Capacitance Input Power Supply Rejection (PSR), CIN(+) to EXC = 4 pF, the Same Configuration as in Figure 30

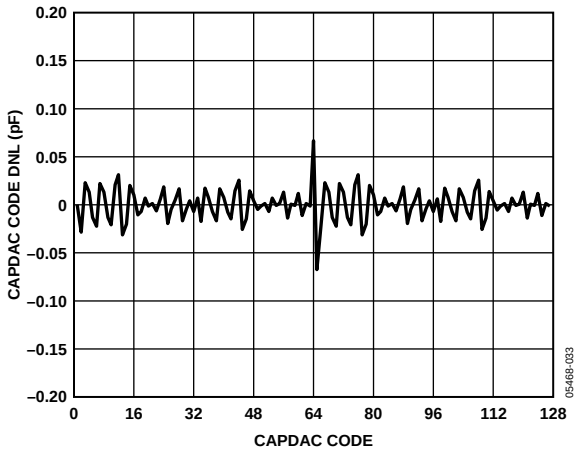


Figure 17. CAPDAC Differential Nonlinearity (DNL)

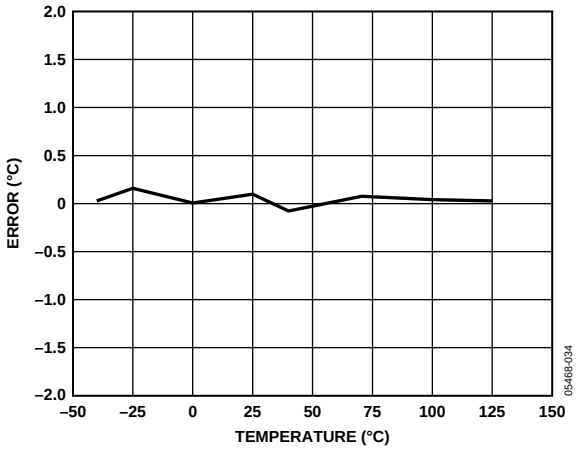


Figure 18. Internal Temperature Sensor Error vs. Temperature

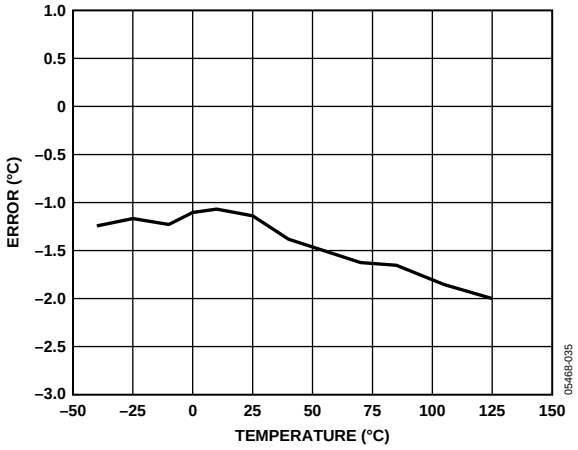


Figure 19. External Temperature Sensor Error vs. Temperature

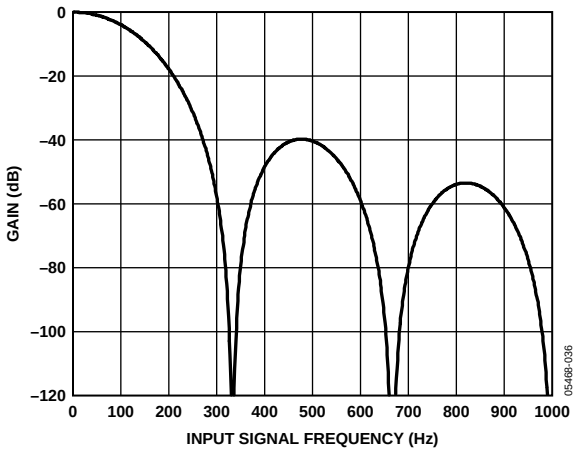


Figure 20. Capacitance Channel Frequency Response, Conversion Time = 11 ms

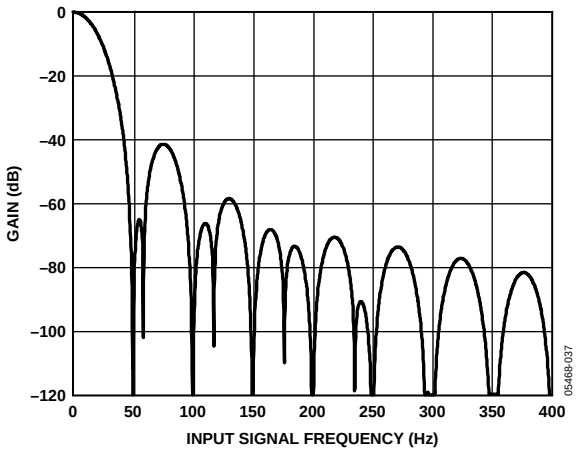


Figure 21. Capacitance Channel Frequency Response, Conversion Time = 62 ms

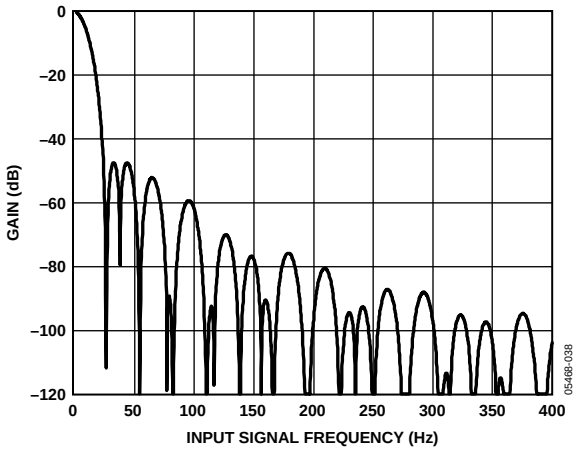


Figure 22. Capacitance Channel Frequency Response, Conversion Time = 109.6 ms

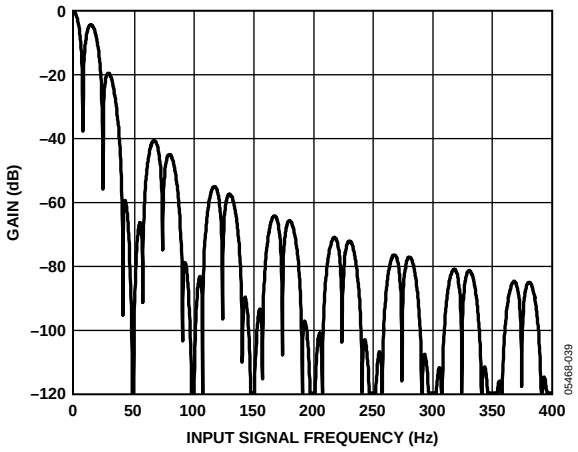


Figure 23. Voltage Channel Frequency Response, Conversion Time = 122.1 ms

OUTPUT NOISE AND RESOLUTION SPECIFICATIONS

The AD7745/AD7746 resolution is limited by noise. The noise performance varies with the selected conversion time.

Table 5 shows typical noise performance and resolution for the capacitive channel. These numbers were generated from 1000 data samples acquired in continuous conversion mode, at an excitation of 32 kHz, $\pm V_{DD}/2$, and with all CIN and EXC pins connected only to the evaluation board (no external capacitors.)

Table 6 and Table 7 show typical noise performance and resolution for the voltage channel. These numbers were generated from 1000 data samples acquired in continuous conversion mode with VIN pins shorted to ground.

RMS noise represents the standard deviation and p-p noise represents the difference between minimum and maximum results in the data. Effective resolution is calculated from rms noise, and p-p resolution is calculated from p-p noise.

Table 5. Typical Capacitive Input Noise and Resolution vs. Conversion Time

Conversion Time (ms)	Output Data Rate (Hz)	–3dB Frequency (Hz)	RMS Noise (aF/√Hz)	RMS Noise (aF)	P-P Noise (aF)	Effective Resolution (Bits)	P-P Resolution (Bits)
11.0	90.9	87.2	4.3	40.0	212.4	17.6	15.2
11.9	83.8	79.0	3.1	27.3	137.7	18.2	15.9
20.0	50.0	43.6	1.8	12.2	82.5	19.4	16.6
38.0	26.3	21.8	1.6	7.3	50.3	20.1	17.3
62.0	16.1	13.8	1.5	5.4	33.7	20.5	17.9
77.0	13.0	10.5	1.5	4.9	28.3	20.7	18.1
92.0	10.9	8.9	1.5	4.4	27.8	20.8	18.2
109.6	9.1	8.0	1.5	4.2	27.3	20.9	18.2

Table 6. Typical Voltage Input Noise and Resolution vs. Conversion Time, Internal Voltage Reference

Conversion Time (ms)	Output Data Rate (Hz)	–3dB Frequency (Hz)	RMS Noise (µV)	P-P Noise (µV)	Effective Resolution (Bits)	P-P Resolution (Bits)
20.1	49.8	26.4	11.4	62	17.6	15.2
32.1	31.2	15.9	7.1	42	18.3	15.7
62.1	16.1	8.0	4.0	28	19.1	16.3
122.1	8.2	4.0	3.0	20	19.5	16.8

Table 7. Typical Voltage Input Noise and Resolution vs. Conversion Time, External 2.5 V Voltage Reference

Conversion Time (ms)	Output Data Rate (Hz)	–3dB Frequency (Hz)	RMS Noise (µV)	P-P Noise (µV)	Effective Resolution (Bits)	P-P Resolution (Bits)
20.1	49.8	26.4	14.9	95	18.3	15.6
32.1	31.2	15.9	6.3	42	19.6	16.8
62.1	16.1	8.0	3.3	22	20.5	17.7
122.1	8.2	4.0	2.1	15	21.1	18.3

SERIAL INTERFACE

The AD7745/AD7746 supports an I²C-compatible 2-wire serial interface. The two wires on the I²C bus are called SCL (clock) and SDA (data). These two wires carry all addressing, control, and data information one bit at a time over the bus to all connected peripheral devices. The SDA wire carries the data, while the SCL wire synchronizes the sender and receiver during the data transfer. I²C devices are classified as either master or slave devices. A device that initiates a data transfer message is called a master, while a device that responds to this message is called a slave.

To control the AD7745/AD7746 device on the bus, the following protocol must be followed. First, the master initiates a data transfer by establishing a start condition, defined by a high-to-low transition on SDA while SCL remains high. This indicates that the start byte follows. This 8-bit start byte is made up of a 7-bit address plus an R/W bit indicator.

All peripherals connected to the bus respond to the start condition and shift in the next 8 bits (7-bit address + R/W bit). The bits arrive MSB first. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as the acknowledge bit. All other devices withdraw from the bus at this point and maintain an idle condition. An exception to this is the general call address, which is described later in this document. The idle condition is where the device monitors the SDA and SCL lines waiting for the start condition and the correct address byte. The R/W bit determines the direction of the data transfer. A Logic 0 LSB in the start byte means that the master writes information to the addressed peripheral. In this case the AD7745/AD7746 becomes a slave receiver. A Logic 1 LSB in the start byte means that the master reads information from the addressed peripheral. In this case, the AD7745/AD7746 becomes a slave transmitter. In all instances, the AD7745/AD7746 acts as a standard slave device on the I²C bus.

The start byte address for the AD7745/AD7746 is 0x90 for a write and 0x91 for a read.

READ OPERATION

When a read is selected in the start byte, the register that is currently addressed by the address pointer is transmitted on to the SDA line by the AD7745/AD7746. This is then clocked out by the master device and the AD7745/AD7746 awaits an acknowledge from the master.

If an acknowledge is received from the master, the address auto-incrementer automatically increments the address pointer register and outputs the next addressed register content on to the SDA line for transmission to the master. If no acknowledge is received, the AD7745/AD7746 return to the idle state and the address pointer is not incremented.

The address pointers' auto-incrementer allow block data to be written or read from the starting address and subsequent incremental addresses.

In continuous conversion mode, the address pointers' auto-incrementer should be used for reading a conversion result. That means, the three data bytes should be read using one multibyte read transaction rather than three separate single byte transactions. The single byte data read transaction may result in the data bytes from two different results being mixed. The same applies for six data bytes if both the capacitive and the voltage/temperature channel are enabled.

The user can also access any unique register (address) on a one-to-one basis without having to update all the registers. The address pointer register contents cannot be read.

If an incorrect address pointer location is accessed or, if the user allows the auto-incrementer to exceed the required register address, the following applies:

- In read mode, the AD7745/AD7746 continues to output various internal register contents until the master device issues a no acknowledge, start, or stop condition. The address pointers' auto-incrementer's contents are reset to point to the status register at Address 0x00 when a stop condition is received at the end of a read operation. This allows the status register to be read (polled) continually without having to constantly write to the address pointer.
- In write mode, the data for the invalid address is not loaded into the AD7745/AD7746 registers but an acknowledge is issued by the AD7745/AD7746.

WRITE OPERATION

When a write is selected, the byte following the start byte is always the register address pointer (subaddress) byte, which points to one of the internal registers on the AD7745/ AD7746. The address pointer byte is automatically loaded into the address pointer register and acknowledged by the AD7745/ AD7746. After the address pointer byte acknowledge, a stop condition, a repeated start condition, or another data byte can follow from the master.

A stop condition is defined by a low-to-high transition on SDA while SCL remains high. If a stop condition is ever encountered by the AD7745/AD7746, it returns to its idle condition and the address pointer is reset to Address 0x00.

If a data byte is transmitted after the register address pointer byte, the AD7745/AD7746 load this byte into the register that is currently addressed by the address pointer register, send an acknowledge, and the address pointer auto-incrementer automatically increments the address pointer register to the next internal register address. Thus, subsequent transmitted data bytes are loaded into sequentially incremented addresses.

If a repeated start condition is encountered after the address pointer byte, all peripherals connected to the bus respond exactly as outlined above for a start condition, that is, a repeated start condition is treated the same as a start condition. When a master device issues a stop condition, it relinquishes control of the bus, allowing another master device to take control of the bus. Hence, a master wanting to retain control of the bus issues successive start conditions known as repeated start conditions.

AD7745/AD7746 RESET

To reset the AD7745/AD7746 without having to reset the entire I²C bus, an explicit reset command is provided. This uses a particular address pointer word as a command word to reset the part and upload all default settings. The AD7745/AD7746 do not respond to the I²C bus commands (do not acknowledge) during the default values upload for approximately 150 µs (max 200 µs).

The reset command address word is 0xBF.

GENERAL CALL

When a master issues a slave address consisting of seven 0s with the eighth bit (R/W bit) set to 0, this is known as the general call address. The general call address is for addressing every device connected to the I²C bus. The AD7745/AD7746 acknowledge this address and read in the following data byte.

If the second byte is 0x06, the AD7745/AD7746 are reset, completely uploading all default values. The AD7745/AD7746 do not respond to the I²C bus commands (do not acknowledge) during the default values upload for approximately 150 µs (max 200 µs).

The AD7745/AD7746 do not acknowledge any other general call commands.

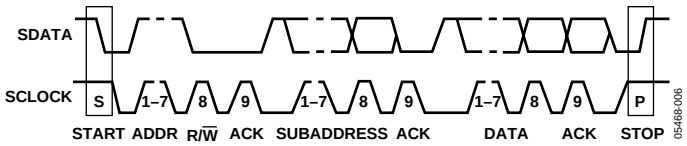


Figure 24. Bus Data Transfer

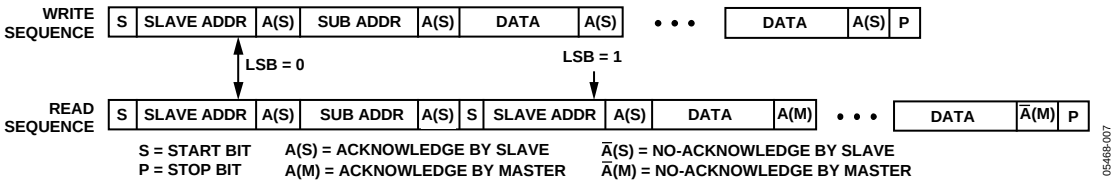


Figure 25. Write and Read Sequences

REGISTER DESCRIPTIONS

The master can write to or read from all of the AD7745/AD7746 registers except the address pointer register, which is a write-only register. The address pointer register determines which register the next read or write operation accesses. All communications with the part through the bus start with an access to the address pointer register. After the part has been accessed over the bus and a read/write operation is selected, the address pointer register is set up. The address pointer register determines from or to which register the operation takes place. A read/write operation is performed from/to the target address, which then increments to the next address until a stop command on the bus is performed.

Table 8. Register Summary

	Address Pointer			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Register	**(Dec)**	**(Hex)**	**Dir**	**Default Value**							
Status	0	0x00	R	-	-	-	-	EXCERR	RDY	RDYVT	RDYCAP
				0	0	0	0	0	1	1	1
Cap Data H	1	0x01	R	Capacitive channel data—high byte, 0x00							
Cap Data M	2	0x02	R	Capacitive channel data—middle byte, 0x00							
Cap Data L	3	0x03	R	Capacitive channel data—low byte, 0x00							
VT Data H	4	0x04	R	Voltage/temperature channel data—high byte, 0x00							
VT Data M	5	0x05	R	Voltage/temperature channel data—middle byte, 0x00							
VT Data L	6	0x06	R	Voltage/temperature channel data—low byte, 0x00							
Cap Setup	7	0x07	R/W	CAPEN	CIN2[1]	CAPDIFF	-	-	-	-	CAPCHOP
				0	0	0	0	0	0	0	0
VT Setup	8	0x08	R/W	VTEN	VTMD1	VTMD0	EXTREF	-	-	VTSHORT	VTCHOP
				0	0	0	0	0	0	0	0
EXC Setup	9	0x09	R/W	CLKCTRL	EXCON	EXCB	$\overline{\text{EXCB}}$	EXCA	$\overline{\text{EXCA}}$	EXCLVL1	EXCLVL0
				0	0	0	0	0	0	1	1
Configuration	10	0x0A	R/W	VTFS1	VTFS0	CAPFS2	CAPFS1	CAPFS0	MD2	MD1	MD0
				1	0	1	0	0	0	0	0
Cap DAC A	11	0x0B	R/W	DACAENA	DACA—7-Bit Value						
				0	0x00						
Cap DAC B	12	0x0C	R/W	DACBENB	DACB—7-Bit Value						
				0	0x00						
Cap Offset H	13	0x0D	R/W	Capacitive offset calibration—high byte, 0x80							
Cap Offset L	14	0x0E	R/W	Capacitive offset calibration—low byte, 0x00							
Cap Gain H	15	0x0F	R/W	Capacitive gain calibration—high byte, factory calibrated							
Cap Gain L	16	0x10	R/W	Capacitive gain calibration—low byte, factory calibrated							
Volt Gain H	17	0x11	R/W	Voltage gain calibration—high byte, factory calibrated							
Volt Gain L	18	0x12	R/W	Voltage gain calibration—low byte, factory calibrated							

[1] The CIN2 bit is relevant only for AD7746. The CIN2 bit should always be 0 on the AD7745.

STATUS REGISTER

Address Pointer 0x00, Read Only, Default Value 0x07

This register indicates the status of the converter. The status register can be read via the 2-wire serial interface to query a finished conversion.

The $\overline{RDY}$ pin reflects the status of the RDY bit. Therefore, the $\overline{RDY}$ pin high-to-low transition can be used as an alternative indication of the finished conversion.

Table 9. Status Register Bit Map

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	-	-	-	-	EXCERR	RDY	RDYVT	RDYCAP
Default	0	0	0	0	0	1	1	1

Table 10.

Bit	Mnemonic	Description
7-4	-	Not used, always read 0.
3	EXCERR	EXCERR = 1 indicates that the excitation output cannot be driven properly. The possible reason can be a short circuit or too high capacitance between the excitation pin and ground.
2	RDY	RDY = 0 indicates that conversion on the enabled channel(s) has been finished and new unread data is available. If both capacitive and voltage/temperature channels are enabled, the RDY bit is changed to 0 after conversion on both channels is finished. The RDY bit returns to 1 either when data is read or prior to finishing the next conversion. If, for example, only the capacitive channel is enabled, then the RDY bit reflects the RDYCAP bit.
1	RDYVT	RDYVT = 0 indicates that a conversion on the voltage/temperature channel has been finished and new unread data is available.
0	RDYCAP	RDYCAP = 0 indicates that a conversion on the capacitive channel has been finished and new unread data is available.

CAP DATA REGISTER

24 Bits, Address Pointer 0x01, 0x02, 0x03, Read-Only, Default Value 0x000000

Capacitive channel output data. The register is updated after finished conversion on the capacitive channel, with one exception: When the serial interface read operation from the CAP DATA register is in progress, the data register is not updated and the new capacitance conversion result is lost.

The stop condition on the serial interface is considered to be the end of the read operation. Therefore, to prevent data corruption, all three bytes of the data register should be read sequentially using the register address pointer auto-increment feature of the serial interface.

To prevent losing some of the results, the CAP DATA register should be read before the next conversion on the capacitive channel is finished.

The 0x000000 code represents negative full scale (–4.096 pF), the 0x800000 code represents zero scale (0 pF), and the 0xFFFFFF code represents positive full scale (+4.096 pF).

VT DATA REGISTER

24 Bits, Address Pointer 0x04, 0x05, 0x06, Read-Only, Default Value 0x000000

Voltage/temperature channel output data. The register is updated after finished conversion on the voltage channel or temperature channel, with one exception: When the serial interface read operation from the VT DATA register is in progress, the data register is not updated and the new voltage/temperature conversion result is lost.

The stop condition on the serial interface is considered to be the end of the read operation. Therefore, to prevent data corruption, all three bytes of the data register should be read sequentially using the register address pointer auto-increment feature of the serial interface.

For voltage input, Code 0 represents negative full scale ($-V_{REF}$), the 0x800000 code represents zero scale (0 V), and the 0xFFFFFF code represents positive full scale ($+V_{REF}$).

To prevent losing some of the results, the VT DATA register should be read before the next conversion on the voltage/temperature channel is finished.

For the temperature sensor, the temperature can be calculated from code using the following equation:

$$Temperature\ (°C) = (Code/2048) - 4096$$

CAP SET-UP REGISTER

Address Pointer 0x07, Default Value 0x00

Capacitive channel setup.

Table 11. CAP Set-Up Register Bit Map

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	CAPEN	CIN2	CAPDIFF	-	-	-	-	CAPCHOP
Default	0	0	0	0	0	0	0	0

Table 12.

Bit	Mnemonic	Description
7	CAPEN	CAPEN = 1 enables capacitive channel for single conversion, continuous conversion, or calibration.
6	CIN2	CIN2 = 1 switches the internal multiplexer to the second capacitive input on the AD7746.
5	CAPDIFF	DIFF = 1 sets differential mode on the selected capacitive input.
4-1	-	These bits must be 0 for proper operation.
0	CAPCHOP	The CAPCHOP bit should be set to 0 for the specified capacitive channel performance. CAPCHOP = 1 approximately doubles the capacitive channel conversion times and slightly improves the capacitive channel noise performance for the longest conversion times.

VT SET-UP REGISTER

Address Pointer 0x08, Default Value 0x00

Voltage/Temperature channel setup.

Table 13. VT Set-Up Register Bit Map

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	VTEN	VTMD1	VTMD0	EXTREF	-	-	VTSHORT	VTCHOP
Default	0	0	0	0	0	0	0	0

Table 14.

Bit	Mnemonic	Description		
7	VTEN	VTEN = 1 enables voltage/temperature channel for single conversion, continuous conversion, or calibration.		
6 5	VTMD1 VTMD0	Voltage/temperature channel input configuration.		
		VTMD1	**VTMD0**	**Channel Input**
		0	0	Internal temperature sensor
		0	1	External temperature sensor diode
		1	0	V_{DD} monitor
		1	1	External voltage input (VIN)
4	EXTREF	EXTREF = 1 selects an external reference voltage connected to REFIN(+), REFIN(–) for the voltage input or the V_{DD} monitor. EXTREF = 0 selects the on-chip internal reference. The internal reference must be used with the internal temperature sensor for proper operation.		
3-2	-	These bits must be 0 for proper operation.		
1	VTSHORT	VTSHORT = 1 internally shorts the voltage/temperature channel input for test purposes.		
0	VTCHOP = 1	VTCHOP = 1 sets internal chopping on the voltage/temperature channel. The VTCHOP bit must be set to 1 for the specified voltage/temperature channel performance.		

EXC SET-UP REGISTER

Address Pointer 0x09, Default Value 0x03

Capacitive channel excitation setup.

Table 15. EXC Set-Up Bit Map

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	CLKCTRL	EXCON	EXCB	$\overline{\text{EXCB}}$	EXCA	$\overline{\text{EXCA}}$	EXCLVL1	EXCLVL0
Default	0	0	0	0	0	0	0	0

Table 16.

Bit	Mnemonic	Description
7	CLKCTRL	The CLKCTRL bit should be set to 0 for the specified AD7745/AD7746 performance. CLKCTRL = 1 decreases the excitation signal frequency and the modulator clock frequency by factor of 2. This also increases the conversion time on all channels (capacitive, voltage, and temperature) by a factor of 2.
6	EXCON	When EXCON = 0, the excitation signal is present on the output only during capacitance channel conversion. When EXCON = 1, the excitation signal is present on the output during both capacitance and voltage/temperature conversion.
5	EXCB	EXCB = 1 enables EXCB pin as the excitation output.
4	$\overline{\text{EXCB}}$	$\overline{\text{EXCB}}$ = 1 enables EXCB pin as the inverted excitation output. Only one of the EXCB or the $\overline{\text{EXCB}}$ bits should be set for proper operation.
3	EXCA	EXCA = 1 enables EXCA pin as the excitation output.
2	$\overline{\text{EXCA}}$	$\overline{\text{EXCA}}$ = 1 enables EXCA pin as the inverted excitation output. Only one of the EXCA or the $\overline{\text{EXCA}}$ bits should be set for proper operation.
1 0	EXCLVL1, EXCLVL0	Excitation Voltage Level.

EXCLVL1	EXCLVL0	Voltage on Cap	EXC Pin Low Level	EXC Pin High Level
0	0	$\pm V_{DD}/8$	$V_{DD} \times 3/8$	$V_{DD} \times 5/8$
0	1	$\pm V_{DD}/4$	$V_{DD} \times 1/4$	$V_{DD} \times 3/4$
1	0	$\pm V_{DD} \times 3/8$	$V_{DD} \times 1/8$	$V_{DD} \times 7/8$
1	1	$\pm V_{DD}/2$	0	V_{DD}

CONFIGURATION REGISTER

Address Pointer 0x0A, Default Value 0xA0

Converter update rate and mode of operation setup.

Table 17. Configuration Register Bit Map

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	VTF1	VTF0	CAPF2	CAPF1	CAPF0	MD2	MD1	MD0
Default	0	0	0	0	0	0	0	0

Table 18.

Bit	Mnemonic	Description
7 6	VTF1 VTF0	Voltage/temperature channel digital filter setup—conversion time/update rate setup. The conversion times in this table are valid for the CLKCTRL = 0 in the EXC SETUP register. The conversion times are longer by a factor of two for the CLKCTRL = 1.

		VTCHOP = 1		
VTF1	**VTF0**	**Conversion Time (ms)**	**Update Rate (Hz)**	**–3 dB Frequency (Hz)**
0	0	20.1	49.8	26.4
0	1	32.1	31.2	15.9
1	0	62.1	16.1	8.0
1	1	122.1	8.2	4.0

5 4 3	CAPF2 CAPF1 CAPF0	Capacitive channel digital filter setup—conversion time/update rate setup. The conversion times in this table are valid for the CLKCTRL = 0 in the EXC SETUP register. The conversion times are longer by factor of two for the CLKCTRL = 1.

			CAP CHOP = 0		
CAPF2	**CAPF1**	**CAPF0**	**Conversion Time (ms)**	**Update Rate**	**–3 dB Frequency (Hz)**
0	0	0	11.0	90.9	87.2
0	0	1	11.9	83.8	79.0
0	1	0	20.0	50.0	43.6
0	1	1	38.0	26.3	21.8
1	0	0	62.0	16.1	13.1
1	0	1	77.0	13.0	10.5
1	1	0	92.0	10.9	8.9
1	1	1	109.6	9.1	8.0

2 1 0	MD2 MD1 MD0	Converter mode of operation setup.

MD2	**MD1**	**MD0**	**Mode**
0	0	0	Idle
0	0	1	Continuous conversion
0	1	0	Single conversion
0	1	1	Power-Down
1	0	0	-
1	0	1	Capacitance system offset calibration
1	1	0	Capacitance or voltage system gain calibration
1	1	1	

CAP DAC A REGISTER

Address Pointer 0x0B, Default Value 0x00

Capacitive DAC setup.

Table 19. Cap DAC A Register Bit Map

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	DACAENA	DACA—7-Bit Value						
Default	0	0x00						

Table 20.

Bit	Mnemonic	Description
7	DACAENA	DACAENA = 1 connects capacitive DACA to the positive capacitance input.
6-1	DACA	DACA value, Code 0x00 ≈ 0 pF, Code 0x7F ≈ full range.

CAP DAC B REGISTER

Address Pointer 0x0C, Default Value 0x00

Capacitive DAC setup.

Table 21. Cap DAC B Register Bit Map

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	DACBENB	DACB—7-bit value						
Default	0	0x00						

Table 22.

Bit	Mnemonic	Description
7	DACBENB	DACBENB = 1 connects capacitive DACB to the negative capacitance input.
6-1	DACB	DACB value, Code 0x00 ≈ 0 pF, Code 0x7F ≈ full range.

CAP OFFSET CALIBRATION REGISTER

16 Bits, Address Pointer 0x0D, 0x0E, Default Value 0x8000

The capacitive offset calibration register holds the capacitive channel zero-scale calibration coefficient. The coefficient is used to digitally remove the capacitive channel offset. The register value is updated automatically following the execution of a capacitance offset calibration. The capacitive offset calibration resolution (cap offset register LSB) is less than 32 aF; the full range is 1 pF.

On the AD7746, the register is shared by the two capacitive channels. If the capacitive channels need to be offset-calibrated individually, the host controller software should read the AD7746 capacitive offset calibration register values after performing the offset calibration on individual channels and then reload the values back to the AD7746 before executing conversion on a different channel.

CAP GAIN CALIBRATION REGISTER

16 Bits, Address Pointer 0x0F, 0x10, Default Value 0xXXXX

Capacitive gain calibration register. The register holds the capacitive channel full-scale factory calibration coefficient. On the AD7746, the register is shared by the two capacitive channels.

VOLT GAIN CALIBRATION REGISTER

16 Bits, Address Pointer 0x11,0x12, Default Value 0xXXXX

Voltage gain calibration register. The register holds the voltage channel full-scale factory calibration coefficient.

CIRCUIT DESCRIPTION

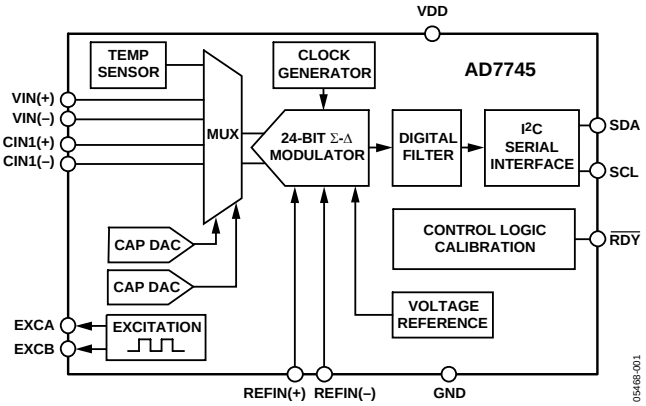


Figure 26. AD7745 Block Diagram

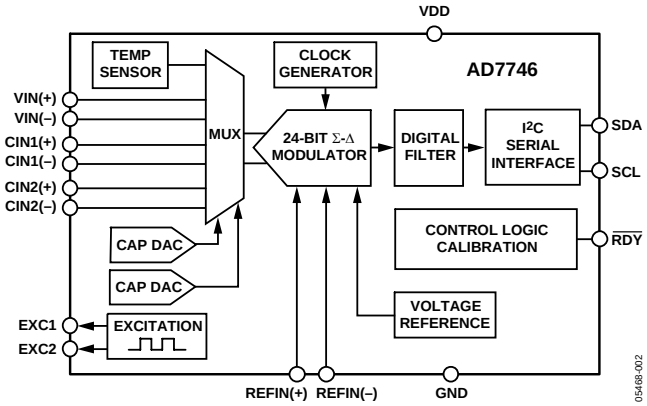


Figure 27. AD7746 Block Diagram

OVERVIEW

The AD7745/AD7746 core is a high precision converter consisting of a second order (Σ-Δ or charge balancing) modulator and a third order digital filter. It works as a CDC for the capacitive inputs and as a classic ADC for the voltage input or for the voltage from a temperature sensor.

In addition to the converter, the AD7745/AD7746 integrates a multiplexer, an excitation source and CAPDACs for the capacitive inputs, a temperature sensor, a voltage reference for the voltage and temperature inputs, a complete clock generator, a control and calibration logic, and an I²C-compatible serial interface.

The AD7745 has one capacitive input, while the AD7746 has two capacitive inputs. All other features and specifications are identical for both parts.

CAPACITANCE-TO-DIGITAL CONVERTER

Figure 28 shows the CDC simplified functional diagram. The measured capacitance C_X is connected between the excitation source and the Σ-Δ modulator input. A square-wave excitation signal is applied on the C_X during the conversion and the modulator continuously samples the charge going through the C_X. The digital filter processes the modulator output, which is a stream of 0s and 1s containing the information in 0 and 1 density. The data from the digital filter is scaled, applying the calibration coefficients, and the final result can be read through the serial interface.

The AD7745/AD7746 is designed for floating capacitive sensors. Therefore, both C_X plates have to be isolated from ground.

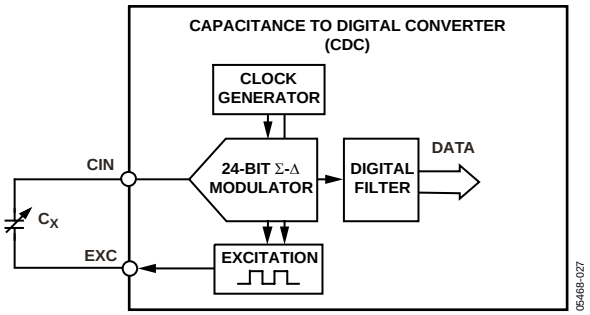


Figure 28. CDC Simplified Block Diagram

EXCITATION SOURCE

The two excitation pins EXCA and EXCB are independently programmable. They are identically functional and therefore either of them can be used for the capacitive sensor excitation.

On the 2-channel AD7746 using a separate excitation pin for each capacitive channel is recommended.

CAPDAC

The AD7745/AD7746 CDC full-scale input range is ±4.096 pF. For simplicity of calculation, however, the following text and diagrams use ±4 pF. The part can accept a higher capacitance on the input and the common-mode or offset (not-changing component) capacitance can be balanced by programmable on-chip CAPDACs.

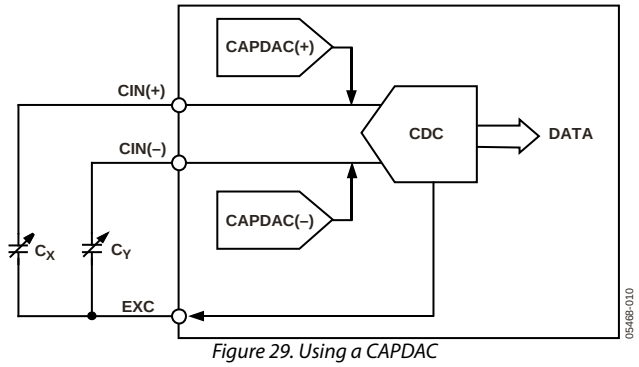


Figure 29. Using a CAPDAC

The CAPDAC can be understood as a negative capacitance connected internally to the CIN pin. There are two independent CAPDACs, one connected to the CIN(+) and the second connected to the CIN(–). The relation between the capacitance input and output data can be expressed as

$$DATA \approx (C_X - CAPDAC(+)) - (C_Y - CAPDAC(-))$$

The CAPDACs have a 7-bit resolution, monotonic transfer function, are well matched to each other, and have a defined temperature coefficient. The CAPDAC full range (absolute value) is not factory calibrated and can vary up to ±20% with the manufacturing process. See the Specifications section and typical performance characteristics in Figure 17.

The CAPDACs are shared by the two capacitive channels on the AD7746. If the CAPDACs need to be set individually, the host controller software should reload the CAPDAC values to the AD7746 before executing conversion on a different channel.

SINGLE-ENDED CAPACITIVE INPUT

When configured for a single-ended mode (the CAPDIFF bit in the Cap Setup register is set to 0), the AD7745/AD7746 CIN(–) pin is disconnected internally. The CDC (without using the CAPDACs) can measure only positive input capacitance in the range of 0 pF to 4 pF (see Figure 30).

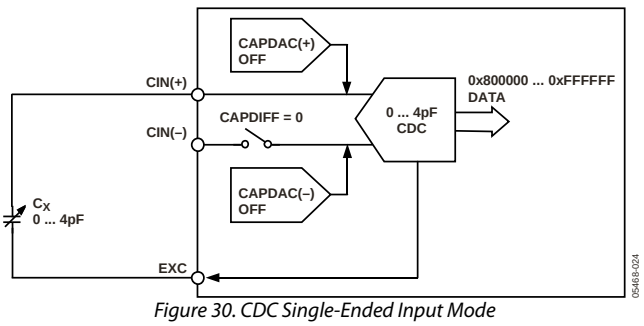


Figure 30. CDC Single-Ended Input Mode

The CAPDAC can be used for programmable shifting the input range. The example in Figure 31 shows how to use the full ±4 pF CDC span to measure capacitance between 0 pF to 8 pF.

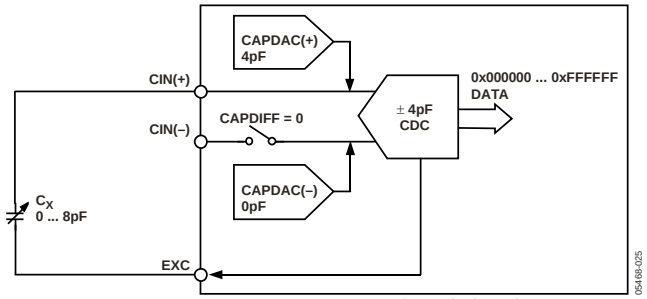


Figure 31. Using CAPDAC in Single-Ended Mode

Figure 32 shows how to shift the input range further, up to 21 pF absolute value of capacitance connected to the CIN(+).

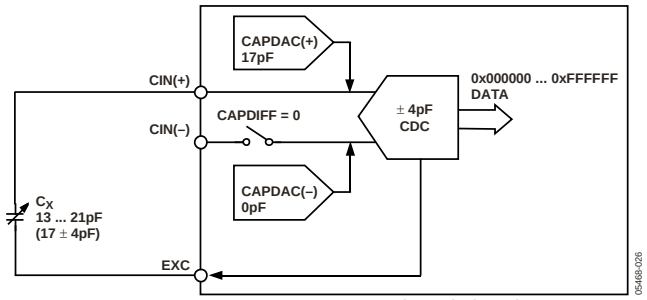


Figure 32. Using CAPDAC in Single-Ended Mode

DIFFERENTIAL CAPACITIVE INPUT

When configured for a differential mode (the CAPDIFF bit in the Cap Setup register set to 1), the AD7745/AD7746 CDC measures the difference between positive and negative capacitance input.

Each of the two input capacitances C_X and C_Y between the EXC and CIN pins must be less than 4 pF (without using the CAPDACs) or must be less than 21 pF and balanced by the CAPDACs. Balancing by the CAPDACs means that both C_X–CAPDAC(+) and C_Y–CAPDAC(–) are less than 4 pF.

If the unbalanced capacitance between the EXC and CIN pins is higher than 4 pF, the CDC introduces a gain error, an offset error, and nonlinearity error.

See the examples shown in Figure 33, Figure 34, and Figure 35.

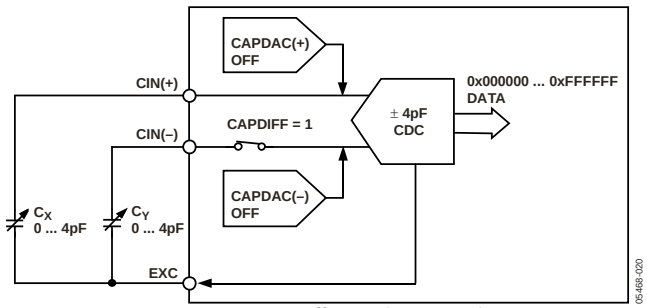


Figure 33. CDC Differential Input Mode

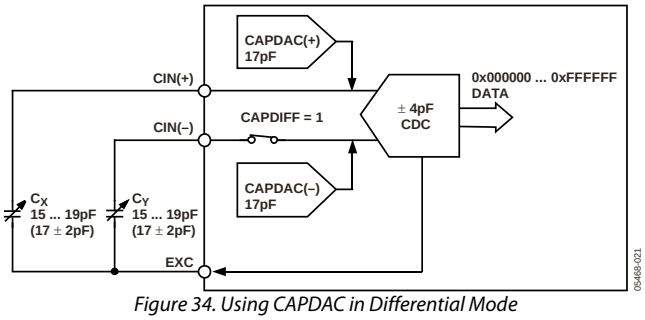


Figure 34. Using CAPDAC in Differential Mode

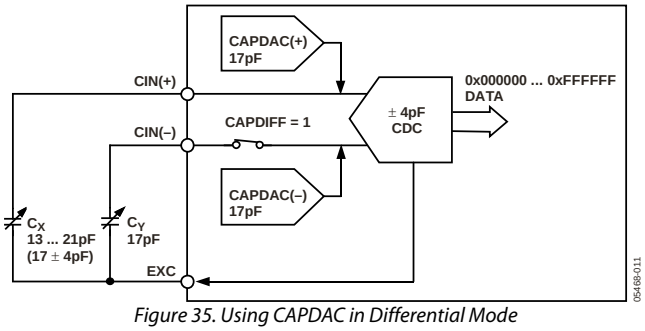


Figure 35. Using CAPDAC in Differential Mode

PARASITIC CAPACITANCE TO GROUND

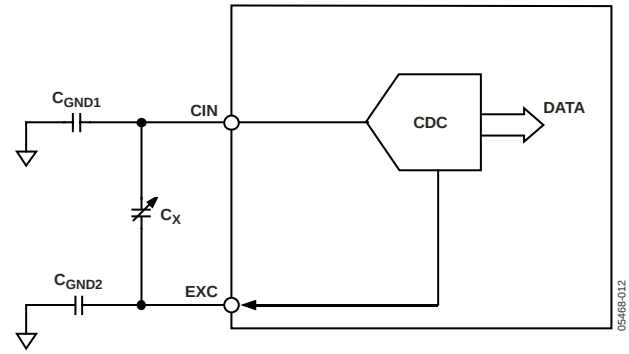


Figure 36. Parasitic Capacitance to Ground

The CDC architecture used in the AD7745/AD7746 measures the capacitance C_X connected between the EXC pin and the CIN pin. In theory, any capacitance C_P to ground should not affect the CDC result (see Figure 36).

The practical implementation of the circuitry in the chip implies certain limits and the result is gradually affected by capacitance to ground. See the allowed capacitance to GND in the specification table for CIN and excitation. Also see the typical performance characteristics shown in Figure 9, Figure 10, and Figure 11.

PARASITIC RESISTANCE TO GROUND

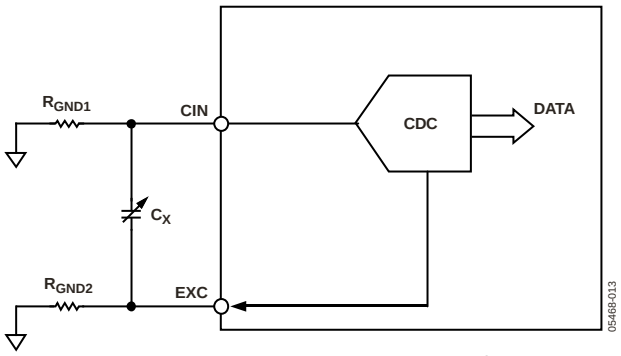


Figure 37. Parasitic Resistance to Ground

The AD7745/AD7746 CDC result would be affected by a leakage current from the C_X to ground, therefore the C_X should be isolated from the ground. The influence of the leakage current varies with the power supply voltage. The following limits can be used as a guideline for the allowed leakage current or the equivalent resistance between the C_X and ground (Figure 37).

$V_{DD} \approx 5$ V: $I_{GND} < 150$ nA (that is, $R_{GND} > 30$ MΩ)

$V_{DD} \geq 3$ V: $I_{GND} < 60$ nA (that is, $R_{GND} > 50$ MΩ)

$V_{DD} \geq 2.7$ V: $I_{GND} < 30$ nA (that is, $R_{GND} > 100$ MΩ)

A higher leakage current to ground results in a gain error, an offset error, and a nonlinearity error. See the typical performance characteristics shown in Figure 12 and Figure 13.

PARASITIC PARALLEL RESISTANCE

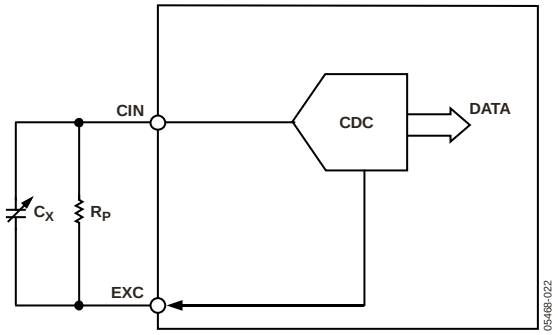


Figure 38. Parasitic Parallel Resistance

The AD7745/AD7746 CDC measures the charge transfer between EXC pin and CIN pin. Any resistance connected in parallel to the measured capacitance CX (see Figure 38), such as the parasitic resistance of the sensor, also transfers charge. Therefore, the parallel resistor is seen as an additional capacitance in the output data. The equivalent parallel capacitance (or error caused by the parallel resistance) can be approximately calculated as

$$C_P = \frac{1}{R_P \times F_{EXC} \times 4}$$

Where R_P is the parallel resistance and C_{EXC} is the excitation frequency. See the typical performance characteristics shown in Figure 14.

PARASITIC SERIAL RESISTANCE

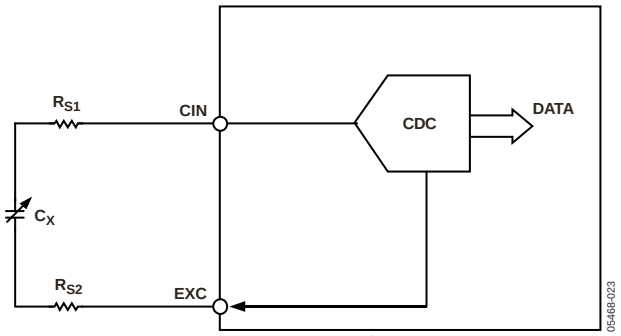


Figure 39. Parasitic Serial Resistance

The AD7745/AD7746 CDC result is affected by a resistance in series with the measured capacitance. The total serial resistance, which refers to R_{S1} + R_{S2} on Figure 39, should be less than 1 kΩ for the specified performance. See typical performance characteristics shown in Figure 15.

CAPACITIVE GAIN CALIBRATION

The AD7745/AD7746 gain is factory calibrated for the full scale of ±4.096 pF in the production for each part individually. The factory gain coefficient is stored in a one-time programmable (OTP) memory and is copied to the capacitive gain register at power-up or after reset.

The gain can be changed by executing a capacitance gain calibration mode, for which an external full-scale capacitance needs to be connected to the capacitance input, or by writing a user value to the capacitive gain register. This change would be only temporary and the factory gain coefficient would be reloaded back after power-up or reset. The part is tested and specified only for use with the default factory calibration coefficient.

CAPACITIVE SYSTEM OFFSET CALIBRATION

The capacitive offset is dominated by the parasitic offset in the application, such as the initial capacitance of the sensor, any parasitic capacitance of tracks on the board, and the capacitance of any other connections between the sensor and the CDC. Therefore, the AD7745/AD7746 are not factory calibrated for capacitive offset. It is the user's responsibility to calibrate the system capacitance offset in the application.

Any offset in the capacitance input larger than ±1 pF should first be removed using the on-chip CAPDACs. The small offset within ±1 pF can then be removed by using the capacitance offset calibration register.

One method of adjusting the offset is to connect a zero-scale capacitance to the input and execute the capacitance offset calibration mode. The calibration sets the midpoint of the ±4.096 pF range (that is, Output Code 0x800000) to that zero-scale input.

Another method would be to calculate and write the offset calibration register value, the LSB is value 31.25 aF (4.096 pF/2^{17}).

The offset calibration register is reloaded by the default value at power-on or after reset. Therefore, if the offset calibration is not repeated after each system power-up, the calibration coefficient value should be stored by the host controller and reloaded as part of the AD7745/AD7746 setup.

On the AD7746, the register is shared by the two capacitive channels. If the capacitive channels need to be offset calibrated individually, the host controller software should read the AD7746 capacitive offset calibration register values after performing the offset calibration on individual channels and then reload the values back to the AD7746 before executing a conversion on a different channel.

INTERNAL TEMPERATURE SENSOR

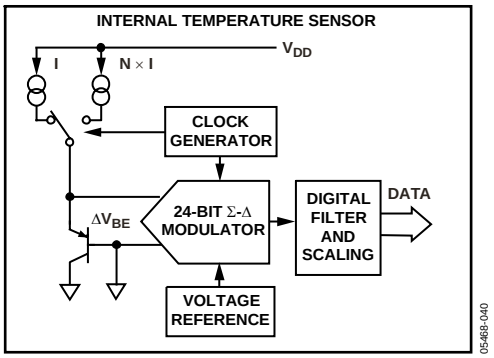


Figure 40. Internal Temperature Sensor

The temperature sensing method used in the AD7745/AD7746 is to measure a difference in ΔV_{BE} voltage of a transistor operated at two different currents (see Figure 40). The ΔV_{BE} change with temperature is linear and can be expressed as

$$\Delta V_{BE} = (n_f)\frac{KT}{q} \times \ln(N)$$

where:

K is Boltzmann's constant (1.38×10^{-23}).

T is the absolute temperature in Kelvin.

q is the charge on the electron (1.6×10^{-19} coulombs).

N is the ratio of the two currents.

n_f is the ideality factor of the thermal diode.

The AD7745/AD7746 uses an on-chip transistor to measure the temperature of the silicon chip inside the package. The Σ-Δ ADC converts the ΔV_{BE} to digital, the data are scaled using factory calibration coefficients, thus the output code is proportional to temperature:

$$Temperature(°C) = \frac{Code}{2048} - 4096$$

The AD7745/AD7746 has a low power consumption resulting in only a small effect due to the part self-heating (less than 0.5°C at V_{DD} = 5 V).

If the capacitive sensor can be considered to be at the same temperature as the AD7745/AD7746 chip, the internal temperature sensor can be used as a system temperature sensor. That means the complete system temperature drift compensation can be based on the AD7745/AD7746 internal temperature sensor without need for any additional external components. See the typical performance characteristics in Figure 18.

EXTERNAL TEMPERATURE SENSOR

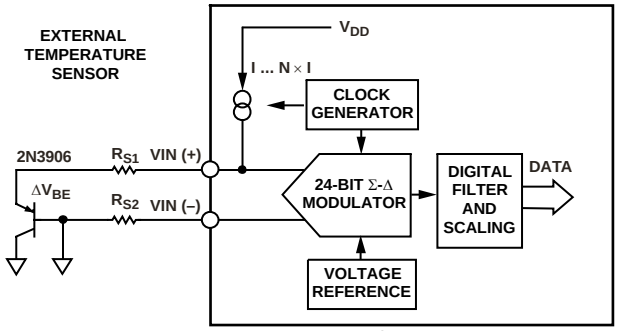


Figure 41. Transistor as an External Temperature Sensor

The AD7745/AD7746 provide the option of using an external transistor as a temperature sensor in the system. The ΔV_{BE} method, which is similar to the internal temperature sensor method, is used. However, it is modified to compensate for the serial resistance of connections to the sensor. Total serial resistance (R_{S1} + R_{S2} in Figure 41) up to 100 Ω is compensated. The VIN(–) pin must be grounded for proper external temperature sensor operation.

The AD7745/AD7746 are factory calibrated for Transistor 2N3906 with the ideality factor n_f = 1.008. See the typical performance characteristics shown in Figure 19.

VOLTAGE INPUT

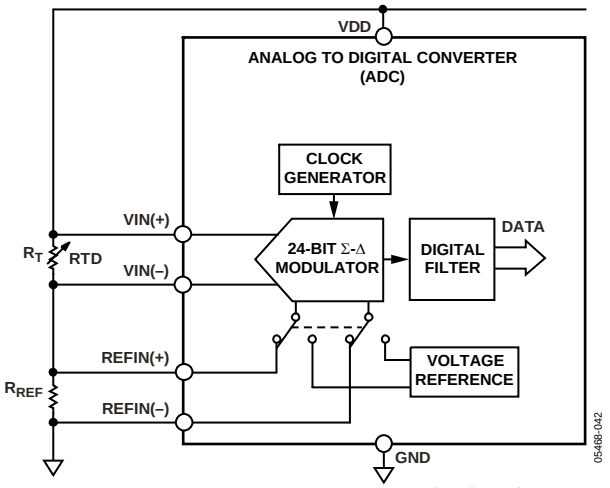


Figure 42. Resistive Temperature Sensor Connected to the Voltage Input

The AD7745/AD7746 Σ-Δ core can work as a high resolution (up to 21 ENOB) classic ADC with a fully differential voltage input. The ADC can be used either with the on-chip high precision, low drift, 1.17 V voltage reference, or an external reference connected to the fully differential reference input pins.

The voltage and reference inputs are continuously sampled by a Σ-Δ modulator during the conversion. Therefore, the input source impedance should be kept low. See the application example in Figure 42.

V_{DD} MONITOR

Along with converting external voltages, the AD7745/AD7746 Σ-Δ ADC can be used for monitoring the V_{DD} voltage. The voltage from the VDD pin is internally attenuated by 6.

TYPICAL APPLICATION DIAGRAM

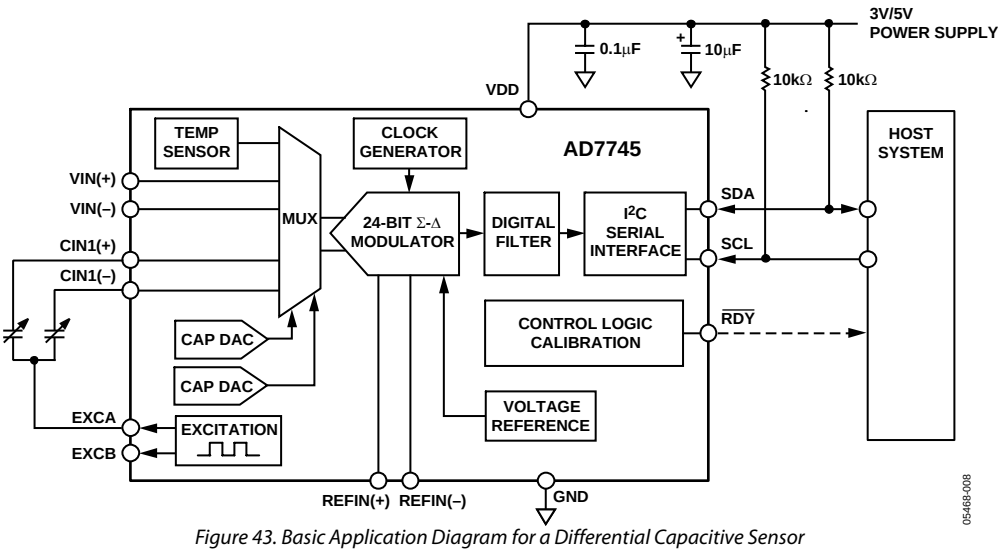
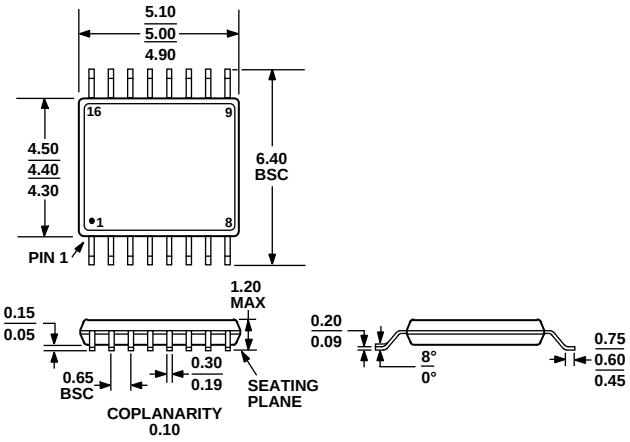


Figure 43. Basic Application Diagram for a Differential Capacitive Sensor

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 44. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD7745ARUZ[1]	–40°C to +125°C	16-Lead TSSOP	RU-16
AD7745ARUZ-REEL[1]	–40°C to +125°C	16-Lead TSSOP	RU-16
AD7745ARUZ-REEL7[1]	–40°C to +125°C	16-Lead TSSOP	RU-16
AD7746ARUZ[1]	–40°C to +125°C	16-Lead TSSOP	RU-16
AD7746ARUZ-REEL[1]	–40°C to +125°C	16-Lead TSSOP	RU-16
AD7746ARUZ-REEL7[1]	–40°C to +125°C	16-Lead TSSOP	RU-16
EVAL-AD7746EB		Evaluation Board	

[1] Z = Pb-free part.

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