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# FUNCTIONAL BLOCK DIAGRAM

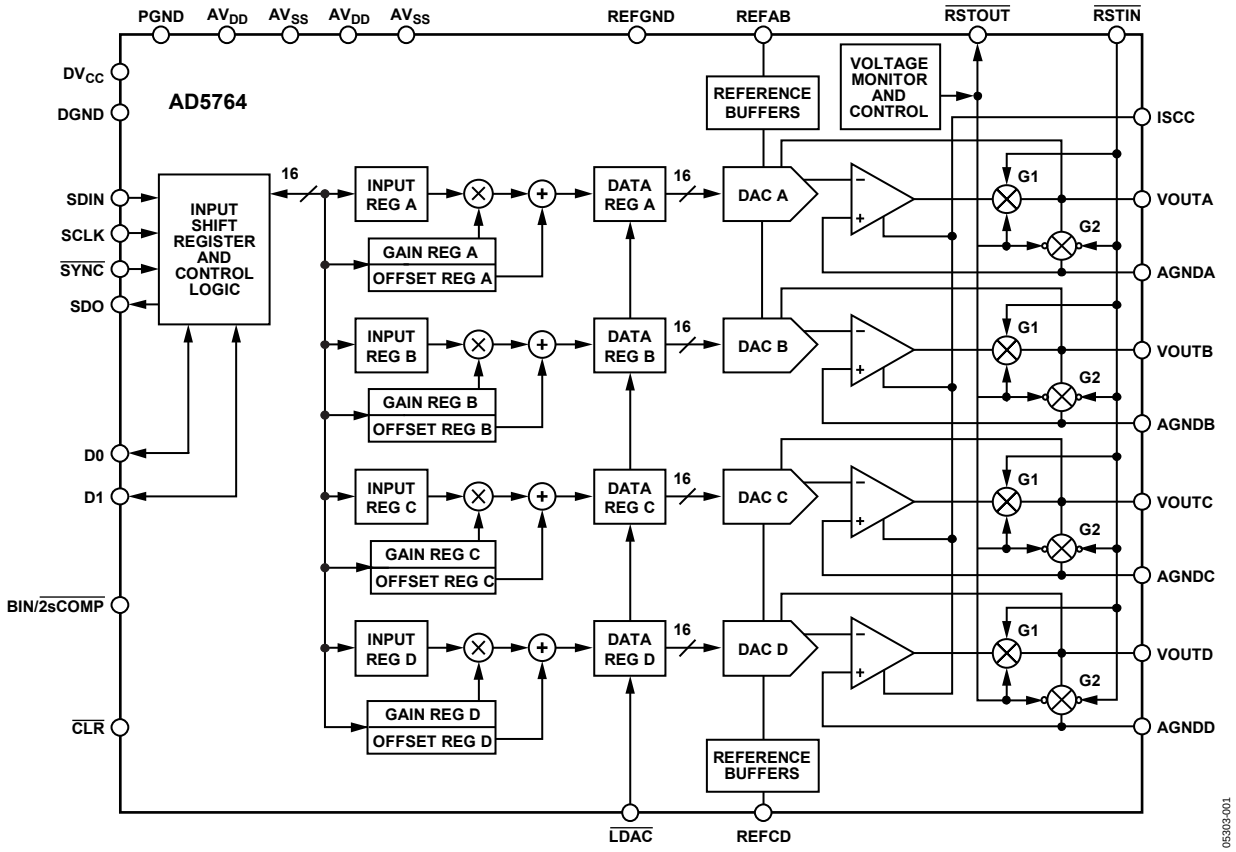



*Figure 1.*

# SPECIFICATIONS

$AV_{DD}$ = 11.4 V to 16.5 V, $AV_{SS}$ = −11.4 V to −16.5 V, AGNDx = DGND = REFGND = PGND = 0 V; REFAB = REFCD = 5 V; $DV_{CC}$ = 2.7 V to 5.25 V, $R_{LOAD}$ = 10 kΩ, $C_L$ = 200 pF. Temperature range: −40°C to +85°C; typical at +25°C. Device functionality is guaranteed to +105°C with degraded performance. All specifications $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

**Table 2.**

| Parameter | A Grade | B Grade | C Grade | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| ACCURACY | | | | | Outputs unloaded |
| Resolution | 16 | 16 | 16 | Bits | |
| Relative Accuracy (INL) | ±4 | ±2 | ±1 | LSB max | |
| Differential Nonlinearity | ±1 | ±1 | ±1 | LSB max | Guaranteed monotonic |
| Bipolar Zero Error | ±2 | ±2 | ±2 | mV max | At 25°C; error at other temperatures obtained using bipolar zero TC |
| Bipolar Zero Temperature Coefficient (TC)[1] | ±2 | ±2 | ±2 | ppm FSR/°C max | |
| Zero-Scale Error | ±2 | ±2 | ±2 | mV max | At 25°C; error at other temperatures obtained using zero-scale TC |
| Zero-Scale TC[1] | ±2 | ±2 | ±2 | ppm FSR/°C max | |
| Gain Error | ±0.02 | ±0.02 | ±0.02 | % FSR max | At 25°C; error at other temperatures obtained using gain TC |
| Gain TC[1] | ±2 | ±2 | ±2 | ppm FSR/°C max | |
| DC Crosstalk[1] | 0.5 | 0.5 | 0.5 | LSB max | |
| REFERENCE INPUT[1] | | | | | |
| Reference Input Voltage | 5 | 5 | 5 | V nom | ±1% for specified performance |
| DC Input Impedance | 1 | 1 | 1 | MΩ min | Typically 100 MΩ |
| Input Current | ±10 | ±10 | ±10 | µA max | Typically ±30 nA |
| Reference Range | 1 to 7 | 1 to 7 | 1 to 7 | V min to V max | |
| OUTPUT CHARACTERISTICS[1] | | | | | |
| Output Voltage Range[2] | ±10.5263 | ±10.5263 | ±10.5263 | V min to V max | $AV_{DD}/AV_{SS}$ = ±11.4 V, $V_{REFIN}$ = 5 V |
| | ±14 | ±14 | ±14 | V min to V max | $AV_{DD}/AV_{SS}$ = ±16.5 V, $V_{REFIN}$ = 7 V |
| Output Voltage Drift vs. Time | ±13 | ±13 | ±13 | ppm FSR/ 500 hours typ | |
| | ±15 | ±15 | ±15 | ppm FSR/ 1000 hours typ | |
| Short-Circuit Current | 10 | 10 | 10 | mA typ | $R_{ISCC}$ = 6 kΩ, see Figure 31 |
| Load Current | ±1 | ±1 | ±1 | mA max | For specified performance |
| Capacitive Load Stability | | | | | |
| $R_{LOAD}$ = ∞ | 200 | 200 | 200 | pF max | |
| $R_{LOAD}$ = 10 kΩ | 1000 | 1000 | 1000 | pF max | |
| DC Output Impedance | 0.3 | 0.3 | 0.3 | Ω max | |
| DIGITAL INPUTS | | | | | $DV_{CC}$ = 2.7 V to 5.25 V, JEDEC compliant |
| Input High Voltage, $V_{IH}$ | 2 | 2 | 2 | V min | |
| Input Low Voltage, $V_{IL}$ | 0.8 | 0.8 | 0.8 | V max | |
| Input Current | ±1 | ±1 | ±1 | µA max | Per pin |
| Pin Capacitance | 10 | 10 | 10 | pF max | Per pin |

| Parameter | A Grade | B Grade | C Grade | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| DIGITAL OUTPUTS (D0, D1, SDO)[1] | | | | | |
| Output Low Voltage | 0.4 | 0.4 | 0.4 | V max | $DV_{CC}$ = 5 V ± 5%, sinking 200 µA |
| Output High Voltage | $DV_{CC}$ − 1 | $DV_{CC}$ − 1 | $DV_{CC}$ − 1 | V min | $DV_{CC}$ = 5 V ± 5%, sourcing 200 µA |
| Output Low Voltage | 0.4 | 0.4 | 0.4 | V max | $DV_{CC}$ = 2.7 V to 3.6 V, sinking 200 µA |
| Output High Voltage | $DV_{CC}$ − 0.5 | $DV_{CC}$ − 0.5 | $DV_{CC}$ − 0.5 | V min | $DV_{CC}$ = 2.7 V to 3.6 V, sourcing 200 µA |
| High Impedance Leakage Current | ±1 | ±1 | ±1 | µA max | SDO only |
| High Impedance Output Capacitance | 5 | 5 | 5 | pF typ | SDO only |
| POWER REQUIREMENTS | | | | | |
| $AV_{DD}/AV_{SS}$ | ±11.4 to ±16.5 | ±11.4 to ±16.5 | ±11.4 to ±16.5 | V min to V max | |
| $DV_{CC}$ | 2.7 to 5.25 | 2.7 to 5.25 | 2.7 to 5.25 | V min to V max | |
| Power Supply Sensitivity[1] | | | | | |
| $\Delta V_{OUT}/\Delta AV_{DD}$ | −85 | −85 | −85 | dB typ | |
| $AI_{DD}$ | 3.5 | 3.5 | 3.5 | mA/channel max | Outputs unloaded |
| $AI_{SS}$ | 2.75 | 2.75 | 2.75 | mA/channel max | Outputs unloaded |
| $DI_{CC}$ | 1.2 | 1.2 | 1.2 | mA max | $V_{IH} = DV_{CC}$, $V_{IL}$ = DGND, 750 µA typical |
| Power Dissipation | 275 | 275 | 275 | mW typ | ±12 V operation output unloaded |

[1] Guaranteed by design and characterization; not production tested.
[2] Output amplifier headroom requirement is 1.4 V minimum.

## AC PERFORMANCE CHARACTERISTICS

$AV_{DD}$ = 11.4 V to 16.5 V, $AV_{SS}$ = −11.4 V to −16.5 V, AGNDx = DGND = REFGND = PGND = 0 V; REFAB = REFCD = 5 V; $DV_{CC}$ = 2.7 V to 5.25 V, $R_{LOAD}$ = 10 kΩ, $C_L$ = 200 pF. All specifications $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

**Table 3.**

| Parameter | A Grade | B Grade | C Grade | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| DYNAMIC PERFORMANCE[1] | | | | | |
| Output Voltage Settling Time | 8 | 8 | 8 | µs typ | Full-scale step to ±1 LSB |
| | 10 | 10 | 10 | µs max | |
| | 2 | 2 | 2 | µs typ | 512 LSB step settling |
| Slew Rate | 5 | 5 | 5 | V/µs typ | |
| Digital-to-Analog Glitch Energy | 8 | 8 | 8 | nV-sec typ | |
| Glitch Impulse Peak Amplitude | 25 | 25 | 25 | mV max | |
| Channel-to-Channel Isolation | 80 | 80 | 80 | dB typ | |
| DAC-to-DAC Crosstalk | 8 | 8 | 8 | nV-sec typ | |
| Digital Crosstalk | 2 | 2 | 2 | nV-sec typ | |
| Digital Feedthrough | 2 | 2 | 2 | nV-sec typ | Effect of input bus activity on DAC outputs |
| Output Noise (0.1 Hz to 10 Hz) | 0.1 | 0.1 | 0.1 | LSB p-p typ | |
| Output Noise (0.1 Hz to 100 kHz) | 45 | 45 | 45 | µV rms max | |
| 1/f Corner Frequency | 1 | 1 | 1 | kHz typ | |
| Output Noise Spectral Density | 60 | 60 | 60 | nV/√Hz typ | Measured at 10 kHz |
| Complete System Output Noise Spectral Density[2] | 80 | 80 | 80 | nV/√Hz typ | Measured at 10 kHz |

[1] Guaranteed by design and characterization; not production tested.
[2] Includes noise contributions from integrated reference buffers, 16-bit DAC, and output amplifier.

## TIMING CHARACTERISTICS

$AV_{DD}$ = 11.4 V to 16.5 V, $AV_{SS}$ = −11.4 V to −16.5 V, AGNDx = DGND = REFGND = PGND = 0 V; REFAB = REFCD = 5 V; $DV_{CC}$ = 2.7 V to 5.25 V, $R_{LOAD}$ = 10 kΩ, $C_L$ = 200 pF. All specifications $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

**Table 4.**

| Parameter[1, 2, 3] | Limit at $T_{MIN}$, $T_{MAX}$ | Unit | Description |
|---|---|---|---|
| $t_1$ | 33 | ns min | SCLK cycle time |
| $t_2$ | 13 | ns min | SCLK high time |
| $t_3$ | 13 | ns min | SCLK low time |
| $t_4$ | 13 | ns min | $\overline{SYNC}$ falling edge to SCLK falling edge setup time |
| $t_5$[4] | 13 | ns min | 24th SCLK falling edge to $\overline{SYNC}$ rising edge |
| $t_6$ | 90 | ns min | Minimum $\overline{SYNC}$ high time |
| $t_7$ | 2 | ns min | Data setup time |
| $t_8$ | 5 | ns min | Data hold time |
| $t_9$ | 1.7 | µs min | $\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge (all DACs updated) |
| | 480 | ns min | $\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge (single DAC updated) |
| $t_{10}$ | 10 | ns min | $\overline{LDAC}$ pulse width low |
| $t_{11}$ | 500 | ns max | $\overline{LDAC}$ falling edge to DAC output response time |
| $t_{12}$ | 10 | µs max | DAC output settling time |
| $t_{13}$ | 10 | ns min | $\overline{CLR}$ pulse width low |
| $t_{14}$ | 2 | µs max | $\overline{CLR}$ pulse activation time |
| $t_{15}$[5, 6] | 25 | ns max | SCLK rising edge to SDO valid |
| $t_{16}$ | 13 | ns min | $\overline{SYNC}$ rising edge to SCLK falling edge |
| $t_{17}$ | 2 | µs max | $\overline{SYNC}$ rising edge to DAC output response time ($\overline{LDAC}$ = 0) |
| $t_{18}$ | 170 | ns min | $\overline{LDAC}$ falling edge to $\overline{SYNC}$ rising edge |

[1] Guaranteed by design and characterization; not production tested.
[2] All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of $DV_{CC}$) and timed from a voltage level of 1.2 V.
[3] See Figure 2, Figure 3, and Figure 4.
[4] Standalone mode only.
[5] Measured with the load circuit of Figure 5.
[6] Daisy-chain mode only.

### *Timing Diagrams*

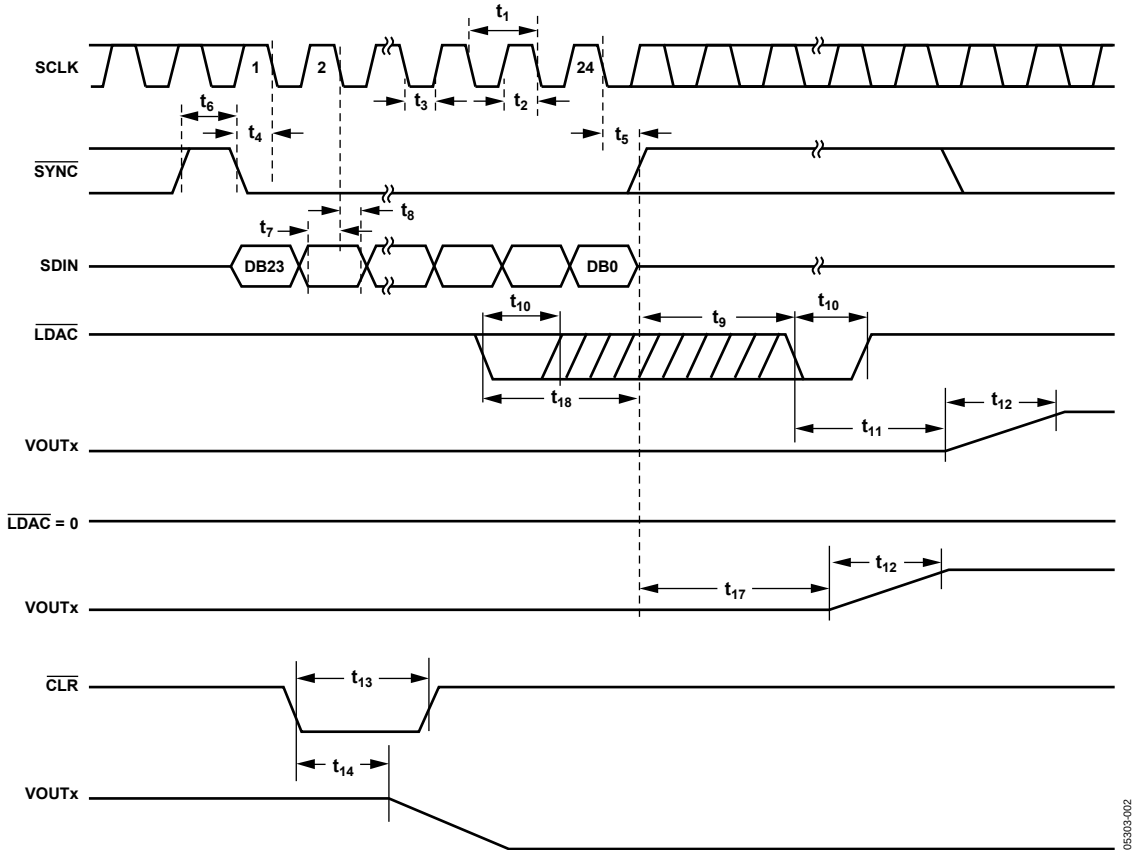



*Figure 2. Serial Interface Timing Diagram*

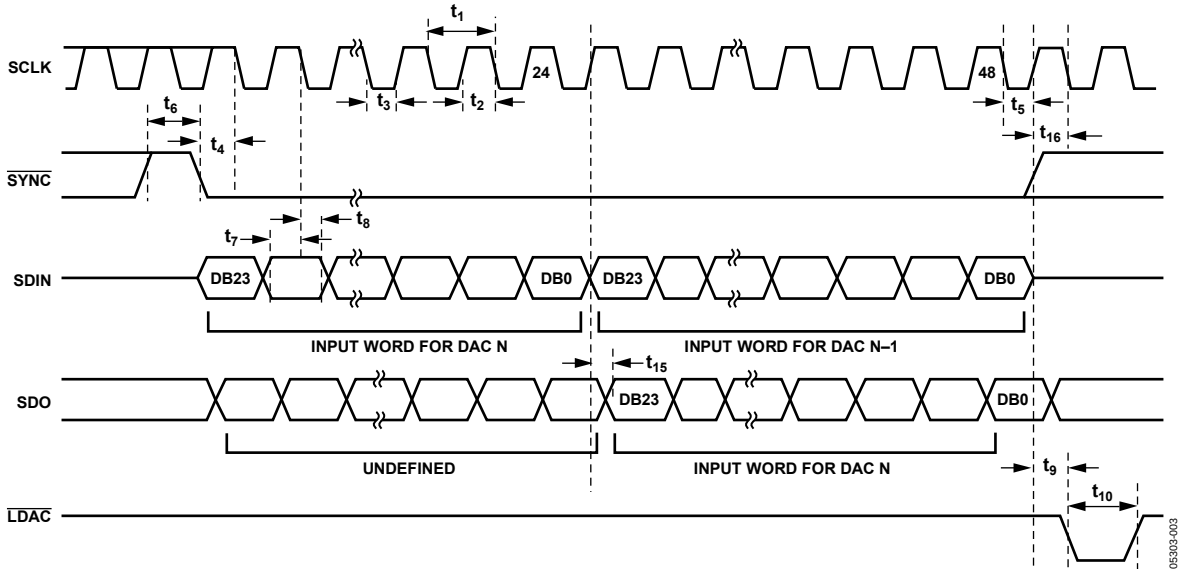



*Figure 3. Daisy-Chain Timing Diagram*

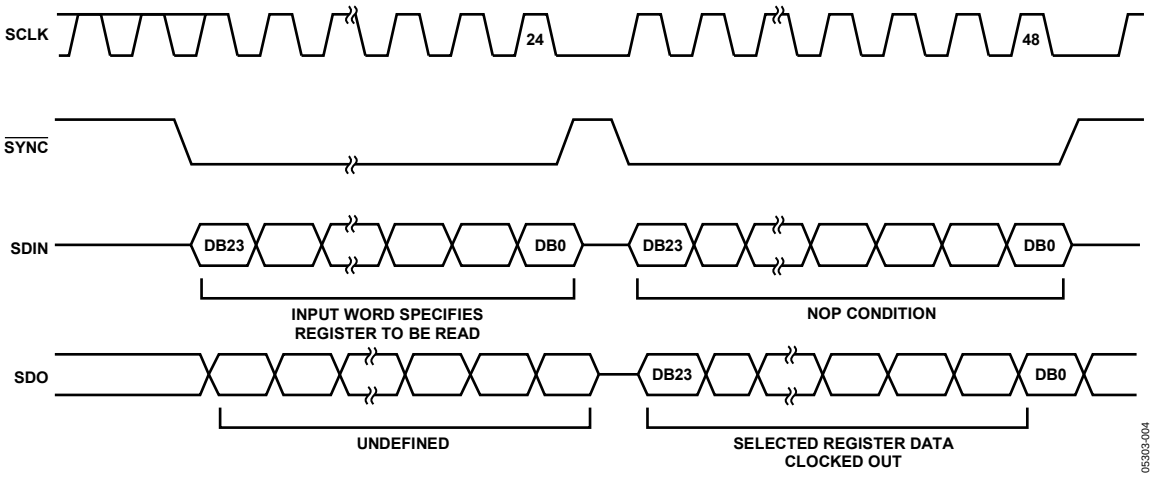



*Figure 4. Readback Timing Diagram*

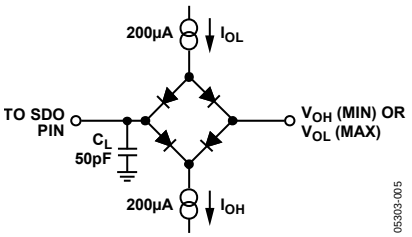



*Figure 5. Load Circuit for SDO Timing Diagram*

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C, unless otherwise noted. Transient currents of up to 100 mA do not cause SCR latch-up.

**Table 5.**

| Parameter | Rating |
|---|---|
| $AV_{DD}$ to AGNDx, DGND | −0.3 V to +17 V |
| $AV_{SS}$ to AGNDx, DGND | +0.3 V to −17 V |
| $DV_{CC}$ to DGND | −0.3 V to +7 V |
| Digital Inputs to DGND | −0.3 V to $DV_{CC}$ + 0.3 V or 7 V (whichever is less) |
| Digital Outputs to DGND | −0.3 V to $DV_{CC}$ + 0.3 V |
| REFAB, REFCD to AGNDx, PGND | −0.3 V to $AV_{DD}$ + 0.3 V |
| VOUTA, VOUTB, VOUTC, VOUTD to AGNDx | $AV_{SS}$ to $AV_{DD}$ |
| AGNDx to DGND | −0.3 V to +0.3 V |
| Operating Temperature Range | |
| Industrial | −40°C to +85°C |
| Storage Temperature Range | −65°C to +150°C |
| Junction Temperature ($T_J$ max) | 150°C |
| 32-Lead TQFP | |
| $\theta_{JA}$ Thermal Impedance | 65°C/W |
| $\theta_{JC}$ Thermal Impedance | 12°C/W |
| Lead Temperature | JEDEC industry standard |
| Soldering | J-STD-020 |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

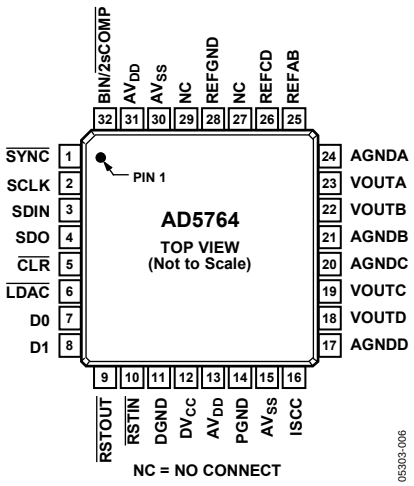



*Figure 6. Pin Configuration*

**Table 6. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | $\overline{\text{SYNC}}$ | Active Low Input. This is the frame synchronization signal for the serial interface. While $\overline{\text{SYNC}}$ is low, data is transferred in on the falling edge of SCLK. |
| 2 | SCLK | Serial Clock Input. Data is clocked into the input shift register on the falling edge of SCLK. This operates at clock speeds up to 30 MHz. |
| 3 | SDIN | Serial Data Input. Data must be valid on the falling edge of SCLK. |
| 4 | SDO | Serial Data Output. Used to clock data from the serial register in daisy-chain or readback mode. |
| 5 | $\overline{\text{CLR}}$ | Negative Edge Triggered Input. Asserting this pin sets the data register to 0x0000. There is an internal pull-up device on this logic input. Therefore, this pin can be left floating and defaults to a Logic 1 condition. |
| 6 | $\overline{\text{LDAC}}$ | Load DAC. Logic input. This is used to update the data register and consequently the analog outputs. When tied permanently low, the addressed data register is updated on the rising edge of $\overline{\text{SYNC}}$. If $\overline{\text{LDAC}}$ is held high during the write cycle, the DAC input shift register is updated but the output update is held off until the falling edge of $\overline{\text{LDAC}}$. In this mode, all analog outputs can be updated simultaneously on the falling edge of $\overline{\text{LDAC}}$. The $\overline{\text{LDAC}}$ pin must not be left unconnected. |
| 7, 8 | D0, D1 | Digital I/O Port. The user can set up these pins as inputs or outputs that are configurable and readable over the serial interface. When configured as inputs, these pins have weak internal pull-ups to $DV_{CC}$. When programmed as outputs, D0 and D1 are referenced by $DV_{CC}$ and DGND. |
| 9 | $\overline{\text{RSTOUT}}$ | Reset Logic Output. This is the output from the on-chip voltage monitor used in the reset circuit. If desired, it can be used to control other system components. |
| 10 | $\overline{\text{RSTIN}}$ | Reset Logic Input. This input allows external access to the internal reset logic. Applying a Logic 0 to this input clamps the DAC outputs to 0 V. In normal operation, $\overline{\text{RSTIN}}$ should be tied to Logic 1. Register values remain unchanged. |
| 11 | DGND | Digital Ground. |
| 12 | $DV_{CC}$ | Digital Supply. Voltage ranges from 2.7 V to 5.25 V. |
| 13, 31 | $AV_{DD}$ | Positive Analog Supply. Voltage ranges from 11.4 V to 16.5 V. |
| 14 | PGND | Ground Reference Point for Analog Circuitry. |
| 15, 30 | $AV_{SS}$ | Negative Analog Supply. Voltage ranges from −11.4 V to −16.5 V. |
| 16 | ISCC | Resistor Connection for Pin Programmable Short-Circuit Current. This pin is used in association with an optional external resistor to AGND to program the short-circuit current of the output amplifiers. Refer to the Design Features section for further details. |
| 17 | AGNDD | Ground Reference Pin for DAC D Output Amplifier. |
| 18 | VOUTD | Analog Output Voltage of DAC D. This pin is a buffered output with a nominal full-scale output range of ±10 V. The output amplifier is capable of directly driving a 10 kΩ, 200 pF load. |
| 19 | VOUTC | Analog Output Voltage of DAC C. This pin is a buffered output with a nominal full-scale output range of ±10 V. The output amplifier is capable of directly driving a 10 kΩ, 200 pF load. |
| 20 | AGNDC | Ground Reference Pin for DAC C Output Amplifier. |

| Pin No. | Mnemonic | Description |
|---|---|---|
| 21 | AGNDB | Ground Reference Pin for DAC B Output Amplifier. |
| 22 | VOUTB | Analog Output Voltage of DAC B. Buffered output with a nominal full-scale output range of ±10 V. The output amplifier is capable of directly driving a 10 kΩ, 200 pF load. |
| 23 | VOUTA | Analog Output Voltage of DAC A. Buffered output with a nominal full-scale output range of ±10 V. The output amplifier is capable of directly driving a 10 kΩ, 200 pF load. |
| 24 | AGNDA | Ground Reference Pin for DAC A Output Amplifier. |
| 25 | REFAB | External Reference Voltage Input for Channel A and Channel B. Reference input range is 1 V to 7 V; programs the full-scale output voltage. $V_{REFIN}$ = 5 V for specified performance. |
| 26 | REFCD | External Reference Voltage Input for Channel C and Channel D. Reference input range is 1 V to 7 V; programs the full-scale output voltage. $V_{REFIN}$ = 5 V for specified performance. |
| 27, 29 | NC | No Connect. |
| 28 | REFGND | Reference Ground Return for the Reference Generator and Buffers. |
| 32 | BIN/$\overline{2sCOMP}$ | Determines the DAC Coding. This pin should be hardwired to either $DV_{CC}$ or DGND. When hardwired to $DV_{CC}$, input coding is offset binary. When hardwired to DGND, input coding is twos complement (see Table 7 and Table 8). |

# TYPICAL PERFORMANCE CHARACTERISTICS

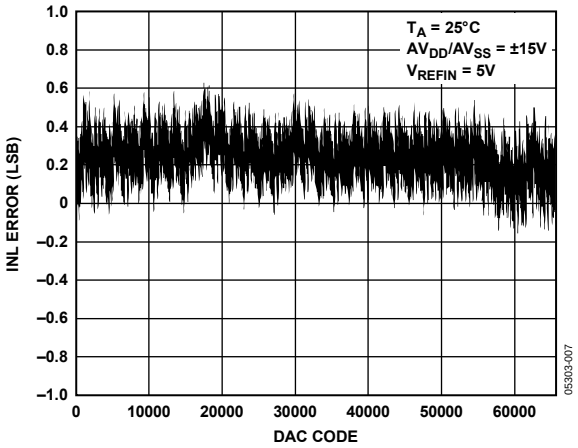



*Figure 7. Integral Nonlinearity Error vs. Code, $AV_{DD}/AV_{SS}$ = ±15 V*

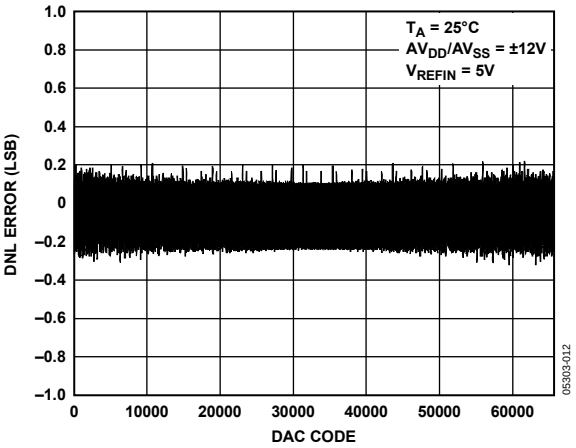



*Figure 10. Differential Nonlinearity Error vs. Code, $AV_{DD}/AV_{SS}$ = ±12 V*

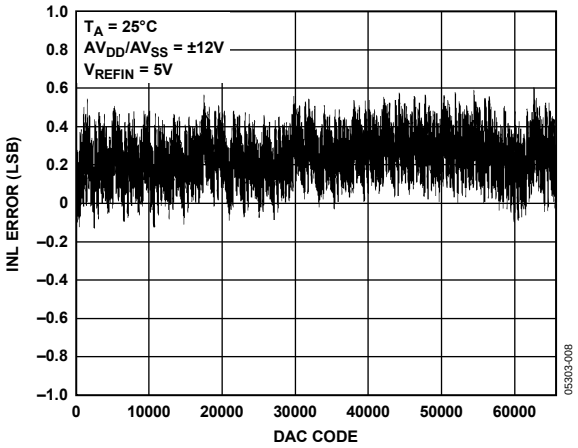



*Figure 8. Integral Nonlinearity Error vs. Code, $AV_{DD}/AV_{SS}$ = ±12 V*

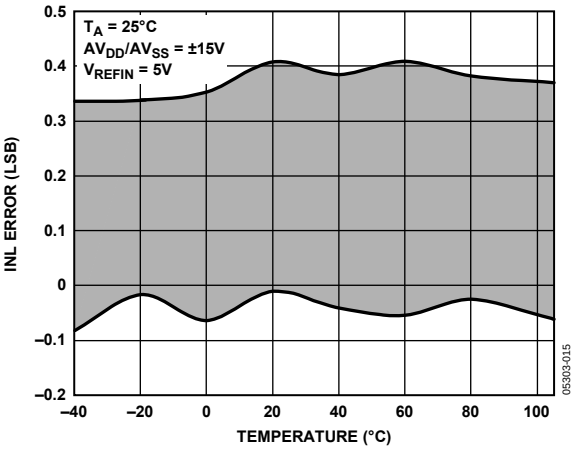



*Figure 11. Integral Nonlinearity Error vs. Temperature, $AV_{DD}/AV_{SS}$ = ±15 V*

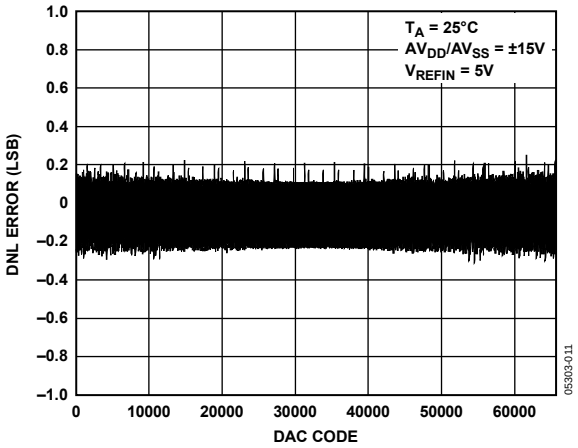



*Figure 9. Differential Nonlinearity Error vs. Code, $AV_{DD}/AV_{SS}$ = ±15 V*

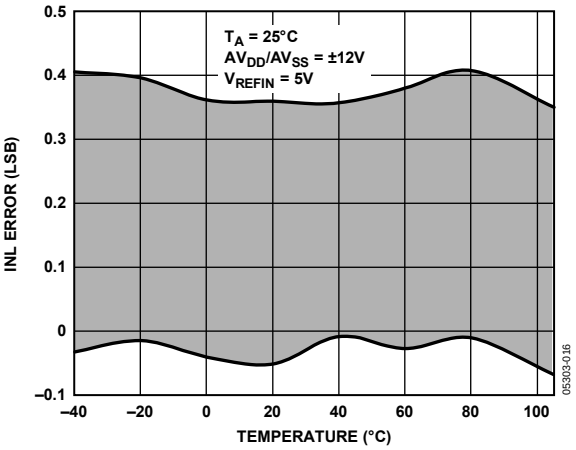



*Figure 12. Integral Nonlinearity Error vs. Temperature, $AV_{DD}/AV_{SS}$ = ±12 V*

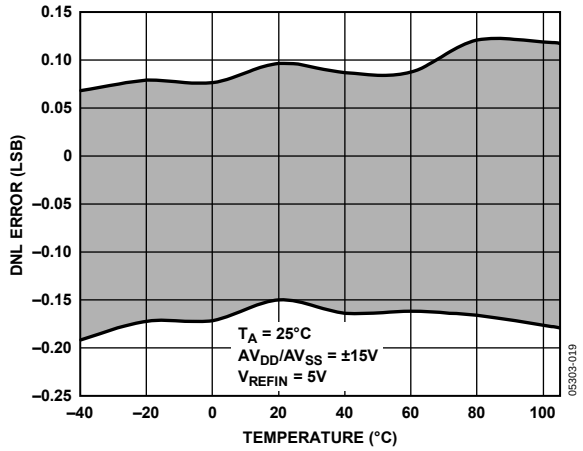



Figure 13. Differential Nonlinearity Error vs. Temperature, $AV_{DD}/AV_{SS}$ = ±15 V

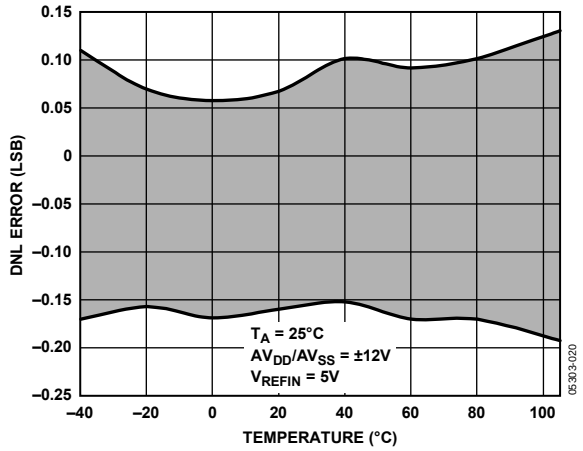



Figure 14. Differential Nonlinearity Error vs. Temperature, $AV_{DD}/AV_{SS}$ = ±12 V

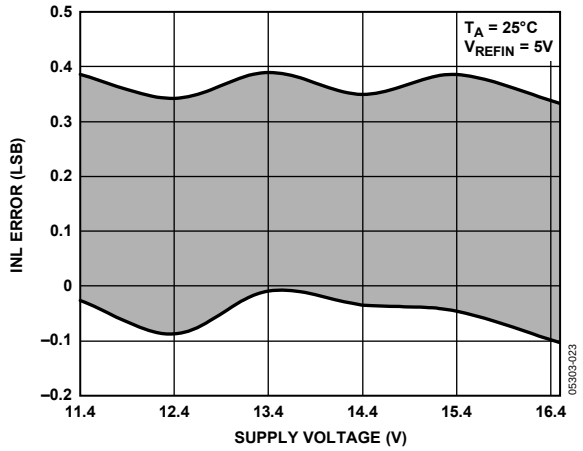



Figure 15. Integral Nonlinearity Error vs. Supply Voltage

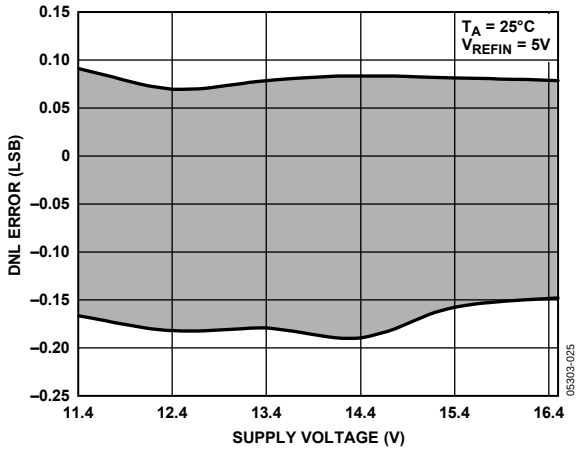



Figure 16. Differential Nonlinearity Error vs. Supply Voltage

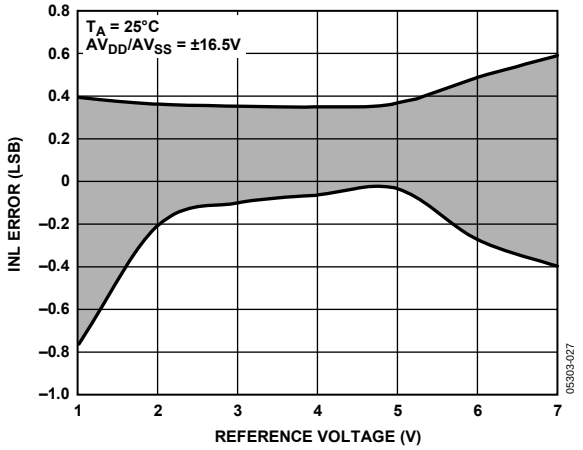



Figure 17. Integral Nonlinearity Error vs. Reference Voltage, $AV_{DD}/AV_{SS}$ = ±16.5 V

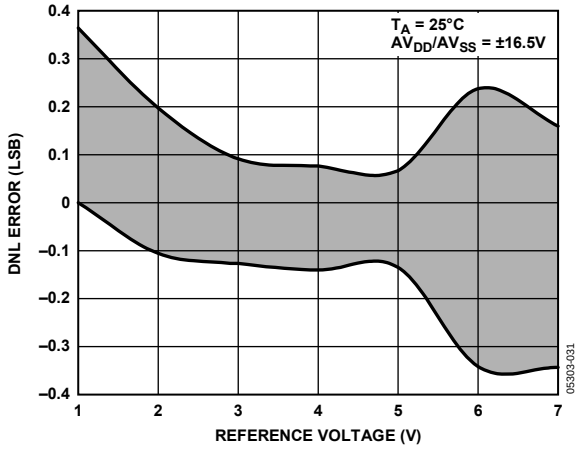



Figure 18. Differential Nonlinearity Error vs. Reference Voltage, $AV_{DD}/AV_{SS}$ = ±16.5 V

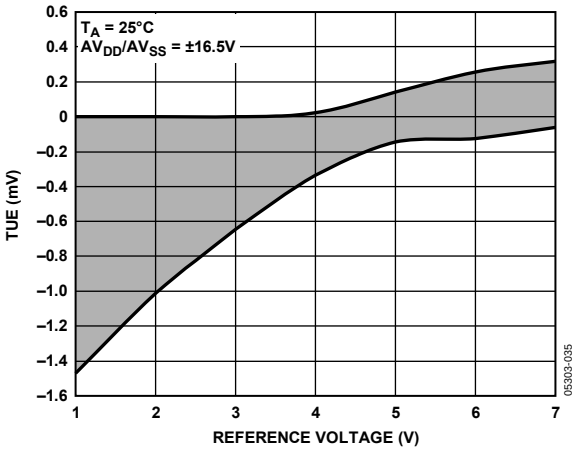



*Figure 19. Total Unadjusted Error vs. Reference Voltage, $AV_{DD}/AV_{SS}$ = ±16.5 V*

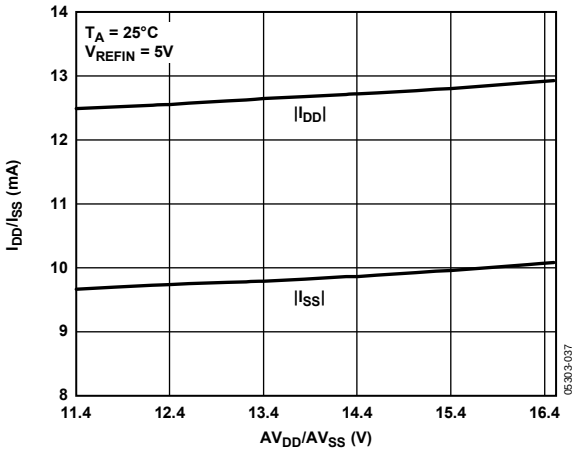



*Figure 20. $I_{DD}/I_{SS}$ vs. $AV_{DD}/AV_{SS}$*

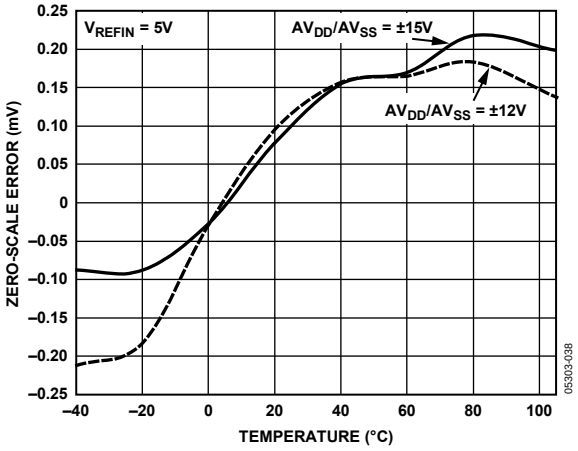



*Figure 21. Zero-Scale Error vs. Temperature*

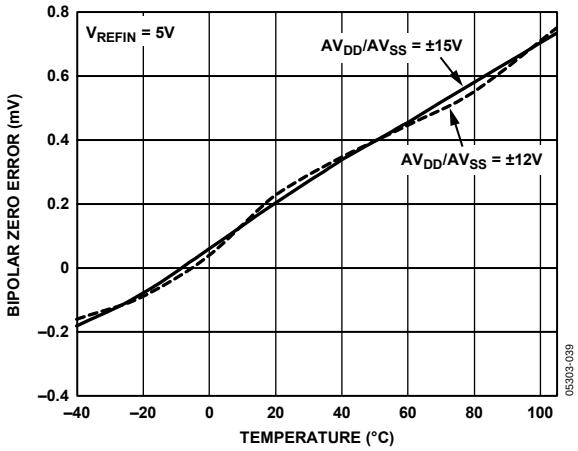



*Figure 22. Bipolar Zero Error vs. Temperature*

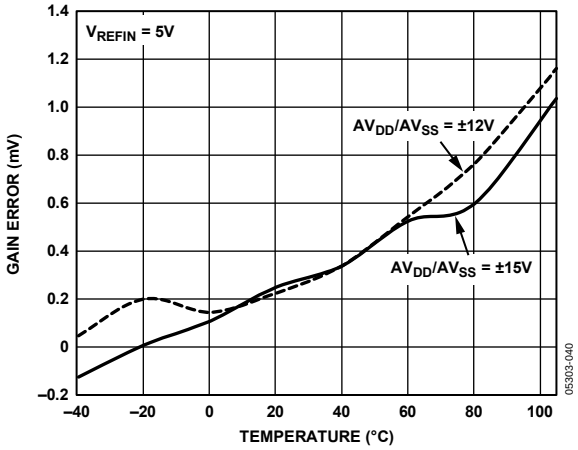



*Figure 23. Gain Error vs. Temperature*

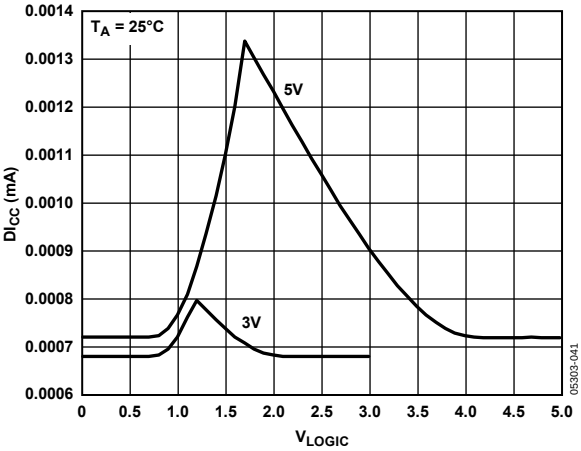



*Figure 24. $DI_{CC}$ vs. Logic Input Voltage*

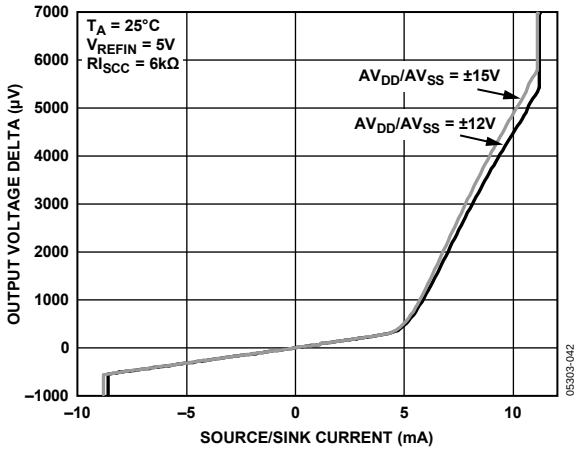



*Figure 25. Source and Sink Capability of Output Amplifier with Positive Full Scale Loaded*

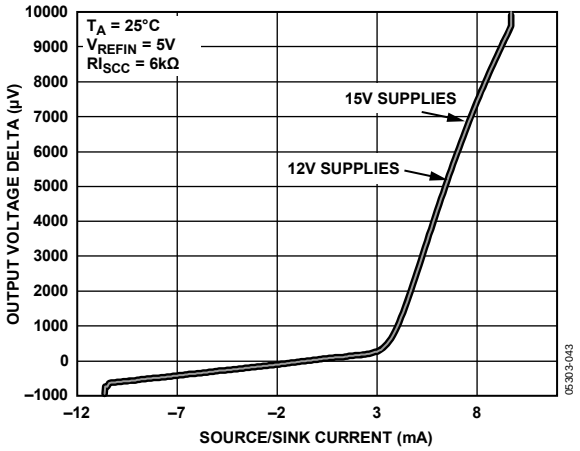



*Figure 26. Source and Sink Capability of Output Amplifier with Negative Full Scale Loaded*

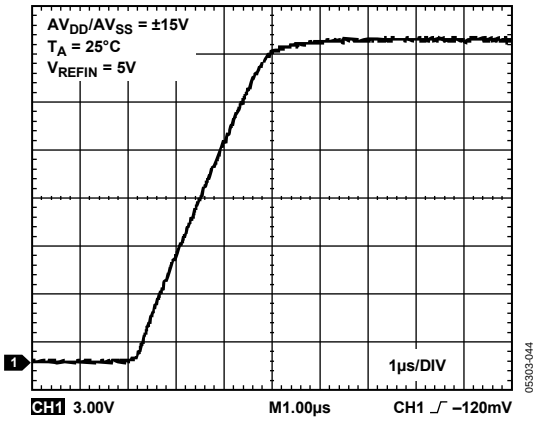



*Figure 27. Full-Scale Settling Time*

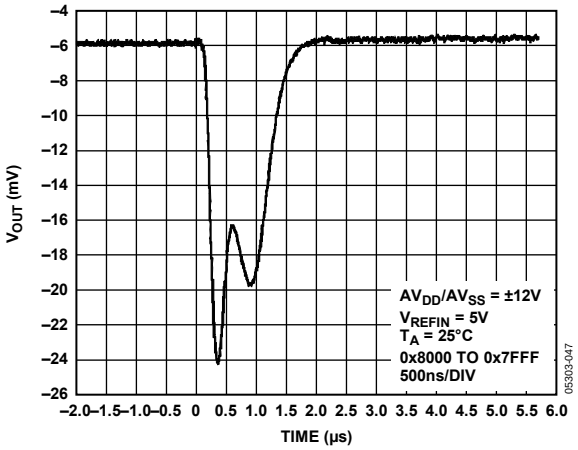



*Figure 28. Major Code Transition Glitch Energy, $AV_{DD}/AV_{SS}$ = ±12 V*

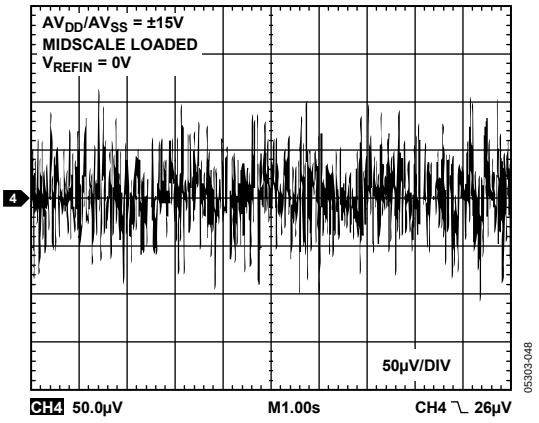



Figure 29. Peak-to-Peak Noise (100 kHz Bandwidth)

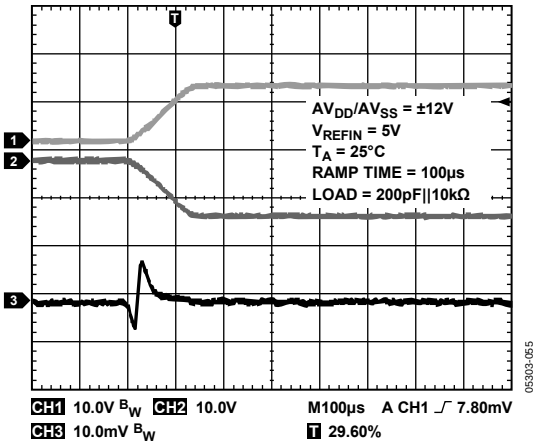



Figure 30. $V_{OUT}$ vs. $AV_{DD}/AV_{SS}$ on Power-Up

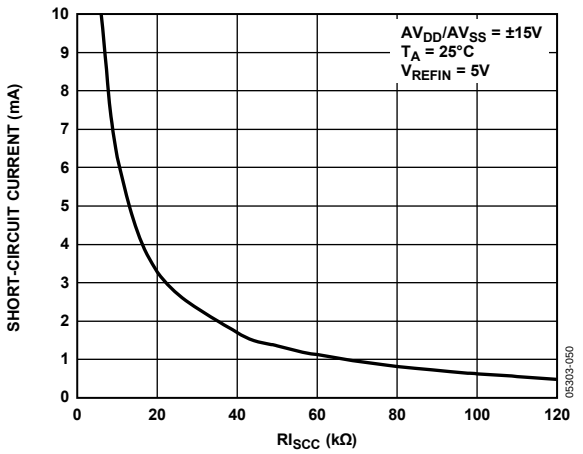



Figure 31. Short-Circuit Current vs. $RI_{SCC}$

# TERMINOLOGY

**Relative Accuracy or Integral Nonlinearity (INL)**
For the DAC, relative accuracy or integral nonlinearity (INL) is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. A typical INL vs. code plot can be seen in Figure 7.

**Differential Nonlinearity (DNL)**
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic. A typical DNL vs. code plot can be seen in Figure 9.

**Monotonicity**
A DAC is monotonic if the output either increases or remains constant for increasing digital input code. The AD5764 is monotonic over its full operating temperature range.

**Bipolar Zero Error**
Bipolar zero error is the deviation of the analog output from the ideal half-scale output of 0 V when the data register is loaded with 0x8000 (offset binary coding) or 0x0000 (twos complement coding). A plot of bipolar zero error vs. temperature can be seen in Figure 22.

**Bipolar Zero Temperature Coefficient (TC)**
Bipolar zero TC is the measure of the change in the bipolar zero error with a change in temperature. It is expressed in ppm FSR/°C.

**Full-Scale Error**
Full-scale error is a measure of the output error when full-scale code is loaded to the data register. Ideally, the output voltage should be $2 \times V_{REF} - 1$ LSB. Full-scale error is expressed in percentage of full-scale range.

**Negative Full-Scale Error/Zero-Scale Error**
Negative full-scale error is the error in the DAC output voltage when 0x0000 (offset binary coding) or 0x8000 (twos complement coding) is loaded to the data register. Ideally, the output voltage should be $-2 \times V_{REF}$. A plot of zero-scale error vs. temperature can be seen in Figure 21.

**Output Voltage Settling Time**
Output voltage settling time is the amount of time it takes for the output to settle to a specified level for a full-scale input change.

**Slew Rate**
The slew rate of a device is a limitation in the rate of change of the output voltage. The output slewing speed of a voltage-output DAC is usually limited by the slew rate of the amplifier used at its output. Slew rate is measured from 10% to 90% of the output signal and is given in V/µs.

**Gain Error**
Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal, expressed as a percentage of the full-scale range. A plot of gain error vs. temperature can be seen in Figure 23.

**Total Unadjusted Error**
Total unadjusted error (TUE) is a measure of the output error considering all the various errors. A plot of total unadjusted error vs. reference voltage can be seen in Figure 19.

**Zero-Scale Error Temperature Coefficient (TC)**
Zero-scale error TC is a measure of the change in zero-scale error with a change in temperature. Zero-scale error TC is expressed in ppm FSR/°C.

**Gain Error Temperature Coefficient (TC)**
Gain error TC is a measure of the change in gain error with changes in temperature. Gain error TC is expressed in ppm FSR/°C.

**Digital-to-Analog Glitch Energy**
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the data register changes state. It is normally specified as the area of the glitch in nV-sec, and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000); see Figure 28.

**Digital Feedthrough**
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC but is measured when the DAC output is not updated. It is specified in nV-sec and measured with a full-scale code change on the data bus, that is, from all 0s to all 1s, and vice versa.

**Power Supply Sensitivity**
Power supply sensitivity indicates how the output of the DAC is affected by changes in the power supply voltage.

**DC Crosstalk**
DC crosstalk is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC while monitoring another DAC, and is expressed in LSBs.

**DAC-to-DAC Crosstalk**
DAC-to-DAC crosstalk is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent output change of another DAC. This includes both digital and analog crosstalk. It is measured by loading one of the DACs with a full-scale code change (all 0s to all 1s and vice versa) with $\overline{\text{LDAC}}$ low and monitoring the output of another DAC. The energy of the glitch is expressed in nV-sec.

**Channel-to-Channel Isolation**
Channel-to-channel isolation is the ratio of the amplitude of the signal at the output of one DAC to a sine wave on the reference input of another DAC. It is measured in dB.

**Digital Crosstalk**
Digital crosstalk is a measure of the impulse injected into the analog output of one DAC from the digital inputs of another DAC, but is measured when the DAC output is not updated. It is specified in nV-sec and measured with a full-scale code change on the data bus, that is, from all 0s to all 1s, and vice versa.

# THEORY OF OPERATION

The AD5764 is a quad, 16-bit, serial input, bipolar voltage output DAC and operates from supply voltages of ±11.4 V to ±16.5 V and has a buffered output voltage of up to ±10.5263 V. Data is written to the AD5764 in a 24-bit word format, via a 3-wire serial interface. The device also offers an SDO pin that is available for daisy-chaining or readback.

The AD5764 incorporates a power-on reset circuit, which ensures that the data register powers up loaded with 0x0000. The AD5764 features a digital I/O port that can be programmed via the serial interface, on-chip reference buffers and per channel digital gain, and offset registers.

## DAC ARCHITECTURE

The DAC architecture of the AD5764 consists of a 16-bit, current mode, segmented R-2R DAC. The simplified circuit diagram for the DAC section is shown in Figure 32.

The four MSBs of the 16-bit data word are decoded to drive 15 switches, E1 to E15. Each of these switches connects one of the 15 matched resistors to either AGNDx or IOUT. The remaining 12 bits of the data-word drive Switch S0 to Switch S11 of the 12-bit R-2R ladder network.

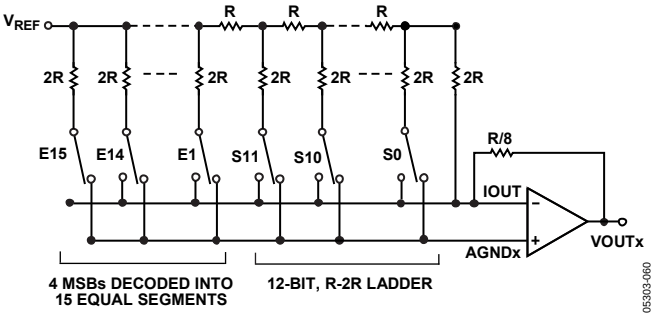



*Figure 32. DAC Ladder Structure*

## REFERENCE BUFFERS

The AD5764 operates with an external reference. The reference inputs (REFAB and REFCD) have an input range up to 7 V. This input voltage is used to provide a buffered positive and negative reference for the DAC cores. The positive reference is given by

$$+V_{REF} = 2 \times V_{REF}$$

The negative reference to the DAC cores is given by

$$-V_{REF} = -2 \times V_{REF}$$

These positive and negative reference voltages (along with the gain register values) define the output ranges of the DACs.

## SERIAL INTERFACE

The AD5764 is controlled over a versatile 3-wire serial interface that operates at clock rates of up to 30 MHz and is compatible with SPI, QSPI™, MICROWIRE™, and DSP standards.

### *Input Shift Register*

The input shift register is 24 bits wide. Data is loaded into the device MSB first as a 24-bit word under the control of a serial clock input, SCLK. The input shift register consists of a read/write bit, three register select bits, three DAC address bits, and 16 data bits, as shown in Table 9. The timing diagram for this operation is shown in Figure 2.

Upon power-up, the data register is loaded with zero code (0x0000), and the outputs are clamped to 0 V via a low impedance path. The outputs can be updated with the zero code value at this time by asserting either $\overline{\text{LDAC}}$ or $\overline{\text{CLR}}$. The corresponding output voltage depends on the state of the BIN/$\overline{\text{2sCOMP}}$ pin. If the BIN/$\overline{\text{2sCOMP}}$ pin is tied to DGND, the data coding is twos complement, and the outputs update to 0 V. If the BIN/$\overline{\text{2sCOMP}}$ pin is tied to $DV_{CC}$, the data coding is offset binary, and the outputs update to negative full scale. To power up the outputs with zero code loaded to the outputs, hold the $\overline{\text{CLR}}$ pin low during power-up.

### *Standalone Operation*

The serial interface works with both a continuous and noncontinuous serial clock. A continuous SCLK source can only be used if $\overline{\text{SYNC}}$ is held low for the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles must be used and $\overline{\text{SYNC}}$ must be taken high after the final clock to latch the data. The first falling edge of $\overline{\text{SYNC}}$ starts the write cycle. Exactly 24 falling clock edges must be applied to SCLK before $\overline{\text{SYNC}}$ is brought high again. If $\overline{\text{SYNC}}$ is brought high before the 24th falling SCLK edge, the data written is invalid. If more than 24 falling SCLK edges are applied before $\overline{\text{SYNC}}$ is brought high, the input data is also invalid. The input shift register addressed is updated on the rising edge of $\overline{\text{SYNC}}$. For another serial transfer to take place, $\overline{\text{SYNC}}$ must be brought low again. After the end of the serial data transfer, data is automatically transferred from the input shift register to the addressed register.

When the data has been transferred into the chosen register of the addressed DAC, the data register and outputs can be updated by taking $\overline{\text{LDAC}}$ low.

### Daisy-Chain Operation

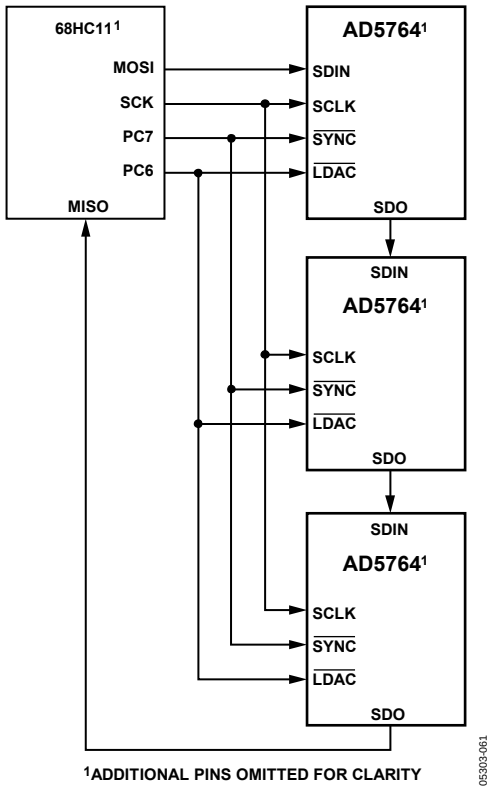



*Figure 33. Daisy-Chaining the AD5764*

For systems that contain several devices, the SDO pin can be used to daisy-chain several devices together. This daisy-chain mode can be useful in system diagnostics and in reducing the number of serial interface lines. The first falling edge of $\overline{\text{SYNC}}$ starts the write cycle. The SCLK is continuously applied to the input shift register when $\overline{\text{SYNC}}$ is low. If more than 24 clock pulses are applied, the data ripples out of the input shift register and appears on the SDO line. This data is clocked out on the rising edge of SCLK and is valid on the falling edge. By connecting the SDO of the first device to the SDIN input of the next device in the chain, a multidevice interface is constructed. Each device in the system requires 24 clock pulses. Therefore, the total number of clock cycles must equal 24N, where N is the total number of AD5764 devices in the chain. When the serial transfer to all devices is complete, $\overline{\text{SYNC}}$ is taken high. This latches the input data in each device in the daisy chain and prevents any further data from being clocked into the input shift register. The serial clock can be a continuous or a gated clock.

A continuous SCLK source can only be used if $\overline{\text{SYNC}}$ is held low for the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles must be used, and $\overline{\text{SYNC}}$ must be taken high after the final clock to latch the data.

### Readback Operation

Before a readback operation is initiated, the SDO pin must be enabled by writing to the function register and clearing the SDO disable bit; this bit is cleared by default. Readback mode is invoked by setting the R/$\overline{\text{W}}$ bit = 1 in the serial input shift register write. With R/$\overline{\text{W}}$ = 1, Bit A2 to Bit A0, in association with Bit REG2, Bit REG1, and Bit REG0, select the register to be read. The remaining data bits in the write sequence are don't cares. During the next SPI write, the data appearing on the SDO output contain the data from the previously addressed register. For a read of a single register, the NOP command can be used in clocking out the data from the selected register on SDO. The readback diagram in Figure 4 shows the readback sequence. For example, to read back the fine gain register of Channel A on the AD5764, implement the following:

1. Write 0xA0XXXX to the AD5764 input shift register. This configures the AD5764 for read mode with the fine gain register of Channel A selected. Note that all the data bits, DB15 to DB0, are don't cares.
2. Follow this with a second write, an NOP condition, 0x00XXXX. During this write, the data from the fine gain register is clocked out on the SDO line, that is, data clocked out contain the data from the fine gain register in Bit DB5 to Bit DB0.

## SIMULTANEOUS UPDATING VIA $\overline{\text{LDAC}}$

Depending on the status of both $\overline{\text{SYNC}}$ and $\overline{\text{LDAC}}$, and after data has been transferred into the input register of the DACs, there are two ways in which the data register and DAC outputs can be updated.

### Individual DAC Updating

In this mode, $\overline{\text{LDAC}}$ is held low while data is being clocked into the input shift register. The addressed DAC output is updated on the rising edge of $\overline{\text{SYNC}}$.

### Simultaneous Updating of All DACs

In this mode, $\overline{\text{LDAC}}$ is held high while data is being clocked into the input shift register. All DAC outputs are updated by taking $\overline{\text{LDAC}}$ low any time after $\overline{\text{SYNC}}$ has been taken high. The update now occurs on the falling edge of $\overline{\text{LDAC}}$.

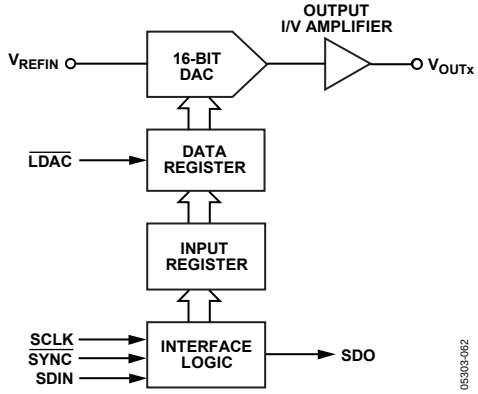



*Figure 34. Simplified Serial Interface of Input Loading Circuitry for One DAC Channel*

## TRANSFER FUNCTION

Table 7 and Table 8 show the ideal input code to output voltage relationship for the AD5764 for both offset binary and twos complement data coding, respectively.

**Table 7. Ideal Output Voltage to Input Code Relationship—Offset Binary Data Coding**

| Digital Input | | | | Analog Output |
|---|---|---|---|---|
| **MSB** | | | **LSB** | **VOUTx** |
| 1111 | 1111 | 1111 | 1111 | +2 $V_{REF}$ × (32,767/32,768) |
| 1000 | 0000 | 0000 | 0001 | +2 $V_{REF}$ × (1/32,768) |
| 1000 | 0000 | 0000 | 0000 | 0 V |
| 0111 | 1111 | 1111 | 1111 | −2 $V_{REF}$ × (1/32,768) |
| 0000 | 0000 | 0000 | 0000 | −2 $V_{REF}$ × (32,767/32,768) |

**Table 8. Ideal Output Voltage to Input Code Relationship—Twos Complement Data Coding**

| Digital Input | | | | Analog Output |
|---|---|---|---|---|
| **MSB** | | | **LSB** | **VOUTx** |
| 0111 | 1111 | 1111 | 1111 | +2 $V_{REF}$ × (32,767/32,768) |
| 0000 | 0000 | 0000 | 0001 | +2 $V_{REF}$ × (1/32,768) |
| 0000 | 0000 | 0000 | 0000 | 0 V |
| 1111 | 1111 | 1111 | 1111 | −2 $V_{REF}$ × (1/32,768) |
| 1000 | 0000 | 0000 | 0000 | −2 $V_{REF}$ × (32,767/32,768) |

The output voltage expression for the AD5764 is given by

$$V_{OUT} = -2 \times V_{REFIN} + 4 \times V_{REFIN}\left[\frac{D}{65{,}536}\right]$$

where:
*D* is the decimal equivalent of the code loaded to the DAC.
$V_{REFIN}$ is the reference voltage applied at the REFAB/REFCD pins.

## ASYNCHRONOUS CLEAR ($\overline{CLR}$)

$\overline{CLR}$ is a negative edge triggered clear that allows the outputs to be cleared to either 0 V (twos complement coding) or negative full scale (offset binary coding). It is necessary to maintain $\overline{CLR}$ low for a minimum amount of time (see Figure 2) for the operation to complete. When the $\overline{CLR}$ signal is returned high, the output remains at the cleared value until a new value is programmed. If at power-on, $\overline{CLR}$ is at 0 V, then all DAC outputs are updated with the clear value. A clear can also be initiated through software by writing Command 0x04XXXX to the AD5764.

**Table 9. Input Shift Register Bit Map**

**MSB** **LSB**

| DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15:DB0 |
|---|---|---|---|---|---|---|---|---|
| R/$\overline{W}$ | 0 | REG2 | REG1 | REG0 | A2 | A1 | A0 | Data |

**Table 10. Input Shift Register Bit Functions**

| Bit | Description | | | |
|---|---|---|---|---|
| R/$\overline{W}$ | Indicates a read from or a write to the addressed register. | | | |
| REG2, REG1, REG0 | Used in association with the address bits to determine if a read or write operation is to the data register, offset register, coarse gain register, fine gain register, or function register. | | | |
| | **REG2** | **REG1** | **REG0** | **Function** |
| | 0 | 0 | 0 | Function register |
| | 0 | 1 | 0 | Data register |
| | 0 | 1 | 1 | Coarse gain register |
| | 1 | 0 | 0 | Fine gain register |
| | 1 | 0 | 1 | Offset register |
| A2, A1, A0 | These bits are used to decode the DAC channels. | | | |
| | **A2** | **A1** | **A0** | **Channel Address** |
| | 0 | 0 | 0 | DAC A |
| | 0 | 0 | 1 | DAC B |
| | 0 | 1 | 0 | DAC C |
| | 0 | 1 | 1 | DAC D |
| | 1 | 0 | 0 | All DACs |
| Data | Data bits. | | | |

## FUNCTION REGISTER

The function register is addressed by setting the three REG bits to 000. The values written to the address bits and the data bits determine the function addressed. The functions available via the function register are outlined in Table 11 and Table 12.

**Table 11. Function Register Options**

| REG2 | REG1 | REG0 | A2 | A1 | A0 | DB15:DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | NOP, data = don't care | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 1 | Don't care | Local ground offset adjust | D1 direction | D1 value | D0 direction | D0 value | SDO disable |
| 0 | 0 | 0 | 1 | 0 | 0 | Clear, data = don't care | | | | | | |
| 0 | 0 | 0 | 1 | 0 | 1 | Load, data = don't care | | | | | | |

**Table 12. Explanation of Function Register Options**

| Option | Description |
|---|---|
| NOP | No operation instruction used in readback operations. |
| Local Ground Offset Adjust | Set by the user to enable the local ground offset adjust function. Cleared by the user to disable the local ground offset adjust function (default). Refer to the Design Features section for further details. |
| D0/D1 Direction | Set by the user to enable D0/D1 as outputs. Cleared by the user to enable D0/D1 as inputs (default). Refer to the Design Features section for further details. |
| D0/D1 Value | I/O port status bits. Logic values written to these locations determine the logic outputs on the D0 and D1 pins when configured as outputs. These bits indicate the status of the D0 and D1 pins when the I/O port is active as an input. When enabled as inputs, these bits are don't cares during a write operation. |
| SDO Disable | Set by the user to disable the SDO output. Cleared by the user to enable the SDO output (default). |
| Clear | Addressing this function resets the DAC outputs to 0 V in twos complement mode and negative full scale in binary mode. |
| Load | Addressing this function updates the data register and consequently the analog outputs. |

## DATA REGISTER

The data register is addressed by setting the three REG bits to 010. The DAC address bits select with which DAC channel the data transfer is to take place (see Table 10). The data bits are in Position DB15 to Position DB0, as shown in Table 13.

**Table 13. Programming the Data Register Bit Map**

| REG2 | REG1 | REG0 | A2 | A1 | A0 | DB15:DB0 |
|---|---|---|---|---|---|---|
| 0 | 1 | 0 | DAC address | | | 16-bit DAC data |

## COARSE GAIN REGISTER

The coarse gain register is addressed by setting the three REG bits to 011. The DAC address bits select with which DAC channel the data transfer is to take place (see Table 10). The coarse gain register is a 2-bit register and allows the user to select the output range of each DAC, as shown in Table 14 and Table 15.

**Table 14. Programming the Coarse Gain Register Bit Map**

| REG2 | REG1 | REG0 | A2 | A1 | A0 | DB15: DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | DAC address | | | Don't care | CG1 | CG0 |

**Table 15. Output Range Selection**

| Output Range | CG1 | CG0 |
|---|---|---|
| ±10 V (Default) | 0 | 0 |
| ±10.2564 V | 0 | 1 |
| ±10.5263 V | 1 | 0 |

## FINE GAIN REGISTER

The fine gain register is addressed by setting the three REG bits to 100. The DAC address bits select with which DAC channel the data transfer is to take place (see Table 10). The fine gain register is a 6-bit register and allows the user to adjust the gain of each DAC channel by −32 LSBs to +31 LSBs in 1 LSB increments, as shown in Table 16 and Table 17. The adjustment is made to both the positive full-scale points and the negative full-scale points simultaneously, each point being adjusted by ½ of one step. The fine gain register coding is twos complement.

## OFFSET REGISTER

The offset register is addressed by setting the three REG bits to 101. The DAC address bits select with which DAC channel the data transfer is to take place (see Table 10). The AD5764 offset register is an 8-bit register and allows the user to adjust the offset of each channel by −16 LSBs to +15.875 LSBs in increments of ⅛ LSB, as shown in Table 18 and Table 19. The offset register coding is twos complement.

**Table 16. Programming the Fine Gain Register Bit Map**

| REG2 | REG1 | REG0 | A2 | A1 | A0 | DB15:DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | DAC address | | | Don't care | FG5 | FG4 | FG3 | FG2 | FG1 | FG0 |

**Table 17. Fine Gain Register Options**

| Gain Adjustment | FG5 | FG4 | FG3 | FG2 | FG1 | FG0 |
|---|---|---|---|---|---|---|
| +31 LSBs | 0 | 1 | 1 | 1 | 1 | 1 |
| +30 LSBs | 0 | 1 | 1 | 1 | 1 | 0 |
| … | … | … | … | … | … | … |
| +2 LSBs | 0 | 0 | 0 | 0 | 1 | 0 |
| +1 LSB | 0 | 0 | 0 | 0 | 0 | 1 |
| No Adjustment (Default) | 0 | 0 | 0 | 0 | 0 | 0 |
| −1 LSB | 1 | 1 | 1 | 1 | 1 | 1 |
| −2 LSBs | 1 | 1 | 1 | 1 | 1 | 0 |
| … | … | … | … | … | … | … |
| −31 LSBs | 1 | 0 | 0 | 0 | 0 | 1 |
| −32 LSBs | 1 | 0 | 0 | 0 | 0 | 0 |

**Table 18. Programming the Offset Register Bit Map**

| REG2 | REG1 | REG0 | A2 | A1 | A0 | DB15:DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | DAC address | | | Don't care | OF7 | OF6 | OF5 | OF4 | OF3 | OF2 | OF1 | OF0 |

**Table 19. AD5764 Offset Register Options**

| Offset Adjustment | OF7 | OF6 | OF5 | OF4 | OF3 | OF2 | OF1 | OF0 |
|---|---|---|---|---|---|---|---|---|
| +15.875 LSBs | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| +15.75 LSBs | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| … | … | … | … | … | … | … | … | … |
| +0.25 LSBs | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| +0.125 LSBs | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| No Adjustment (Default) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| −0.125 LSBs | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| −0.25 LSBs | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| … | … | … | … | … | … | … | … | … |
| −15.875 LSBs | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| −16 LSBs | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## OFFSET AND GAIN ADJUSTMENT WORKED EXAMPLE

Using the information provided in the Fine Gain Register and Offset Register sections, the following worked example demonstrates how the AD5764 functions can be used to eliminate both offset and gain errors. Because the AD5764 is factory calibrated, offset and gain errors should be negligible. However, errors can be introduced by the system that the AD5764 is operating within; for example, a voltage reference value that is not equal to 5 V introduces a gain error. An output range of ±10 V and twos complement data coding is assumed.

### *Removing Offset Error*

The AD5764 can eliminate an offset error in the range of −4.88 mV to +4.84 mV with a step size of ⅛ of a 16-bit LSB.

Calculate the step size of the offset adjustment.

$$Offset\ Adjust\ Step\ Size = \frac{20}{2^{16} \times 8} = 38.14\ \mu V$$

Measure the offset error by programming 0x0000 to the data register and measuring the resulting output voltage. For this example, the measured value is 614 µV.

Calculate the number of offset adjustment steps that this value represents.

$$Number of\ Steps = \frac{Measured\ Offset\ \ Value}{Offset\ Step\ Size} =$$

$$\frac{614\ \mu V}{38.14\ \mu V} = 16\ \text{Steps}$$

The offset error measured is positive, therefore, a negative adjustment of 16 steps is required. The offset register is eight bits wide and the coding is twos complement. The required offset register value can be calculated as follows:

Convert the adjustment value to binary: 00010000.

Convert this to a negative twos complement number by inverting all bits and adding 1 to obtain 11110000, the value that should be programmed to the offset register.

Note that this twos complement conversion is not necessary in the case of a positive offset adjustment. The value to be programmed to the offset register is simply the binary representation of the adjustment value.

### *Removing Gain Error*

The AD5764 can eliminate a gain error at negative full-scale output in the range of −9.77 mV to +9.46 mV with a step size of ½ of a 16-bit LSB.

Calculate the step size of the gain adjustment.

$$Gain\ Adjust\ Step\ Size = \frac{20}{2^{16} \times 2} = 152.59\ \mu V$$

Measure the gain error by programming 0x8000 to the data register and measuring the resulting output voltage. The gain error is the difference between this value and −10 V. For this example, the gain error is −1.2 mV.

Calculate how many gain adjustment steps this value represents.

$$Number of\ Steps = \frac{Measured\ Gain\ \ Value}{Gain\ \ Step\ \ Size} =$$

$$\frac{1.2\ mV}{152.59\ \mu V} = 8\ \ \text{Steps}$$

The gain error measured is negative (in terms of magnitude); therefore, a positive adjustment of eight steps is required. The gain register is 6 bits wide and the coding is twos complement, the required gain register value can be determined as follows:

Convert the adjustment value to binary: 001000.

The value to be programmed to the gain register is simply this binary number.

# DESIGN FEATURES

## ANALOG OUTPUT CONTROL

In many industrial process control applications, it is vital that the output voltage be controlled during power-up and during brownout conditions. When the supply voltages are changing, the VOUTx pins are clamped to 0 V via a low impedance path. To prevent the output amp being shorted to 0 V during this time, Transmission Gate G1 is also opened (see Figure 35). These conditions are maintained until the power supplies stabilize and a valid word is written to the data register. At this time, G2 opens and G1 closes. Both transmission gates are also externally controllable via the reset logic ($\overline{\text{RSTIN}}$) control input. For instance, if $\overline{\text{RSTIN}}$ is driven from a battery supervisor chip, the $\overline{\text{RSTIN}}$ input is driven low to open G1 and close G2 upon power-down or during a brownout. Conversely, the on-chip voltage detector output ($\overline{\text{RSTOUT}}$) is also available to the user to control other parts of the system. The basic transmission gate functionality is shown in Figure 35.

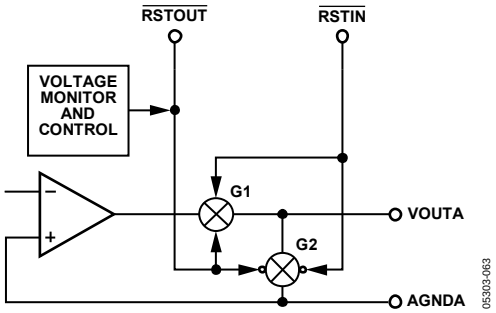



*Figure 35. Analog Output Control Circuitry*

## DIGITAL OFFSET AND GAIN CONTROL

The AD5764 incorporates a digital offset adjust function with a ±16 LSB adjust range and 0.125 LSB resolution. The coarse gain register allows the user to adjust the AD5764 full-scale output range. The full-scale output can be programmed to achieve full-scale ranges of ±10 V, ±10.2564 V, and ±10.5263 V. A fine gain trim is also provided.

## PROGRAMMABLE SHORT-CIRCUIT PROTECTION

The short-circuit current of the output amplifiers can be programmed by inserting an external resistor between the ISCC pin and PGND. The programmable range for the current is 500 μA to 10 mA, corresponding to a resistor range of 120 kΩ to 6 kΩ. The resistor value is calculated as follows:

$$R = \frac{60}{I_{SC}}$$

If the ISCC pin is left unconnected, the short-circuit current limit defaults to 5 mA. Note that limiting the short-circuit current to a small value can affect the slew rate of the output when driving into a capacitive load; therefore, the value of the programmed short circuit should take into account the size of the capacitive load being driven.

## DIGITAL I/O PORT

The AD5764 contains a 2-bit digital I/O port (D1 and D0). These bits can be configured as inputs or outputs independently, and can be driven or have their values read back via the serial interface. The I/O port signals are referenced to $DV_{CC}$ and DGND. When configured as outputs, they can be used as control signals to multiplexers or can be used to control calibration circuitry elsewhere in the system. When configured as inputs, the logic signals from limit switches can, for example, be applied to D0 and D1 and can be read back via the digital interface.

## LOCAL GROUND OFFSET ADJUST

The AD5764 incorporates a local ground offset adjust feature that, when enabled in the function register, adjusts the DAC outputs for voltage differences between the individual DAC ground pins, AGNDx, and the REFGND pin, ensuring that the DAC output voltages are always with respect to the local DAC ground pin. For instance, if Pin AGNDA is at +5 mV with respect to the REFGND pin and VOUTA is measured with respect to AGNDA, a –5 mV error results, enabling the local ground offset adjust feature to adjust VOUTA by +5 mV, eliminating the error.

# APPLICATIONS INFORMATION

## TYPICAL OPERATING CIRCUIT

Figure 36 shows the typical operating circuit for the AD5764. The only external components needed for this precision 16-bit DAC are a reference voltage source, decoupling capacitors on the supply pins and reference inputs, and an optional short-circuit current setting resistor. Because the device incorporates reference buffers, it eliminates the need for an external bipolar reference and associated buffers. This leads to an overall savings in both cost and board space.

In Figure 36, $AV_{DD}$ is connected to +15 V and $AV_{SS}$ is connected to −15 V. However, $AV_{DD}$ can operate with supplies from +11.4 V to +16.5 V and $AV_{SS}$ can operate with supplies from −11.4 V to −16.5 V.

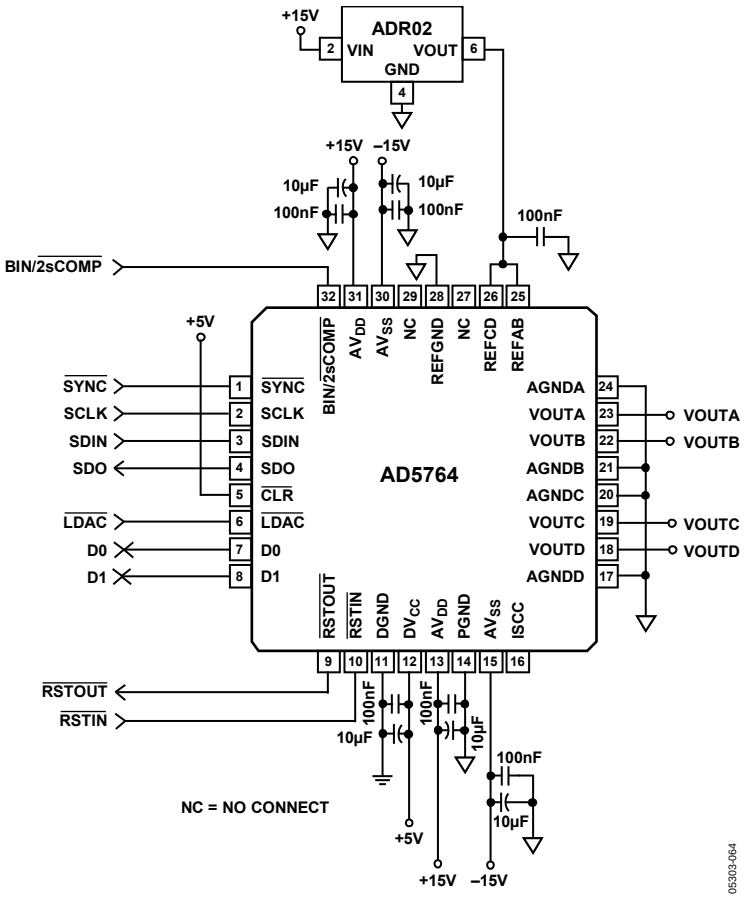



*Figure 36. Typical Operating Circuit*

### *Precision Voltage Reference Selection*

To achieve the optimum performance from the AD5764 over its full operating temperature range, a precision voltage reference must be used. Consideration should be given to the selection of a precision voltage reference. The AD5764 has two reference inputs, REFAB and REFCD. The voltages applied to the reference inputs are used to provide a buffered positive and negative reference for the DAC cores. Therefore, any error in the voltage reference is reflected in the outputs of the device.

There are four possible sources of error to consider when choosing a voltage reference for high accuracy applications: initial accuracy, temperature coefficient of the output voltage, long-term drift, and output voltage noise.

Initial accuracy error on the output voltage of an external reference can lead to a full-scale error in the DAC. Therefore, to minimize these errors, a reference with low initial accuracy error specification is preferred. Choosing a reference with an output trim adjustment, such as the ADR425, allows a system designer to trim system errors out by setting the reference voltage to a voltage other than the nominal. The trim adjustment can also be used at temperature to trim out any error.

Long-term drift is a measure of how much the reference output voltage drifts over time. A reference with a tight long-term drift specification ensures that the overall solution remains relatively stable over its entire lifetime.

The temperature coefficient of a reference output voltage affects INL, DNL, and TUE. Choose a reference with a tight temperature coefficient specification to reduce the dependence of the DAC output voltage on ambient conditions.

In high accuracy applications, which have a relatively low noise budget, reference output voltage noise needs to be considered. Choosing a reference with as low an output noise voltage as practical for the system resolution required is important. Precision voltage references such as the ADR435 (XFET® design) produce low output noise in the 0.1 Hz to 10 Hz region. However, as the circuit bandwidth increases, filtering the output of the reference may be required to minimize the output noise.

**Table 20. Some Precision References Recommended for Use with the AD5764**

| Part No. | Initial Accuracy (mV Max) | Long-Term Drift (ppm Typ) | Temp Drift (ppm/°C Max) | 0.1 Hz to 10 Hz Noise (μV p-p Typ) |
|---|---|---|---|---|
| ADR435 | ±2 | 40 | 3 | 8 |
| ADR425 | ±2 | 50 | 3 | 3.4 |
| ADR02 | ±5 | 50 | 3 | 10 |
| ADR395 | ±5 | 50 | 9 | 8 |

# LAYOUT GUIDELINES

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The PCB on which the AD5764 is mounted must be designed so that the analog and digital sections are separated and confined to certain areas of the board. If the AD5764 is in a system where multiple devices require an AGND-to-DGND connection, the connection is to be made at one point only. The star ground point is established as close as possible to the device. The AD5764 must have ample supply bypassing of 10 µF in parallel with 0.1 µF on each supply, located as close to the package as possible, ideally right up against the device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor must have low effective series resistance (ESR) and low effective series inductance (ESI), such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

The power supply lines of the AD5764 must be as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals, such as clocks, must be shielded with digital ground to avoid radiating noise to other parts of the board, and must never be run near the reference inputs. A ground line routed between the SDIN and SCLK lines helps reduce crosstalk between them (not required on a multilayer board, which has a separate ground plane; however, it is helpful to separate the lines). It is essential to minimize noise on the reference inputs because it couples through to the DAC output. Avoid crossover of digital and analog signals. Traces on opposite sides of the board must run at right angles to each other. This reduces the effects of feedthrough on the board. A microstrip technique is recommended, but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to the ground plane, and signal traces are placed on the solder side.

## GALVANICALLY ISOLATED INTERFACE

In many process control applications, it is necessary to provide an isolation barrier between the controller and the unit being controlled to protect and isolate the controlling circuitry from any hazardous common-mode voltages that may occur. Isocouplers provide voltage isolation in excess of 2.5 kV. The serial loading structure of the AD5764 makes it ideal for isolated interfaces because the number of interface lines is kept to a minimum. Figure 37 shows a 4-channel isolated interface to the AD5764 using an ADuM1400. For more information, go to www.analog.com.

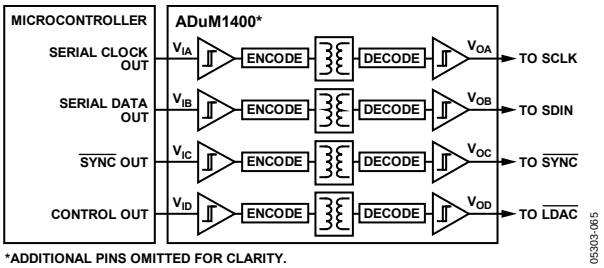



*Figure 37. Isolated Interface*

## MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD5764 is via a serial bus that uses a standard protocol that is compatible with microcontrollers and DSP processors. The communications channel is a 3-wire (minimum) interface consisting of a clock signal, a data signal, and a synchronization signal. The AD5764 requires a 24-bit data-word with data valid on the falling edge of SCLK.

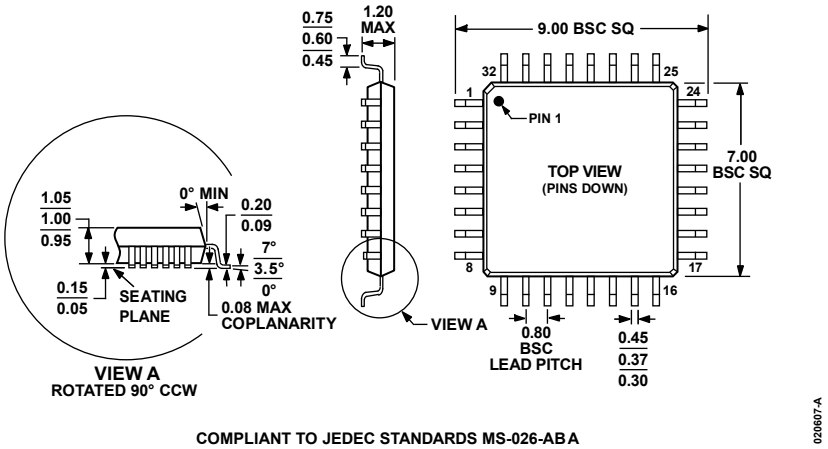
For all the interfaces, the DAC output update can be performed automatically when all the data is clocked in, or it can be done under the control of LDAC. The contents of the data register can be read using the readback function.

## EVALUATION BOARD

The AD5764 comes with a full evaluation board to aid designers in evaluating the high performance of the part with minimum effort. All that is required with the evaluation board is a power supply and a PC. The AD5764 evaluation kit includes a populated, tested AD5764 PCB. The evaluation board interfaces to the USB port of the PC. Software is available with the evaluation board, which allows the user to easily program the AD5764. The software runs on any PC that has Microsoft® Windows® 2000/NT/XP installed.

The EVAL-AD5764EB data sheet is available, which gives full details on the operation of the evaluation board.

# OUTLINE DIMENSIONS




COMPLIANT TO JEDEC STANDARDS MS-026-ABA

*Figure 38. 32-Lead Thin Plastic Quad Flat Package [TQFP]*
*(SU-32-2)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | INL | Temperature Range | Package Description | Package Option |
|---|---|---|---|---|
| AD5764ASUZ | ±4 LSB max | −40°C to +85°C | 32-Lead TQFP | SU-32-2 |
| AD5764ASUZ-REEL7 | ±4 LSB max | −40°C to +85°C | 32-Lead TQFP | SU-32-2 |
| AD5764BSUZ | ±2 LSB max | −40°C to +85°C | 32-Lead TQFP | SU-32-2 |
| AD5764BSUZ-REEL7 | ±2 LSB max | −40°C to +85°C | 32-Lead TQFP | SU-32-2 |
| AD5764CSUZ | ±1 LSB max | −40°C to +85°C | 32-Lead TQFP | SU-32-2 |
| AD5764CSUZ-REEL7 | ±1 LSB max | −40°C to +85°C | 32-Lead TQFP | SU-32-2 |
| EVAL-AD5764EBZ | | | Evaluation Board | |

[1] Z = RoHS Compliant Part.