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1 Block diagram and pin description

Figure 1. Block diagram

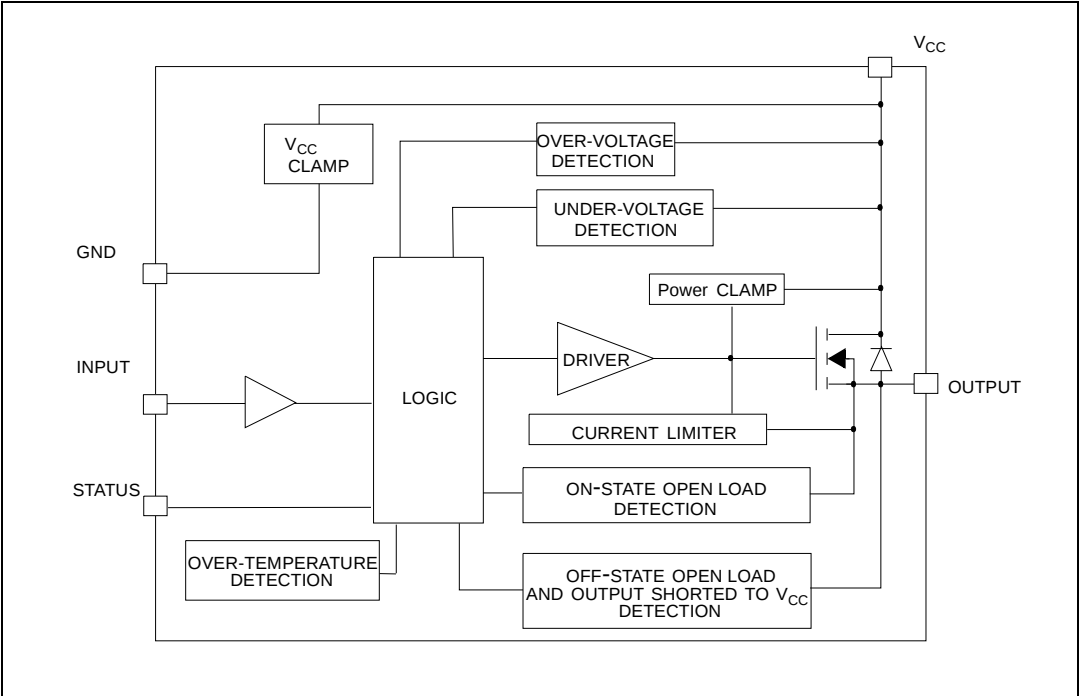


Figure 2. Configuration diagram (top view)

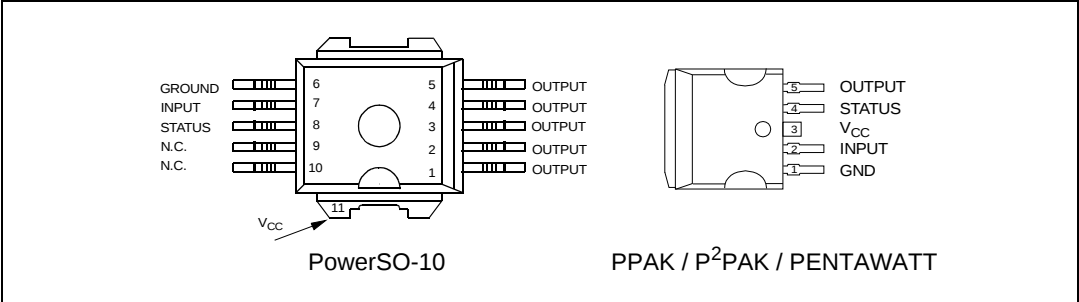
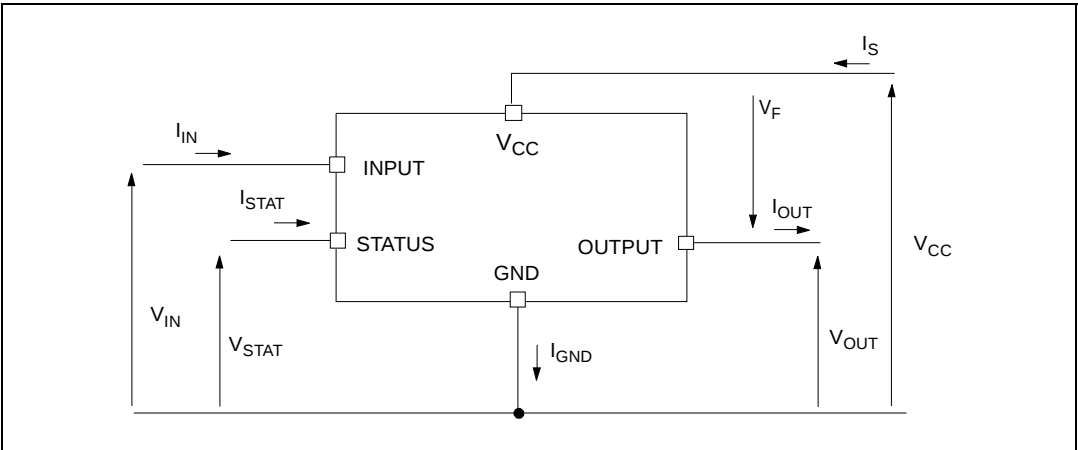


Table 2. Suggested connections for unused and not connected pins

Connection / pin	Status	N.C.	Output	Input
Floating	X	X	X	X
To ground		X		Through 10 KΩ resistor

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Stressing the device above the rating listed in the [Table 3](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to Absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value				Unit
		PowerSO-10	PENTAWATT	P ² PAK	PPAK	
V_{CC}	DC supply voltage	41				V
$-V_{CC}$	Reverse DC supply voltage	- 0.3				V
$-I_{gnd}$	DC reverse ground pin current	- 200				mA
I_{OUT}	DC output current	Internally limited				A
$-I_{OUT}$	Reverse DC output current	- 9				A
I_{IN}	DC input current	+/- 10				mA
I_{STAT}	DC Status current	+/- 10				mA
V_{ESD}	Electrostatic discharge (human body model: $R = 1.5\text{ K}\Omega$; $C = 100\text{ pF}$)					
	– INPUT	4000				V
	– STATUS	4000				V
	– OUTPUT	5000				V
	– V_{CC}	5000				V

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value				Unit
		PowerSO-10	PENTAWATT	P ² PAK	PPAK	
E_{MAX}	Maximum switching energy ($L = 1.4 \text{ mH}$; $R_L = 0 \text{ }\Omega$; $V_{bat} = 13.5 \text{ V}$; $T_{jstart} = 150^\circ\text{C}$; $I_L = 13 \text{ A}$)	156				mJ
P_{tot}	Power dissipation $T_C = 25^\circ\text{C}$	65.8				W
T_j	Junction operating temperature	Internally limited				$^\circ\text{C}$
T_c	Case operating temperature	-40 to 150				$^\circ\text{C}$
T_{stg}	Storage temperature	-55 to 150				$^\circ\text{C}$

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Max. value				Unit
		PowerSO-10	PENTAWATT	P ² PAK	PPAK	
$R_{thj-case}$	Thermal resistance junction-case	1.9	1.9	1.9	1.9	$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	51.9 ⁽¹⁾	61.9 ⁽²⁾	51.9 ⁽²⁾	76.9 ⁽²⁾	$^\circ\text{C/W}$
		37 ⁽²⁾	-	37 ⁽⁴⁾	45 ⁽⁴⁾	$^\circ\text{C/W}$

1. When mounted on a standard single-sided FR-4 board with 0.5 cm^2 of Cu (at least $35 \text{ }\mu\text{m}$ thick).
2. When mounted on a standard single-sided FR-4 board with 6 cm^2 of Cu (at least $35 \text{ }\mu\text{m}$ thick).

2.3 Electrical characteristics

Values specified in this section are for $8\text{ V} < V_{CC} < 36\text{ V}$; $-40^{\circ}\text{C} < T_j < 150^{\circ}\text{C}$, unless otherwise stated.

Table 5. Power

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		5.5	13	36	V
V_{USD}	Under-voltage shutdown		3	4	5.5	V
$V_{USDhyst}$	Under-voltage shutdown hysteresis			0.5		V
V_{OV}	Over-voltage shutdown		36			V
R_{ON}	On-state resistance	$I_{OUT} = 3\text{ A}$; $T_j = 25^{\circ}\text{C}$; $V_{CC} > 8\text{ V}$			40	m Ω
		$I_{OUT} = 3\text{ A}$; $V_{CC} > 8\text{ V}$			80	m Ω
I_S	Supply current	Off-state; $V_{CC} = 13\text{ V}$; $V_{IN} = V_{OUT} = 0\text{ V}$		10	25	μA
		Off-state; $V_{CC} = 13\text{ V}$; $V_{IN} = V_{OUT} = 0\text{ V}$; $T_j = 25^{\circ}\text{C}$		10	20	μA
		On-state; $V_{CC} = 13\text{ V}$; $V_{IN} = 5\text{ V}$; $I_{OUT} = 0\text{ A}$		2	3.5	mA
$I_{L(off1)}$	Off-state output current	$V_{IN} = V_{OUT} = 0\text{ V}$	0		50	μA
$I_{L(off2)}$	Off-state output current	$V_{IN} = 0\text{ V}$; $V_{OUT} = 3.5\text{ V}$	-75		0	μA
$I_{L(off3)}$	Off-state output current	$V_{IN} = V_{OUT} = 0\text{ V}$; $V_{CC} = 13\text{ V}$; $T_j = 125^{\circ}\text{C}$			5	μA
$I_{L(off4)}$	Off-state output current	$V_{IN} = V_{OUT} = 0\text{ V}$; $V_{CC} = 13\text{ V}$; $T_j = 25^{\circ}\text{C}$			3	μA

Table 6. Switching ($V_{CC}=13\text{V}$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$R_L = 4.3\text{ }\Omega$ from V_{IN} rising edge to $V_{OUT} = 1.3\text{ V}$		30		μs
$t_{d(off)}$	Turn-off delay time	$R_L = 4.3\text{ }\Omega$ from V_{IN} falling edge to $V_{OUT} = 11.7\text{ V}$		30		μs
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	$R_L = 4.3\text{ }\Omega$ from $V_{OUT} = 1.3\text{ V}$ to $V_{OUT}=10.4\text{ V}$	See Figure 21			V/ μs
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	$R_L = 4.3\text{ }\Omega$ from $V_{OUT} = 11.7\text{ V}$ to $V_{OUT} = 1.3\text{ V}$	See Figure 22			V/ μs

Table 7. Input pin

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level				1.25	V
I_{IL}	Low level input current	$V_{IN} = 1.25\text{ V}$	1			μA

Table 7. Input pin (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IH}	Input high level		3.25			V
I_{IH}	High level input current	$V_{IN} = 3.25\text{ V}$			10	μA
V_{hyst}	Input hysteresis voltage		0.5			V
V_{ICL}	Input clamp voltage	$I_{IN} = 1\text{ mA}$	6	6.8	8	V
		$I_{IN} = -1\text{ mA}$		-0.7		V

Table 8. V_{CC} output diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_F	Forward on voltage	$-I_{OUT} = 2\text{ A}$; $T_J = 150^\circ\text{C}$	—	—	0.6	V

Table 9. Status pin

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{STAT}	Status low output voltage	$I_{STAT} = 1.6\text{ mA}$			0.5	V
I_{LSTAT}	Status leakage current	Normal operation; $V_{STAT} = 5\text{ V}$			10	μA
C_{STAT}	Status pin input capacitance	Normal operation; $V_{STAT} = 5\text{ V}$			100	pF
V_{SCL}	Status clamp voltage	$I_{STAT} = 1\text{ mA}$	6	6.8	8	V
		$I_{STAT} = -1\text{ mA}$		-0.7		V

Table 10. Protections⁽¹⁾

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{TSD}	Shutdown temperature		150	175	200	$^\circ\text{C}$
T_R	Reset temperature		135			$^\circ\text{C}$
T_{hyst}	Thermal hysteresis		7	15		$^\circ\text{C}$
t_{SDL}	Status delay in over-load condition	$T_J > T_{jsh}$			20	ms
I_{lim}	Current limitation	$9\text{ V} < V_{CC} < 36\text{ V}$	9	13	20	A
		$5.5\text{ V} < V_{CC} < 36\text{ V}$			20	A
V_{demag}	Turn-off output clamp voltage	$I_{OUT} = 3\text{ A}$; $V_{IN} = 0\text{ V}$; $L = 6\text{ mH}$	$V_{CC} - 41$	$V_{CC} - 48$	$V_{CC} - 55$	V

1. To ensure long term reliability under heavy over-load or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device operates under abnormal conditions this software must limit the duration and number of activation cycles.

Table 11. Open-load detection

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{OL}	Open-load on-state detection threshold	$V_{IN} = 5\text{ V}$	70	150	300	mA
$t_{DOL(on)}$	Open-load on-state detection delay	$I_{OUT} = 0\text{ A}$			200	μs
V_{OL}	Open-load off-state voltage detection threshold	$V_{IN} = 0\text{ V}$	1.5	2.5	3.5	V
$t_{DOL(off)}$	Open-load detection delay at turn-off				1000	μs

Figure 4. Status timings

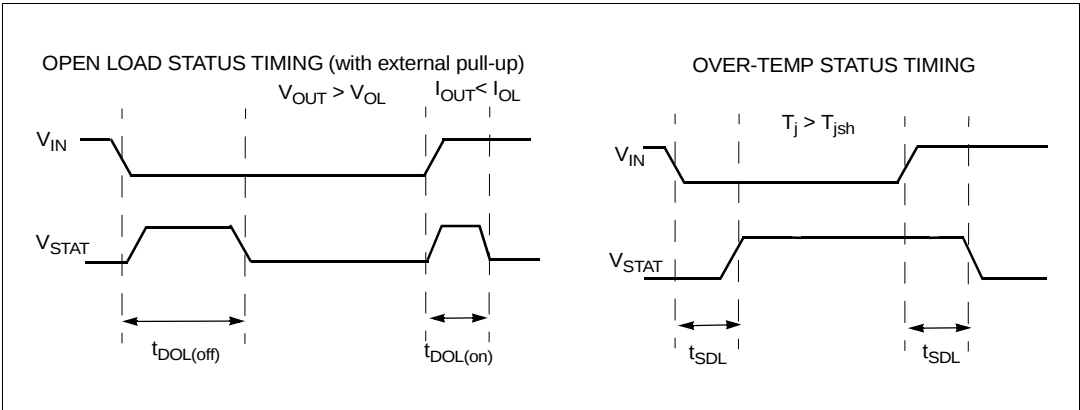


Figure 5. Switching time waveforms

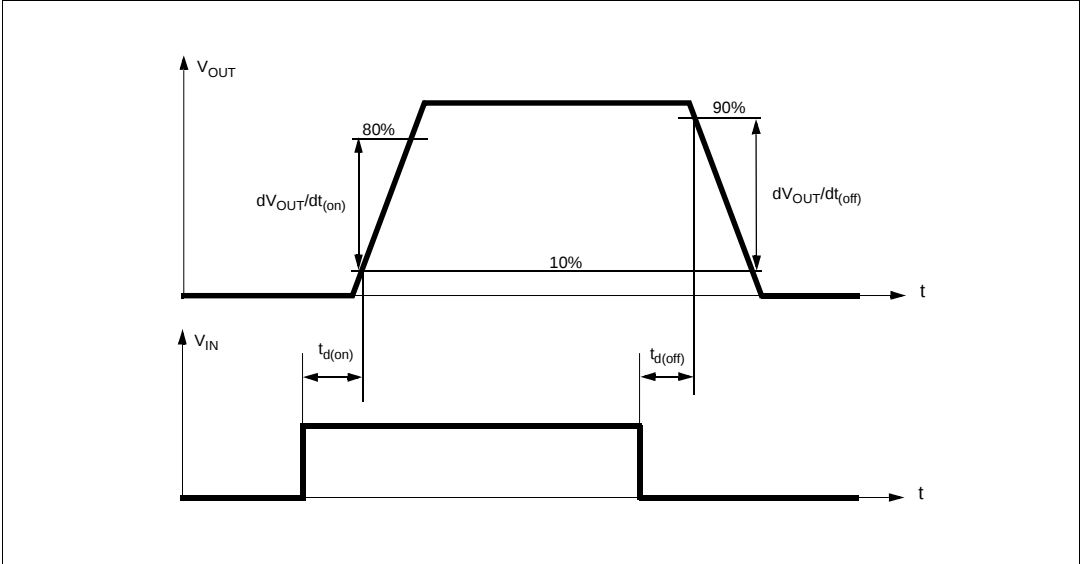


Table 12. Truth table

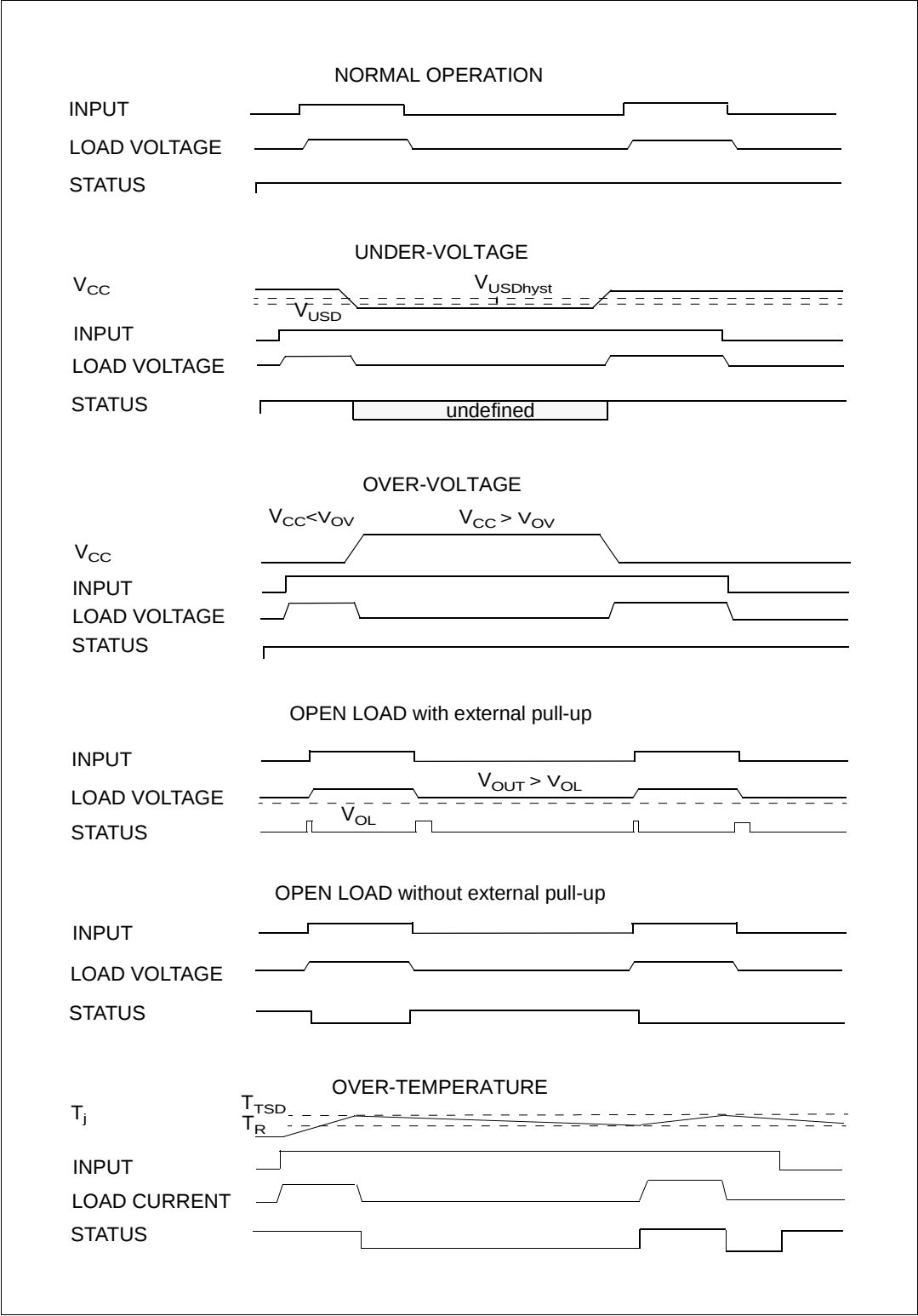
Conditions	Input	Output	Status
Normal operation	L	L	H
	H	H	H
Current limitation	L	L	H
	H	X	$(T_j < T_{TSD})$ H
	H	X	$(T_j > T_{TSD})$ L
Over-temperature	L	L	H
	H	L	L
Under-voltage	L	L	X
	H	L	X
Over-voltage	L	L	H
	H	L	H
Output voltage > V_{OL}	L	H	L
	H	H	H
Output current < I_{OL}	L	L	H
	H	H	L

Table 13. Electrical transient requirements

ISO T/R 7637/1 Test pulse	Test level				
	I	II	III	IV	Delays and impedance
1	- 25V ⁽¹⁾	- 50V ⁽¹⁾	- 75V ⁽¹⁾	- 100V ⁽¹⁾	2ms, 10Ω
2	+ 25V ⁽¹⁾	+ 50V ⁽¹⁾	+ 75V ⁽¹⁾	+ 100V ⁽¹⁾	0.2ms, 10Ω
3a	- 25V ⁽¹⁾	- 50V ⁽¹⁾	- 100V ⁽¹⁾	- 150V ⁽¹⁾	0.1μs, 50Ω
3b	+ 25V ⁽¹⁾	+ 50V ⁽¹⁾	+ 75V ⁽¹⁾	+ 100V ⁽¹⁾	0.1μs, 50Ω
4	- 4V ⁽¹⁾	- 5V ⁽¹⁾	- 6V ⁽¹⁾	- 7V ⁽¹⁾	100ms, 0.01Ω
5	+ 26.5V ⁽¹⁾	+ 46.5V ⁽²⁾	+ 66.5V ⁽²⁾	+ 86.5V ⁽²⁾	400ms, 2Ω

1. All functions of the device are performed as designed after exposure to disturbance.
2. One or more functions of the device is not performed as designed after exposure and cannot be returned to proper operation without replacing the device.

Figure 6. Waveforms



2.4 Electrical characteristics curves

Figure 7. Off-state output current

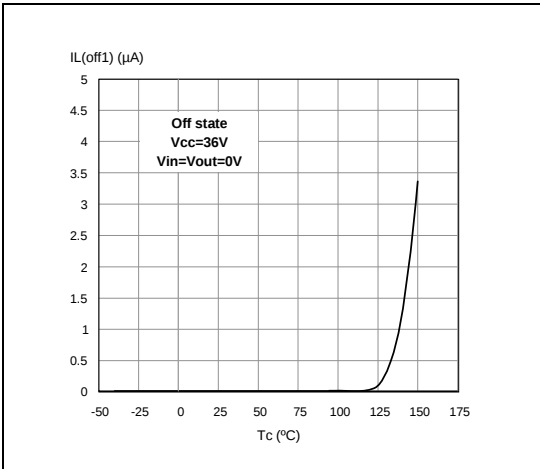


Figure 8. High level input current

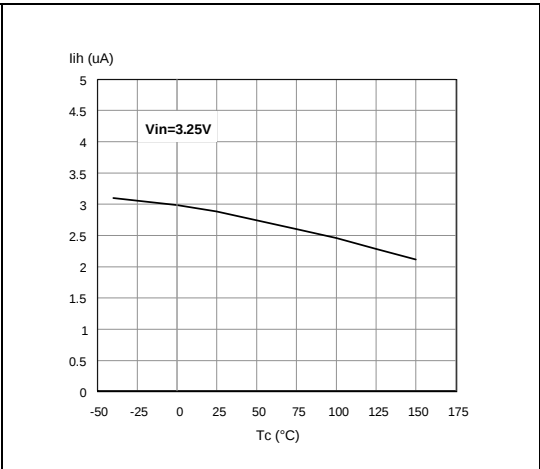


Figure 9. Input clamp voltage

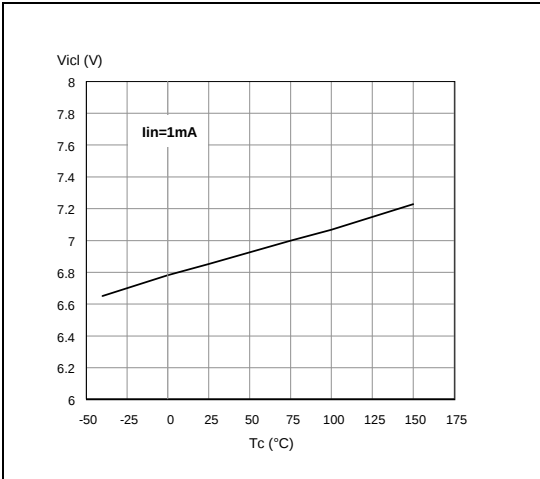


Figure 10. Status leakage current

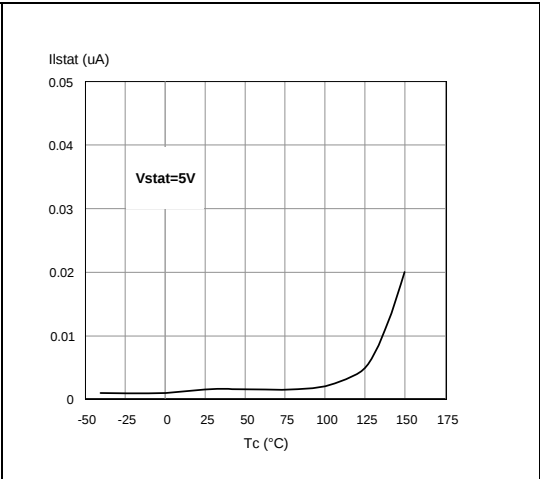


Figure 11. Status low output voltage

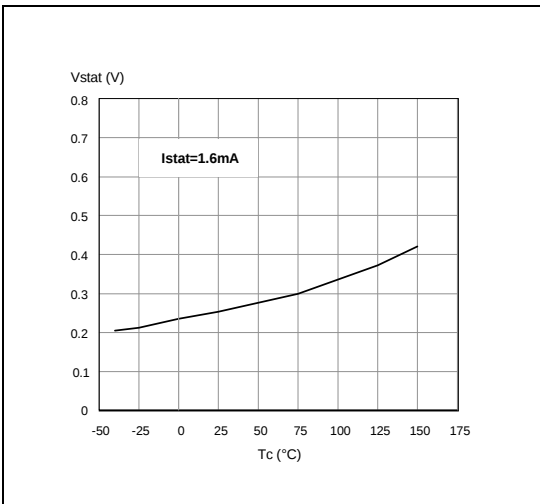


Figure 12. Status clamp voltage

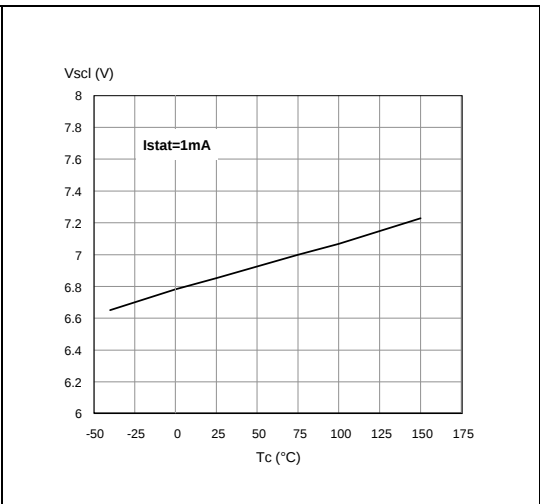


Figure 13. On-state resistance Vs T_{case}

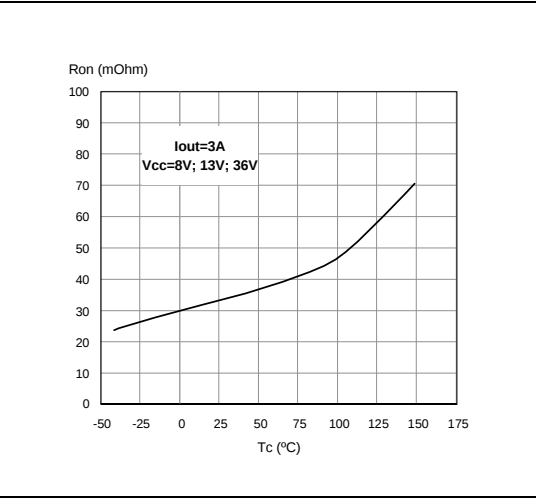


Figure 14. On-state resistance Vs V_{CC}

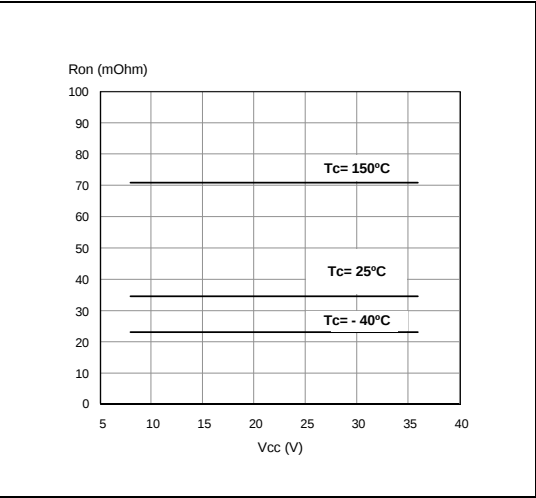


Figure 15. Open load on-state detection threshold

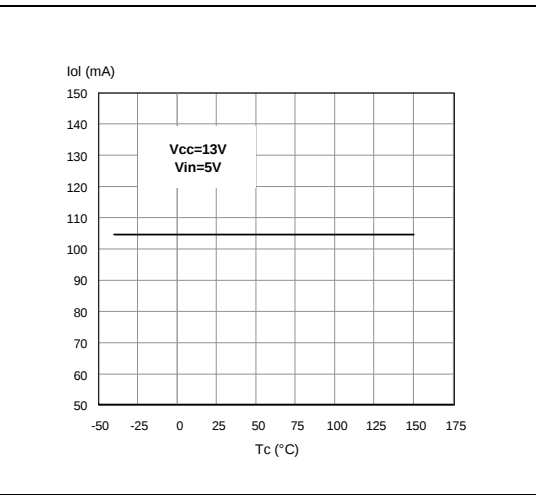


Figure 16. Input high level

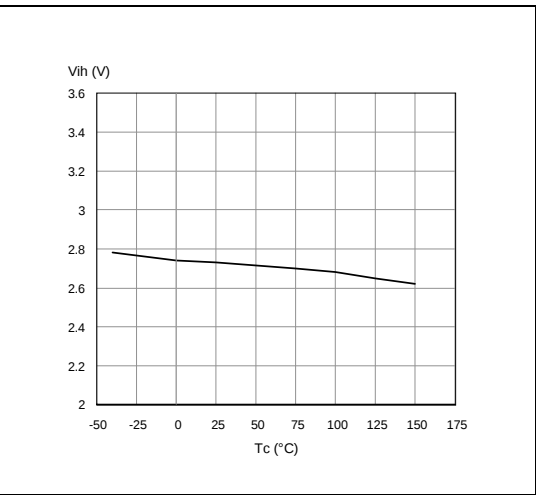


Figure 17. Input low level

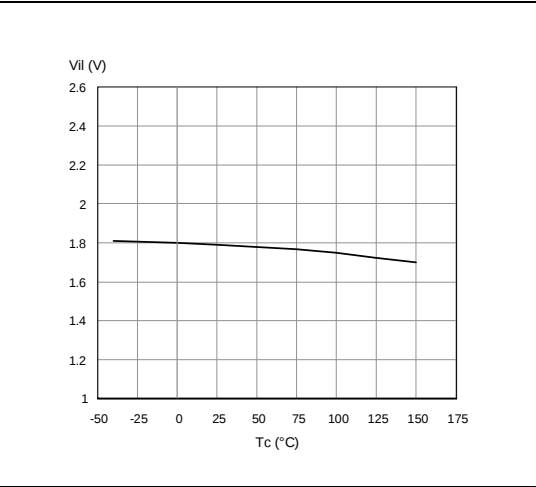


Figure 18. Input hysteresis voltage

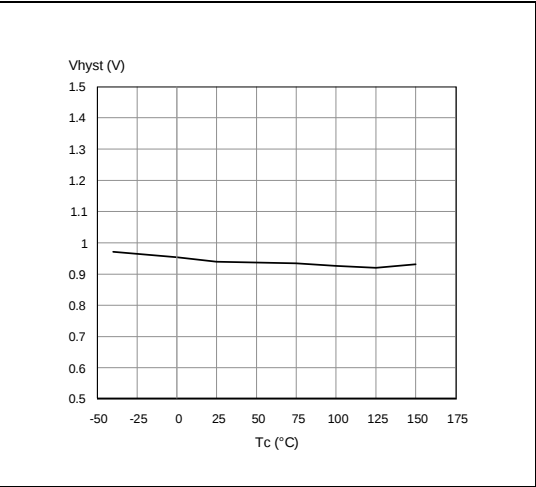


Figure 19. Over-voltage shutdown

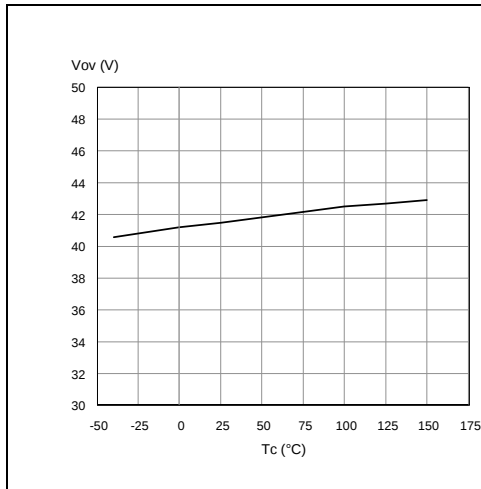


Figure 20. Open load off-state voltage detection threshold

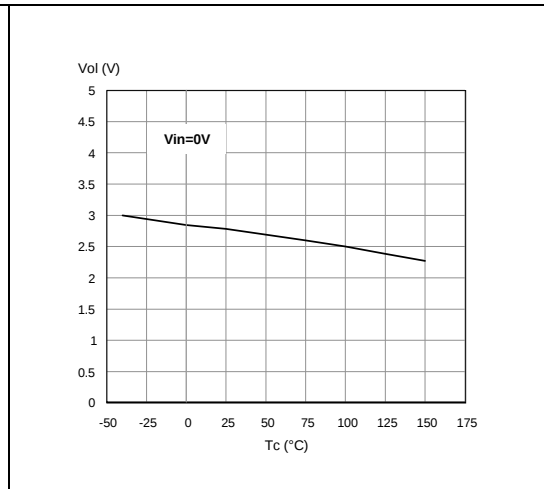


Figure 21. Turn-on voltage slope

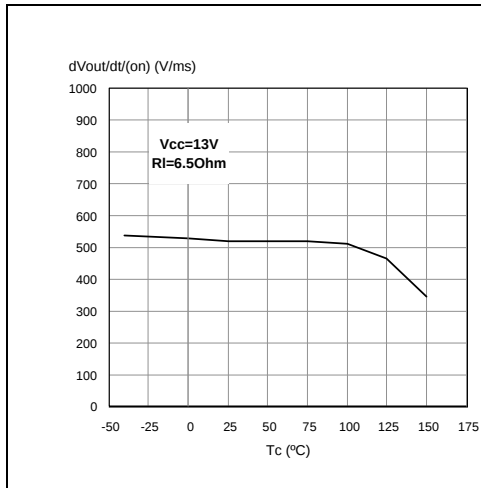
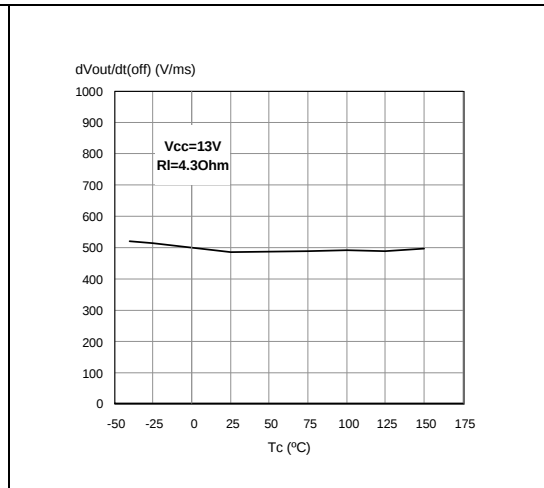
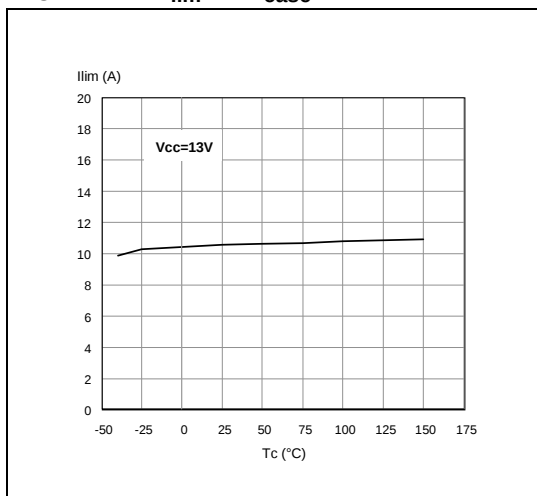
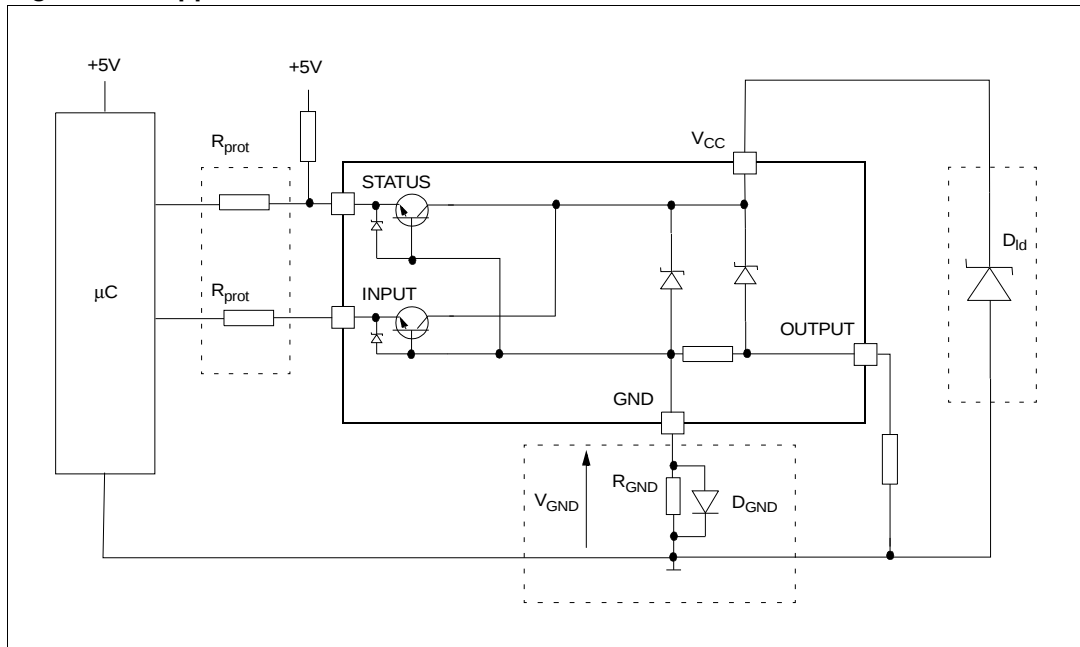


Figure 22. Turn-off voltage slope

Figure 23. I_{lim} Vs T_{case} 

3 Application information

Figure 24. Application schematic



3.1 GND protection network against reverse battery

3.1.1 Solution 1: resistor in the ground line (R_{GND} only)

This can be used with any type of load.

The following is an indication on how to size the R_{GND} resistor.

1. $R_{GND} \leq 600 \text{ mV} / (I_{S(on)max})$
2. $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power Dissipation in R_{GND} (when $V_{CC} < 0$: during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R_{GND} will produce a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high-side drivers sharing the same R_{GND} .

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to utilize Solution 2 (see below).

3.1.2 Solution 2: diode (D_{GND}) in the ground line

A resistor ($R_{GND} = 1\text{ k}\Omega$) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network produces a shift ($\approx 600\text{ mV}$) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift does not vary if more than one HSD shares the same diode/resistor network.

Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the absolute maximum rating.

Safest configuration for unused INPUT and STATUS pin is to leave them unconnected.

3.2 Load dump protection

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the V_{CC} max DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO 7637-2: 2004(E) table.

3.3 MCU I/Os protection

If a ground protection network is used and negative transient are present on the V_{CC} line, the control pins are pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the microcontroller I/O pins from latching-up.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os.

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

For $V_{CCpeak} = -100\text{V}$ and $I_{latchup} \geq 20\text{mA}$; $V_{OH\mu C} \geq 4.5\text{V}$

$$5\text{k}\Omega \leq R_{prot} \leq 65\text{k}\Omega.$$

Recommended values: $R_{prot} = 10\text{k}\Omega$.

3.4 Open load detection in off-state

Off-state open load detection requires an external pull-up resistor (R_{PU}) connected between OUTPUT pin and a positive supply voltage (V_{PU}) like the +5V line used to supply the microprocessor.

The external resistor has to be selected according to the following requirements:

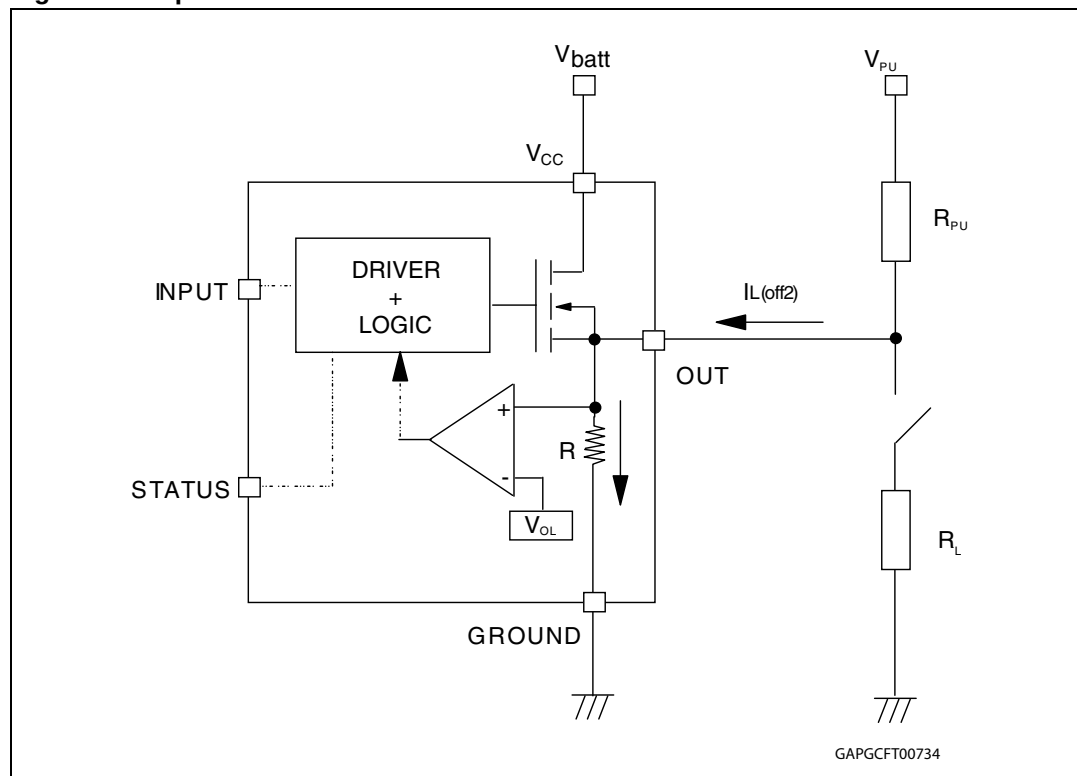
1. no false open load indication when load is connected: in this case we have to avoid V_{OUT} to be higher than V_{OLmin} ; this results in the following condition

$$V_{OUT} = (V_{PU} / (R_L + R_{PU})) R_L < V_{OLmin}$$
2. no misdetection when load is disconnected: in this case the V_{OUT} has to be higher than V_{OLmax} ; this results in the following condition $R_{PU} < (V_{PU} - V_{OLmax}) / I_{L(off2)}$.

Because $I_{S(OFF)}$ may significantly increase if V_{out} is pulled high (up to several mA), the pull-up resistor R_{PU} should be connected to a supply that is switched off when the module is in standby.

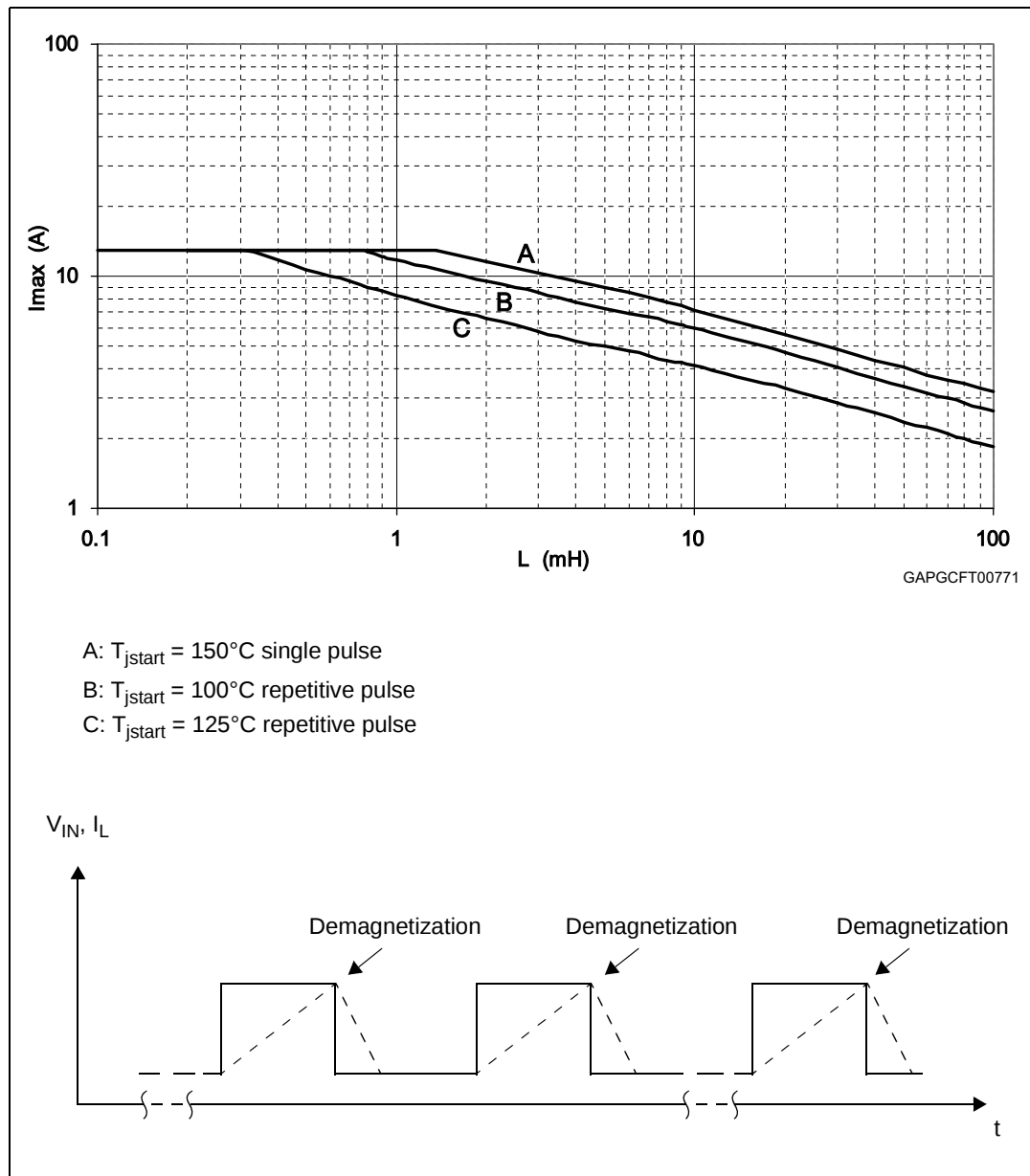
The values of V_{OLmin} , V_{OLmax} and $I_{L(off2)}$ are available in the electrical characteristics section.

Figure 25. Open load detection in off-state



3.5 PowerSO-10, P²PAK, PPAK, PENTAWATT maximum demagnetization energy ($V_{CC} = 13.5V$)

Figure 26. PowerSO-10, P²PAK, PPAK, PENTAWATT maximum turn-off current versus inductance



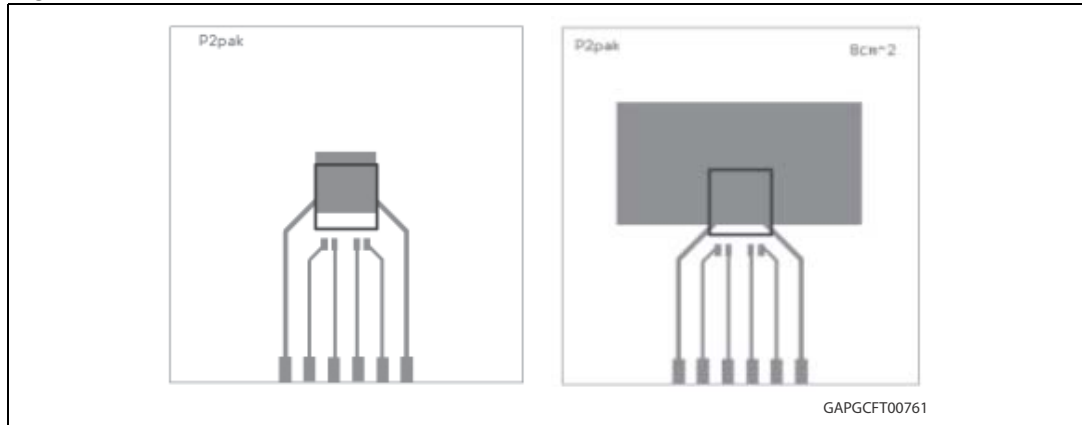
Note:

Values are generated with $R_L = 0 \Omega$. In case of repetitive pulses, T_{jstart} (at the beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and PCB thermal data

4.1 P²PAK thermal data

Figure 27. PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 60 mm x 60 mm, PCB thickness = 2 mm, Cu thickness = 35 μ m, Copper areas: 0.97 cm², 8 cm²).

Figure 28. $R_{thj-amb}$ vs PCB copper area in open box free air condition

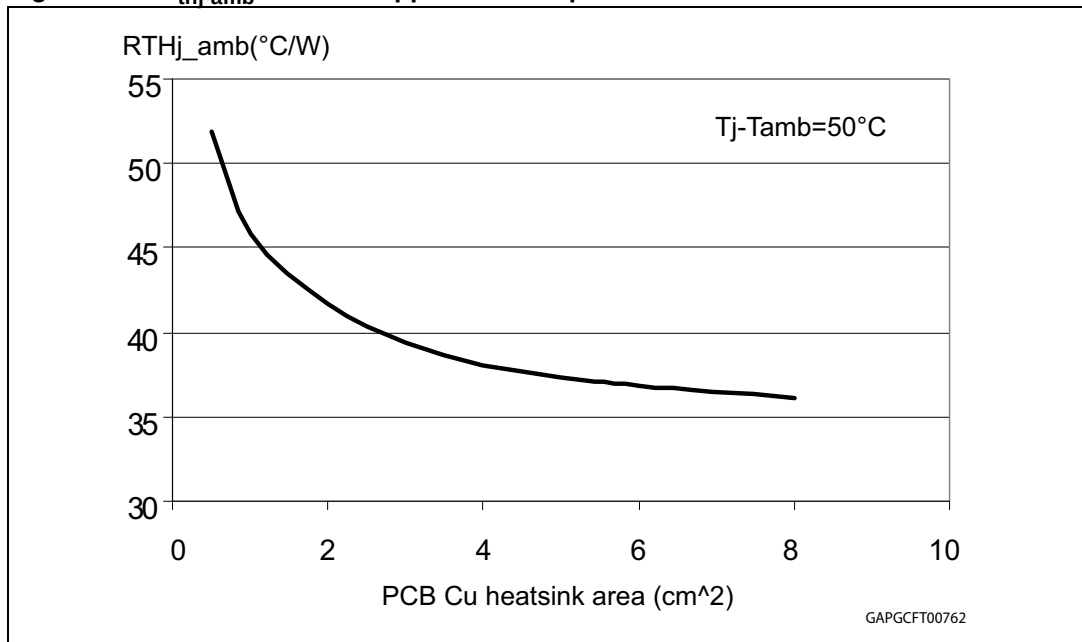
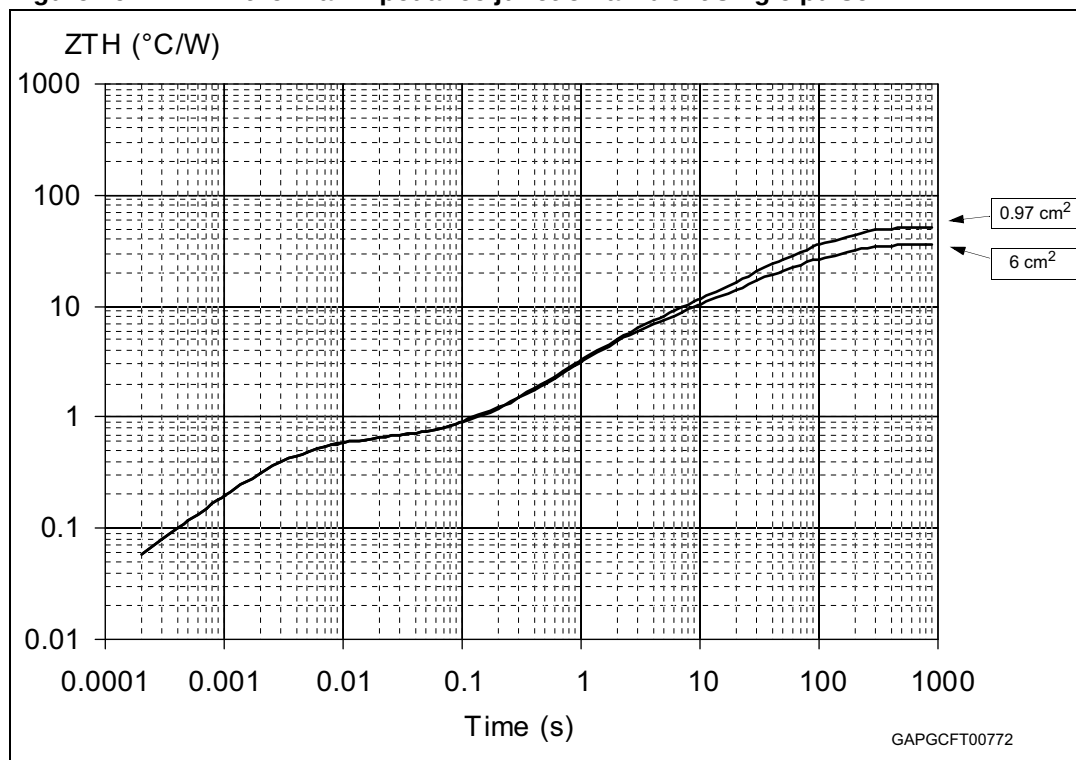


Figure 29. P²PAK thermal impedance junction ambient single pulse

Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Figure 30. Thermal fitting model of a single channel

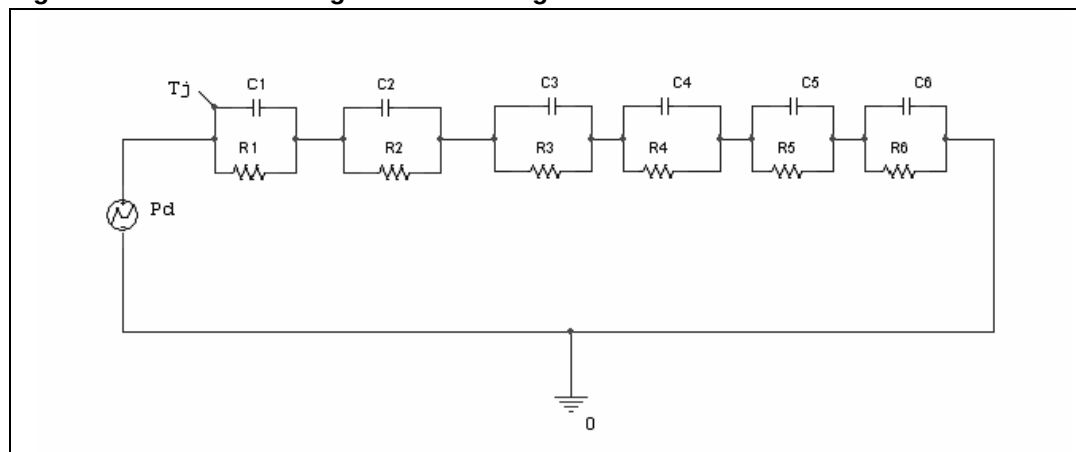
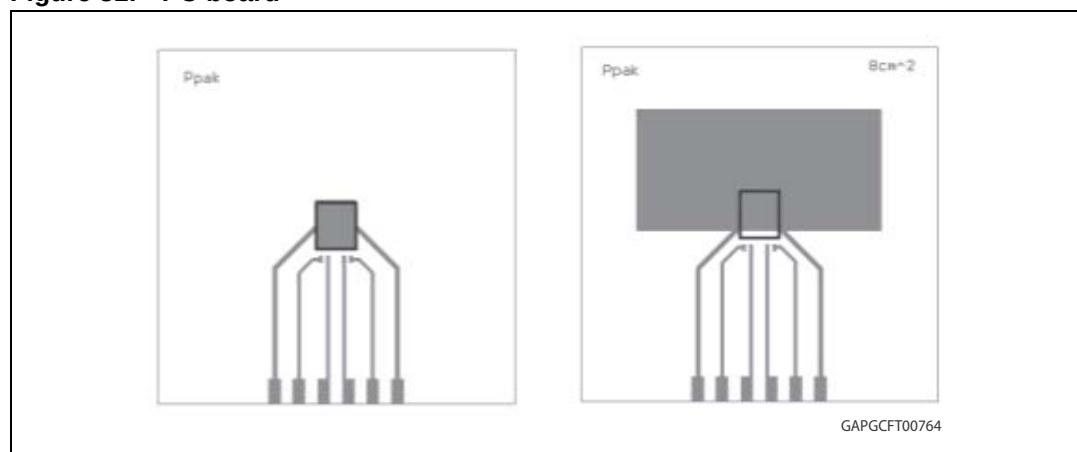


Table 14. Thermal parameter

Area/island (cm ²)	0.97	6
R1 (°C/W)	0.04	
R2 (°C/W)	0.25	
R3 (°C/W)	0.3	
R4 (°C/W)	4	
R5 (°C/W)	9	
R6 (°C/W)	37	22
C1 (W·s/°C)	0.0008	
C2 (W·s/°C)	0.007	
C3 (W·s/°C)	0.015	
C4 (W·s/°C)	0.4	
C5 (W·s/°C)	2	
C6 (W·s/°C)	3	5

4.2 PPAK thermal data

Figure 31. PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 60 mm x 60 mm, PCB thickness = 2 mm, Cu thickness=35 μ m, Copper areas: 0.44 cm², 8 cm²).

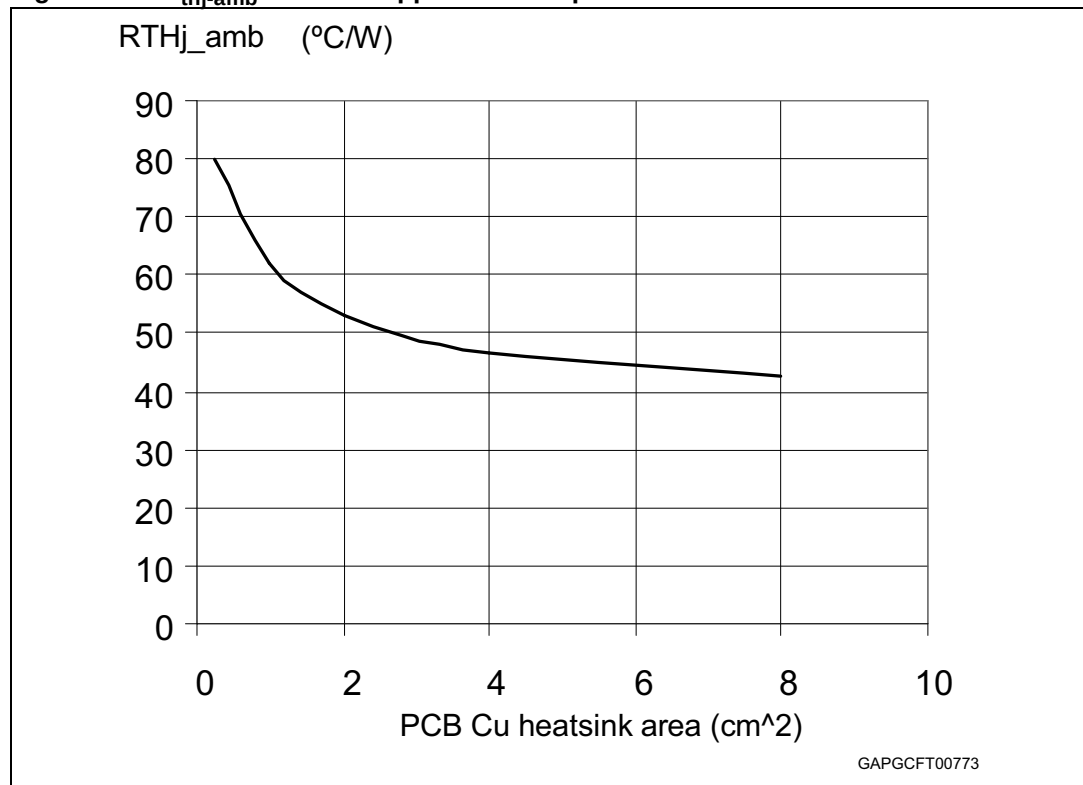
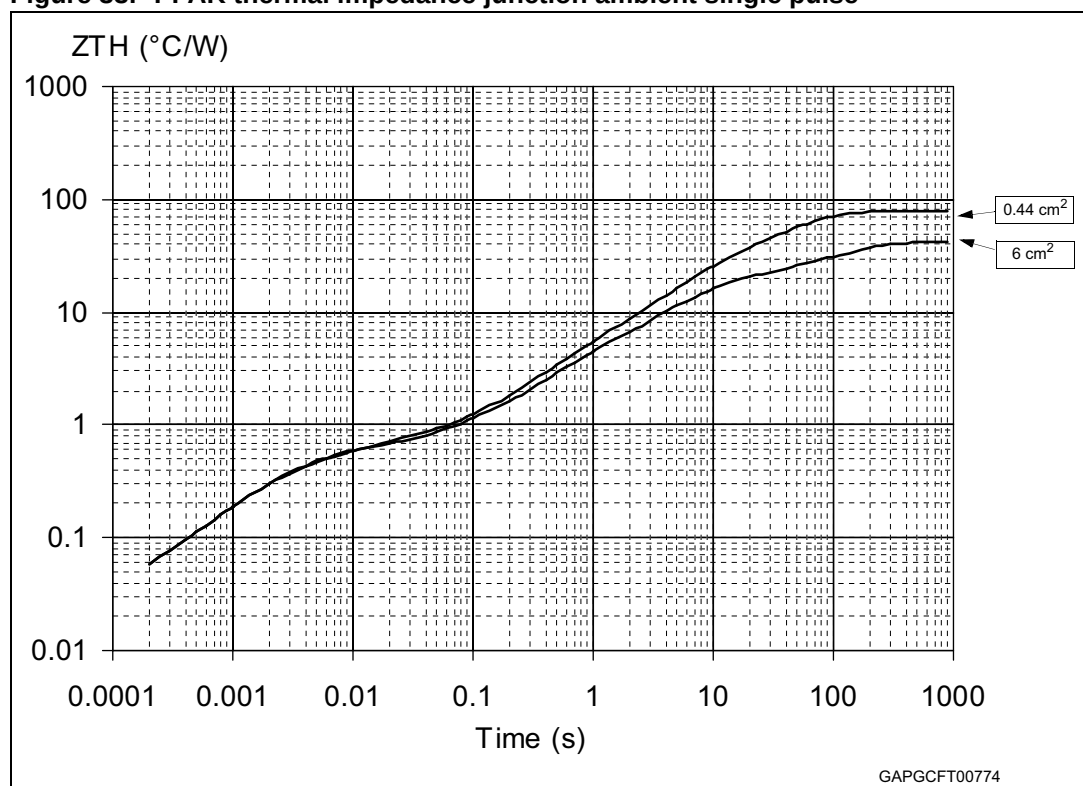
Figure 32. $R_{thj-amb}$ vs PCB copper area in open box free air condition

Figure 33. PPAK thermal impedance junction ambient single pulse



Equation 2: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Figure 34. Thermal fitting model of a single channel

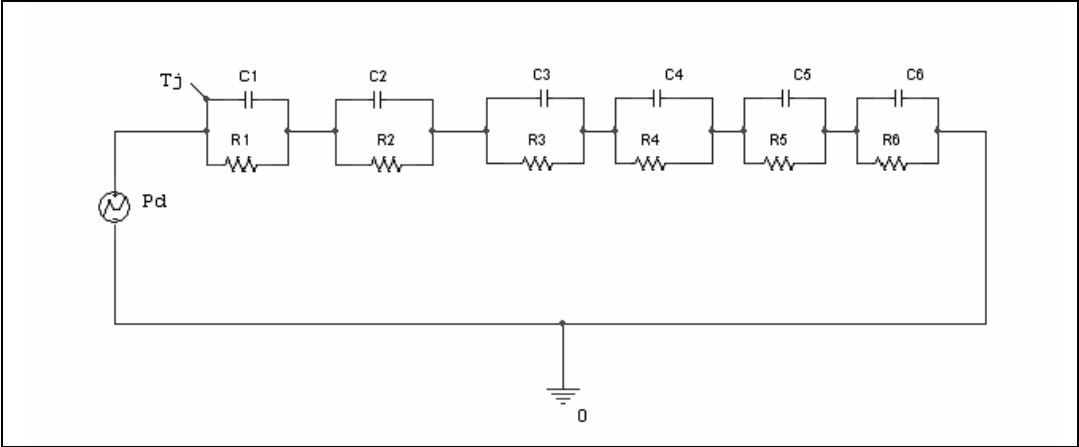
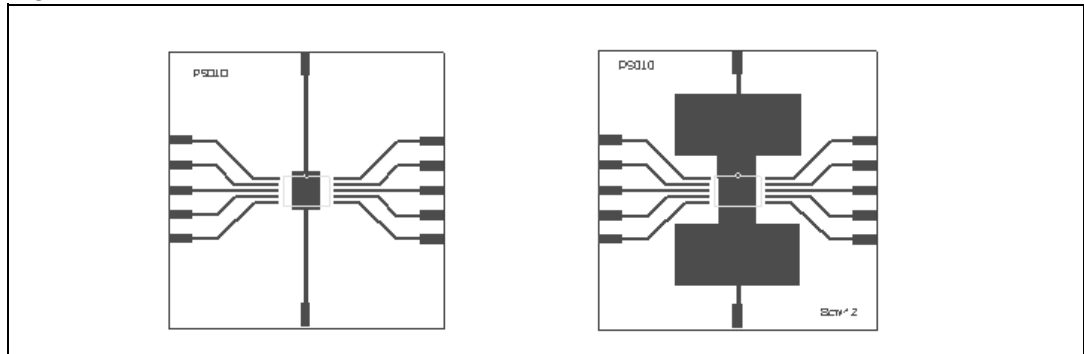


Table 15. Thermal parameter

Area/island (cm ²)	0.44	6
R1 (°C/W)	0.04	
R2 (°C/W)	0.25	
R3 (°C/W)	0.3	
R4 (°C/W)	2	
R5 (°C/W)	15	
R6 (°C/W)	61	24
C1 (W·s/°C)	0.0008	
C2 (W·s/°C)	0.007	
C3 (W·s/°C)	0.02	
C4 (W·s/°C)	0.3	
C5 (W·s/°C)	0.45	
C6 (W·s/°C)	0.8	5

4.3 PowerSO-10 thermal data

Figure 35. PowerSO-10 PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 58 mm x 58 mm, PCB thickness = 2 mm, Cu thickness = 35 μ m, Copper areas: from minimum pad lay-out to 8 cm²).

Figure 36. $R_{thj-amb}$ vs PCB copper area in open box free air condition

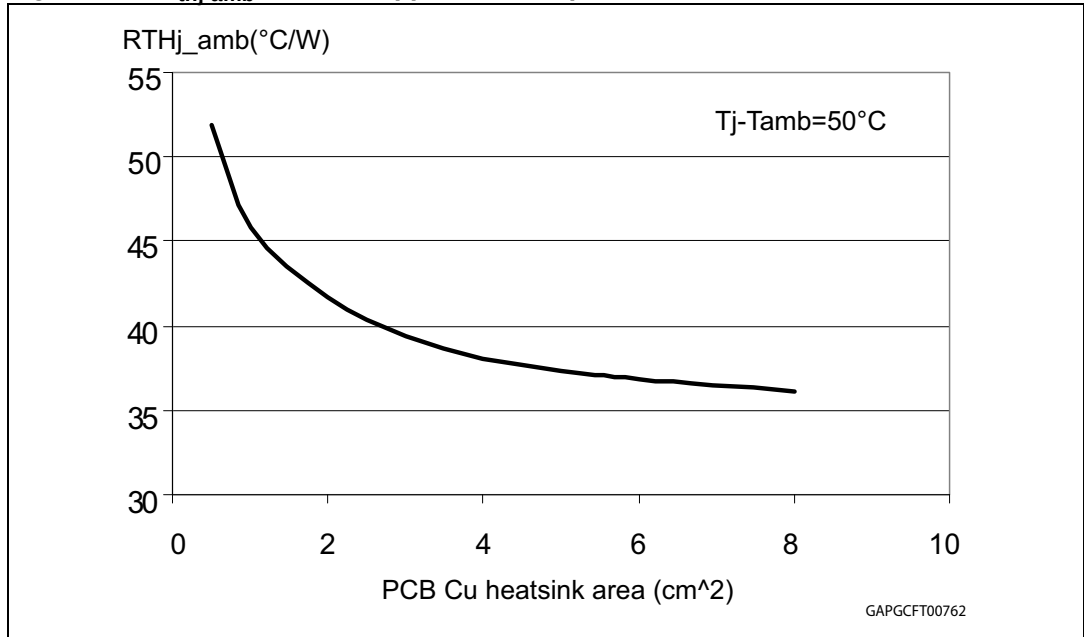
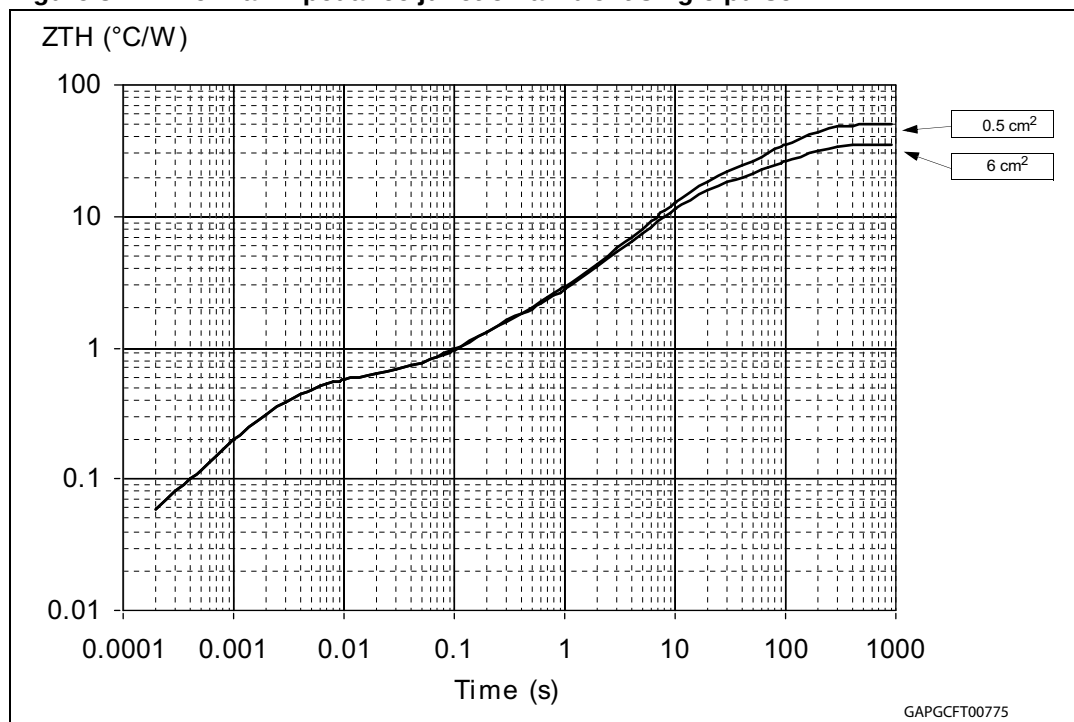


Figure 37. Thermal impedance junction ambient single pulse**Equation 3: pulse calculation formula**

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

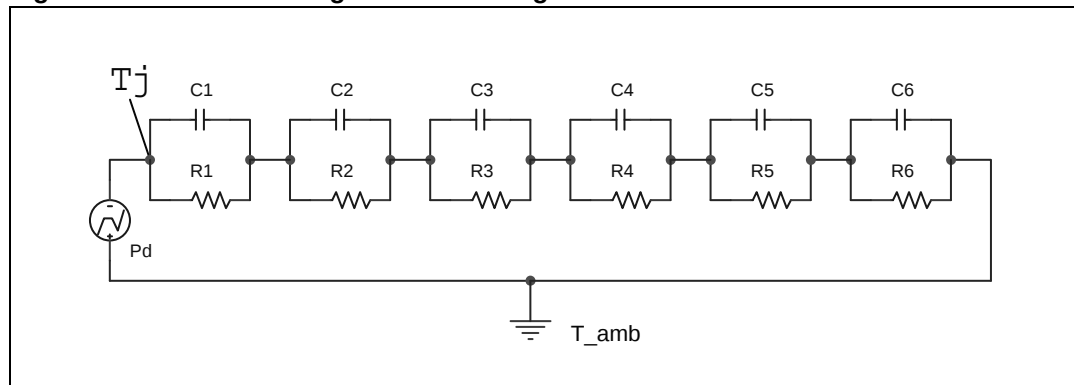
Figure 38. Thermal fitting model of a single channel HSD in PowerSO-10

Table 16. Thermal parameters

Area / island (cm ²)	Footprint	6
R1 (°C/W)	0.04	
R2 (°C/W)	0.25	
R3 (°C/W)	0.25	
R4 (°C/W)	0.8	
R5 (°C/W)	12	
R6 (°C/W)	37	22
C1 (W.s/°C)	0.0008	
C2 (W.s/°C)	7E-03	
C3 (W.s/°C)	0.015	
C4 (W.s/°C)	0.3	
C5 (W.s/°C)	0.75	
C6 (W.s/°C)	3	5

5 Package and packing information

5.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

5.2 PENTAWATT mechanical data

Figure 39. PENTAWATT package dimensions

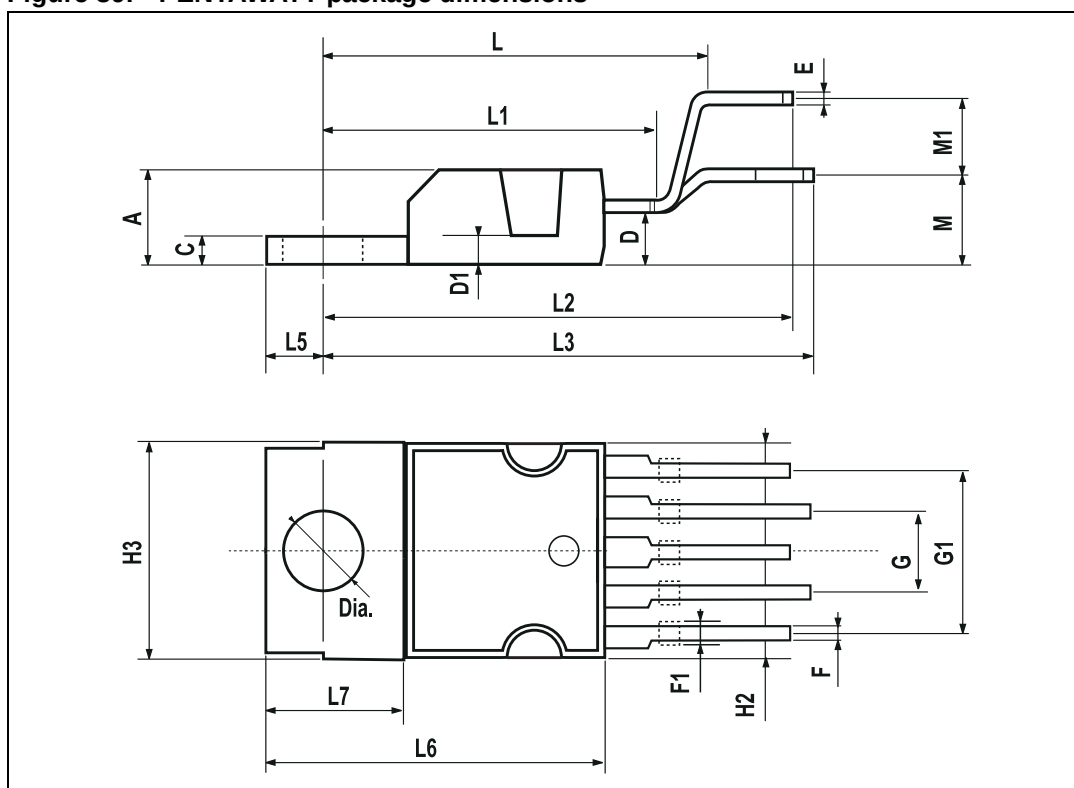


Table 17. PENTAWATT mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			4.8
C			1.37
D	2.4		2.8
D1	1.2		1.35
E	0.35		0.55
F	0.8		1.05
F1	1		1.4
G	3.2	3.4	3.6
G1	6.6	6.8	7
H2			10.4
H3	10.05		10.4
L		17.85	
L1		15.75	
L2		21.4	
L3		22.5	
L5	2.6		3
L6	15.1		15.8
L7	6		6.6
M		4.5	
M1		4	
Diam.	3.65		3.85

5.3 P²PAK mechanical data

Figure 40. P²PAK package dimensions

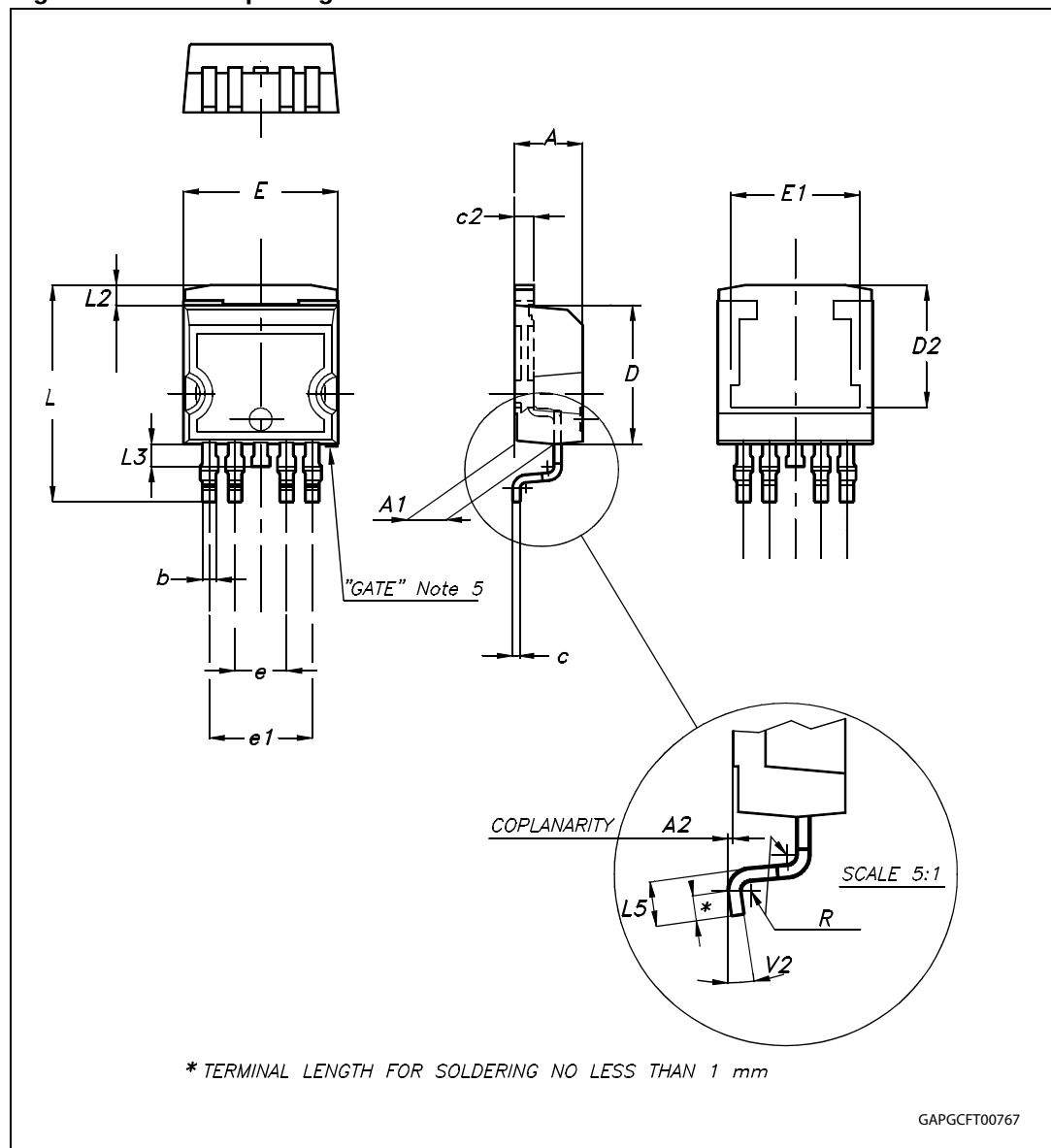


Table 18. P²PAK mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.80
A1	2.40		2.80
A2	0.03		0.23
b	0.80		1.05
c	0.45		0.60
c2	1.17		1.37
D	8.95		9.35
D2		8.00	
E	10.00		10.40
E1		8.50	
e	3.20		3.60
e1	6.60		7.00
L	13.70		14.50
L2	1.25		1.40
L3	0.90		1.70
L5	1.55		2.40
R		0.40	
V2	0°		8°
Package weight	1.40 Gr (typ)		

5.4 PPAK mechanical data

Figure 41. PPAK package dimensions

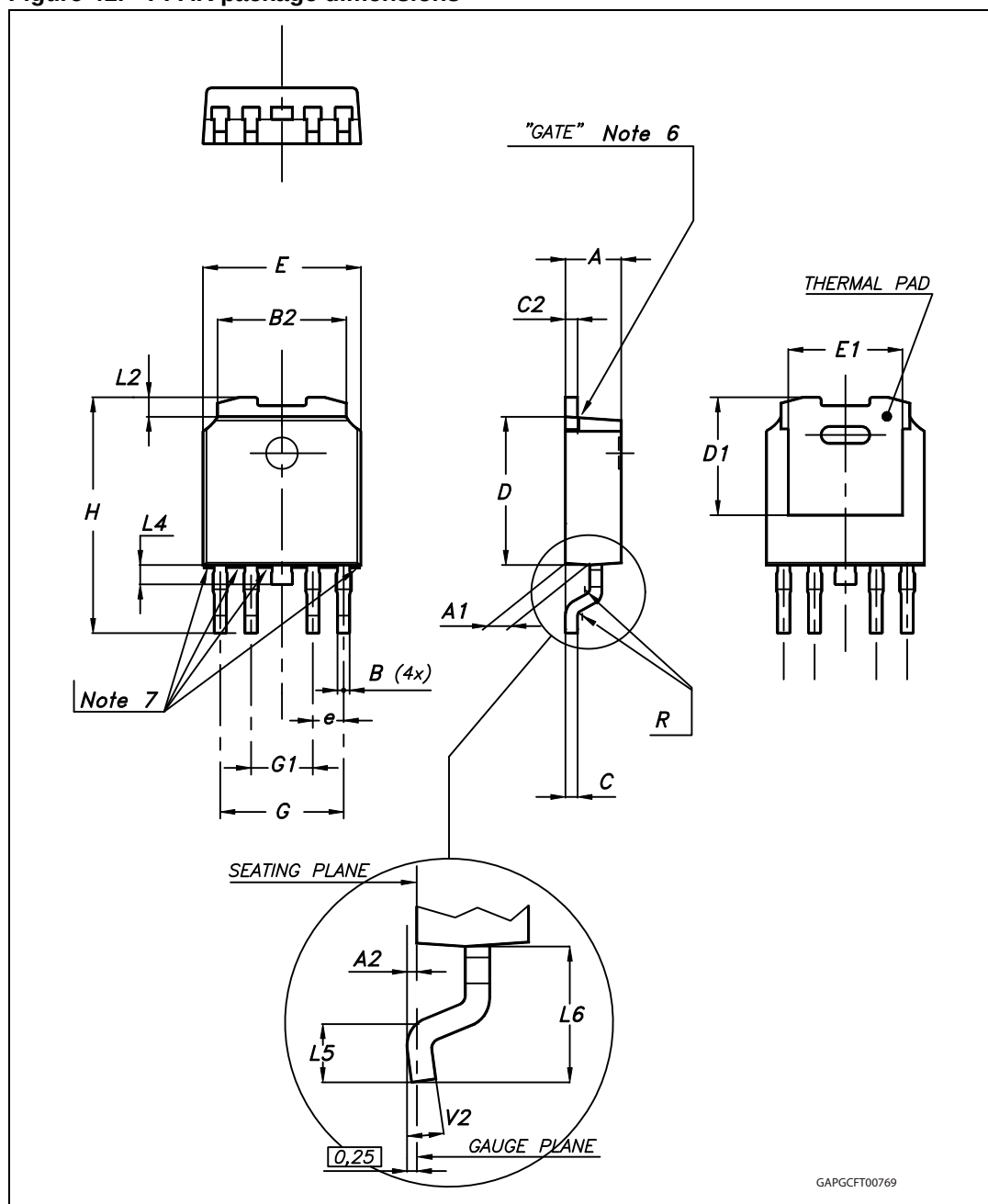


Table 19. PPAK mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
B	0.40		0.60
B2	5.20		5.40
C	0.45		0.60
C2	0.48		0.60
D	6.00		6.20
D1		5.1	
E	6.40		6.60
E1		4.7	
e		1.27	
G	4.90		5.25
G1	2.38		2.70
H	9.35		10.10
L2		0.8	1.00
L4	0.60		1.00
L5	1		—
L6		2.80	
R		0.2	
V2	0°		8°
Package weight	Gr. 0.3		

5.5 PowerSO-10 mechanical data

Figure 42. PowerSO-10 package dimensions

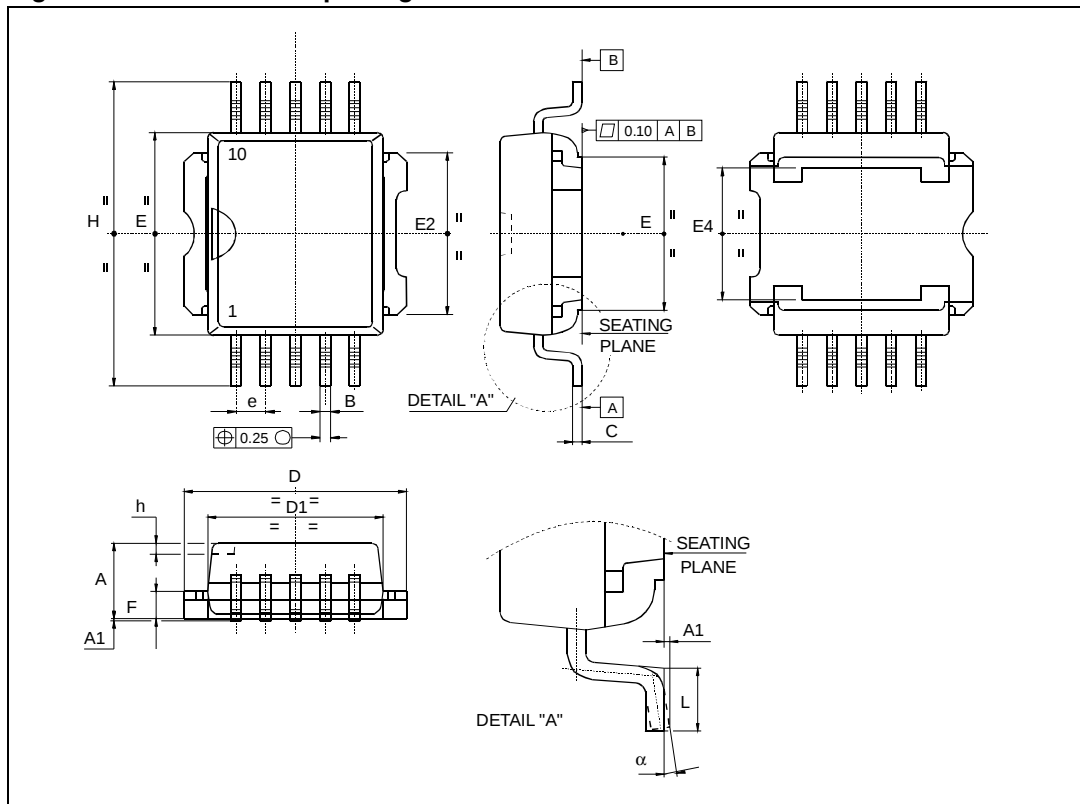


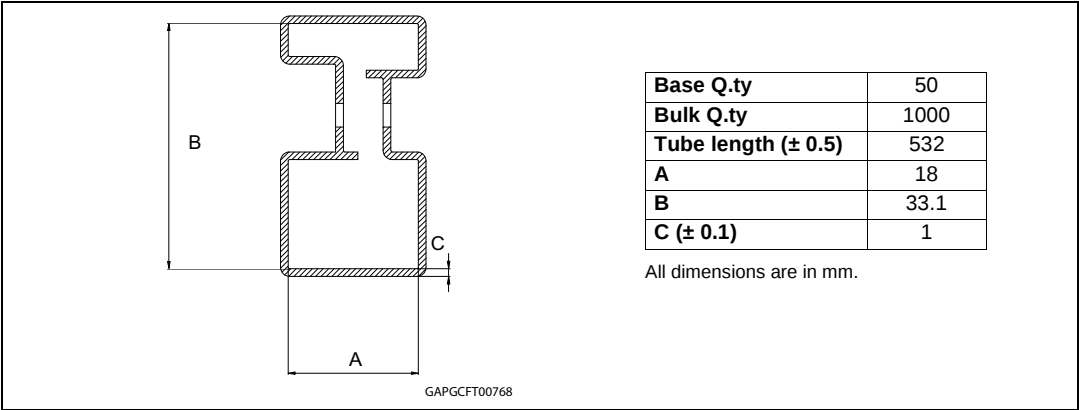
Table 20. PowerSO-10 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	3.35		3.65
A ⁽¹⁾	3.4		3.6
A1	0		0.10
B	0.40		0.60
B ⁽¹⁾	0.37		0.53
C	0.35		0.55
C ⁽¹⁾	0.23		0.32
D	9.40		9.60
D1	7.40		7.60
E	9.30		9.50
E2	7.20		7.60
E2 ⁽¹⁾	7.30		7.50
E4	5.90		6.10
E4 ⁽¹⁾	5.90		6.30
e		1.27	
F	1.25		1.35
F ⁽¹⁾	1.20		1.40
H	13.80		14.40
H ⁽¹⁾	13.85		14.35
h		0.50	
L	1.20		1.80
L ⁽¹⁾	0.80		1.10
α	0°		8°
$\alpha^{(1)}$	2°		8°

1. Muar only POA P013P.

5.6 PENTAWATT packing information

Figure 43. PENTAWATT tube shipment (no suffix)



5.7 P²PAK packing information

Figure 44. P²PAK tube shipment (no suffix)

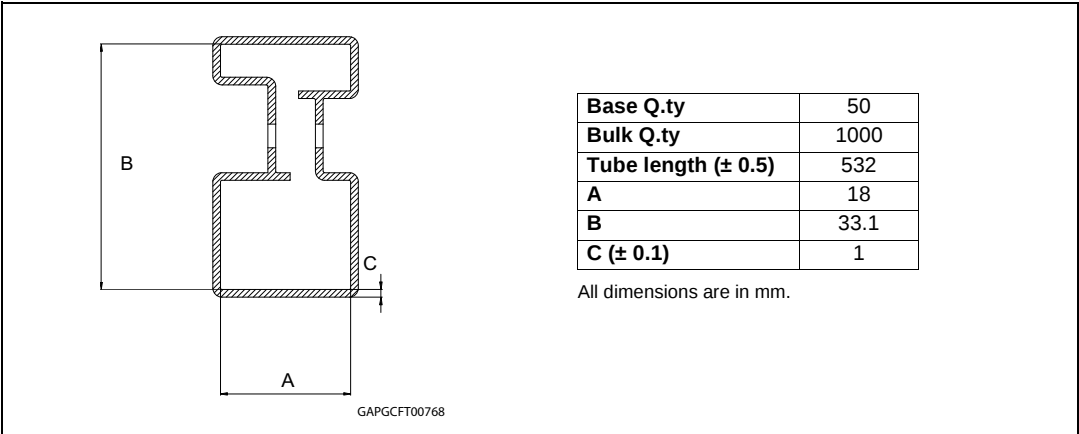
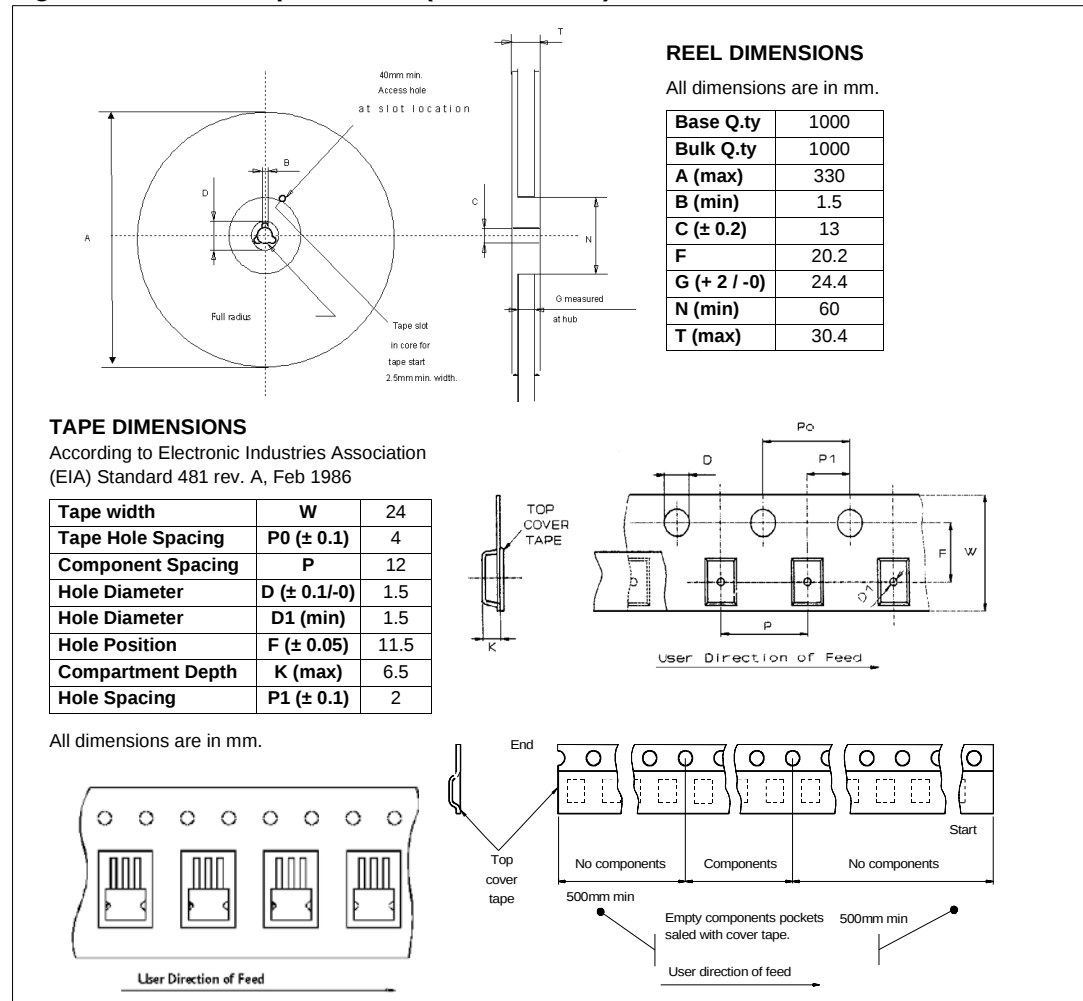


Figure 45. P²PAK tape and reel (suffix “13TR”)

5.8 PPAK packing information

Figure 46. PPAK suggested pad layout

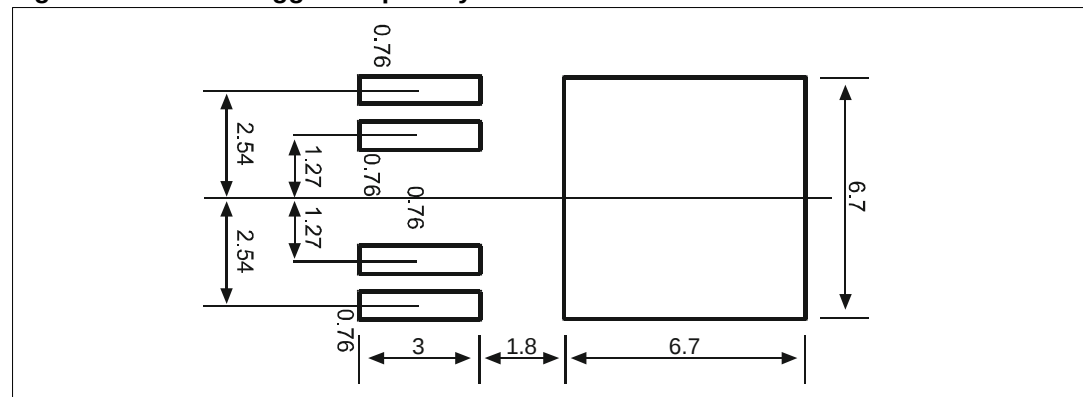


Figure 47. PPAK tube shipment (no suffix)

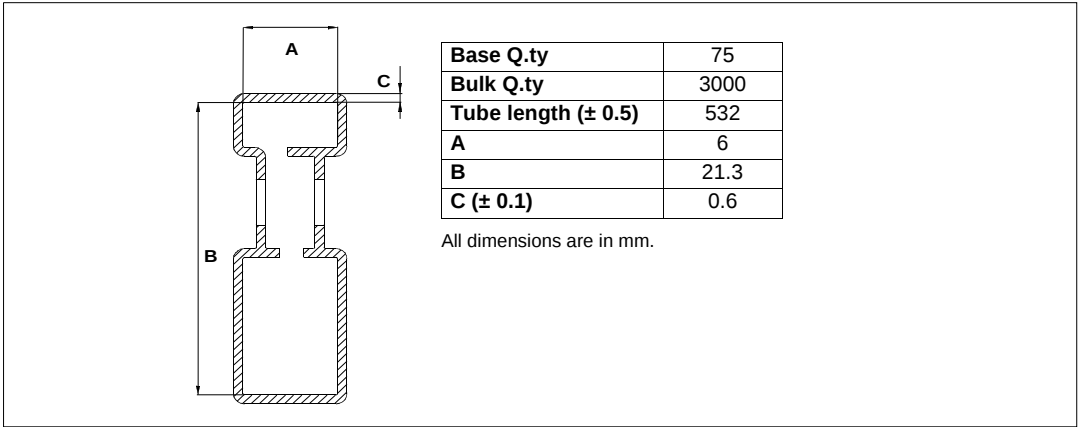
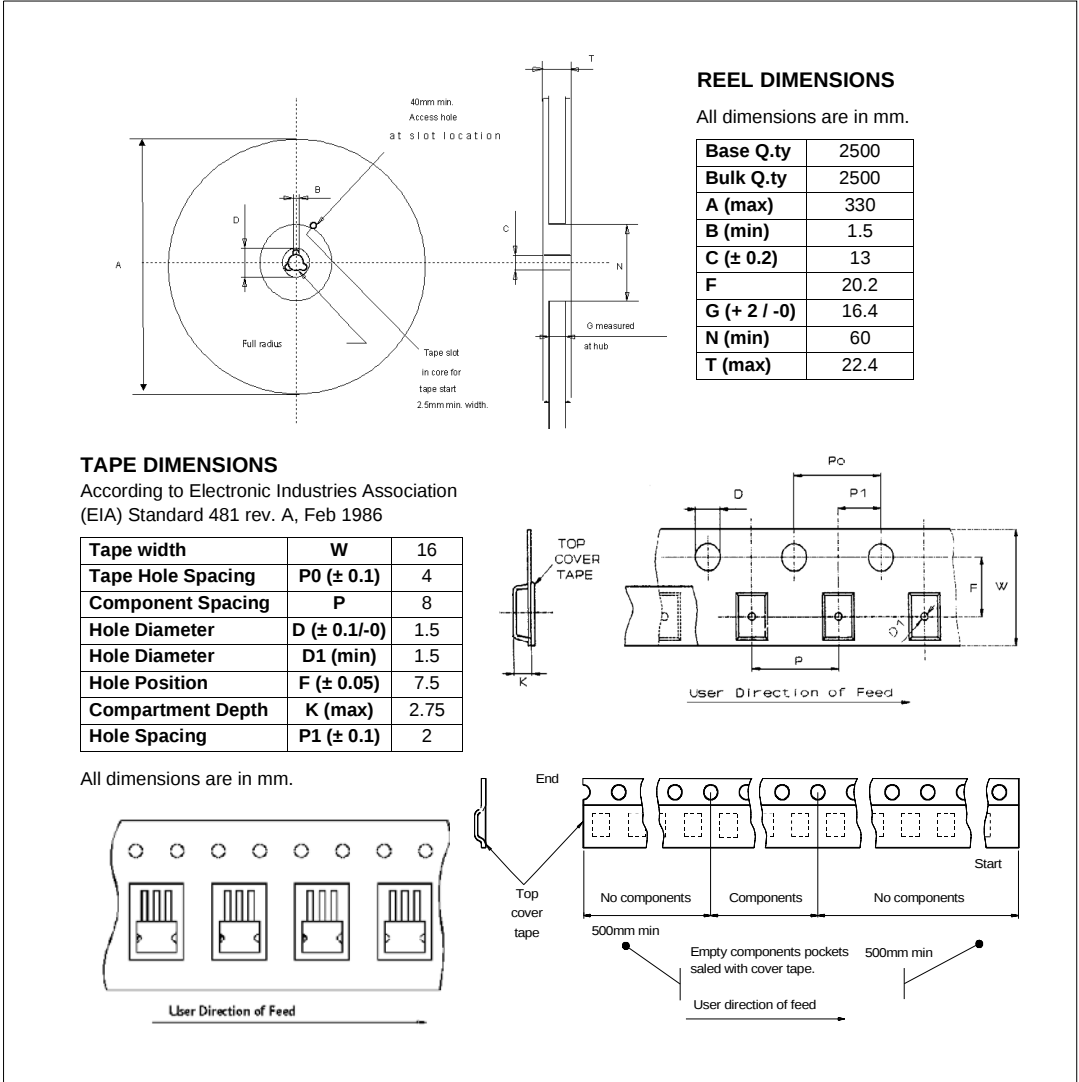


Figure 48. PPAK tape and reel (suffix "13TR")



5.9 PowerSO-10 packing information

Figure 49. PowerSO-10 suggested pad layout **Figure 50. PowerSO-10 tube shipment (no suffix)**

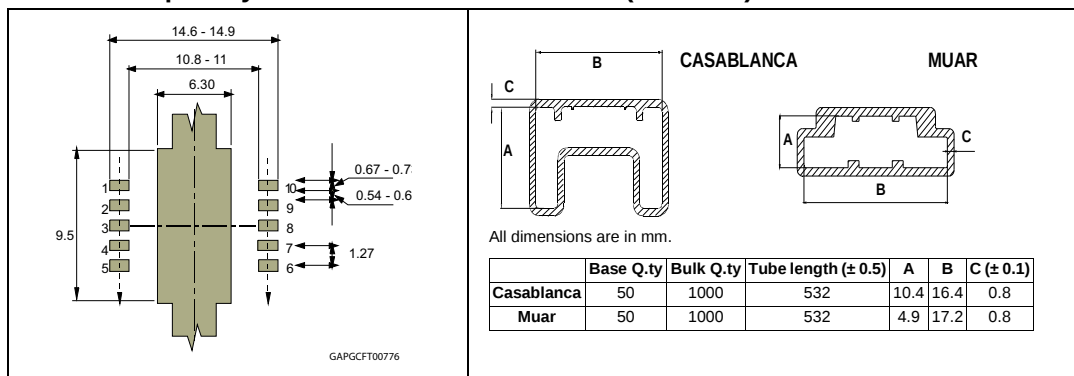
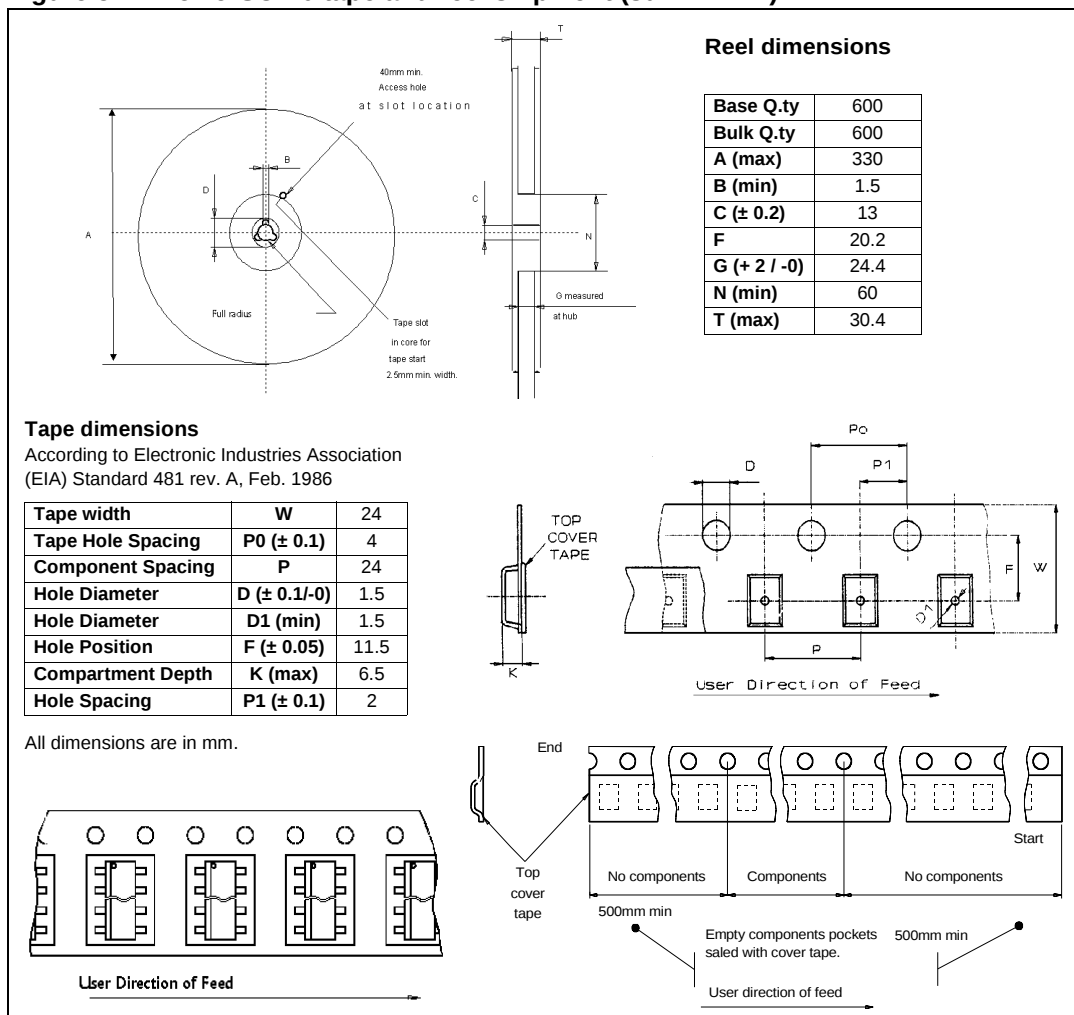


Figure 51. PowerSO-10 tape and reel shipment (suffix "TR")



6 Revision history

Table 21. Document revision history

Date	Revision	Changes
07-Jul-2004	1	Initial release.
03-May-2006	2	Minor changes Current and voltage convention update (page 2). Configuration diagram (top view) and suggested connections for unused and n.c. pins insertion (page 2). 6 cm ² Cu condition insertion in thermal data table (page 3). V _{CC} - output diode section update (page 4). Revision history table insertion (page 34). Disclaimers update (page 35).
17-Dec-2008	3	Document reformatted and restructured. Added content, list of figures and tables. Added <i>ECOPACK[®] packages</i> information. Updated <i>Figure 45.: P²PAK tape and reel (suffix "13TR")</i> : – changed component spacing (P) in tape dimensions table from 16 mm to 12 mm.
31-Mar-2010	4	Updated document template. Updated features list. Removed SO-16L package into the document: – Updated <i>Table 1: Device summary</i> – Updated <i>Table 3: Absolute maximum ratings</i> – Updated <i>Table 4: Thermal data</i> – Updated <i>Section 3.5: PowerSO-10, P²PAK, PPAK, PENTAWATT maximum demagnetization energy (VCC = 13.5V)</i> – Updated <i>Section 4: Package and PCB thermal data</i> – Updated <i>Section 5: Package and packing information</i>
06-Jun-2012	5	Updated <i>Section 5.8: PPAK packing information</i>
20-Sep-2013	6	Updated Disclaimer.

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