### 1.0 ELECTRICAL CHARACTERISTICS

## **Absolute Maximum Ratings†**

Drain-to-Source Voltage	BV <sub>DSS</sub>
Drain-to-Gate Voltage	
Gate-to-Source Voltage	
Operating Ambient Temperature, T <sub>A</sub>	
Storage Temperature, T <sub>S</sub>	

**† Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

# DC ELECTRICAL CHARACTERISTICS

**Electrical Specifications:**  $T_A = 25^{\circ}$ C unless otherwise specified. All DC parameters are 100% tested at 25°C unless otherwise stated. Pulse test: 300 µs pulse, 2% duty cycle

Parameter	Sym.	Min.	Тур.	Max.	Unit	Conditions
Drain-to-Source Breakdown Voltage	BV <sub>DSS</sub>	-220	_	_	V	$V_{GS} = 0V$ , $I_D = -2$ mA
Gate Threshold Voltage	V <sub>GS(th)</sub>	<b>–</b> 1	_	-2.4	V	$V_{GS} = V_{DS}$ , $I_D = -1 \text{ mA}$
Change in V <sub>GS(th)</sub> with Temperature	$\Delta V_{GS(th)}$	_	_	4.5	mV/°C	$V_{GS} = V_{DS}, I_{D} = -1 \text{ mA}$ (Note 1)
Gate Body Leakage Current	I <sub>GSS</sub>	_	_	-100	nA	$V_{GS}$ = ±20V, $V_{DS}$ = 0V
		_		-10	μΑ	V <sub>DS</sub> = Maximum rating, V <sub>GS</sub> = 0V
Zero-Gate Voltage Drain Current	I <sub>DSS</sub>		l	-1	mA	$V_{DS}$ = 0.8 Maximum rating, $V_{GS}$ = 0V, $T_A$ = 125°C (Note 1)
On-State Drain Current	I <sub>D(ON)</sub>	-0.7	-0.95	_	Α	$V_{GS} = -10V, V_{DS} = -25V$
Static Drain-to-Source On-State Resistance	P	_	10	15	Ω	$V_{GS} = -4.5V$ , $I_{D} = -100 \text{ mA}$
Static Drain-to-Source On-State Resistance	R <sub>DS(ON)</sub>		8	12	Ω	$V_{GS} = -10V$ , $I_{D} = -200$ mA
Change in R <sub>DS(ON)</sub> with Temperature	$\Delta R_{DS(ON)}$	_	_	1.7	%/°C	$V_{GS} = -10V, I_D = -200 \text{ mA}$ (Note 1)

**Note 1:** Specification is obtained by characterization and is not 100% tested.

# **AC ELECTRICAL CHARACTERISTICS**

Electrical Specifications:	T <sub>A</sub> = 25°C unless otherwise specified. Specification is obtained by characterization and
is not 100% tested	

Parameter	Sym.	Min.	Тур.	Max.	Unit	Conditions
Forward Transconductance	G <sub>FS</sub>	100	250	_	mmho	$V_{GS} = -10V$ , $I_D = -200$ mA
Input Capacitance	C <sub>ISS</sub>	_	_	110	pF	$V_{GS} = 0V$ ,
Common Source Output Capacitance	Coss	_	_	45	pF	V <sub>DS</sub> =–25V,
Reverse Transfer Capacitance	C <sub>RSS</sub>	_	_	20	pF	f = 1 MHz
Turn-On Delay Time	t <sub>d(ON)</sub>	_	_	10	ns	
Rise Time	t <sub>r</sub>	_	_	15	ns	$V_{DD} = -25V,$
Turn-Off Delay Time	t <sub>d(OFF)</sub>	_	_	20	ns	$I_D = -700 \text{ mA},$ $R_{GEN} = 25\Omega,$
Fall Time	t <sub>f</sub>	_	_	15	ns	
DIODE PARAMETER	_					
Diode Forward Voltage Drop	$V_{SD}$	_		-1.8	V	$V_{GS} = 0V$ , $I_{SD} = -500$ mA ( <b>Note 1</b> )
Reverse Recovery Time	t <sub>rr</sub>	_	300	_	ns	$V_{GS} = 0V$ , $I_{SD} = -500 \text{ mA}$

Note 1: Unless otherwise stated, all DC parameters are 100% tested at 25°C. Pulse test: 300 μs pulse, 2% duty cycle

# **TEMPERATURE SPECIFICATIONS**

Parameter	Sym.	Min.	Тур.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Ambient Temperature	T <sub>A</sub>	-55	_	+150	°C	
Storage Temperature	T <sub>S</sub>	-55	_	+150	°C	
PACKAGE THERMAL RESISTANCE						
3-lead SOT-23	$\theta_{JA}$	_	203	_	°C/W	
3-lead SOT-89	$\theta_{JA}$	_	133	_	°C/W	

# THERMAL CHARACTERISTICS

Package	I <sub>D</sub> (Note 1) (Continuous) (mA)	I <sub>D</sub> (Pulsed) (mA)	Power Dissipation at T <sub>A</sub> = 25°C (W)	I <sub>DR</sub> (Note 1) (mA)	I <sub>DRM</sub> (mA)
3-lead SOT-23	-120	-700	0.36	-120	-700
3-lead SOT-89	-260	-0.90	1.6 (Note 2)	-260	-0.90

**Note 1:**  $I_D$  (continuous) is limited by maximum rated  $T_J$ .

<sup>2:</sup> Mounted on an FR4 board, 25 mm x 25 mm x 1.57 mm

# 2.0 PIN DESCRIPTION

The details on the pins of TP5322 3-lead SOT-23 and 3-lead SOT-89 packages are listed in Table 2-1 and Table 2-2, respectively. Refer to **Package Types** for the location of pins.

### TABLE 2-1: 3-LEAD SOT-23 PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	Gate	Gate
2	Source	Source
3	Drain	Drain

### TABLE 2-2: 3-LEAD SOT-89 PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	Gate	Gate
2,4	Drain	Drain
3	Source	Source

# 3.0 FUNCTIONAL DESCRIPTION

Figure 3-1 illustrates the switching waveforms and test circuit for TP5322.

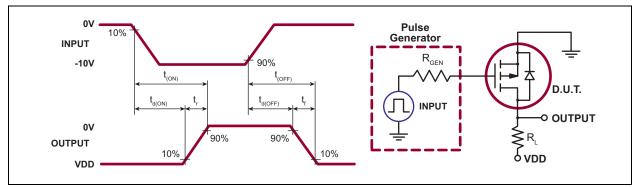


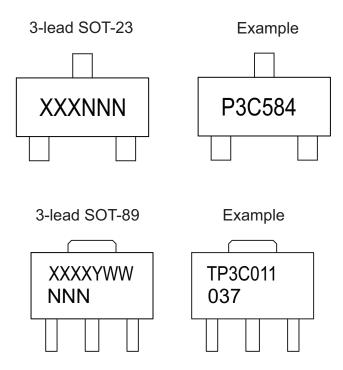
FIGURE 3-1: Switching Waveforms and Test Circuit.

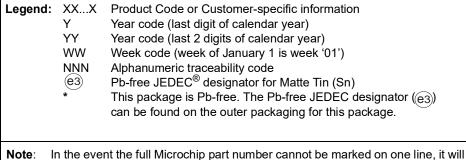
TABLE 3-1: PRODUCT SUMMARY

BV <sub>DSS</sub> /BV <sub>DGS</sub> (V)	R <sub>DS(ON)</sub> (Maximum) (Ω)	V <sub>GS(TH)</sub> (Maximum) (V)	I <sub>D(ON)</sub> (Minimum) (mA)
-220	12	-2.4	-700

### 4.0 PACKAGING INFORMATION

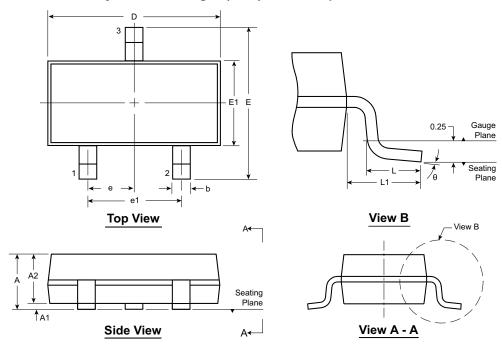
# 4.1 Package Marking Information





In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

# 3-Lead TO-236AB (SOT-23) Package Outline (K1/T) 2.90x1.30mm body, 1.12mm height (max), 1.90mm pitch

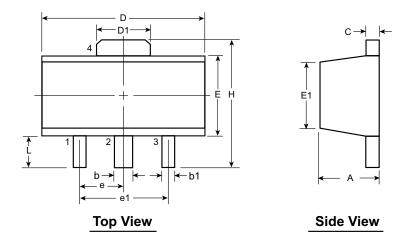


Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Symb	ol	Α	A1	A2	b	D	E	E1	е	e1	L	L1	θ
<u>.</u>	MIN	0.89	0.01	0.88	0.30	2.80	2.10	1.20		4.00	0.20 <sup>†</sup>		0°
Dimension (mm)	NOM	-	-	0.95	-	2.90	-	1.30	0.95 BSC	1.90 BSC	0.50	0.54 REF	-
(11111)	MAX	1.12	0.10	1.02	0.50	3.04	2.64	1.40	ВОО		0.60	1 ( )	80

JEDEC Registration TO-236, Variation AB, Issue H, Jan. 1999. † This dimension differs from the JEDEC drawing. Drawings not to scale.

# 3-Lead TO-243AA (SOT-89) Package Outline (N8)



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Symbo	ol	Α	b	b1	С	D	D1	E	E1	е	e1	Н	L
	MIN	1.40	0.44	0.36	0.35	4.40	1.62	2.29	2.00 <sup>†</sup>			3.94	0.73 <sup>†</sup>
Dimensions (mm)	NOM	1	1	-	-	-	-	-	-	1.50 BSC	3.00 BSC	-	-
(*****)	MAX	1.60	0.56	0.48	0.44	4.60	1.83	2.60	2.29			4.25	1.20

JEDEC Registration TO-243, Variation AA, Issue C, July 1986. † This dimension differs from the JEDEC drawing Drawings not to scale.

# APPENDIX A: REVISION HISTORY

# Revision A (June 2020)

- Converted Supertex Doc# DSFP-TP5322 to Microchip DS20005973A
- Added a pin function table
- · Changed the package marking format
- Made minor text changes throughout the document

# PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO	<u>. xx</u>		- <b>X</b> - <b>X</b>	Examples:	
Device	Packa Optio		Environmental Media Type	a) TP5322K1-G:	P-Channel Enhancement- Mode, Vertical DMOS FET, 3-lead SOT-23, 3000/Reel
Device:	TP5322	=	P-Channel Enhancement-Mode Vertical DMOS FET	b) TP5322N8-G:	P-Channel Enhancement- Mode, Vertical DMOS FET, 3-lead SOT-89, 2000/Reel
Packages:	K1	=	3-lead SOT-23		
	N8	=	3-lead SOT-89		
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package		
Media Types:	(blank)	=	3000/Reel for a K1 Package		
	(blank)	=	2000/Reel for an N8 Package		

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ISBN: 978-1-5224-6175-3

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