5-V low drop fixed voltage regulator



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Block diagram

1 Block diagram

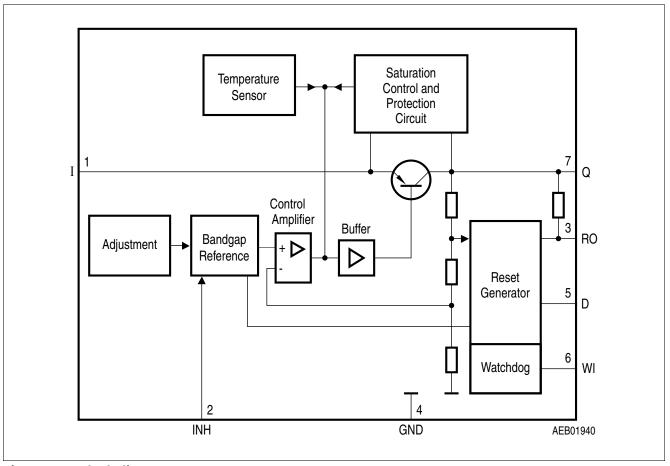


Figure 1 Block diagram

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Pin configuration

2 Pin configuration

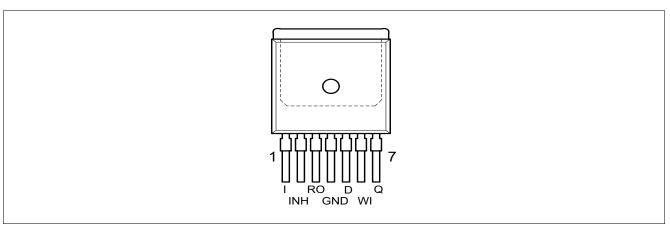


Figure 2 Pin configuration (top view)

Table 1 Pin definitions and functions

Pin	Symbol	Function
1	1	Input
		Block to ground directly on the IC with ceramic capacitor.
2	INH	Inhibit
3	RO	Reset output The open collector output is connected to the 5 V output via an integrated resistor of 30 k Ω .
4	GND	Ground
5	D	Reset delay Connect a capacitor to ground for delay time adjustment.
6	WI	Watchdog input
7	Q	5-V output Block to ground with 22 μ F capacitor, ESR < 3 Ω .

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General product characteristics

3 General product characteristics

3.1 Absolute maximum ratings

Table 2 Absolute maximum ratings

 $T_i = -40$ °C to 150°C

Parameter	Symbol	Values			Unit	Note or
		Min.	Тур.	Max.		Test Condition
Input	,	1	1	<u> </u>	<u> </u>	
Voltage	V _I	-42	_	42	V	_
Voltage	V _I	_	_	65	V	<i>t</i> ≤ 400 ms
Current	1,	_	_	_	mA	Internally limited
Inhibit			·	·	·	
Voltage	V_{INH}	-42	_	42	V	_
Voltage	V_{INH}	_	_	65	V	<i>t</i> ≤ 400 ms
Current	I _{INH}	_	_	_	mA	Internally limited
Reset output		•				
Voltage	V_{RO}	-0.3	_	42	V	_
Current	I _{RO}	_	_	-	mA	Internally limited
Reset delay						
Voltage	V_{D}	-0.3	_	7	V	_
Current	I _D	-5	_	5	mA	_
Watchdog			·	·	·	
Voltage	V_{W}	-0.3	_	7	V	_
Current	I _w	-5	_	5	mA	_
Output						
Voltage	V_{Q}	-1.0	_	16	V	_
Current	I_{Q}	-5	_	_	mA	Internally limited
Ground						
Current	I_{GND}	-0.5	_	_	Α	_
Temperatures						
Junction temperature	T _j	_	_	150	°C	_
Storage temperature	$T_{\rm stg}$	-50	_	150	°C	_

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General product characteristics

3.2 Operating range

Table 3 Operating range

Parameter	Symbol	Values			Unit	Note or	
		Min.	Тур.	Max.		Test Condition	
Input voltage	V _I	6	_	40	V	_	
Junction temperature	T _i	-40	_	150	°C	_	
Thermal resistance	, ,					1	
Junction ambient	R_{thja}	_	_	65	K/W	_	
		_	_	70	K/W	PG-TO263-7	
Junction case	$R_{ m thjc}$	_	_	3	K/W	_	
	$Z_{ m thic}$	_	_	2	K/W	<i>t</i> < 1 ms	

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General product characteristics

3.3 Characteristics

Table 4 Characteristics

 $V_{\rm I}$ = 13.5 V; $T_{\rm i}$ = -40°C to 125°C; $V_{\rm INH}$ > $V_{\rm U,INH}$ (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or	
		Min. Typ.		Max.		Test Condition	
Output voltage	V_{Q}	4.90	5.00	5.10	V	$I_Q = 5 \text{ mA to } 550 \text{ mA};$ $V_I = 6 \text{ V to } 26 \text{ V}$	
Output voltage	$V_{\rm Q}$	4.90	5.00	5.10	V	$V_1 = 26 \text{ V to } 36 \text{ V};$ $I_Q \le 300 \text{ mA}$	
Output current limiting	I _{Qmax}	650	800	_	mA	V _Q = 0 V	
Current consumption $I_q = I_1$	I_{q}	-	_	6	μΑ	$V_{\text{INH}} = 0 \text{ V};$ $I_{\text{Q}} = 0 \text{ mA}$	
Current consumption $I_q = I_1$	Iq	-	800	-	μΑ	$V_{\text{INH}} = 5 \text{ V};$ $I_{\text{Q}} = 0 \text{ mA}$	
Current consumption $I_q = I_1 - I_Q$	I _q	-	1	1.5	mA	I _Q = 5 mA	
Current consumption $I_q = I_1 - I_Q$	I _q	-	55	75	mA	I _Q = 550 mA	
Current consumption $I_q = I_1 - I_Q$	I _q	-	70	90	mA	$I_{\rm Q}$ = 550 mA; $V_{\rm I}$ = 5 V	
Drop voltage	$V_{\rm dr}$	_	350	700	mV	$I_{\rm Q} = 550 \; {\rm mA}^{1)}$	
Load regulation	$\Delta V_{ m Q}$	-	25	50	mV	$I_{\rm Q}$ = 5 mA to 550 mA; $V_{\rm I}$ = 6 V	
Supply voltage regulation	$\Delta V_{ m Q}$	-	12	25	mV	$V_1 = 6 \text{ V to } 26 \text{ V};$ $I_Q = 5 \text{ mA}$	
Power supply ripple rejection	PSRR	-	54	-	dB	$f_{\rm r} = 100 \text{Hz};$ $V_{\rm r} = 0.5 \text{Vpp}$	
Reset generator			*				
Switching threshold	V_{RT}	4.5	4.65	4.8	V	_	
Reset high voltage	V_{ROH}	4.5	_	_	V	_	
Saturation voltage	$V_{\rm RO,SAT}$	-	60	_	mV	$R_{\text{intern}} = 30 \text{ k}\Omega;$ $V_{Q} = 1.0 \text{ V to } 4.5 \text{ V}$	
Saturation voltage	$V_{\rm RO,SAT}$	-	200	400	mV	$I_{\rm R} = 3 \text{ mA}^{2};$ $V_{\rm Q} = 4.4 \text{ V}$	
Reset pull-up	R	18	30	46	kΩ	Internally connected to Q	
Lower reset timing threshold	V_{LD}	0.2	0.45	0.8	٧	$V_{\rm Q} < V_{\rm RT}$	
Charge current	I _D	8	14	25	μΑ	V _D = 1.0 V	
Upper timing threshold	$V_{\sf UD}$	1.4	1.8	2.3	٧	-	
Delay time	t_{D}	8	13	18	ms	C _D = 100 nF	
Reset reaction time	t_{RR}	_	_	3	μs	C _D = 100 nF	

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General product characteristics

Table 4 Characteristics (cont'd)

 $V_{\rm I}$ = 13.5 V; $T_{\rm j}$ = -40°C to 125°C; $V_{\rm INH}$ > $V_{\rm U,INH}$ (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or	
		Min.	Тур.	Max.		Test Condition	
Overvoltage protection							
Turn-off voltage	$V_{\rm I,ov}$	40	44	46	V	_	
Inhibit	•	•			•		
Turn-on voltage	$V_{\rm U,INH}$	1.0	2.0	3.5	V	V _Q = high (> 4.5 V)	
Turn-off voltage	$V_{L,INH}$	0.8	1.3	3.3	V	$V_{\rm Q} = {\rm low} (< 0.8 {\rm V})$	
Inhibit current	I _{INH}	8	12	25	μΑ	V _{INH} = 5 V	
Watchdog							
Upper watchdog switching threshold	V_{UDW}	1.4	1.8	2.3	V	-	
Lower watchdog switching threshold	V_{LDW}	0.2	0.45	0.8	V	-	
Discharge current	I _{DWD}	1.5	2.7	3.5	μΑ	V _D = 1 V	
Charge current	I _{DWC}	8	14	25	μΑ	<i>V</i> _D = 1 V	
Watchdog period	$t_{WD,P}$	40	55	80	ms	C _D = 100 nF	
Watchdog trigger time $t_{ m WI,tr}$		30	45	66	ms	C _D = 100 nF see diagram	
Watchdog pulse slew rate V_{WI}		5	_	_	V/µs	From 20% to 80% V	

¹⁾ Drop voltage = V_1 - V_Q (measured when the output voltage has dropped 100 mV from the nominal value obtained at 13.5 V input).

²⁾ Test condition not applicable during delay time for power-on reset.

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Circuit description

4 Circuit description

The control amplifier compares a reference voltage, which is kept highly accurate by resistance adjustment, to a voltage that is proportional to the output voltage and drives the base of a series transistor via a buffer. Saturation control as a function of the load current prevents any over-saturation of the power element.

The reset output RO is in high-state if the voltage on the delay capacitor C_D is greater or equal V_{UD} . The delay capacitor C_D is charged with the current I_D for output voltages greater than the reset threshold V_{RT} . If the output voltage gets lower than V_{RT} ('reset condition') a fast discharge of the delay capacitor C_D sets in and as soon as V_D gets lower than V_{LD} the reset output RO is set to low-level.

The time for the delay capacitor charge from $V_{\rm LD}$ to $V_{\rm LD}$ is the reset delay time $t_{\rm D}$.

When the voltage on the delay capacitor has reached $V_{\rm UD}$ and reset was set to high, the watchdog circuit is enabled and discharges $C_{\rm D}$ with the constant current $I_{\rm DWD}$. If there is no rising edge observed at the watchdog input, $C_{\rm D}$ will be discharge down to $V_{\rm LDW}$, then reset output RO will be set to low and $C_{\rm D}$ will be charged again with the current $I_{\rm DWC}$ until $V_{\rm D}$ reaches $V_{\rm UD}$ and reset will be set high again.

If the watchdog pulse (rising edge at watchdog input WI) occurs during the discharge period C_D is charged again and the reset output stays high. After V_D has reached V_{UD} , the periodical behavior starts again.

Internal protection circuits protect the IC against:

- Overload
- Overvoltage
- Overtemperature
- Reverse polarity

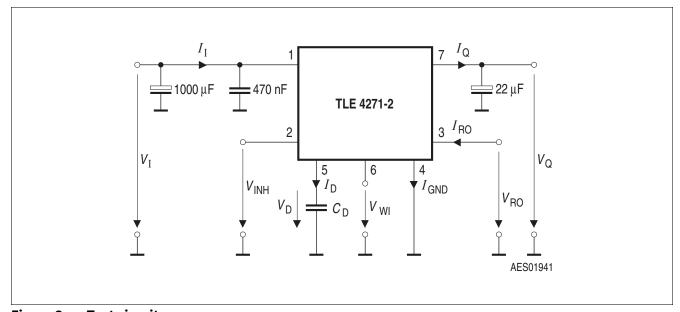


Figure 3 Test circuit

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Circuit description

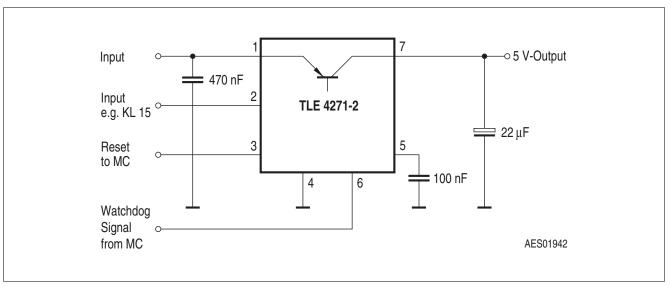


Figure 4 Circuit

Application description

The IC regulates an input voltage in the range of 6 V < $V_{\rm I}$ < 40 V to $V_{\rm Qnom}$ = 5.0 V. Up to 26 V it produces a regulated output current of more than 550 mA. Above 26 V the save-operating-area protection allows operation up to 36 V with a regulated output current of more than 300 mA. Overvoltage protection limits operation at 42 V. The overvoltage protection hysteresis restores operation if the input voltage has dropped below 36 V. The IC can be switched off via the inhibit input, which causes the quiescent current to drop below 10 μ A. A reset signal is generated for an output voltage of $V_{\rm Q}$ < 4.5 V. The watchdog circuit monitors a connected controller. If there is no positive-going edge at the watchdog input within a fixed time, the reset output is set to low. The delay for power-on reset and the maximum permitted watchdog-pulse period can be set externally with a capacitor.

Design notes for external components

An input capacitor C_l is necessary for compensation of line influences. The resonant circuit consisting of lead inductance and input capacitance can be damped by a resistor of approx. 1Ω in series with C_l . An output capacitor C_Q is necessary for the stability of the regulating circuit. Stability is guaranteed at values of $C_Q \ge 22 \mu F$ and an ESR of $< 3 \Omega$.

Reset circuitry

If the output voltage decreases below 4.5 V, an external capacitor $C_{\rm D}$ on pin D will be discharged by the reset generator. If the voltage on this capacitor drops below $V_{\rm DRL}$, a reset signal is generated on pin RO, i.e. reset output is set low. If the output voltage rises above the reset threshold, $C_{\rm D}$ will be charged with constant current. After the power-on-reset time the voltage on the capacitor reaches $V_{\rm DU}$ and the reset output will be set high again. The value of the power-on-reset time can be set within a wide range depending of the capacitance of $C_{\rm D}$.

Reset timing

The power-on reset delay time is defined by the charging time of an external capacitor C_d which can be calculated as follows:

$$t_{\rm D} = C_{\rm D} \times \Delta V / I_{\rm D} \tag{4.1}$$

Definitions:

• C_D = delay capacitor

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Circuit description

- t_D = reset delay time
- I_D = charge current, typical 14 μA
- $\Delta V = V_{UD}$, typical 1.8 V
- V_{UD} = upper delay timing threshold at C_D for reset delay time

The reset reaction time $t_{\rm rr}$ is the time it takes the voltage regulator to set the reset out LOW after the output voltage has dropped below the reset threshold. It is typically 1 μ s for delay capacitor of 47 nF. For other values for $C_{\rm d}$ the reaction time can be estimated using the following equation:

$$t_{\rm RR} \approx 20 \text{ s/F} \times C_{\rm d}$$
 (4.2)

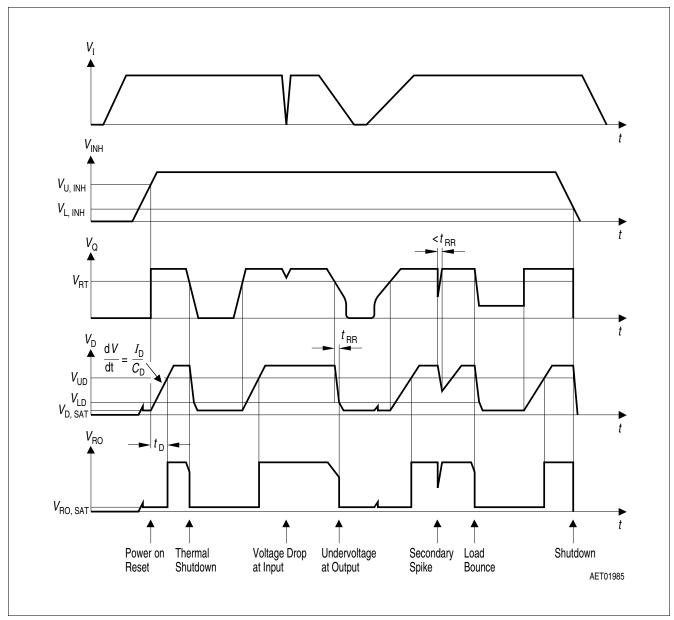


Figure 5 Time response

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Circuit description

Watchdog timing

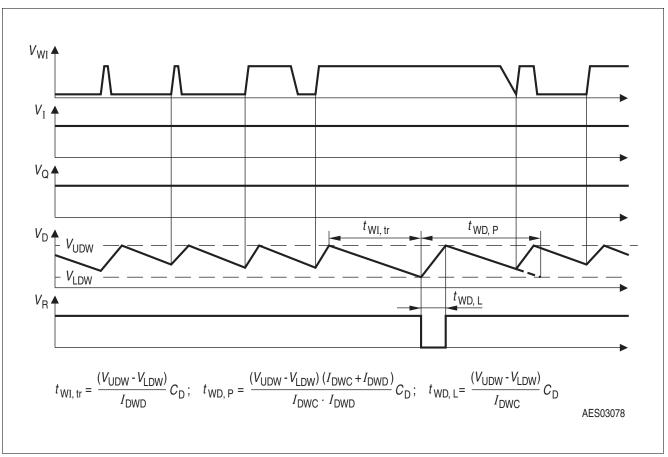


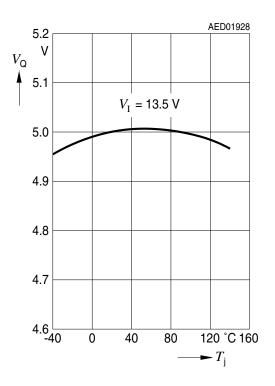
Figure 6 Time response, watchdog behavior



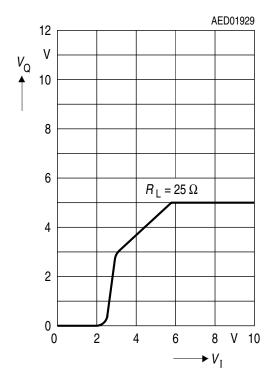
Typical performance characteristics

5 Typical performance characteristics

Output voltage $V_{\rm Q}$ versus junction temperature $T_{\rm j}$



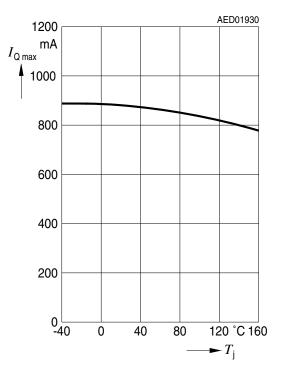
Output voltage V_{Q} versus input voltage V_{I} ($V_{INH} = V_{I}$)



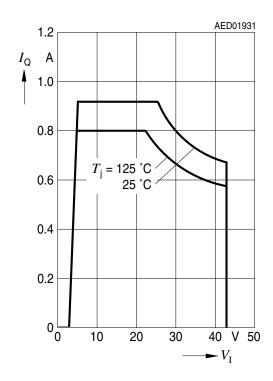
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Typical performance characteristics

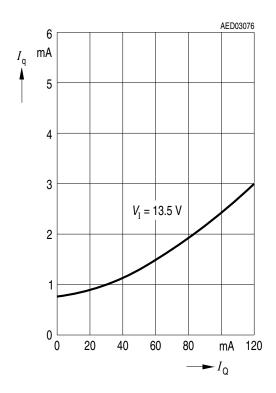
Output current limit I_Q versus junction temperature T_i



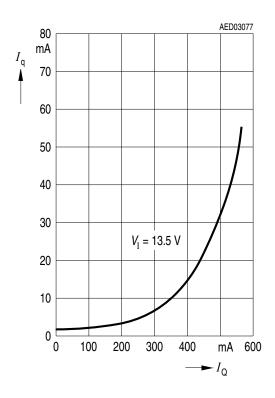
Output current I_Q versus input voltage V₁



Current consumption I_q versus output current Io



Current consumption I_q versus output current I_0

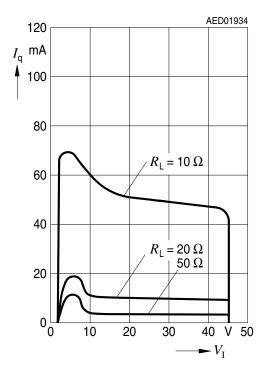


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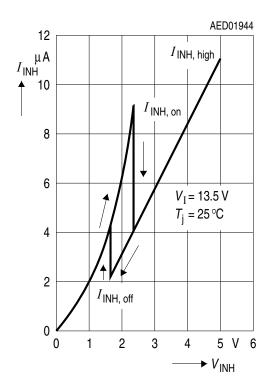
Typical performance characteristics



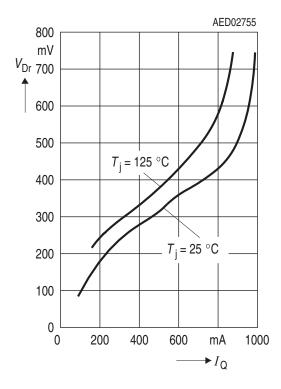
Current consumption I_q versus input voltage V_I



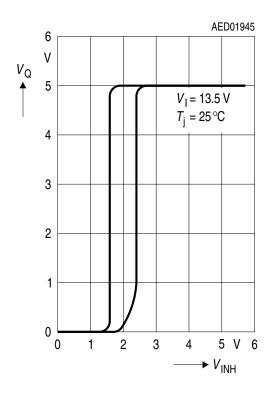
Inhibit current $I_{\rm INH}$ versus inhibit voltage $V_{\rm INH}$



Drop voltage $V_{\rm dr}$ versus output current $I_{\rm O}$



Output voltage $V_{\rm Q}$ versus inhibit voltage $V_{\rm INH}$

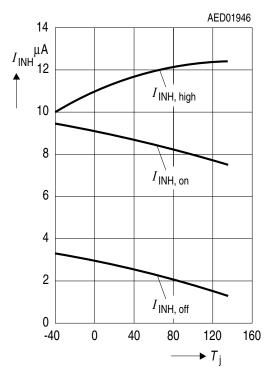


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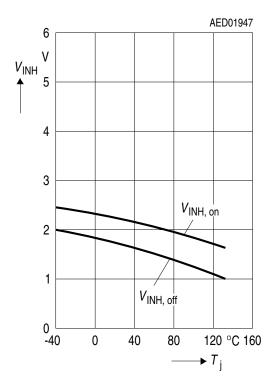


Typical performance characteristics

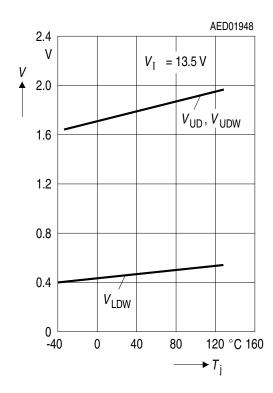
Inhibit current consumptions I_{INH} versus temperature T_{i}



Inhibit voltages V_{INH} versus junction temperature T_{j}



Switching voltage $V_{\rm UD}$ and $V_{\rm LDW}$ versus junction temperature $T_{\rm i}$

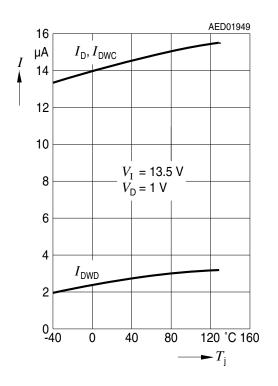


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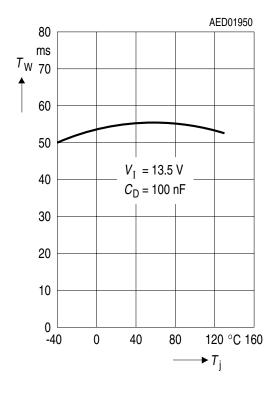


Typical performance characteristics

Charge current $I_{\rm D}$, $I_{\rm DWC}$ and discharge current $I_{\rm DWD}$ versus junction temperature $T_{\rm i}$



Watchdog pulse time $T_{\rm w}$ versus junction temperature $T_{\rm i}$



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Package information

6 Package information

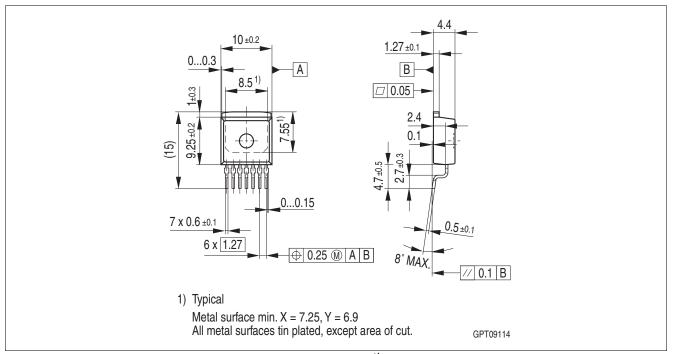


Figure 7 PG-TO263-7 (Plastic transistor single outline)¹⁾

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e. Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

https://www.infineon.com/packages

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Revision history

7 Revision history

Revision	Date	Changes
2.8	2019-07-30	Deleted both packages: PG-TO-220-7 Updated layout and structure frontpage: updated packaged drawings "TLE4271-2" Editorial changes
2.7	2007-03-20	Initial version of RoHS-compliant derivate of TLE4271-2 Page 1: AEC certified statement added Page 1 and Page 18ff: RoHS compliance statement and Green product feature added Page 1 and Page 18ff: Package changed to RoHS compliant version Legal Disclaimer updated

Trademarks

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