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1 Block diagram

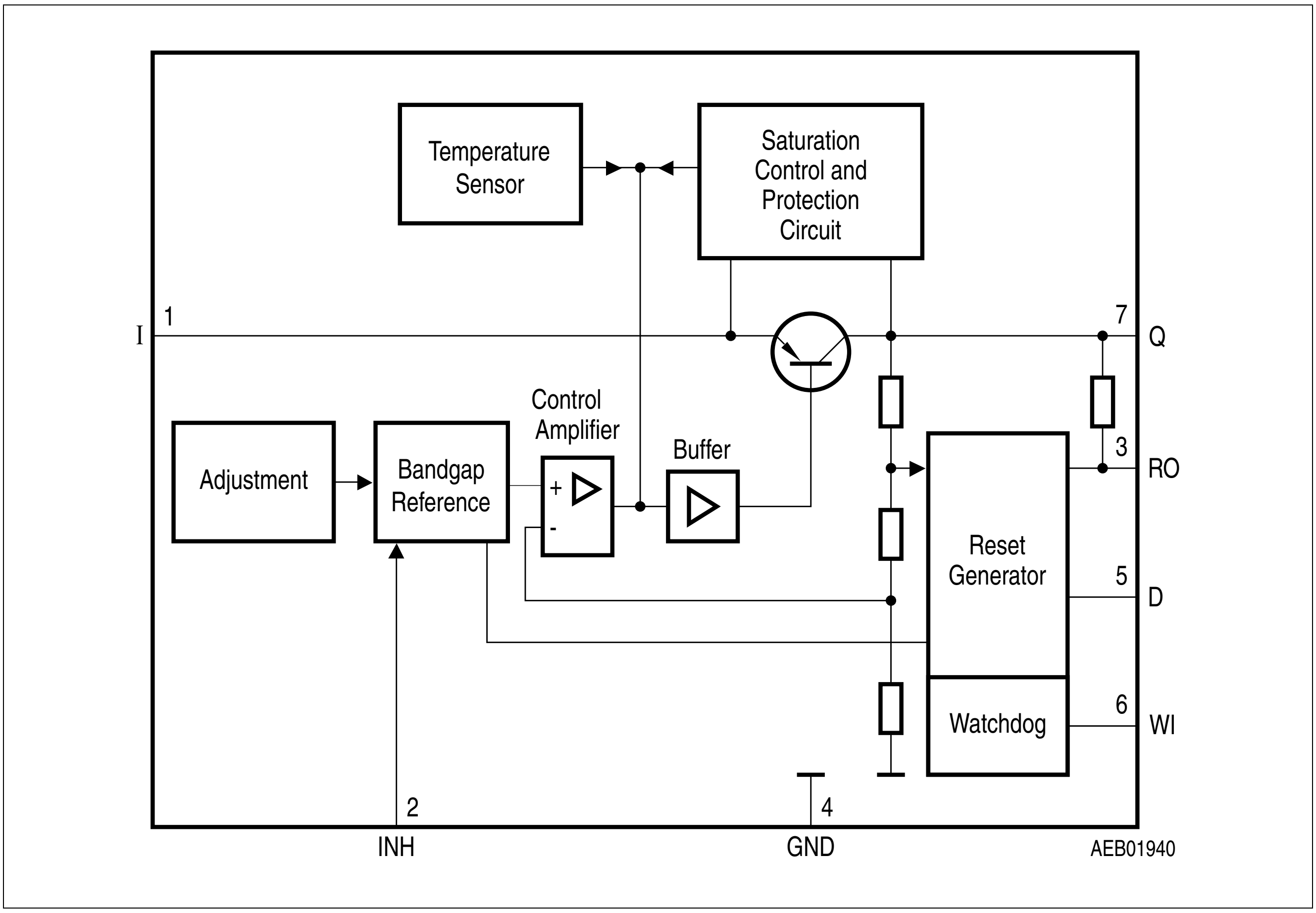


Figure 1 Block diagram

2 Pin configuration

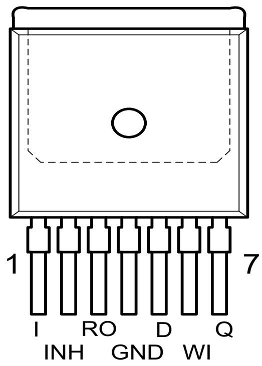


Figure 2 Pin configuration (top view)

Table 1 Pin definitions and functions

Pin	Symbol	Function
1	I	**Input** Block to ground directly on the IC with ceramic capacitor.
2	INH	**Inhibit**
3	RO	**Reset output** The open collector output is connected to the 5 V output via an integrated resistor of 30 kΩ.
4	GND	**Ground**
5	D	**Reset delay** Connect a capacitor to ground for delay time adjustment.
6	WI	**Watchdog input**
7	Q	**5-V output** Block to ground with 22 µF capacitor, ESR < 3 Ω.

3 General product characteristics

3.1 Absolute maximum ratings

Table 2 Absolute maximum ratings

T_j = -40°C to 150°C

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input						
Voltage	V_I	-42	–	42	V	–
Voltage	V_I	–	–	65	V	$t \leq 400$ ms
Current	I_I	–	–	–	mA	Internally limited
Inhibit						
Voltage	V_{INH}	-42	–	42	V	–
Voltage	V_{INH}	–	–	65	V	$t \leq 400$ ms
Current	I_{INH}	–	–	–	mA	Internally limited
Reset output						
Voltage	V_{RO}	-0.3	–	42	V	–
Current	I_{RO}	–	–	–	mA	Internally limited
Reset delay						
Voltage	V_D	-0.3	–	7	V	–
Current	I_D	-5	–	5	mA	–
Watchdog						
Voltage	V_W	-0.3	–	7	V	–
Current	I_W	-5	–	5	mA	–
Output						
Voltage	V_Q	-1.0	–	16	V	–
Current	I_Q	-5	–	–	mA	Internally limited
Ground						
Current	I_{GND}	-0.5	–	–	A	–
Temperatures						
Junction temperature	T_j	–	–	150	°C	–
Storage temperature	T_{stg}	-50	–	150	°C	–

3.2 Operating range

Table 3 Operating range

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input voltage	V_I	6	–	40	V	–
Junction temperature	T_j	-40	–	150	°C	–
Thermal resistance						
Junction ambient	R_{thja}	–	–	65	K/W	–
		–	–	70	K/W	PG-TO263-7
Junction case	R_{thjc}	–	–	3	K/W	–
	Z_{thjc}	–	–	2	K/W	$t < 1$ ms

3.3 Characteristics

Table 4 Characteristics

V_I = 13.5 V; T_j = -40°C to 125°C; $V_{INH} > V_{U,INH}$ (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Output voltage	V_Q	4.90	5.00	5.10	V	I_Q = 5 mA to 550 mA; V_I = 6 V to 26 V
Output voltage	V_Q	4.90	5.00	5.10	V	V_I = 26 V to 36 V; $I_Q \leq$ 300 mA
Output current limiting	I_{Qmax}	650	800	–	mA	V_Q = 0 V
Current consumption $I_q = I_I$	I_q	–	–	6	µA	V_{INH} = 0 V; I_Q = 0 mA
Current consumption $I_q = I_I$	I_q	–	800	–	µA	V_{INH} = 5 V; I_Q = 0 mA
Current consumption $I_q = I_I - I_Q$	I_q	–	1	1.5	mA	I_Q = 5 mA
Current consumption $I_q = I_I - I_Q$	I_q	–	55	75	mA	I_Q = 550 mA
Current consumption $I_q = I_I - I_Q$	I_q	–	70	90	mA	I_Q = 550 mA; V_I = 5 V
Drop voltage	V_{dr}	–	350	700	mV	I_Q = 550 mA[1)]
Load regulation	ΔV_Q	–	25	50	mV	I_Q = 5 mA to 550 mA; V_I = 6 V
Supply voltage regulation	ΔV_Q	–	12	25	mV	V_I = 6 V to 26 V; I_Q = 5 mA
Power supply ripple rejection	*PSRR*	–	54	–	dB	f_r = 100 Hz; V_r = 0.5 Vpp
Reset generator						
Switching threshold	V_{RT}	4.5	4.65	4.8	V	–
Reset high voltage	V_{ROH}	4.5	–	–	V	–
Saturation voltage	$V_{RO,SAT}$	–	60	–	mV	R_{intern} = 30 kΩ; V_Q = 1.0 V to 4.5 V
Saturation voltage	$V_{RO,SAT}$	–	200	400	mV	I_R = 3 mA[2)]; V_Q = 4.4 V
Reset pull-up	*R*	18	30	46	kΩ	Internally connected to Q
Lower reset timing threshold	V_{LD}	0.2	0.45	0.8	V	$V_Q < V_{RT}$
Charge current	I_D	8	14	25	µA	V_D = 1.0 V
Upper timing threshold	V_{UD}	1.4	1.8	2.3	V	–
Delay time	t_D	8	13	18	ms	C_D = 100 nF
Reset reaction time	t_{RR}	–	–	3	µs	C_D = 100 nF

Table 4 Characteristics (cont'd)

V_I = 13.5 V; T_j = -40°C to 125°C; $V_{INH} > V_{U,INH}$ (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Overvoltage protection						
Turn-off voltage	$V_{I, ov}$	40	44	46	V	–
Inhibit						
Turn-on voltage	$V_{U,INH}$	1.0	2.0	3.5	V	V_Q = high (> 4.5 V)
Turn-off voltage	$V_{L,INH}$	0.8	1.3	3.3	V	V_Q = low (< 0.8 V)
Inhibit current	I_{INH}	8	12	25	µA	V_{INH} = 5 V
Watchdog						
Upper watchdog switching threshold	V_{UDW}	1.4	1.8	2.3	V	–
Lower watchdog switching threshold	V_{LDW}	0.2	0.45	0.8	V	–
Discharge current	I_{DWD}	1.5	2.7	3.5	µA	V_D = 1 V
Charge current	I_{DWC}	8	14	25	µA	V_D = 1 V
Watchdog period	$t_{WD,P}$	40	55	80	ms	C_D = 100 nF
Watchdog trigger time	$t_{WI,tr}$	30	45	66	ms	C_D = 100 nF see diagram
Watchdog pulse slew rate	V_{WI}	5	–	–	V/µs	From 20% to 80% V_Q

1) Drop voltage = V_I - V_Q (measured when the output voltage has dropped 100 mV from the nominal value obtained at 13.5 V input).

2) Test condition not applicable during delay time for power-on reset.

4 Circuit description

The control amplifier compares a reference voltage, which is kept highly accurate by resistance adjustment, to a voltage that is proportional to the output voltage and drives the base of a series transistor via a buffer. Saturation control as a function of the load current prevents any over-saturation of the power element.

The reset output RO is in high-state if the voltage on the delay capacitor C_D is greater or equal V_{UD}. The delay capacitor C_D is charged with the current I_D for output voltages greater than the reset threshold V_{RT}. If the output voltage gets lower than V_{RT} ('reset condition') a fast discharge of the delay capacitor C_D sets in and as soon as V_D gets lower than V_{LD} the reset output RO is set to low-level.

The time for the delay capacitor charge from V_{UD} to V_{LD} is the reset delay time t_D.

When the voltage on the delay capacitor has reached V_{UD} and reset was set to high, the watchdog circuit is enabled and discharges C_D with the constant current I_{DWD}. If there is no rising edge observed at the watchdog input, C_D will be discharge down to V_{LDW}, then reset output RO will be set to low and C_D will be charged again with the current I_{DWC} until V_D reaches V_{UD} and reset will be set high again.

If the watchdog pulse (rising edge at watchdog input WI) occurs during the discharge period C_D is charged again and the reset output stays high. After V_D has reached V_{UD}, the periodical behavior starts again.

Internal protection circuits protect the IC against:

- Overload
- Overvoltage
- Overtemperature
- Reverse polarity

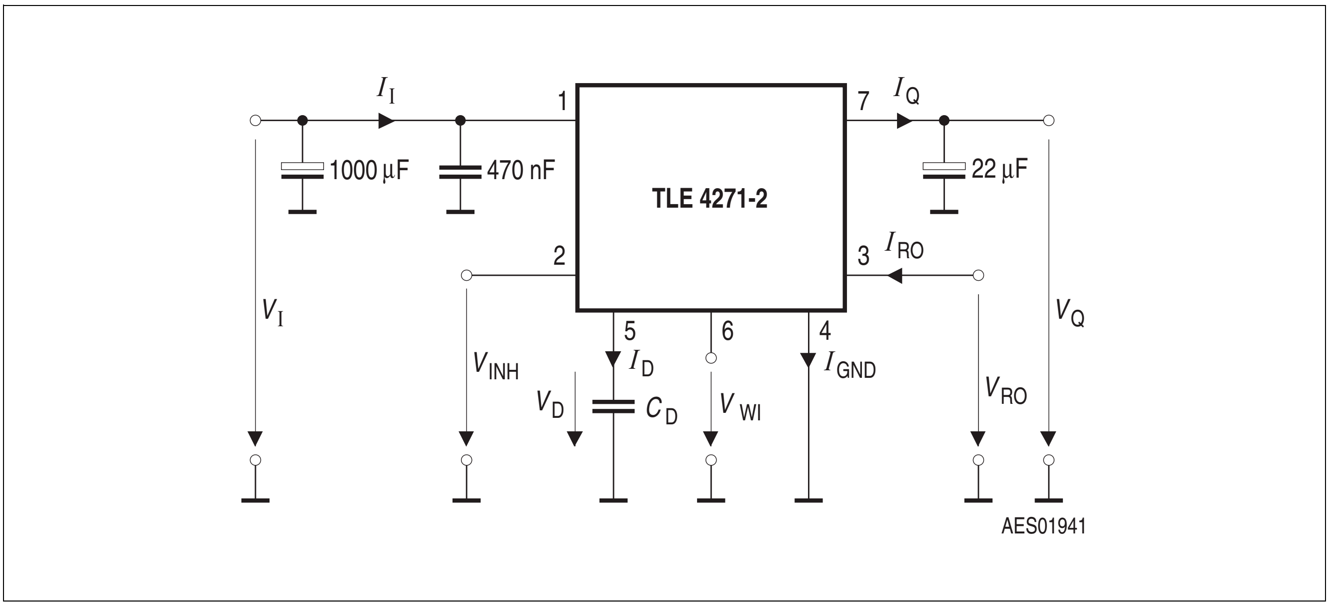


Figure 3 Test circuit

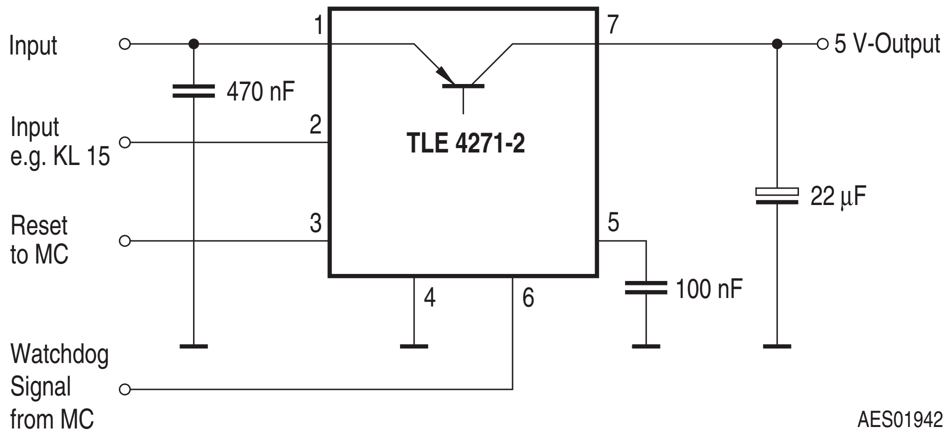


Figure 4 Circuit

Application description

The IC regulates an input voltage in the range of 6 V < V_I < 40 V to V_{Qnom} = 5.0 V. Up to 26 V it produces a regulated output current of more than 550 mA. Above 26 V the save-operating-area protection allows operation up to 36 V with a regulated output current of more than 300 mA. Overvoltage protection limits operation at 42 V. The overvoltage protection hysteresis restores operation if the input voltage has dropped below 36 V. The IC can be switched off via the inhibit input, which causes the quiescent current to drop below 10 µA. A reset signal is generated for an output voltage of V_Q < 4.5 V. The watchdog circuit monitors a connected controller. If there is no positive-going edge at the watchdog input within a fixed time, the reset output is set to low. The delay for power-on reset and the maximum permitted watchdog-pulse period can be set externally with a capacitor.

Design notes for external components

An input capacitor C_I is necessary for compensation of line influences. The resonant circuit consisting of lead inductance and input capacitance can be damped by a resistor of approx. 1 Ω in series with C_I. An output capacitor C_Q is necessary for the stability of the regulating circuit. Stability is guaranteed at values of C_Q ≥ 22 µF and an ESR of < 3 Ω.

Reset circuitry

If the output voltage decreases below 4.5 V, an external capacitor C_D on pin D will be discharged by the reset generator. If the voltage on this capacitor drops below V_{DRL}, a reset signal is generated on pin RO, i.e. reset output is set low. If the output voltage rises above the reset threshold, C_D will be charged with constant current. After the power-on-reset time the voltage on the capacitor reaches V_{DU} and the reset output will be set high again. The value of the power-on-reset time can be set within a wide range depending of the capacitance of C_D.

Reset timing

The power-on reset delay time is defined by the charging time of an external capacitor C_d which can be calculated as follows:

$$t_D = C_D \times \Delta V / I_D \tag{4.1}$$

Definitions:

- C_D = delay capacitor

Circuit description

- t_D = reset delay time
- I_D = charge current, typical 14 µA
- $\Delta V = V_{UD}$, typical 1.8 V
- V_{UD} = upper delay timing threshold at C_D for reset delay time

The reset reaction time t_{rr} is the time it takes the voltage regulator to set the reset out LOW after the output voltage has dropped below the reset threshold. It is typically 1 µs for delay capacitor of 47 nF. For other values for C_d the reaction time can be estimated using the following equation:

$$t_{RR} \approx 20\ \text{s/F} \times C_d \qquad (4.2)$$

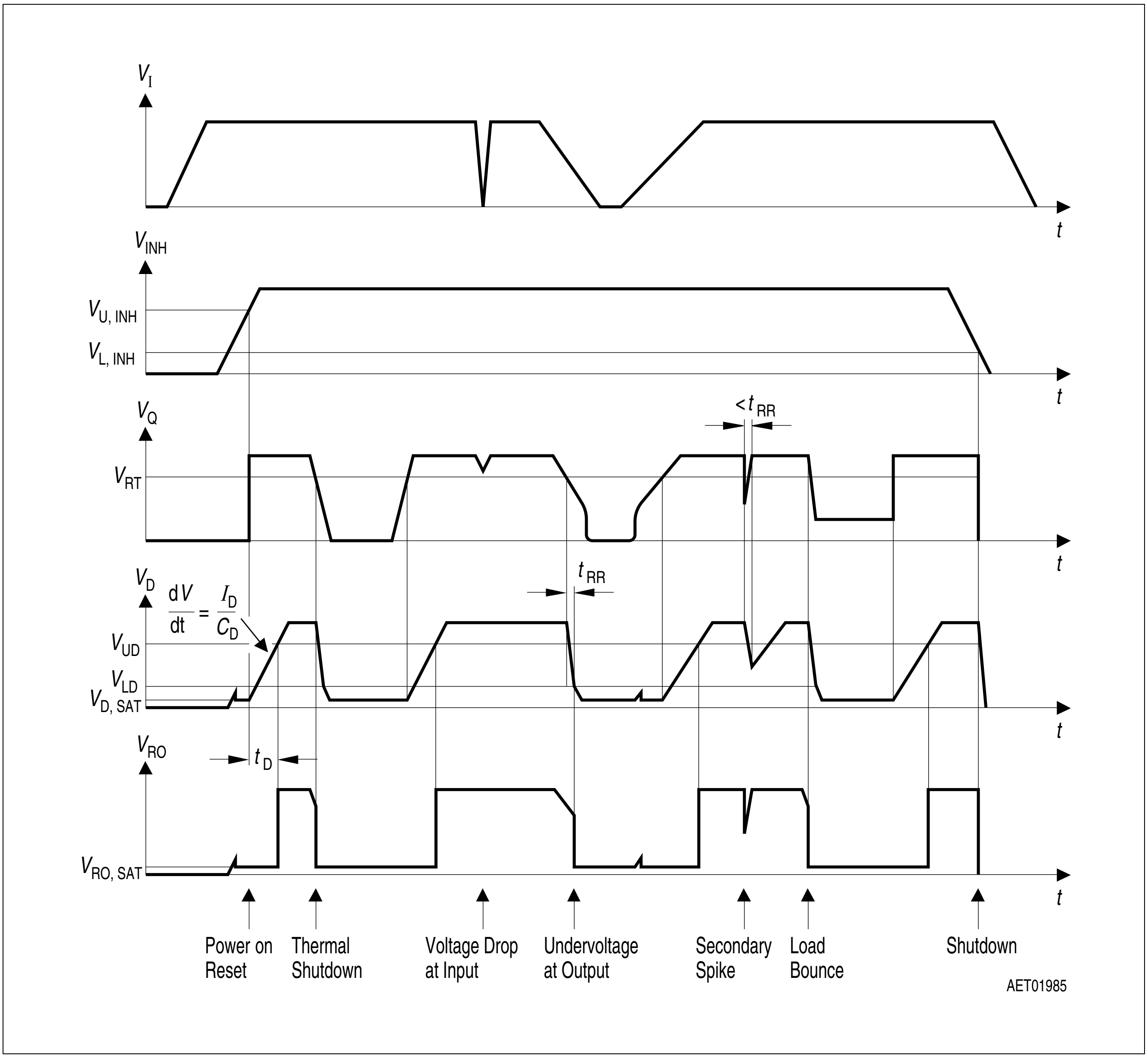


Figure 5 Time response

Watchdog timing

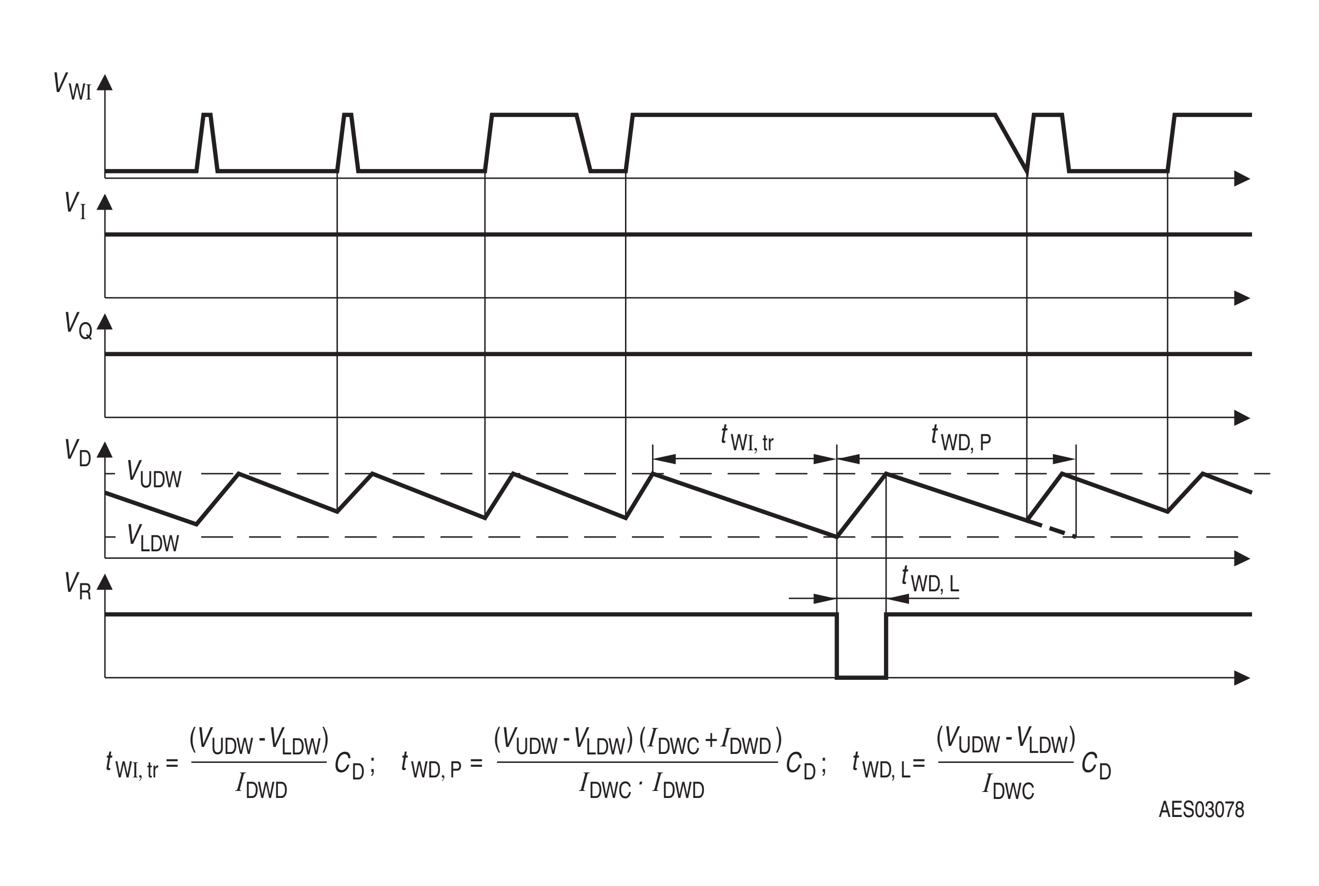
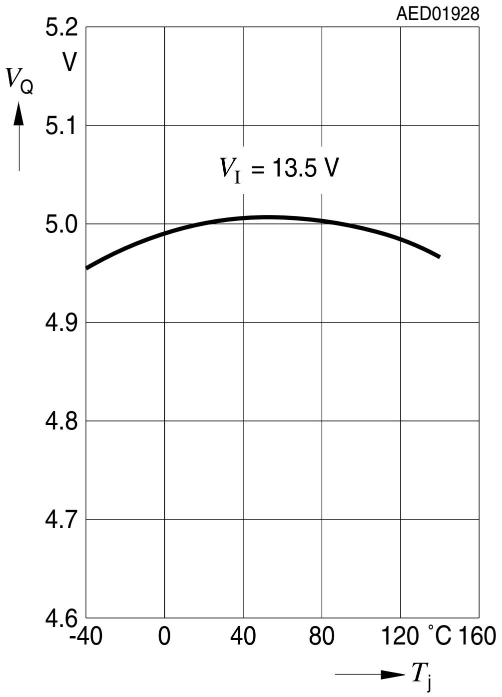


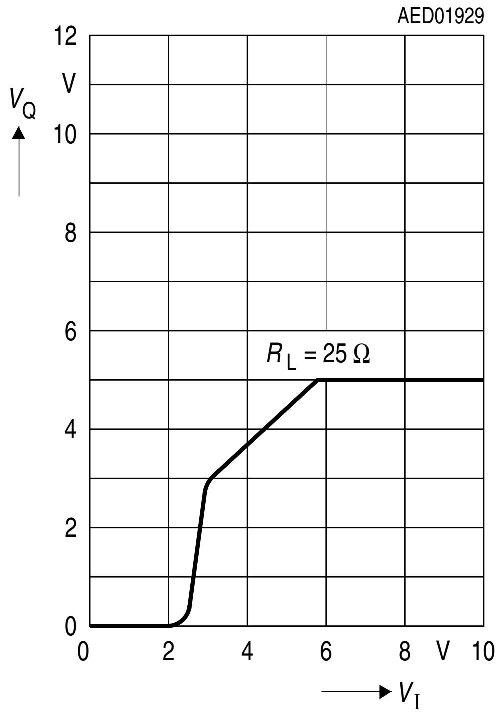
Figure 6 Time response, watchdog behavior

5 Typical performance characteristics

Output voltage V_Q versus junction temperature T_j

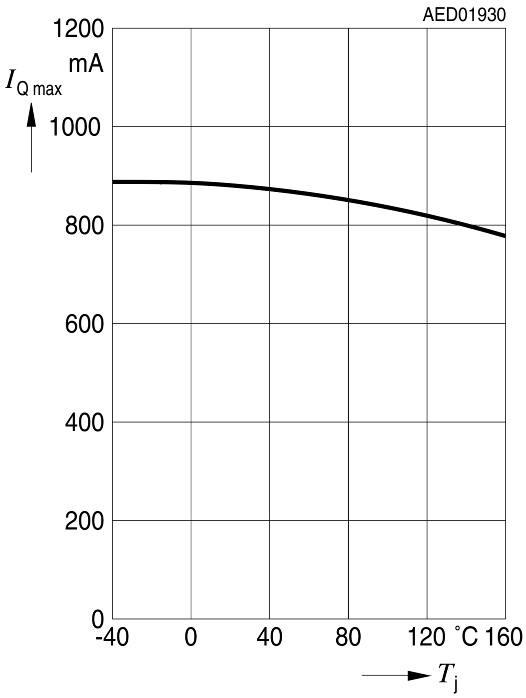


Output voltage V_Q versus input voltage V_I ($V_{INH} = V_I$)

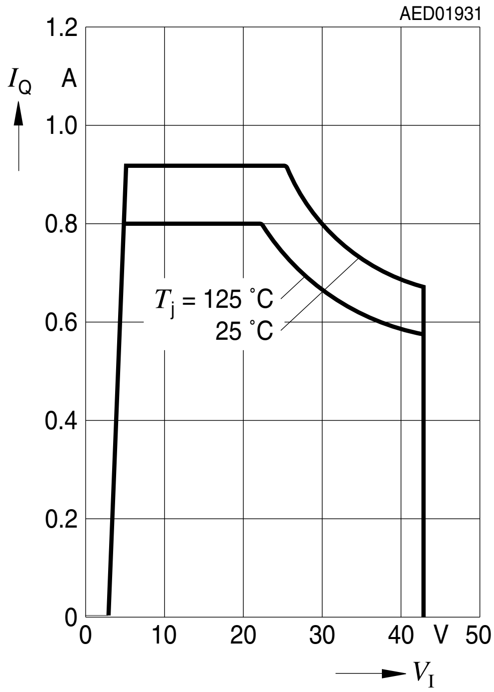


Typical performance characteristics

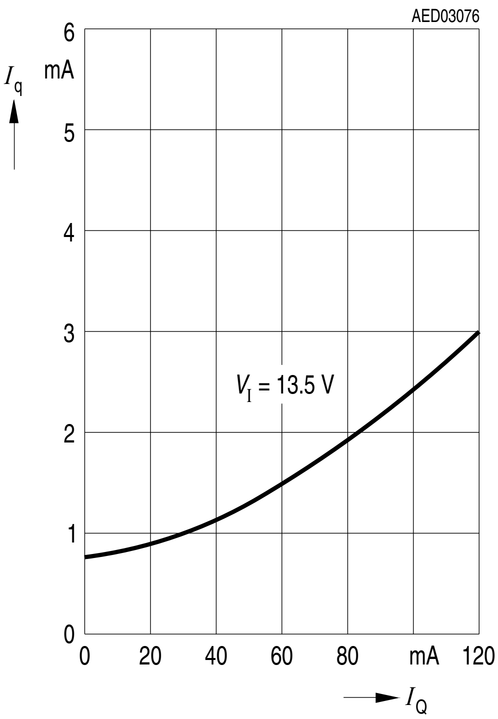
Output current limit I_Q versus junction temperature T_j



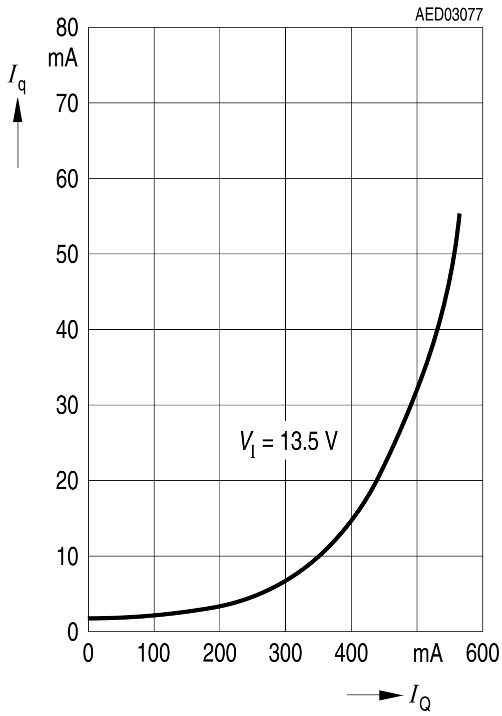
Output current I_Q versus input voltage V_I



Current consumption I_q versus output current I_Q

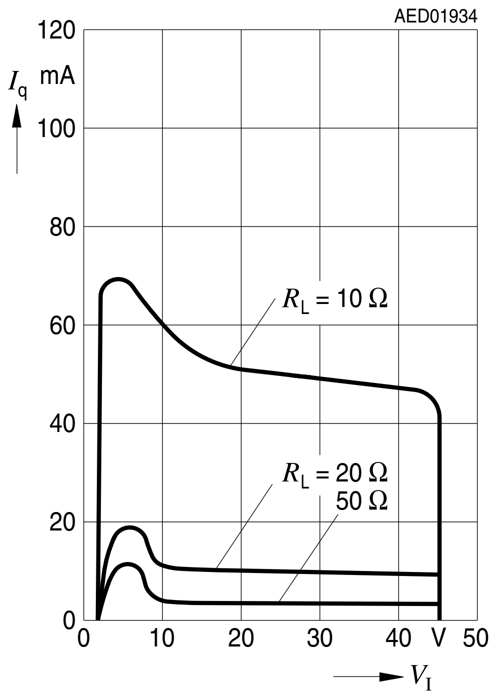


Current consumption I_q versus output current I_Q

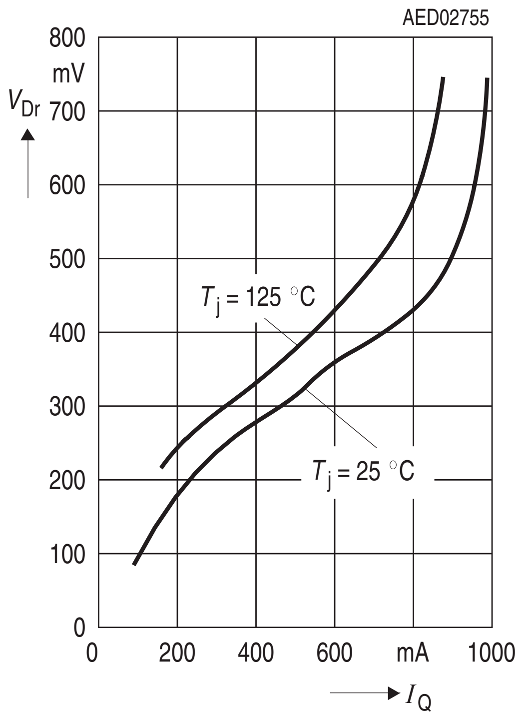


Typical performance characteristics

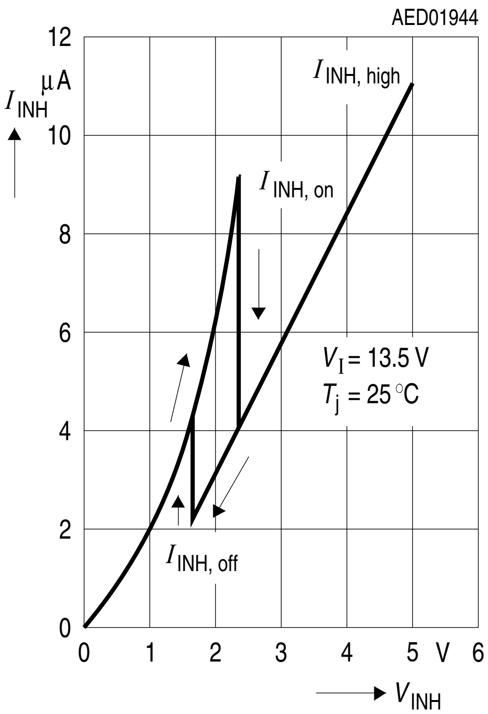
Current consumption I_q versus input voltage V_I



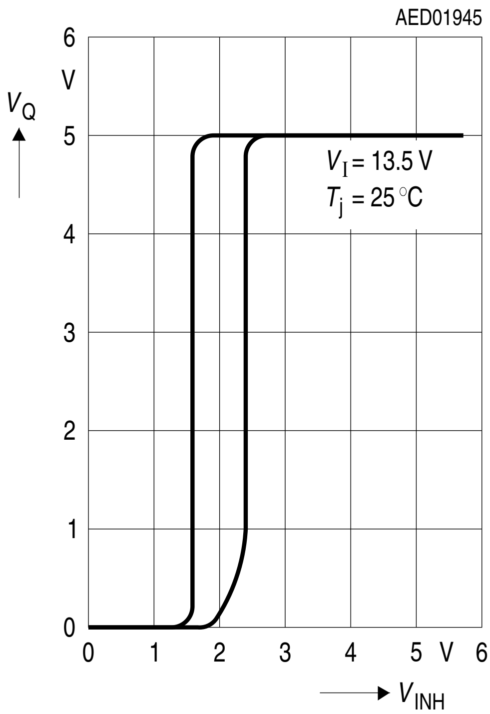
Drop voltage V_{dr} versus output current I_Q



Inhibit current I_{INH} versus inhibit voltage V_{INH}

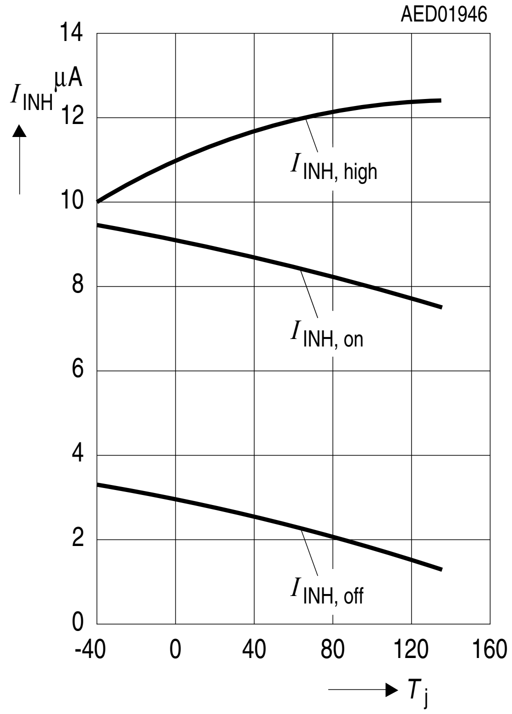


Output voltage V_Q versus inhibit voltage V_{INH}

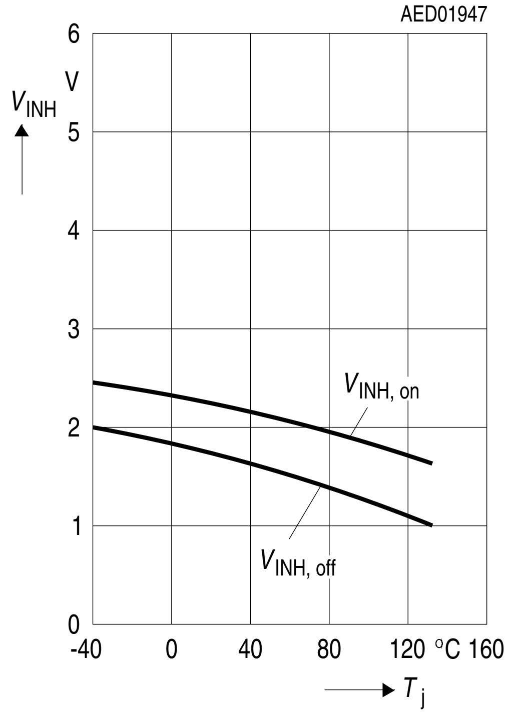


Typical performance characteristics

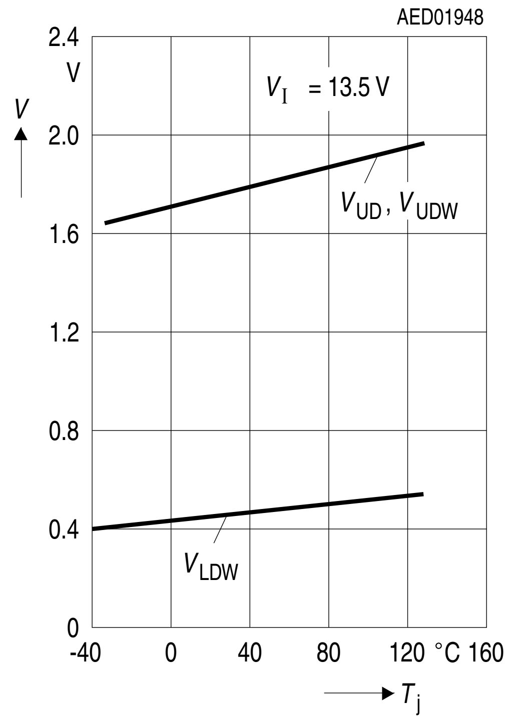
Inhibit current consumptions I_{INH} versus temperature T_j



Inhibit voltages V_{INH} versus junction temperature T_j

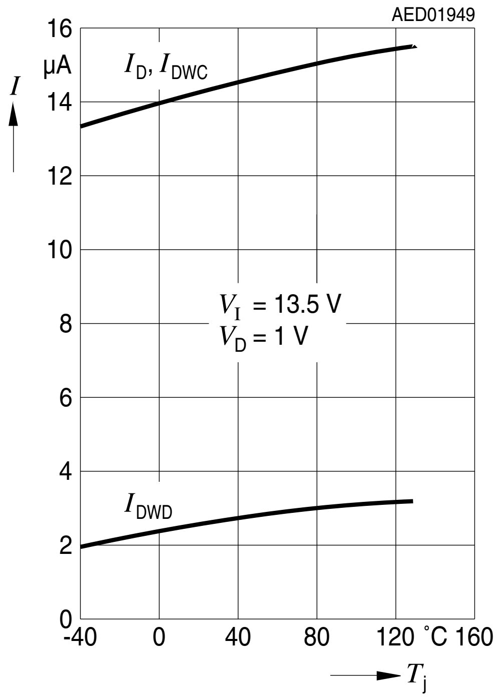


Switching voltage V_{UD} and V_{LDW} versus junction temperature T_j

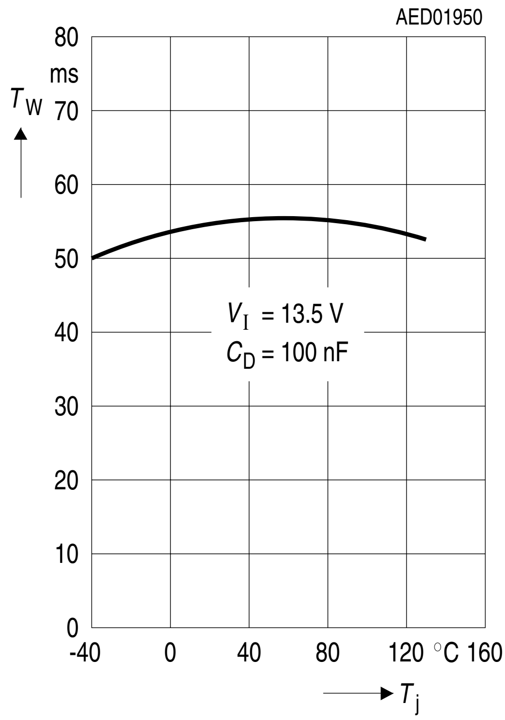


Typical performance characteristics

Charge current I_D, I_{DWC} and discharge current I_{DWD} versus junction temperature T_j



Watchdog pulse time T_w versus junction temperature T_j



6 Package information

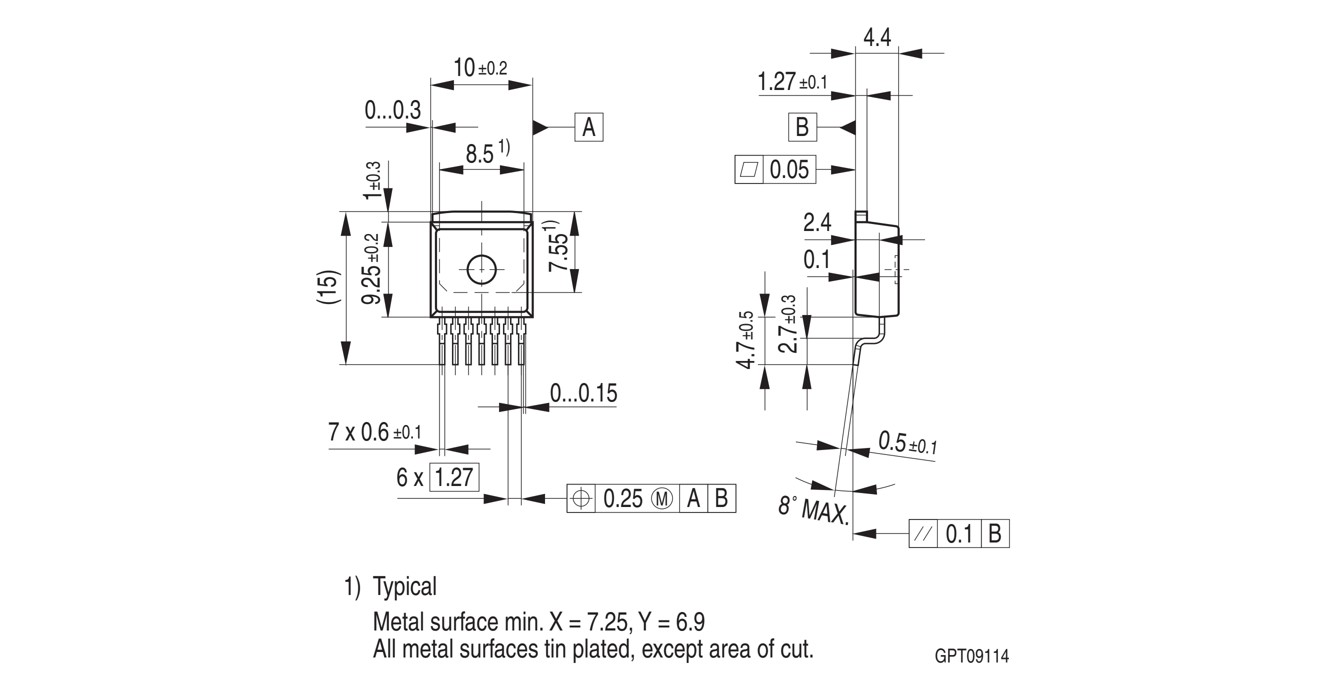


Figure 7 PG-TO263-7 (Plastic transistor single outline)[1)]

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e. Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

https://www.infineon.com/packages

1) Dimensions in mm

7 Revision history

Revision	Date	Changes
2.8	2019-07-30	Deleted both packages: PG-TO-220-7 Updated layout and structure frontpage: updated packaged drawings "TLE4271-2" Editorial changes
2.7	2007-03-20	Initial version of RoHS-compliant derivate of TLE4271-2 Page 1: AEC certified statement added Page 1 and Page 18ff: RoHS compliance statement and Green product feature added Page 1 and Page 18ff: Package changed to RoHS compliant version Legal Disclaimer updated

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