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Data Sheet, V 1.2, April 2008

# TDK5100F

434 MHz ASK/FSK Transmitter in 10-pin  
Package

Wireless Control  
Components



Never stop thinking.

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**TDK5100F****Revision History:**      **2008-04-04**

V 1.2

Previous Version:      V1.1 as of November 2005

Page	Subjects (major changes since last revision)
31-33, 35	Added Min.-/Max.-values of output power and supply current
31, 33, 35	Added values of frequency range and for possible extension of frequency range

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## 1 Product Description

### 1.1 Overview

The TDK 5100 F is a single chip ASK/FSK transmitter for operation in the frequency band 433-435 MHz. The IC offers a high level of integration and needs only a few external components. The device contains a fully integrated PLL synthesizer and a high efficiency power amplifier to drive a loop antenna. A special circuit design and an unique power amplifier design are used to save current consumption and therefore to save battery life. Additional features are a power down mode and a divided clock output.

### 1.2 Features

- fully integrated frequency synthesizer
- VCO without external components
- ASK and FSK modulation
- frequency range 433-435 MHz
- high efficiency power amplifier (typically 5 dBm)
- low supply current
- voltage supply range 2.1 ... 4 V
- temperature range -40 ... +125°C
- power down mode
- crystal oscillator 13.56 MHz
- FSK-switch
- divided clock output for  $\mu$ C
- low external component count

### 1.3 Application

- Tire pressure monitoring systems
- Keyless entry systems
- Remote control systems
- Alarm systems
- Communication systems

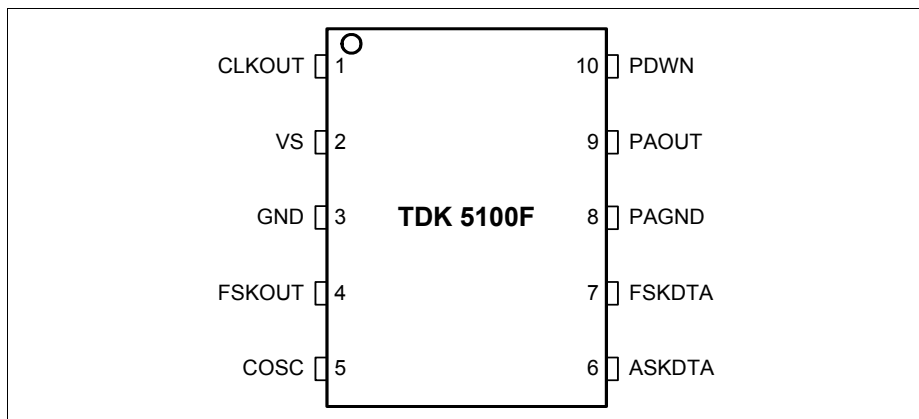
### 1.4 Order Information

**Table 1** Order Information

Type	Ordering Code	Package
TDK5100F	SP000014745	PG-TSSOP-10
available on tape and reel		

## 2 Functional Description

### 2.1 Pin Configuration



**Figure 1 IC Pin Configuration**

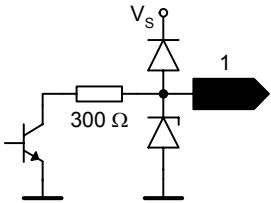
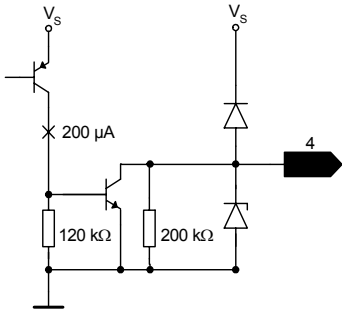
### 2.2 Pin Definition and Functions

**Table 2 Pin Definition and Functions - Overview**

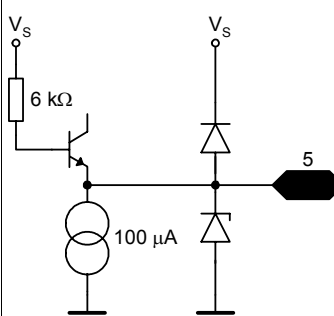
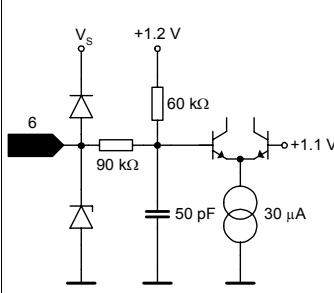
Pin No.	Symbol	Function
1	CLKOUT	Clock Driver Output (847.5 kHz)
2	VS	Voltage Supply
3	GND	Ground
4	FSKOUT	Frequency Shift Keying Switch Output
5	COSC	Crystal Oscillator Input (13.56 MHz)
6	ASKDTA	Amplitude Shift Keying Data Input
7	FSKDTA	Frequency Shift Keying Data Input
8	PAGND	Power Amplifier Ground
9	PAOUT	Power Amplifier Output (434 MHz)
10	PDWN	Power Down Mode Control

## Functional Description

**Table 3** Pin Definition and Function<sup>1)</sup>

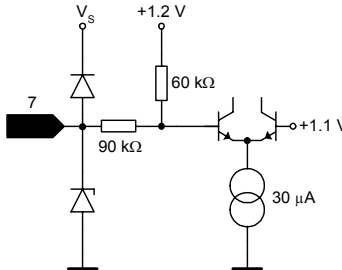
Pin No.	Symbol	Interface Schematic	Function
1	CLKOUT		<p>Clock output to supply an external device.</p> <p>An external pull-up resistor has to be added in accordance to the driving requirements of the external device.</p> <p>The clock frequency is 847.5 kHz.</p>
2	VS		<p>This pin is the positive supply of the transmitter electronics.</p> <p>An RF bypass capacitor should be connected directly to this pin and returned to GND (pin 3) as short as possible.</p>
3	GND		General ground connection.
4	FSKOUT		<p>This pin is connected to a switch to GND (pin 3).</p> <p>The switch is closed when the signal at FSKDTA (pin 7) is in a logic low state.</p> <p>The switch is open when the signal at FSKDTA (pin 7) is in a logic high state.</p> <p>FSKOUT can switch an additional capacitor to the reference crystal network to pull the crystal frequency by an amount resulting in the desired FSK frequency shift of the transmitter output frequency.</p>

### Functional Description

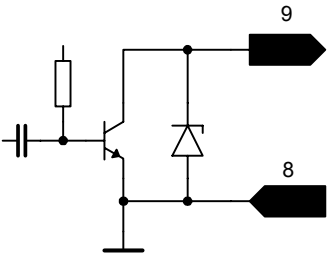
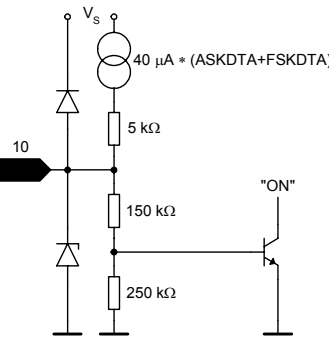
Pin No.	Symbol	Interface Schematic	Function
5	COSC	 <p>The schematic for the COSC pin shows a voltage source <math>V_S</math> connected to a <math>6\text{ k}\Omega</math> resistor. The other end of the resistor is connected to the base of an NPN transistor. The emitter of the transistor is connected to ground. The collector of the transistor is connected to the COSC pin (pin 5). The collector is also connected to a diode with its anode to <math>V_S</math> and its cathode to the collector. A <math>100\text{ }\mu\text{A}</math> current source is connected from the collector to ground.</p>	<p>This pin is connected to the reference oscillator circuit. The reference oscillator is working as a negative impedance converter. It presents a negative resistance in series to an inductance at the COSC pin.</p>
6	ASKDTA	 <p>The schematic for the ASKDTA pin shows a voltage source <math>V_S</math> connected to a diode with its anode to <math>V_S</math> and its cathode to the ASKDTA pin (pin 6). The ASKDTA pin is also connected to a <math>90\text{ k}\Omega</math> resistor. The other end of the resistor is connected to the base of an NPN transistor. The emitter of the transistor is connected to ground. The collector of the transistor is connected to a <math>+1.2\text{ V}</math> source through a <math>60\text{ k}\Omega</math> resistor. The collector is also connected to a <math>50\text{ pF}</math> capacitor to ground and a <math>30\text{ }\mu\text{A}</math> current source to ground. The collector is also connected to a diode with its anode to the collector and its cathode to ground. The collector is also connected to a <math>+1.1\text{ V}</math> source.</p>	<p>Digital amplitude modulation can be imparted to the Power Amplifier through this pin.</p> <p>A logic high (ASKDTA &gt; 1.5 V or open) enables the Power Amplifier.</p> <p>A logic low (ASKDTA &lt; 0.5 V) disables the Power Amplifier.</p>



**Functional Description**

Pin No.	Symbol	Interface Schematic	Function
7	FSKDTA		<p>Digital frequency modulation can be imparted to the Xtal Oscillator by this pin. The VCO-frequency varies in accordance to the frequency of the reference oscillator.</p> <p>A logic high (FSKDTA &gt; 1.5V or open) sets the FSK switch to a high impedance state.</p> <p>A logic low (FSKDTA &lt; 0.5 V) closes the FSK switch from FSKOUT (pin 4) to GND (pin 3). A capacitor can be switched to the reference crystal network this way. The Xtal Oscillator frequency will be shifted giving the designed FSK frequency deviation.</p>

### Functional Description

Pin No.	Symbol	Interface Schematic	Function
8	PAGND		Ground connection of the power amplifier. The RF ground return path of the power amplifier output PAOUT (pin 9) has to be concentrated to this pin.
9	PAOUT		RF output pin of the transmitter. A DC path to the positive supply VS has to be supplied by the antenna matching network.
10	PDWN		Disable pin for the complete transmitter circuit.  A logic low (PDWN < 0.7 V) turns off all transmitter functions.  A logic high (PDWN > 1.5 V) gives access to all transmitter functions.  PDWN input will be pulled up by 40 μA internally by either setting FSKDTA or ASKDTA to a logic high-state.

1) Indicated voltages and currents apply for PLL Enable Mode and Transmit Mode.  
In Power Down Mode, the values are zero or high-ohmic.

## 2.3 Functional Block Diagram

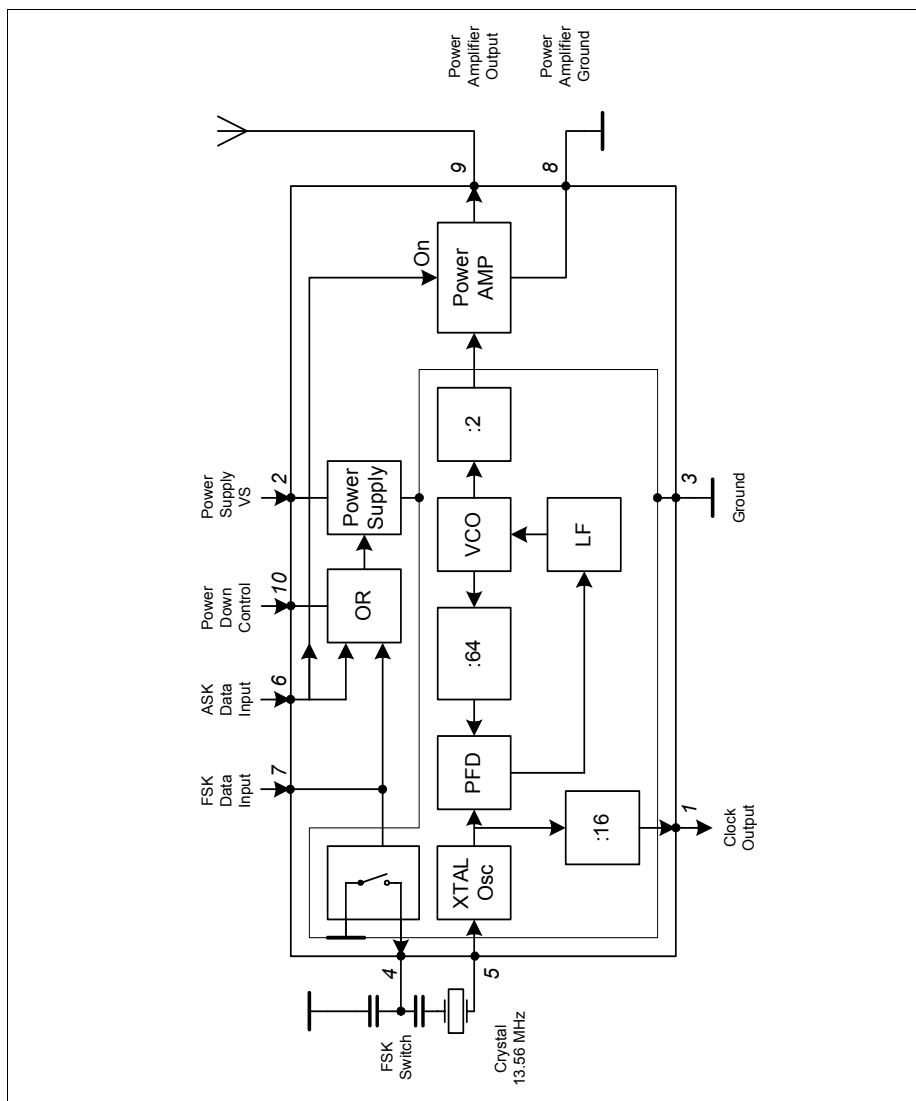


Figure 2 Functional Block Diagram

## 2.4 Functional Block Description

### 2.4.1 PLL Synthesizer

The Phase Locked Loop synthesizer consists of a Voltage Controlled Oscillator (VCO), an asynchronous divider chain, a phase detector, a charge pump and a loop filter. It is fully implemented on chip. The tuning circuit of the VCO consisting of spiral inductors and varactor diodes is on chip, too. Therefore no additional external components are necessary. The nominal center frequency of the VCO is 868 MHz. The oscillator signal is fed both, to the synthesizer divider chain and to the power amplifier. The overall division ratio of the asynchronous divider chain is 64. The phase detector is a Type IV PD with charge pump. The passive loop filter is implemented on chip.

### 2.4.2 Crystal Oscillator

The crystal oscillator operates at 13.56 MHz.

The crystal frequency is divided by 16. The resulting 847.5 kHz are available at the clock output CLKOUT (pin1) to drive the clock input of a micro controller.

To achieve FSK transmission, the oscillator frequency can be detuned by a fixed amount by switching an external capacitor via FSKOUT (pin 4).

The state of the switch is controlled by the signal at FSKDTA (pin 7).

**Table 4 FSKDTA - FSK Switch**

FSKDTA (pin7)	FSK Switch
Low <sup>1)</sup>	CLOSED
Open <sup>2)</sup> , High <sup>3)</sup>	OPEN

1) Low: Voltage at pin < 0.5V

2) Open: Pin open

3) High: Voltage at pin > 1.5V

### 2.4.3 Power Amplifier

The VCO frequency is divided by 2 and fed to the Power Amplifier.

The Power Amplifier can be switched on and off by the signal at ASKDTA (pin 6).

**Table 5 ASKDTA - Power Amplifier**

<b>ASKDTA (pin6)</b>	<b>Power Amplifier</b>
Low <sup>1)</sup>	OFF
Open <sup>2)</sup> , High <sup>3)</sup>	ON

1) Low: Voltage at pin < 0.5V

2) Open: Pin open

3) High: Voltage at pin > 1.5V

The Power Amplifier has an Open Collector output at PAOUT (pin 9) and requires an external pull-up coil to provide bias. The coil is part of the tuning and matching LC circuitry to get best performance with the external loop antenna. To achieve the best power amplifier efficiency, the high frequency voltage swing at PAOUT (pin 9) should be twice the supply voltage.

The power amplifier has its own ground pin PAGND (pin 8) in order to reduce the amount of coupling to the other circuits.

#### **2.4.4 Power Modes**

The IC provides three power modes, the POWER DOWN MODE, the PLL ENABLE MODE and the TRANSMIT MODE.

##### **2.4.4.1 Power Down Mode**

In the POWER DOWN MODE the complete chip is switched off.

The current consumption is typically 0.3 nA at 3 V 25°C.

This current doubles every 8°C. The values for higher temperatures are typically 14 nA at 85°C and typically 600 nA at 125°C.

##### **2.4.4.2 PLL Enable Mode**

In the PLL ENABLE MODE the PLL is switched on but the power amplifier is turned off to avoid undesired power radiation during the time the PLL needs to settle. The turn on time of the PLL is determined mainly by the turn on time of the crystal oscillator and is less than 1 ms when the specified crystal is used.

The current consumption is typically 3.5 mA (in PLL Enable Mode).

#### 2.4.4.3 Transmit Mode

In the TRANSMIT MODE the PLL is switched on and the power amplifier is turned on too. The current consumption of the IC is typically 7 mA when using a proper transforming network at PAOUT, see Figure 8.

#### 2.4.4.4 Power mode control

The bias circuitry is powered up via a voltage  $V > 1.5\text{ V}$  at the pin PDWN (pin10). When the bias circuitry is powered up, the pins ASKDTA and FSKDTA are pulled up internally.

Forcing the voltage at the pins low overrides the internally set state.

Alternatively, if the voltage at ASKDTA or FSKDTA is forced high externally, the PDWN pin is pulled up internally via a current source. In this case, it is not necessary to connect the PDWN pin, it is recommended to leave it open.

The principle schematic of the power mode control circuitry is shown in Figure 3

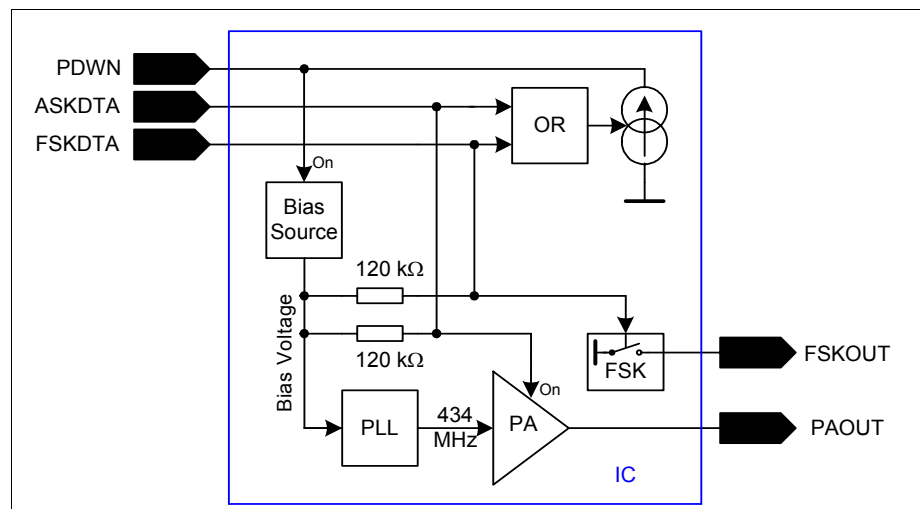


Figure 3 Power mode control circuitry

**Functional Description**

Table 6 provides a listing of how to get into the different power modes

**Table 6      Power Modes**

<b>PDWN</b>	<b>FSKDTA</b>	<b>ASKDTA</b>	<b>MODE</b>
Low <sup>1)</sup>	Low, Open	Low, Open	POWER DOWN
Open <sup>2)</sup>	Low	Low	
High <sup>3)</sup>	Low, Open, High	Low	PLL ENABLE
Open	High	Low	
High	Low, Open, High	Open, High	TRANSMIT
Open	High	Open, High	
Open	Low, Open, High	High	

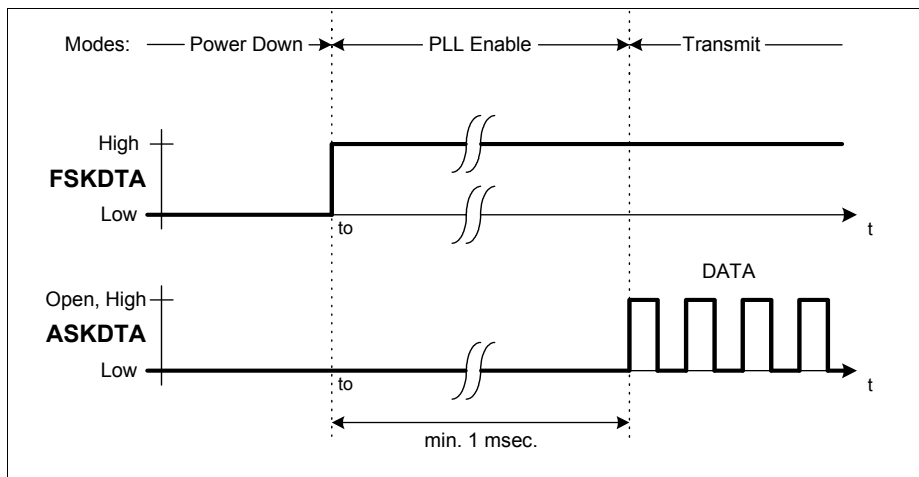
- 1) Low:                      Voltage at pin < 0.7V (PDWN)  
                                     Voltage at pin < 0.5V (FSKDTA, ASKDTA)
- 2) Open:                    Pin open
- 3) High:                    Voltage at pin > 1.5V

Other combinations of the control pins PDWN, FSKDTA and ASKDTA are not recommended.

## Functional Description

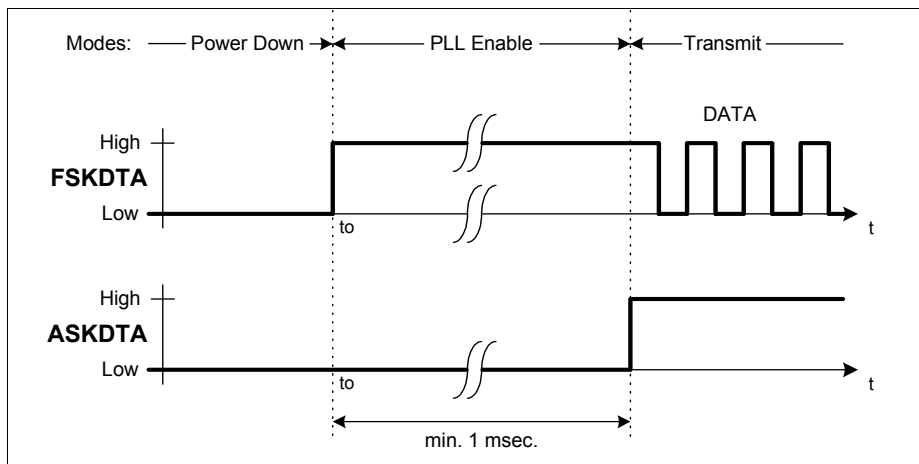
### 2.4.5 Recommended Timing Diagrams for ASK- and FSK-Modulation

ASK Modulation using FSKDTA and ASKDTA, PDWN not connected



**Figure 4 ASK Modulation**

FSK Modulation using FSKDTA and ASKDTA, PDWN not connected.

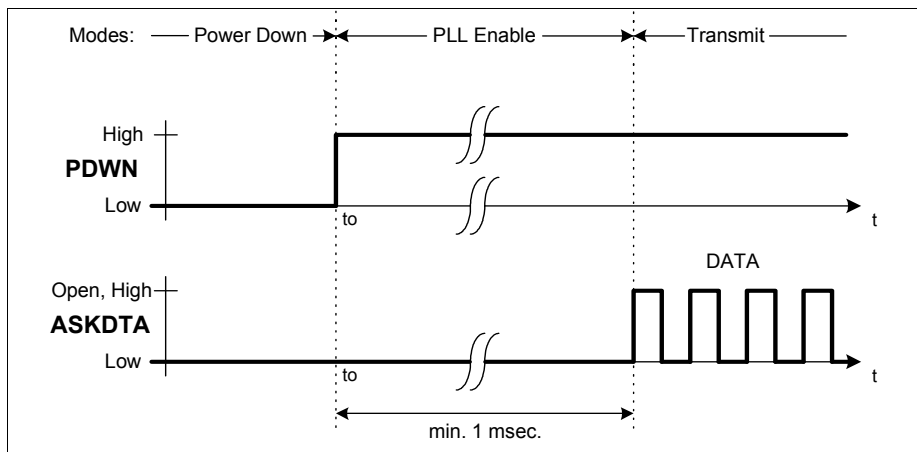


**Figure 5 FSK Modulation**



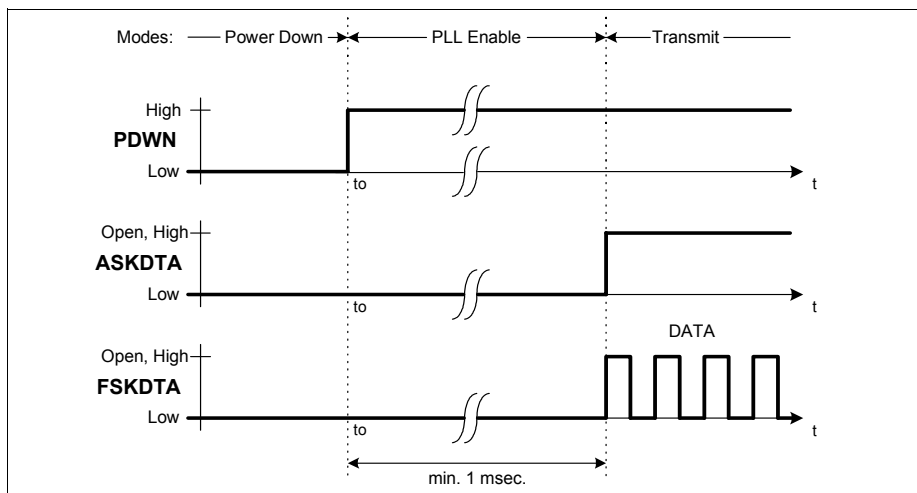
## Functional Description

Alternative ASK Modulation, FSKDTA not connected.



**Figure 6 Alternative ASK Modulation**

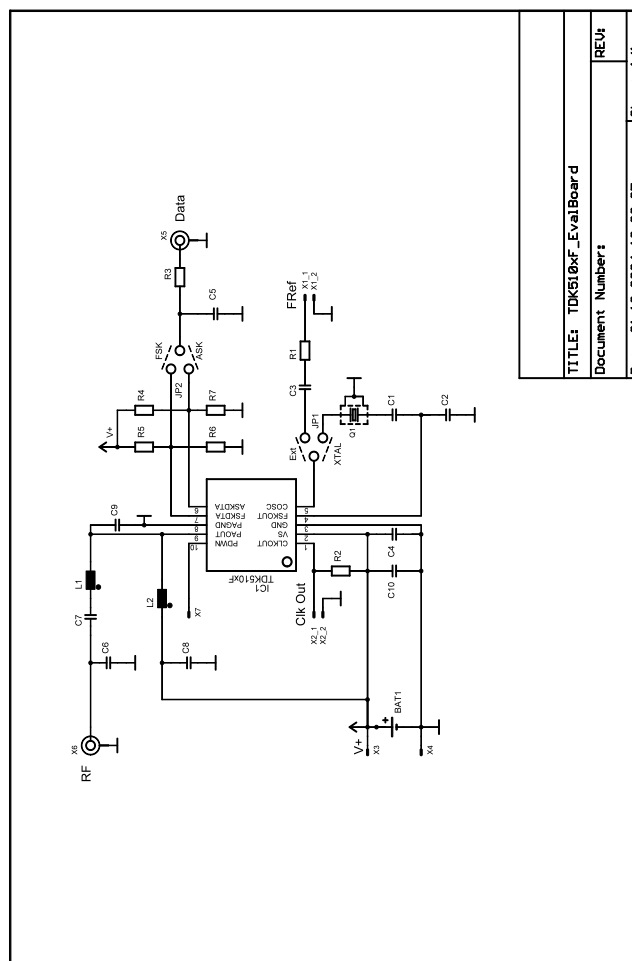
Alternative FSK Modulation



**Figure 7 Alternative FSK Modulation**

### 3 Applications

### 3.1 50 Ohm-Output Testboard Schematic



**Figure 8**      **50 Ohm-output testboard schematic**

### 3.2 50 Ohm-Output Testboard Layout

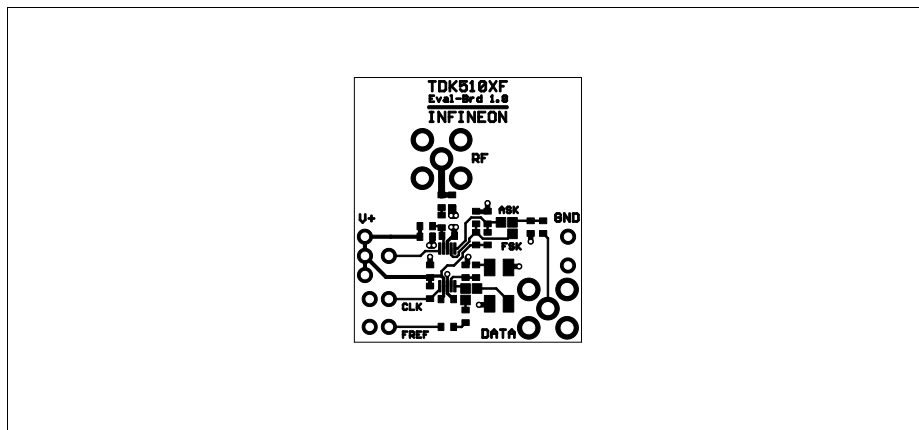


Figure 9 Top Side of TDK5100 F-Testboard with 50 Ohm-Output

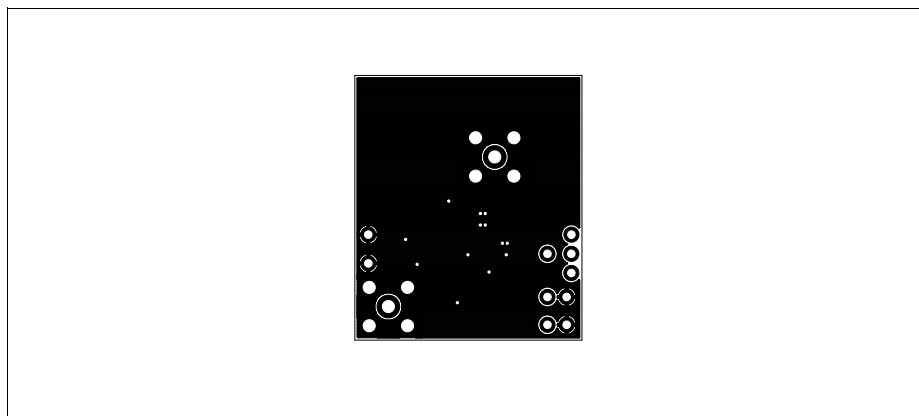


Figure 10 Bottom Side of TDK5100 F-Testboard with 50 Ohm-Output

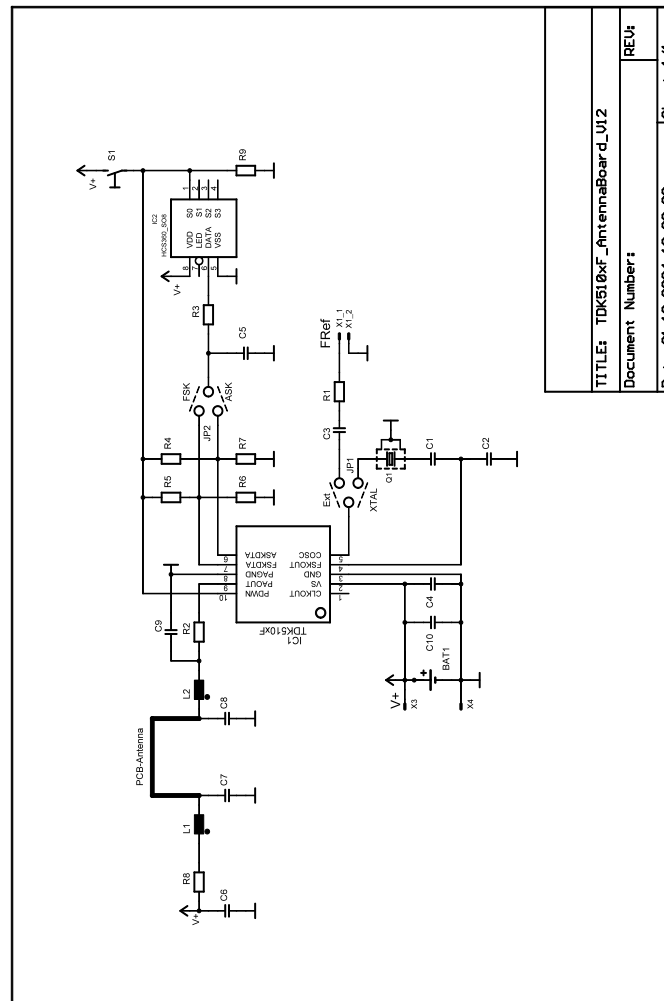
### 3.3 Bill of Material (50 Ohm-Output Evalboard)

Reference	Value	Specification
R1	open	
R2	open	
R3	4k7	0603, +/-5%
R4	12k	0603, +/-5%
R5	open	
R6	15k	0603, +/-5%
R7	open	
C1	10p	0603, C0G, +/-1%
C2	6p8	0603, C0G, +/-0,1p
C3	open	
C4	open	
C5	100p	0603, X7R, +/-10%
C6	12p	0603, C0G, +/-1%
C7	39p	0603, C0G, +/-1%
C8	330p	0603, C0G, +/-5%
C9	3p3	0603, C0G, +/-0,1p
C10	47n	0603, X7R, +/-10%
L1	47n	EPCOS SIMID 0603-C, +/-2%
L2	120n	EPCOS SIMID 0603-C, +/-2%
X1	n.e.	
X2	n.e.	
X3	Pin	single-pole connector, 2,54mm
X4	Pin	single-pole connector, 2,54mm
X5	SMA-connector	
X6	SMA-connector	
X7	n.e.	
JP1	solder bridge	in position "XTAL"
JP2	solder bridge	in position "FSK"
Q1	13,56875 MHz,	Tokyo Denpa TSS-3B 13,56875 MHz Spec.No. 10-50205
IC1	TDK5100F	

**Please note:**

If R2 is placed (Clk Out is activated) a 47nF capacitor has to be used for C4.

### 3.4 Stripline-Antenna Testboard Schematic



**Figure 11 Stripline-antenna testboard schematic**

### 3.5 Stripline-Antenna Testboard Layout

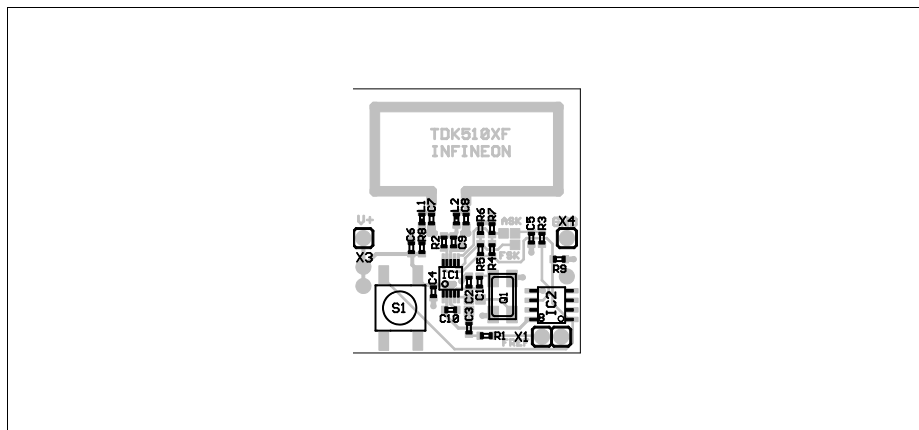


Figure 12 Top Side of TDK5100 F-Testboard with Stripline-Antenna

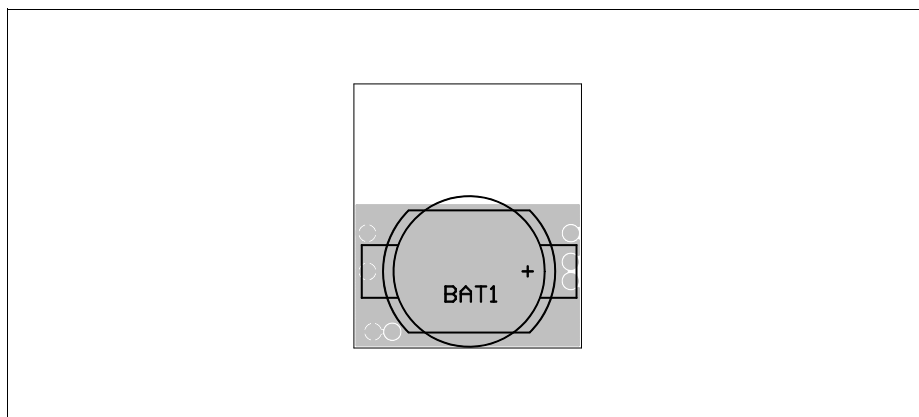


Figure 13 Bottom Side of TDK5100 F-Testboard with Stripline-Antenna

Please note that this board layout may be used for both high- and low-power applications, see also the bill of materials on the subsequent pages.

In case of ASK operation the solder bridge JP2 has to be shortened in the “ASK”-position, in case of FSK modulation in the “FSK” position.

Solder bridge JP1 between C1, C2 and C3 gives a choice of operating the board with the on-board crystal as reference (“XTAL” shortened, i.e. close to C1 and C2) or with an external clock generator (solder bridge shorts pads between C3 and C2).

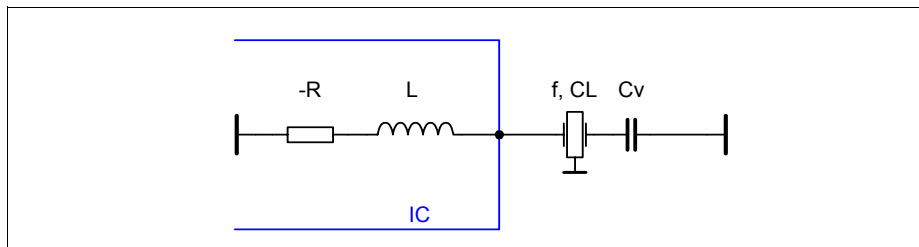
### 3.6 Bill of Material (Antenna board) FSK modulation

Reference	Value	Specification
R1	open	
R2	0R	0603, SMD-Jumper
R3	0R	0603, SMD-Jumper
R4	82k	0603, +/-5%
R5	open	
R6	open	
R7	100n	0603, X7R, +/-10%
R8	39R	0603, +/-1%
R9	15k	0603, +/-5%
C1	10p	0603, C0G, +/-1%
C2	6p8	0603, C0G, +/-0,1p
C3	open	
C4	open	
C5	open	
C6	10n	0603, X7R, +/-10%
C7	5p6	0603, C0G, +/-0,1p
C8	open	
C9	4p7	0603, C0G, +/-0,1p
C10	47n	0603, X7R, +/-10%
L1	100n	0603, EPCOS SIMID, +/-2%
L2	0R	0603, SMD-Jumper
X1	n.e.	
X3	n.e.	
X4	n.e.	
S1	push-button	STTSKHMPW, ALPS
JP1	solder bridge	in position "XTAL"
JP2	solder bridge	in position "FSK"
Q1	13,56875 MHz,	Tokyo Denpa TSS-3B 13,56875 MHz Spec.No. 10-
IC1	TDK5100F	P-TSSOP-10
IC2	HCS360	SO8
BAT1	battery holder	HU2031-1, Renata
	battery	CR2032, Renata

### 3.7 Application Hints on the Crystal Oscillator

#### Application Hints on the crystal oscillator

The crystal oscillator achieves a turn on time less than 1 msec when the specified crystal is used. To achieve this, a NIC oscillator type is implemented in the TDK 5100 F. The input impedance of this oscillator is a negative resistance in series to an inductance. Therefore the load capacitance of the crystal CL (specified by the crystal supplier) is transformed to the capacitance Cv.



**Figure 14 Application Hints**

Formula 1:

$$C_v = \frac{1}{\frac{1}{CL} + \omega^2 L}$$

CL: crystal load capacitance for nominal frequency

$\omega$ : angular frequency

L: inductance of the crystal oscillator

#### Example for the ASK-Mode:

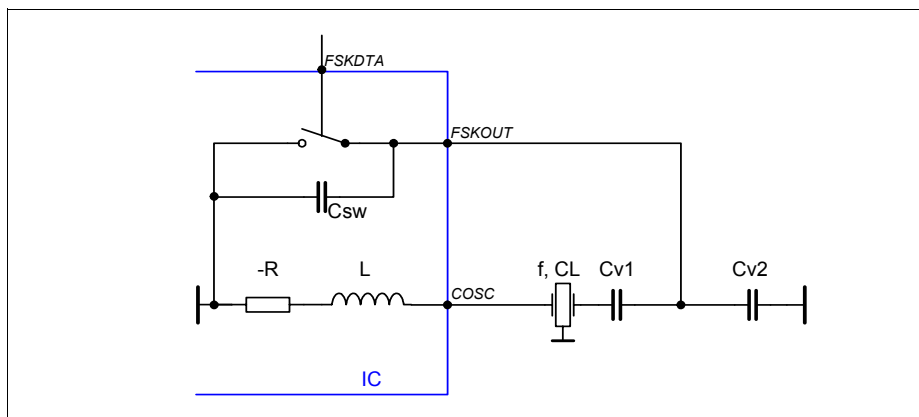
Referring to the application circuit, in ASK-Mode the capacitance C2 is replaced by a short to ground. Assume a crystal frequency of 13.56MHz and a crystal load capacitance of CL = 12 pF. The inductance L at 13.56MHz is about 4.6  $\mu$ H. Therefore C1 is calculated to 10 pF.

$$C_v = \frac{1}{\frac{1}{CL} + \omega^2 L} = C1$$



### Example for the FSK-Mode:

FSK modulation is achieved by switching the load capacitance of the crystal as shown below.



**Figure 15 FSK Mode**

The frequency deviation of the crystal oscillator is multiplied with the divider factor N of the Phase Locked Loop to the output of the power amplifier. In case of small frequency deviations (up to +/- 1000 ppm), the two desired load capacitances can be calculated with the formula below.

$$CL_{\pm} = \frac{CL \mp C_0 \frac{\Delta f}{N * f_1} (1 + \frac{2(C_0 + CL)}{C_1})}{1 \pm \frac{\Delta f}{N * f_1} (1 + \frac{2(C_0 + CL)}{C_1})}$$

- $C_L$ : crystal load capacitance for nominal frequency
- $C_0$ : shunt capacitance of the crystal
- $f$ : frequency
- $\omega$ :  $\omega = 2\pi f$ : angular frequency
- $N$ : division ratio of the PLL
- $df$ : peak frequency deviation

Because of the inductive part of the TDK 5100 F, these values must be corrected by Formula 1 on the preceding page.

The value of  $C_{v\pm}$  can be calculated as

$$C_{v\pm} = \frac{1}{\frac{1}{CL_{\pm}} + \omega^2 L}$$

If the FSK switch is closed,  $C_{v-}$  is equal to  $C_{v1}$  (C1 in the application diagram). If the FSK switch is open,  $C_{v2}$  (C2 in the application diagram) can be calculated.

$$C_{v2} = C2 = \frac{C_{sw} * C_{v1} - (C_{v+}) * (C_{v1} + C_{sw})}{(C_{v+}) - C_{v1}}$$

$C_{sw}$ : parallel capacitance of the FSK switch (3 pF incl. layout parasitics)

Remark: These calculations are only approximations. The necessary values depend on the layout also and must be adapted for the specific application board.

### 3.8 Design Hints on the Clock Output (CLKOUT)

The CLKOUT pin is an open collector output. An external pull up resistor ( $R_L$ ) should be connected between this pin and the positive supply voltage. The value of  $R_L$  is depending on the clock frequency and the load capacitance  $CLD$  (PCB board plus input capacitance of the microcontroller).  $R_L$  can be calculated to:

$$R_L = \frac{1}{f_{CLKOUT} * 8 * CLD}$$

**Table 7 Clock Output**

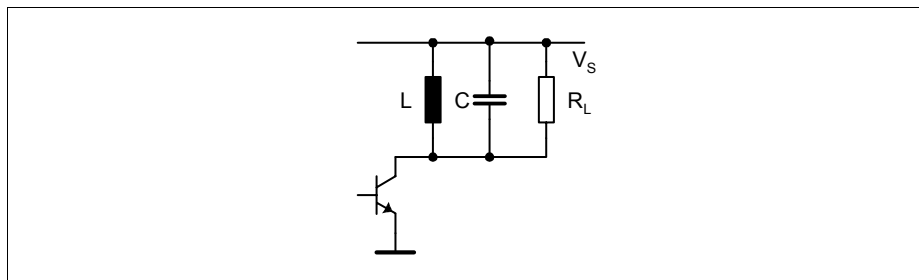
<b>fCLKOUT=847.5 kHz</b>	
<b>CL[pF]</b>	<b>RL[kOhm]</b>
5	27
10	12
20	6.8

Remark: To achieve a low current consumption and a low spurious radiation, the largest possible  $R_L$  should be chosen.

Even harmonics of the signal at CLKOUT can interact with the crystal oscillator input COSC preventing the start-up of oscillation. Care must be taken in layout by sufficient separation of the signal lines to ensure sufficiently small coupling.

### 3.9 Application Hints on the Power-Amplifier

The power amplifier operates in a high efficient class C mode. This mode is characterized by a pulsed operation of the power amplifier transistor at a current flow angle of  $\theta < \pi$ . A frequency selective network at the amplifier output passes the fundamental frequency component of the pulse spectrum of the collector current to the load. The load and its resonance transformation to the collector of the power amplifier can be generalized by the equivalent circuit of Figure 16. The tank circuit L//C//RL in parallel to the output impedance of the transistor should be in resonance at the operating frequency of the transmitter.



**Figure 16** Equivalent power amplifier tank circuit

The optimum load at the collector of the power amplifier for “critical” operation under idealized conditions at resonance is:

$$R_{LC} = \frac{V_s^2}{2 * P_o}$$

The theoretical value of  $R_{LC}$  for an RF output power of  $P_o = 5$  dBm (3.16 mW) is:

$$R_{LC} = \frac{3^2}{2 * 0.00316} = 1423 \Omega$$

“Critical” operation is characterized by the RF peak voltage swing at the collector of the PA transistor to just reach the supply voltage  $V_s$ .

The high degree of efficiency under “critical” operating conditions can be explained by the low power losses at the transistor. During the conducting phase of the transistor, its collector voltage is very small. This way the power loss of the transistor, equal to  $i_C * u_{CE}$  is minimized. This is particularly true for small current flow angles of  $\theta < \pi$ .

## Applications

In practice the RF-saturation voltage of the PA transistor and other parasitics reduce the “critical”  $R_{LC}$ .

The output power  $P_o$  is reduced by operating in an “overcritical” mode characterised by  $R_L > R_{LC}$ .

The power efficiency (and the bandwidth) increase when operating at a slightly higher  $R_L$ , as shown in Figure 17.

The collector efficiency  $E$  is defined as

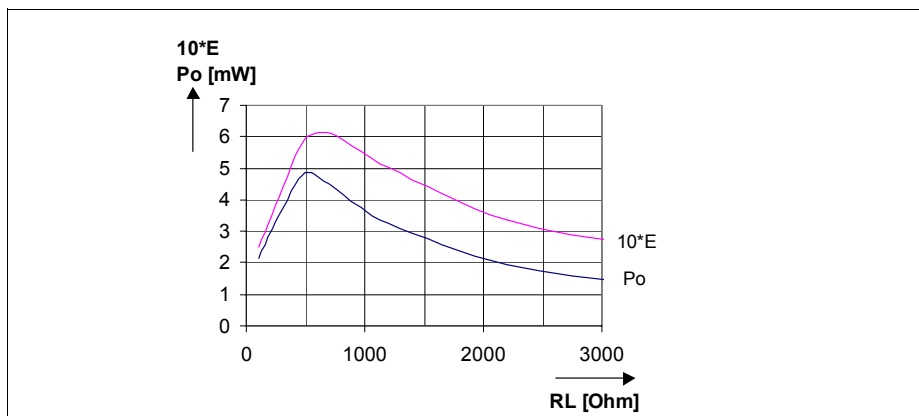
$$E = \frac{P_o}{V_s I_c}$$

The diagram of Figure 17 was measured directly at the PA-output at  $V_s = 3$  V. Losses in the matching circuitry decrease the output power by about 1.5 dB. As can be seen from the diagram,  $550 \Omega$  is the optimum impedance for operation at 3 V. For an approximation of  $R_{OPT}$  and  $P_{OUT}$  at other supply voltages those two formulas can be used:

$$R_{OPT} \sim V_s$$

and

$$P_{OUT} \sim R_{OPT}$$



**Figure 17** Output power  $P_o$  (mW) and collector efficiency  $E$  vs. load resistor  $R_L$ .

The DC collector current  $I_c$  of the power amplifier and the RF output power  $P_o$  vary with the load resistor  $R_L$ . This is typical for overcritical operation of class C amplifiers. The collector current will show a characteristic dip at the resonance frequency for this type of “overcritical” operation. The depth of this dip will increase with higher values of  $R_L$ .

## 4 Reference

### 4.1 Electrical Data

#### 4.1.1 Absolute Maximum Ratings

**Attention:** *The maximum ratings must not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the IC will result.*

**Table 8** Absolute Maximum Ratings,  $T_{\text{amb}} = -40\text{ °C} \dots +125\text{ °C}$

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Junction Temperature	$T_J$	-40	+150	°C	
Storage Temperature	$T_s$	-40	+125	°C	
Thermal Resistance	$R_{\text{thJA}}$		220	K/W	
Supply voltage	$V_S$	-0.3	+4.0	V	
Voltage at any pin excluding pin 9	$V_{\text{pins}}$	-0.3	$V_S + 0.3$	V	
Voltage at pin 9	$V_{\text{pin9}}$	-0.3	$2 * V_S$	V	No ESD-Diode to $V_S$
ESD integrity, all pins	$V_{\text{ESD}}$	-1	+1	kV	JEDEC Standard JESD22-A114-B
ESD integrity, all pins excluding pin 9	$V_{\text{ESD}}$	-2	+2	kV	JEDEC Standard JESD22-A114-B

Ambient Temperature under bias:  $T_A = -40\text{ °C}$  to  $+125\text{ °C}$

Note: All voltages referred to ground (pins) unless stated otherwise.

Pins 3 and 8 are grounded.

## 4.2 Operating Ratings

Within the operational range the IC operates as described in the circuit description.

**Table 9 Operating Ratings**

Parameter	Symbol	Limit Values		Unit	Test Conditions
		min.	max.		
Supply voltage	$V_S$	2.1	4.0	V	
Ambient temperature	$T_A$	-40	125	°C	

## 4.3 AC/DC Characteristics

AC/DC characteristics involve the spread of values guaranteed within the specified supply voltage and ambient temperature. Typical characteristics are the median of the production.

### 4.3.1 AC/DC Characteristic at 3V, 25°C

**Table 10 Supply Voltage  $V_S=3V$ , Ambient temperature  $T_{amb}=25^\circ C$**

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Current consumption						
Power Down mode	I <sub>S PDWN</sub>		0.3	100	nA	V (Pins 10, 6 and 7) < 0.2 V
PLL Enable mode	I <sub>S PLL_EN</sub>		3.5	4.2	mA	
Transmit mode 434 MHz	I <sub>S TRANSM</sub>		7.7	10.4	mA	
Output frequency						
Output frequency	f <sub>OUT</sub>	427	434.5	442	MHz	f <sub>OUT</sub> = 32 * f <sub>COSC</sub>
Clock Driver Output (Pin 1)						
Output current (High)	I <sub>CLKOUT</sub>			5	μA	V <sub>CLKOUT</sub> = V <sub>S</sub>
Saturation Voltage (Low) <sup>1)</sup>	V <sub>SATL</sub>			0.56	V	I <sub>CLKOUT</sub> = 1 mA

**Table 10** Supply Voltage  $V_S=3V$ , Ambient temperature  $T_{amb}=25^{\circ}C$  (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
FSK Switch Output (Pin 4)						
On resistance	$R_{FSKOUT}$			250	$\Omega$	$V_{FSKDTA} = 0\text{ V}$
On capacitance	$C_{FSKOUT}$			6	pF	$V_{FSKDTA} = 0\text{ V}$
Off resistance	$R_{FSKOUT}$	10			k $\Omega$	$V_{FSKDTA} = V_S$
Off capacitance	$C_{FSKOUT}$			1.5	pF	$V_{FSKDTA} = V_S$
Crystal Oscillator Input (Pin 5)						
Load capacitance	$C_{COSCmax}$			5	pF	
Serial Resistance of the crystal				100	$\Omega$	$f = 13.56\text{ MHz}$
Input inductance of the COSC pin			4.6		$\mu\text{H}$	$f = 13.56\text{ MHz}$
ASK Modulation Data Input (Pin 6)						
ASK Transmit disabled	$V_{ASKDTA}$	0		0.5	V	
ASK Transmit enabled	$V_{ASKDTA}$	1.5		$V_S$	V	
Input bias current ASKDTA	$I_{ASKDTA}$			30	$\mu\text{A}$	$V_{ASKDTA} = V_S$
Input bias current ASKDTA	$I_{ASKDTA}$	-20			$\mu\text{A}$	$V_{ASKDTA} = 0\text{ V}$
ASK data rate	$f_{ASKDTA}$			20	kHz	
FSK Modulation Data Input (Pin 7)						
FSK Switch on	$V_{FSKDTA}$	0		0.5	V	
FSK Switch off	$V_{FSKDTA}$	1.5		$V_S$	V	
Input bias current FSKDTA	$I_{FSKDTA}$			30	$\mu\text{A}$	$V_{FSKDTA} = V_S$
Input bias current FSKDTA	$I_{FSKDTA}$	-20			$\mu\text{A}$	$V_{FSKDTA} = 0\text{ V}$
FSK data rate	$f_{FSKDTA}$			20	kHz	
Power Amplifier Output (Pin 9)						
Output Power <sup>2)</sup> at 434 MHz transformed to 50 Ohm	$P_{OUT434}$	3.0	5.2	7.4	dBm	

**Table 10** Supply Voltage  $V_S=3V$ , Ambient temperature  $T_{amb}=25^{\circ}C$  (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Power Down Mode Control (Pin 10)						
Power Down mode	V <sub>PDWN</sub>	0		0.7	V	V <sub>ASKDTA</sub> < 0.2 V V <sub>FSKDTA</sub> < 0.2 V
PLL Enable mode	V <sub>PDWN</sub>	1.5		V <sub>S</sub>	V	V <sub>ASKDTA</sub> < 0.5 V
Transmit mode	V <sub>PDWN</sub>	1.5		V <sub>S</sub>	V	V <sub>ASKDTA</sub> > 1.5 V
Input bias current PDWN	I <sub>PDWN</sub>			30	μA	V <sub>PDWN</sub> = V <sub>S</sub>

- Derating linearly to a saturation voltage of max. 140 mV at  $I_{CLKOUT} = 0$  mA
- Power amplifier in overcritical C-operation  
Matching circuitry as used in the 50 Ohm-Output Testboard at the specified frequency.  
Tolerances of the passive elements not taken into account.

#### 4.3.2 AC/DC Characteristic at 2.1V ...4.0 V, $-40^{\circ}C$ ... $+125^{\circ}C$

**Table 11** Supply Voltage  $V_S=2.1V \dots 4.0V$ ,  $T_{amb}=-40^{\circ}C \dots +125^{\circ}C$ 

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Current consumption						
Power Down mode	I <sub>S PDWN</sub>			4	μA	V (Pins 10, 6 and 7) < 0.2 V
PLL Enable mode	I <sub>S PLL_EN</sub>		3.5	4.6	mA	
Transmit mode	I <sub>S TRANSMIT</sub>		7	10.2	mA	V <sub>S</sub> = 2.1 V
			7.7	10.9	mA	V <sub>S</sub> = 3 V
			8.1	11.4	mA	V <sub>S</sub> = 4 V
Output frequency						
Output frequency <sup>1)</sup>	f <sub>OUT</sub>		434		MHz	f <sub>OUT</sub> = 32 * f <sub>COSC</sub>
Clock Driver Output (Pin 1)						
Output current (High)	I <sub>CLKOUT</sub>			5	μA	V <sub>CLKOUT</sub> = V <sub>S</sub>
Saturation Voltage (Low) <sup>2)</sup>	V <sub>SATL</sub>			0.5	V	I <sub>CLKOUT</sub> = 0.6 mA



**Table 11** Supply Voltage  $V_S=2.1V \dots 4.0V$ ,  $T_{amb}=-40^{\circ}C \dots +125^{\circ}C$  (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
FSK Switch Output (Pin 4)						
On resistance	$R_{FSKOUT}$			280	$\Omega$	$V_{FSKDTA} = 0\text{ V}$
On capacitance	$C_{FSKOUT}$			6	pF	$V_{FSKDTA} = 0\text{ V}$
Off resistance	$R_{FSKOUT}$	10			k $\Omega$	$V_{FSKDTA} = V_S$
Off capacitance	$C_{FSKOUT}$			1.5	pF	$V_{FSKDTA} = V_S$
Crystal Oscillator Input (Pin 5)						
Load capacitance	$C_{COSCmax}$			5	pF	
Serial Resistance of the crystal				100	$\Omega$	$f = 13.56\text{ MHz}$
Input inductance of the COSC pin			4.6		$\mu\text{H}$	$f = 13.56\text{ MHz}$
ASK Modulation Data Input (Pin 6)						
ASK Transmit disabled	$V_{ASKDTA}$	0		0.5	V	
ASK Transmit enabled	$V_{ASKDTA}$	1.5		$V_S$	V	
Input bias current ASKDTA	$I_{ASKDTA}$			33	$\mu\text{A}$	$V_{ASKDTA} = V_S$
Input bias current ASKDTA	$I_{ASKDTA}$	-20			$\mu\text{A}$	$V_{ASKDTA} = 0\text{ V}$
ASK data rate	$f_{ASKDTA}$			20	kHz	
FSK Modulation Data Input (Pin 7)						
FSK Switch on	$V_{FSKDTA}$	0		0.5	V	
FSK Switch off	$V_{FSKDTA}$	1.5		$V_S$	V	
Input bias current FSKDTA	$I_{FSKDTA}$			33	$\mu\text{A}$	$V_{FSKDTA} = V_S$
Input bias current FSKDTA	$I_{FSKDTA}$	-20			$\mu\text{A}$	$V_{FSKDTA} = 0\text{ V}$
FSK data rate	$f_{FSKDTA}$			20	kHz	

**Table 11 Supply Voltage  $V_S=2.1V \dots 4.0V$ ,  $T_{amb}=-40^\circ C \dots +125^\circ C$  (cont'd)**

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Power Amplifier Output (Pin 9)						
Output Power <sup>3)</sup> at 434 MHz transformed to 50 Ohm.	P <sub>OUT, 434</sub>	-0.8	2.4	4.8	dBm	V <sub>S</sub> = 2.1 V
	P <sub>OUT, 434</sub>	0.0	5.2	7.7	dBm	V <sub>S</sub> = 3.0 V
	P <sub>OUT, 434</sub>	0.5	6.9	10.6	dBm	V <sub>S</sub> = 4.0 V
Power Down Mode Control (Pin 10)						
Power Down mode	V <sub>PDWN</sub>	0		0.5	V	V <sub>ASKDTA</sub> < 0.2 V V <sub>FSKDTA</sub> < 0.2 V
PLL Enable mode	V <sub>PDWN</sub>	1.5		V <sub>S</sub>	V	V <sub>ASKDTA</sub> < 0.5 V
Transmit mode	V <sub>PDWN</sub>	1.5		V <sub>S</sub>	V	V <sub>ASKDTA</sub> > 1.5 V
Input bias current PDWN	I <sub>PDWN</sub>			38	μA	V <sub>PDWN</sub> = V <sub>S</sub>

- 1) a) When the minimum  $T_A$  is increased by  $5^\circ C$ , the minimum  $f_{VCO}$  decreases by 1 MHz.  
b) When the maximum  $T_A$  is decreased by  $5^\circ C$ , the maximum  $f_{VCO}$  increases by 1 MHz.  
c) When the minimum  $V_S$  is increased by 25 mV, the maximum  $f_{VCO}$  increases by 1 MHz.  
Restriction of c): The maximum  $f_{VCO}$  must not be increased by more than 40 MHz by increasing  $V_S$ .

All three measures can be taken independently and additive.

- 2) Derating linearly to a saturation voltage of max. 140 mV at  $I_{CLKOUT} = 0$  mA

- 3) Matching circuitry as used in the 50 Ohm-Output Testboard.

Tolerances of the passive elements not taken into account.

Range @ 2.1 V,  $+25^\circ C$ : dBm +/- 2.0 dBm

Typ. temperature dependency at 2.1 V: + 0.4 dBm@ $-40^\circ C$  and - 1.3 dBm@ $+125^\circ C$ , reference  $+25^\circ C$

Range @ 3.0 V,  $+25^\circ C$ : 5.0 dBm +/- 2.2 dBm

Typ. temperature dependency at 3.0 V: + 0.4 dBm@ $-40^\circ C$  and - 2.4 dBm@ $+125^\circ C$ , reference  $+25^\circ C$

Range @ 4.0 V,  $+25^\circ C$ : dBm +/- 3.0 dBm

Typ. temperature dependency at 4.0 V: + 0.8 dBm@ $-40^\circ C$  and - 3.3 dBm@ $+125^\circ C$ , reference  $+25^\circ C$

## 5 Package Outlines

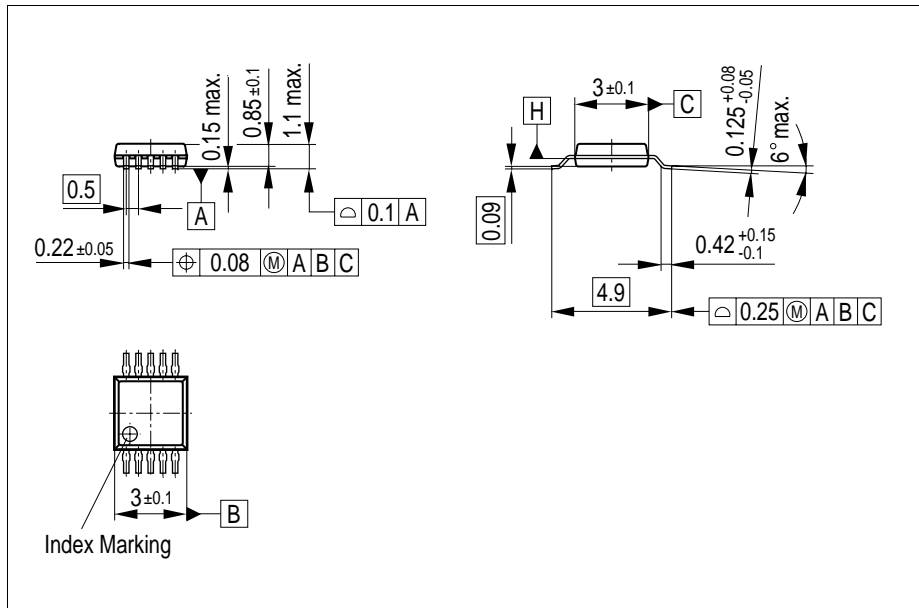


Figure 18 PG-TSSOP-10

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SMD = Surface Mounted Device

Dimensions in mm

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