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Data Sheet, V 1.0, May 2007

TDA7100

434 MHz ASK/FSK Transmitter in 10-pin Package

Wireless Control Components

Never stop thinking.

TDA7100

Revision History: **2007-05-02** V 1.0

Previous Version: none

Page	Subjects (major changes since last revision)

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1 Product Description

1.1 Overview

The TDA7100 is a single chip ASK/FSK transmitter for operation in the frequency band 433-435 MHz. The IC offers a high level of integration and needs only a few external components. The device contains a fully integrated PLL synthesizer and a high efficiency power amplifier to drive a loop antenna. A special circuit design and an unique power amplifier design are used to save current consumption and therefore to save battery life. Additional features are a power down mode and a divided clock output.

1.2 Features

- fully integrated frequency synthesizer
- VCO without external components
- ASK and FSK modulation
- frequency range 433-435 MHz
- high efficiency power amplifier (typically 5 dBm)
- low supply current
- voltage supply range 2.1 ... 4 V
- temperature range –20 ... +70°C
- power down mode
- crystal oscillator 13.56 MHz
- FSK-switch
- divided clock output for µC
- low external component count

1.3 Application

- Remote control systems
- Alarm systems
- Communication systems

Table 1 Order Information

Type	Ordering Code	Package
TDA7100	SP000296466	PG-TSSOP-10
available on tape and reel		

2 Functional Description

2.1 Pin Configuration

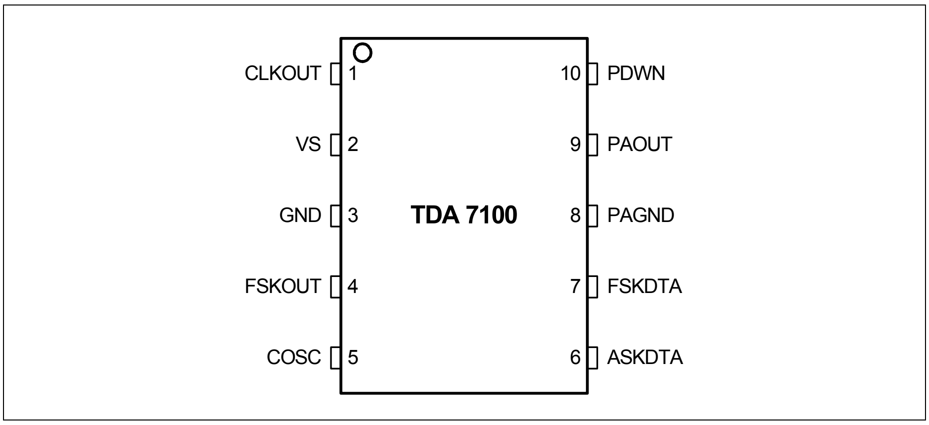

CLKOUT
1
VS
2
GND
3
FSKOUT
4
COSC
5
TDA 7100
10
PDWN
9
PAOUT
8
PAGND
7
FSKDTA
6
ASKDTA

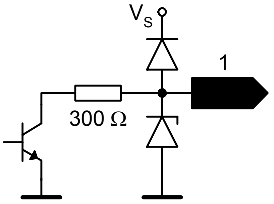
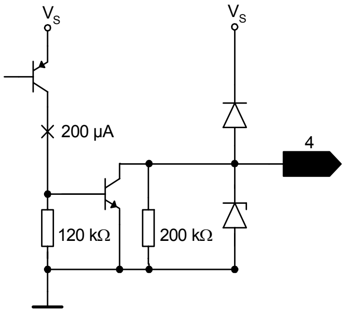
Figure 1 IC Pin Configuration

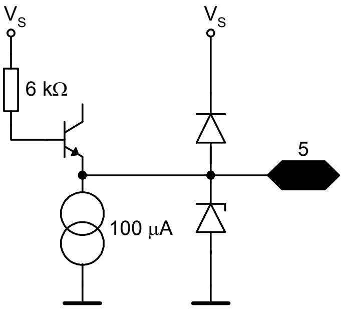
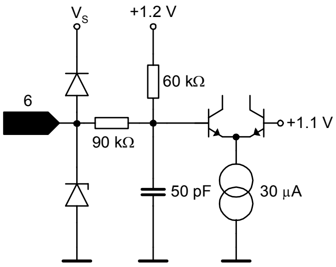
2.2 Pin Definition and Functions

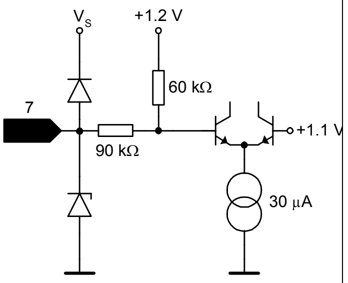
Table 2 Pin Definition and Functions - Overview

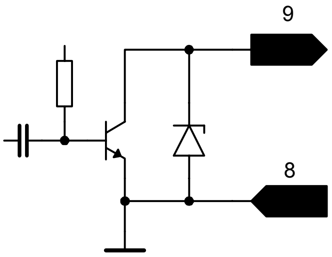
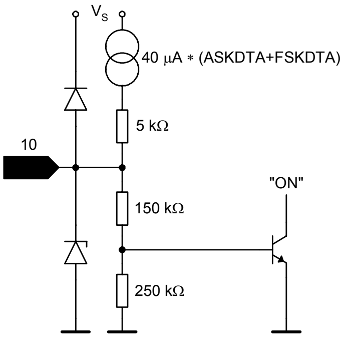
Pin No.	Symbol	Function
1	CLKOUT	Clock Driver Output (847.5 kHz)
2	VS	Voltage Supply
3	GND	Ground
4	FSKOUT	Frequency Shift Keying Switch Output
5	COSC	Crystal Oscillator Input (13.56 MHz)
6	ASKDTA	Amplitude Shift Keying Data Input
7	FSKDTA	Frequency Shift Keying Data Input
8	PAGND	Power Amplifier Ground
9	PAOUT	Power Amplifier Output (434 MHz)
10	PDWN	Power Down Mode Control

Table 3 Pin Definition and Function[1]

Pin No.	Symbol	Interface Schematic	Function
1	CLKOUT		Clock output to supply an external device. An external pull-up resistor has to be added in accordance to the driving requirements of the external device. The clock frequency is 847.5 kHz.
2	VS		This pin is the positive supply of the transmitter electronics. An RF bypass capacitor should be connected directly to this pin and returned to GND (pin 3) as short as possible.
3	GND		General ground connection.
4	FSKOUT	 V_S V_S 200 µA 4 120 kΩ 200 kΩ	This pin is connected to a switch to GND (pin 3). The switch is closed when the signal at FSKDTA (pin 7) is in a logic low state. The switch is open when the signal at FSKDTA (pin 7) is in a logic high state. FSKOUT can switch an additional capacitor to the reference crystal network to pull the crystal frequency by an amount resulting in the desired FSK frequency shift of the transmitter output frequency.

Pin No.	Symbol	Interface Schematic	Function
5	COSC		This pin is connected to the reference oscillator circuit. The reference oscillator is working as a negative impedance converter. It presents a negative resistance in series to an inductance at the COSC pin.
6	ASKDTA	 V_S +1.2 V 60 kΩ 6 +1.1 V 90 kΩ 50 pF 30 µA	Digital amplitude modulation can be imparted to the Power Amplifier through this pin. A logic high (ASKDTA > 1.5 V or open) enables the Power Amplifier. A logic low (ASKDTA < 0.5 V) disables the Power Amplifier.

Pin No.	Symbol	Interface Schematic	Function
7	FSKDTA		Digital frequency modulation can be imparted to the Xtal Oscillator by this pin. The VCO-frequency varies in accordance to the frequency of the reference oscillator. A logic high (FSKDTA > 1.5V or open) sets the FSK switch to a high impedance state. A logic low (FSKDTA < 0.5 V) closes the FSK switch from FSKOUT (pin 4) to GND (pin 3). A capacitor can be switched to the reference crystal network this way. The Xtal Oscillator frequency will be shifted giving the designed FSK frequency deviation.

Pin No.	Symbol	Interface Schematic	Function
8	PAGND		Ground connection of the power amplifier. The RF ground return path of the power amplifier output PAOUT (pin 9) has to be concentrated to this pin.
9	PAOUT		RF output pin of the transmitter. A DC path to the positive supply VS has to be supplied by the antenna matching network.
10	PDWN	 V_S 40 µA * (ASKDTA+FSKDTA) 5 kΩ 10 "ON" 150 kΩ 250 kΩ	Disable pin for the complete transmitter circuit. A logic low (PDWN < 0.7 V) turns off all transmitter functions. A logic high (PDWN > 1.5 V) gives access to all transmitter functions. PDWN input will be pulled up by 40 µA internally by either setting FSKDTA or ASKDTA to a logic high-state.

---

1) Indicated voltages and currents apply for PLL Enable Mode and Transmit Mode.
In Power Down Mode, the values are zero or high-ohmic.

2.3 Functional Block Diagram

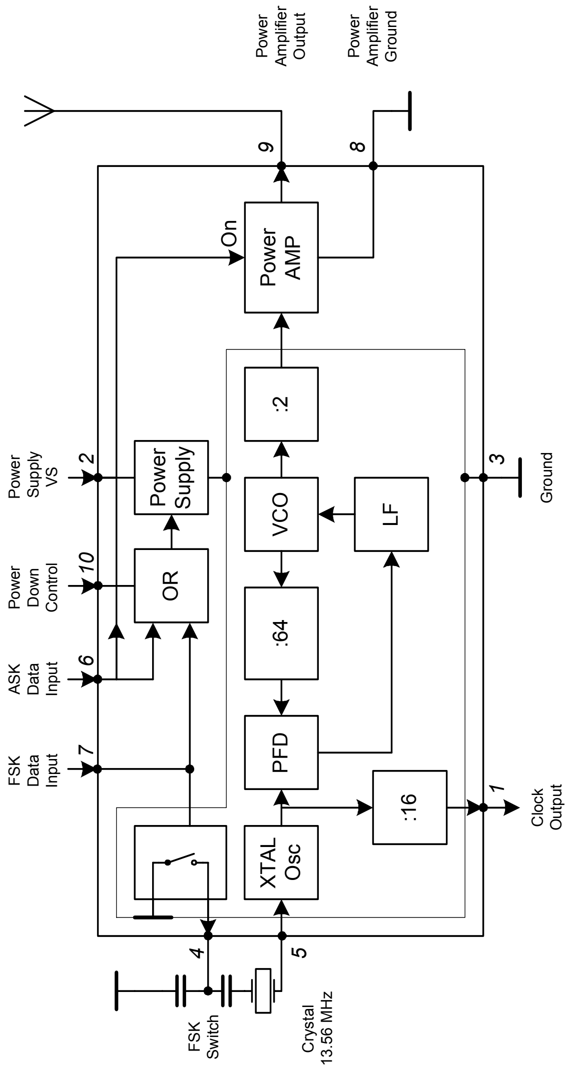

Power Amplifier Output
Power Amplifier Ground
9
8
On
Power AMP
:2
Power Supply VS
2
Power Supply
Power Down Control
10
OR
ASK Data Input
6
FSK Data Input
7
VCO
LF
3
Ground
:64
PFD
:16
1
Clock Output
XTAL Osc
4
5
FSK Switch
Crystal 13.56 MHz

Figure 2 **Functional Block Diagram**

2.4 Functional Block Description

2.4.1 PLL Synthesizer

The Phase Locked Loop synthesizer consists of a Voltage Controlled Oscillator (VCO), an asynchronous divider chain, a phase detector, a charge pump and a loop filter. It is fully implemented on chip. The tuning circuit of the VCO consisting of spiral inductors and varactor diodes is on chip, too. Therefore no additional external components are necessary. The nominal center frequency of the VCO is 868 MHz. The oscillator signal is fed both, to the synthesizer divider chain and to the power amplifier. The overall division ratio of the asynchronous divider chain is 64. The phase detector is a Type IV PD with charge pump. The passive loop filter is realized on chip.

2.4.2 Crystal Oscillator

The crystal oscillator operates at 13.56 MHz.

The crystal frequency is divided by 16. The resulting 847.5 kHz are available at the clock output CLKOUT (pin1) to drive the clock input of a micro controller.

To achieve FSK transmission, the oscillator frequency can be detuned by a fixed amount by switching an external capacitor via FSKOUT (pin 4).

The condition of the switch is controlled by the signal at FSKDTA (pin 7).

Table 4 FSKDTA - FSK Switch

FSKDTA (pin7)	FSK Switch
Low1)	CLOSED
Open2), High3)	OPEN

1) Low:	Voltage at pin < 0.5V
2) Open:	Pin open
3) High:	Voltage at pin > 1.5V

2.4.3 Power Amplifier

The VCO frequency is divided by 2 and fed to the Power Amplifier.

The Power Amplifier can be switched on and off
by the signal at ASKDTA (pin 6).

Table 5 ASKDTA - Power Amplifier

ASKDTA (pin6)	Power Amplifier
Low[1)]	OFF
Open[2)], High[3)]	ON

1) Low:	Voltage at pin < 0.5V
2) Open:	Pin open
3) High:	Voltage at pin > 1.5V

The Power Amplifier has an Open Collector output at PAOUT (pin 9) and requires an external pull-up coil to provide bias. The coil is part of the tuning and matching LC circuitry to get best performance with the external loop antenna. To achieve the best power amplifier efficiency, the high frequency voltage swing at PAOUT (pin 9) should be twice the supply voltage.

The power amplifier has its own ground pin PAGND (pin 8) in order to reduce the amount of coupling to the other circuits.

2.4.4 Power Modes

The IC provides three power modes, the POWER DOWN MODE, the PLL ENABLE MODE and the TRANSMIT MODE.

2.4.4.1 Power Down Mode

In the POWER DOWN MODE the complete chip is switched off.

The current consumption is typically 0.3 nA at 3 V 25°C.

The value is typically 5nA at 70°C.

2.4.4.2 PLL Enable Mode

In the PLL ENABLE MODE the PLL is switched on but the power amplifier is turned off to avoid undesired power radiation during the time the PLL needs to settle. The turn on time of the PLL is determined mainly by the turn on time of the crystal oscillator and is less than 1 msec when the specified crystal is used.

The current consumption is typically 3.5 mA.

2.4.4.3 Transmit Mode

In the TRANSMIT MODE the PLL is switched on and the power amplifier is turned on too.

The current consumption of the IC is typically 7 mA when using a proper transforming network at PAOUT, see Figure 8.

2.4.4.4 Power mode control

The bias circuitry is powered up via a voltage V > 1.5 V at the pin PDWN (pin10).
When the bias circuitry is powered up, the pins ASKDTA and FSKDTA are pulled up internally.
Forcing the voltage at the pins low overrides the internally set state.

Alternatively, if the voltage at ASKDTA or FSKDTA is forced high externally, the PDWN pin is pulled up internally via a current source. In this case, it is not necessary to connect the PDWN pin, it is recommended to leave it open.

The principle schematic of the power mode control circuitry is shown in Figure 3

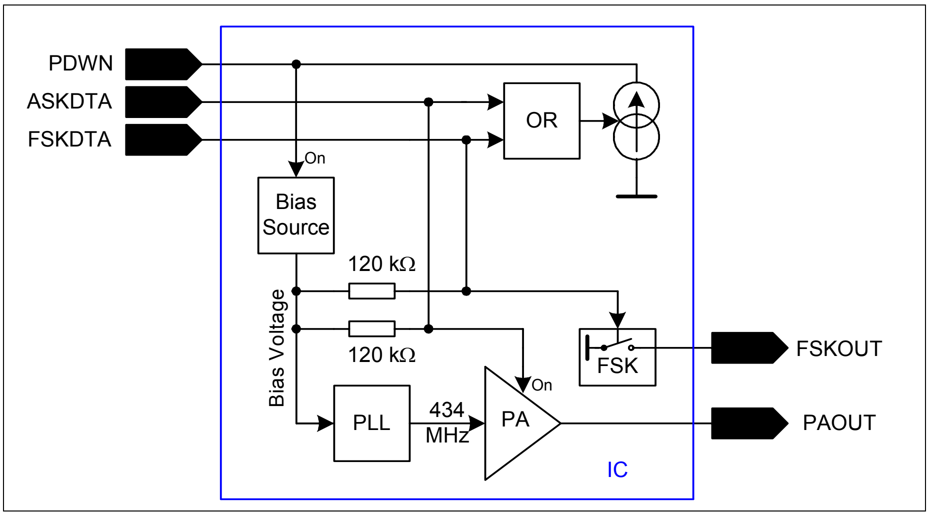


Figure 3 Power mode control circuitry

Table 6 provides a listing of how to get into the different power modes

Table 6 **Power Modes**

PDWN	**FSKDTA**	**ASKDTA**	**MODE**
Low[1]	Low, Open	Low, Open	POWER DOWN
Open[2]	Low	Low	
High[3]	Low, Open, High	Low	PLL ENABLE
Open	High	Low	
High	Low, Open, High	Open, High	TRANSMIT
Open	High	Open, High	
Open	Low, Open, High	High	

1) Low:	Voltage at pin < 0.7V (PDWN)
	Voltage at pin < 0.5V (FSKDTA, ASKDTA)
2) Open:	Pin open
3) High:	Voltage at pin > 1.5V

Other combinations of the control pins PDWN, FSKDTA and ASKDTA are not recommended.

2.4.5 Recommended Timing Diagrams for ASK- and FSK-Modulation

ASK Modulation using FSKDTA and ASKDTA, PDWN not connected

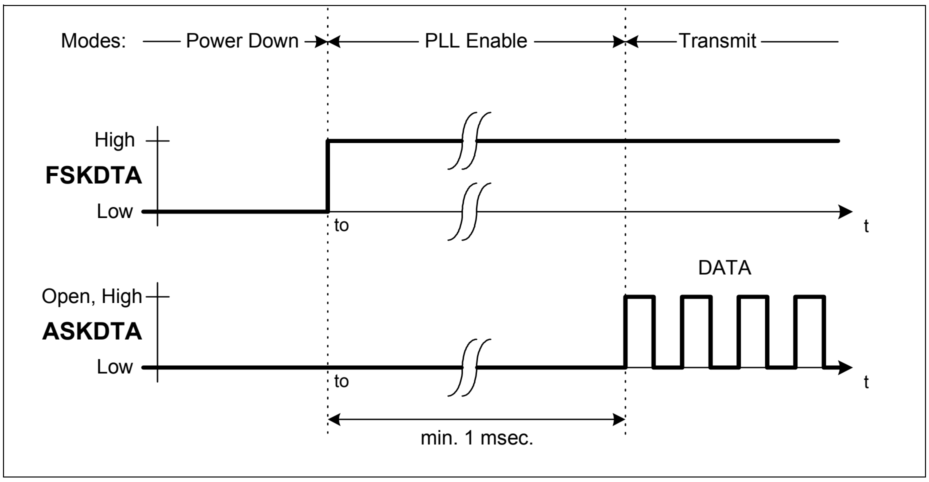

Modes:
Power Down
PLL Enable
Transmit
High
FSKDTA
Low
to
t
DATA
Open, High
ASKDTA
Low
to
t
min. 1 msec.

Figure 4 **ASK Modulation**

FSK Modulation using FSKDTA and ASKDTA, PDWN not connected.

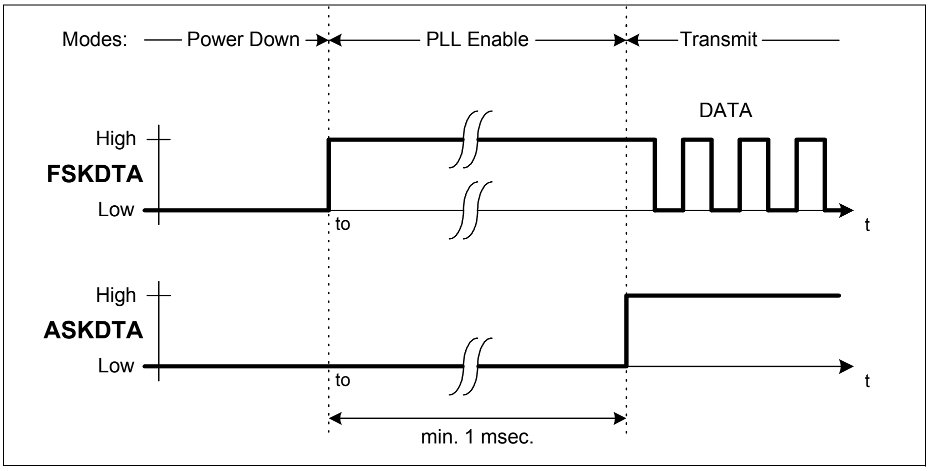

Modes:
Power Down
PLL Enable
Transmit
DATA
High
FSKDTA
Low
to
t
High
ASKDTA
Low
to
t
min. 1 msec.

Figure 5 **FSK Modulation**

Alternative ASK Modulation, FSKDTA not connected.

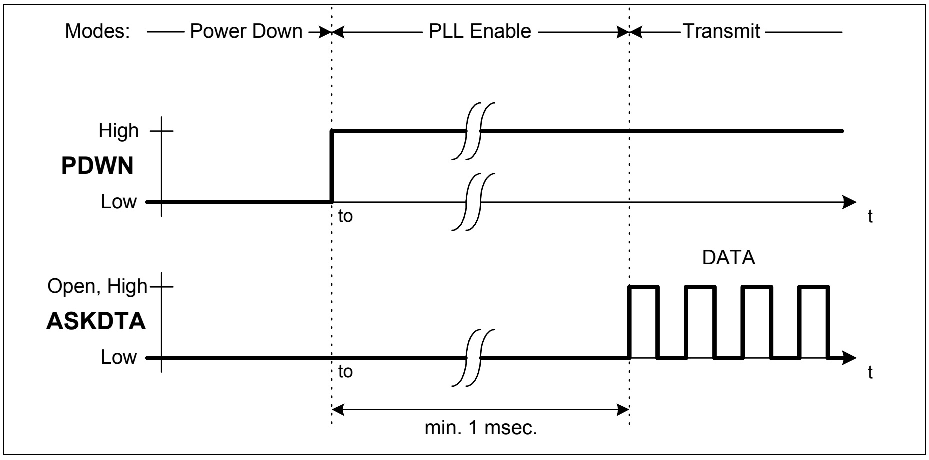

Modes:
Power Down
PLL Enable
Transmit
High
PDWN
Low
to
t
DATA
Open, High
ASKDTA
Low
to
t
min. 1 msec.

Figure 6 **Alternative ASK Modulation**

Alternative FSK Modulation

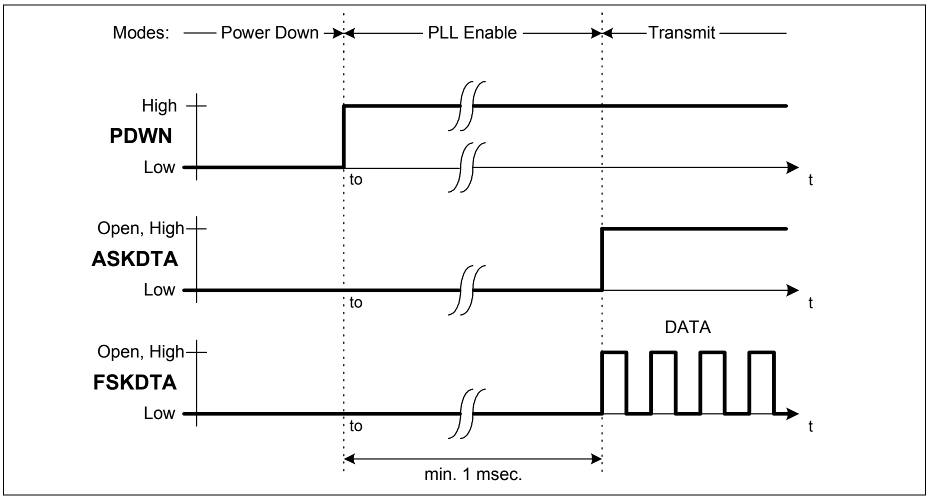

Modes:
Power Down
PLL Enable
Transmit
High
PDWN
Low
to
t
Open, High
ASKDTA
Low
to
t
DATA
Open, High
FSKDTA
Low
to
t
min. 1 msec.

Figure 7 **Alternative FSK Modulation**

3 Applications

3.1 50 Ohm-Output Testboard Schematic

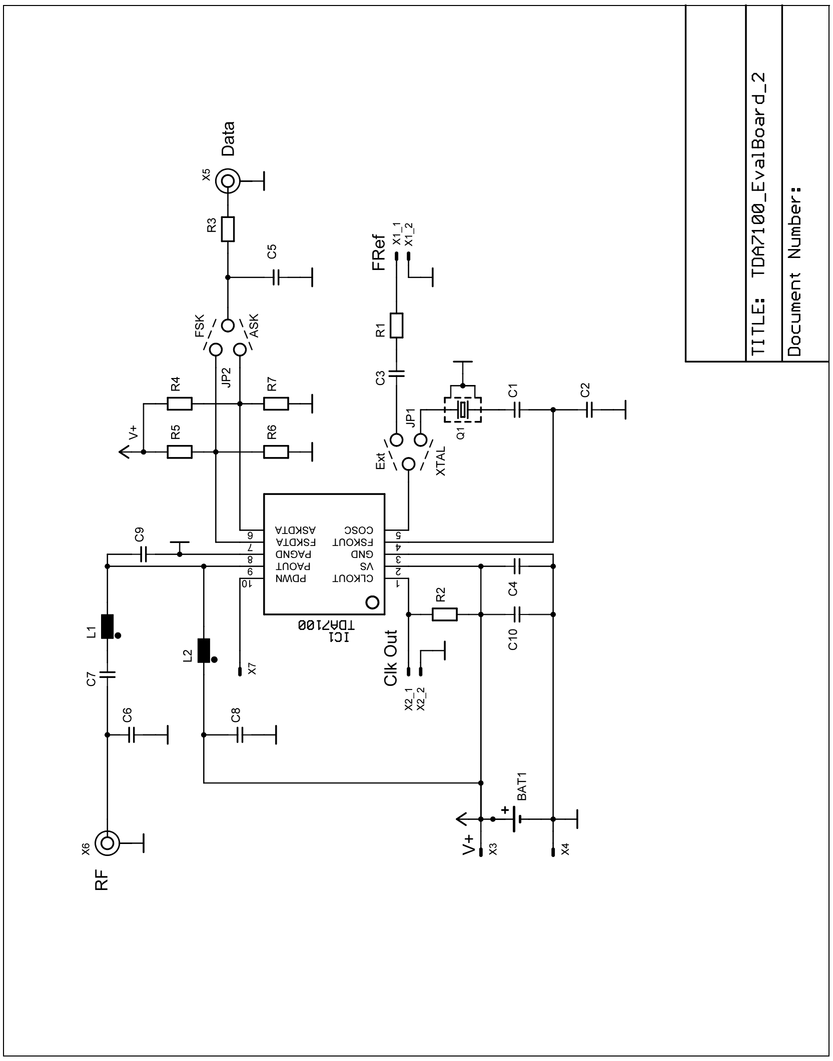

TITLE: TDA7100_EvalBoard_2
Document Number:
Data
X5
R3
C5
FSK
ASK
JP2
R4
R7
V+
R5
R6
FRef
X1_1
X1_2
R1
C3
JP1
Q1
C1
C2
Ext
XTAL
C9
ASKDTA
FSKDTA
PAGND
PAOUT
PDWN
COSC
FSKOUT
GND
VS
CLKOUT
TDA7100
IC1
L1
L2
X7
R2
C4
C10
Clk Out
X2_1
X2_2
C7
C6
C8
BAT1
V+
X3
X4
X6
RF

Figure 8 50 Ohm-output testboard schematic

3.2 50 Ohm-Output Testboard Layout

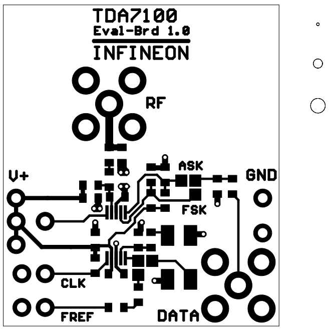

TDA7100
Eval-Brd 1.0
INFINEON
RF
V+
ASK
GND
FSK
CLK
FREF
DATA

Figure 9 Top Side of TDA7100-Testboard with 50 Ohm-Output

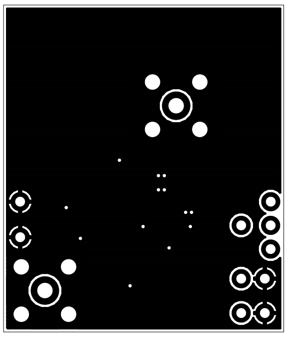


Figure 10 Bottom Side of TDA7100-Testboard with 50 Ohm-Output

3.3 Bill of Material (50 Ohm-Output Evalboard)

Table 7 Bill of Materials (cont'd)

Ref.	Value	Specification
R1	open	
R2	open	
R3	4k7	0603, +/-5%
R4	12k	0603, +/-5%
R5	open	
R6	15k	0603, +/-5%
R7	open	
C1	10p	0603, C0G, +/-1%
C2	6p8	0603, C0G, +/-0.1p
C3	open	
C4	open	
C5	100p	0603, X7R, +/-10%
C6	12p	0603, C0G, +/-1%
C7	39p	0603, C0G, +/-1%
C8	330p	0603, C0G, +/-5%
C9	3p3	0603, C0G, +/-0.1p
C10	47n	0603, X7R, +/-10%
L1	47n	EPCOS SIMID 0603-C, +/-2%
L2	120n	EPCOS SIMID 0603-C, +/-2%

Ref.	Value	Specification
X1	n.e.	
X2	n.e.	
X3	Pin	single-pole connector, 2.54mm
X4	Pin	single-pole connector, 2.54mm
X5	SMA-connector	
X6	SMA-connector	
X7	n.e.	
JP1	solder bridge	in position “XTAL”
JP2	solder bridge	in position “FSK”
Q1	13.56875 MHz	Tokyo Denpa TSS-3B 13.56875 MHz Spec.No. 10-50205
IC1	TDA7100	

3.4 Stripline-Antenna Testboard Schematic

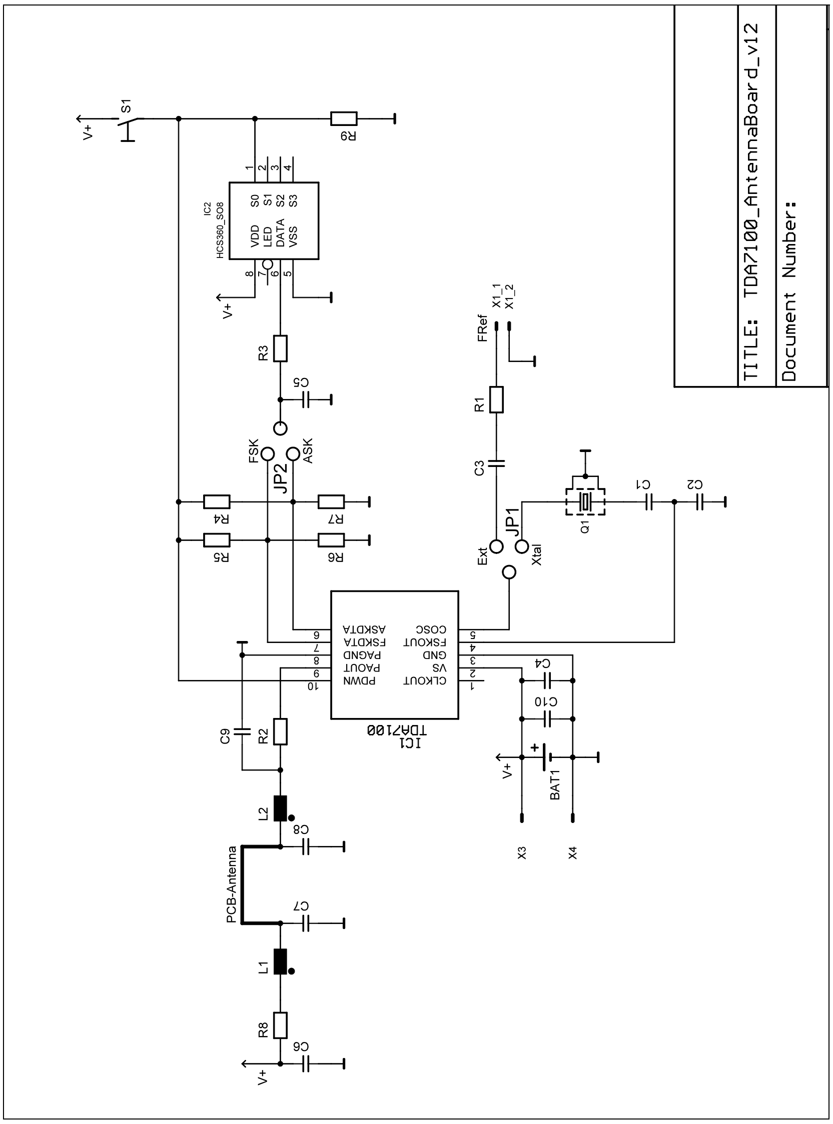

TITLE: TDA7100_AntennaBoard_v12
Document Number:
V+
S1
R9
IC2
HCS360_SO8
VDD
LED
DATA
VSS
S0
S1
S2
S3
R3
C5
FSK
JP2
ASK
R4
R7
R5
R6
FRef
X1_1
X1_2
R1
C3
JP1
Ext
Xtal
Q1
C1
C2
ASKDTA
FSKDTA
PAGND
PAOUT
PDWN
COSC
FSKOUT
GND
VS
CLKOUT
TDA7100
IC1
C4
C10
BAT1
X3
X4
C9
R2
L2
C8
PCB-Antenna
C7
L1
R8
C6

Figure 11 Stripline-antenna testboard schematic

3.5 Stripline-Antenna Testboard Layout

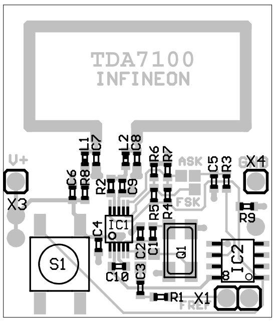


Figure 12 Top Side of TDA7100-Testboard with Stripline-Antenna

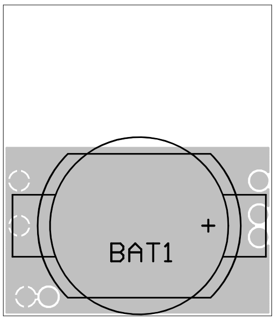


Figure 13 Bottom Side of TDA7100-Testboard with Stripline-Antenna

Please note that this board layout may be used for both high- and low-power applications, see also the bill of materials on the subsequent pages.
In case of ASK operation the solder bridge JP2 has to be shortened in the “ASK”-position, in case of FSK modulation in the“FSK” position.
Solder bridge JP1between C1, C2 and C3) gives a choice of operating the board with the on-board crystal as reference (“XTAL” shortened, i.e. close to C1 and C2) or with an external clock generator (solder bridge shorts pads between C3 and C2).

3.6 Bill of Material (Antenna board) FSK modulation

Table 8 **Bill of Materials** (cont'd)

Ref.	Value	Specification
R1	open	
R2	0R	0603, SMD-Jumper
R3	0R	0603, SMD-Jumper
R4	82k	0603, +/-5%
R5	open	
R6	open	
R7	100n	0603, X7R, +/-10%
R8	39R	0603, +/-1%
R9	15k	0603, +/-5%
C1	10p	0603, C0G, +/-1%
C2	6p8	0603, C0G, +/-0.1p
C3	open	
C4	open	
C5	open	
C6	10n	0603, X7R, +/-10%
C7	5p6	0603, C0G, +/-0.1p
C8	open	
C9	4p7	0603, C0G, +/-0.1p
C10	47n	0603, X7R, +/-10%
L1	100n	0603, EPCOS SIMID, +/-2%
L2	0R	0603, SMD-Jumper
X1	n.e.	
X3	n.e.	
X4	n.e.	
S1	push-button	STTSKHMPW, ALPS
JP1	solder bridge	in position “XTAL”
JP2	solder bridge	in position “FSK”
Q1	13.56875 MHz	Tokyo Denpa TSS-3B 13.56875 MHz Spec.No. 10-50205

Ref.	Value	Specification
IC1	TDA7100	P-TSSOP-10
IC2	HCS360	SO8
BAT1	battery holder	HU2031-1, Renata
	battery	CR2032, Renata

3.7 Application Hints on the Crystal Oscillator

The crystal oscillator achieves a turn on time less than 1 msec when the specified crystal is used. To achieve this, a NIC oscillator type is implemented in the TDA7100. The input impedance of this oscillator is a negative resistance in series to an inductance. Therefore the load capacitance of the crystal CL (specified by the crystal supplier) is transformed to the capacitance Cv.

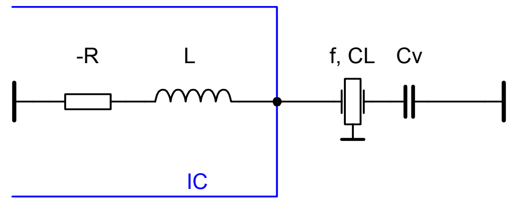


Figure 14 Application Hints

Formula 1:

$$Cv = \frac{1}{\frac{1}{CL} + \omega^2 L}$$

CL: crystal load capacitance for nominal frequency

ω: angular frequency

L: inductance of the crystal oscillator

Example for the ASK-Mode:

Referring to the application circuit, in ASK-Mode the capacitance C2 is replaced by a short to ground. Assume a crystal frequency of 13.56MHz and a crystal load capacitance of CL = 12 pF. The inductance L at 13.56MHz is about 4.6 µH. Therefore C1 is calculated to 10 pF.

$$Cv = \frac{1}{\frac{1}{CL} + \omega^2 L} = C1$$

Example for the FSK-Mode:

FSK modulation is achieved by switching the load capacitance of the crystal as shown below.

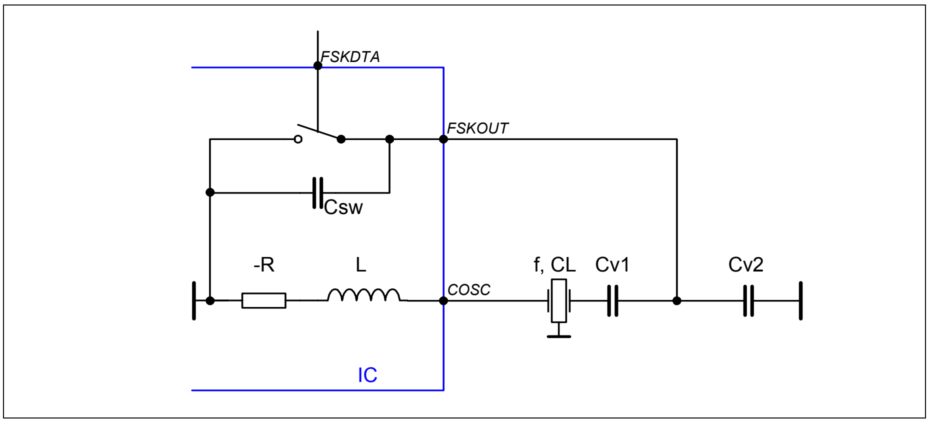


Figure 15 FSK Mode

The frequency deviation of the crystal oscillator is multiplied with the divider factor N of the Phase Locked Loop to the output of the power amplifier. In case of small frequency deviations (up to +/- 1000 ppm), the two desired load capacitances can be calculated with the formula below.

$$CL\pm = \frac{CL \mp C0\frac{\Delta f}{N * f1}(1 + \frac{2(C0 + CL)}{C1})}{1 \pm \frac{\Delta f}{N * f1}(1 + \frac{2(C0 + CL)}{C1})}$$

C_L: crystal load capacitance for nominal frequency

C_0: shunt capacitance of the crystal

f: frequency

ω: $\omega = 2\pi f$: angular frequency

N: division ratio of the PLL

df: peak frequency deviation

Because of the inductive part of the TDA7100, these values must be corrected by Formula 1 on the preceding page. The value of Cv± can be calculated.

$$Cv\pm = \frac{1}{\frac{1}{CL\pm} + \omega^2 L}$$

If the FSK switch is closed, Cv- is equal to Cv1 (C1 in the application diagram). If the FSK switch is open, Cv2 (C2 in the application diagram) can be calculated.

$$Cv2 = C2 = \frac{Csw * Cv1 - (Cv+) * (Cv1 + Csw)}{(Cv+) - Cv1}$$

Csw: parallel capacitance of the FSK switch (3 pF incl. layout parasitics)

Remark: These calculations are only approximations. The necessary values depend on the layout also and must be adapted for the specific application board.

3.8 Design Hints on the Clock Output (CLKOUT)

The CLKOUT pin is an open collector output. An external pull up resistor (RL) should be connected between this pin and the positive supply voltage. The value of RL is depending on the clock frequency and the load capacitance CLD (PCB board plus input capacitance of the microcontroller). RL can be calculated to:

$$RL = \frac{1}{fCLKOUT * 8 * CLD}$$

Table 9 **Clock Output**

fCLKOUT=847.5 kHz	
CL[pF]	RL[kOhm]
5	27
10	12
20	6.8

Remark: To achieve a low current consumption and a low spurious radiation, the largest possible RL should be chosen.

Even harmonics of the signal at CLKOUT can interact with the crystal oscillator input COSC preventing the start-up of oscillation. Care must be taken in layout by sufficient separation of the signal lines to ensure sufficiently small coupling.

3.9 Application Hints on the Power-Amplifier

The power amplifier operates in a high efficient class C mode. This mode is characterized by a pulsed operation of the power amplifier transistor at a current flow angle of $\theta \ll \pi$. A frequency selective network at the amplifier output passes the fundamental frequency component of the pulse spectrum of the collector current to the load. The load and its resonance transformation to the collector of the power amplifier can be generalized by the equivalent circuit of Figure 16. The tank circuit L//C//RL in parallel to the output impedance of the transistor should be in resonance at the operating frequency of the transmitter.

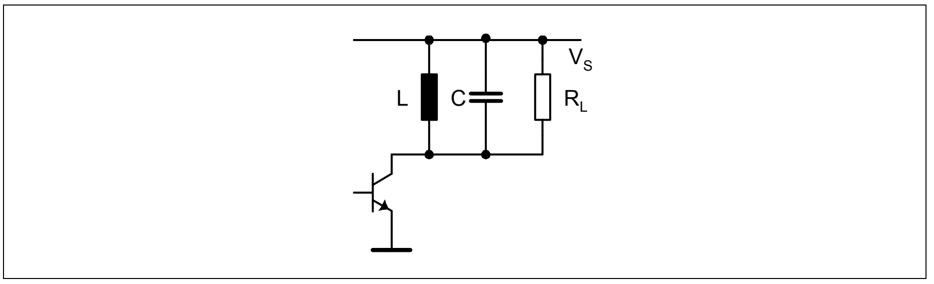


Figure 16 Equivalent power amplifier tank circuit

The optimum load at the collector of the power amplifier for “critical” operation under idealized conditions at resonance is:

$$R_{LC} = \frac{V_S^2}{2 * P_O}$$

The theoretical value of R_{LC} for an RF output power of P_o= 5 dBm (3.16 mW) is:

$$R_{LC} = \frac{3^2}{2 * 0.00316} = 1423\,\Omega$$

“Critical” operation is characterized by the RF peak voltage swing at the collector of the PA transistor to just reach the supply voltage V_S.
The high degree of efficiency under “critical” operating conditions can be explained by the low power losses at the transistor. During the conducting phase of the transistor, its collector voltage is very small. This way the power loss of the transistor, equal to i_C*u_{CE} is minimized. This is particularly true for small current flow angles of $\theta << \pi$.
In practice the RF-saturation voltage of the PA transistor and other parasitics reduce the “critical” R_{LC}.

The output power P_o is reduced by operating in an “overcritical” mode characterised by $R_L > R_{LC}$.
The power efficiency (and the bandwidth) increase when operating at a slightly higher R_L, as shown in Figure 17.
The collector efficiency E is defined as

$$E = \frac{P_O}{V_S I_C}$$

The diagram of Figure 17 was measured directly at the PA-output at V_S = 3 V. Losses in the matching circuitry decrease the output power by about 1.5 dB. As can be seen from the diagram, 550 Ω is the optimum impedance for operation at 3 V. For an approximation of R_{OPT} and P_{OUT} at other supply voltages those two formulas can be used:

$$R_{OPT} \sim V_S$$

and

$$P_{OUT} \sim R_{OPT}$$

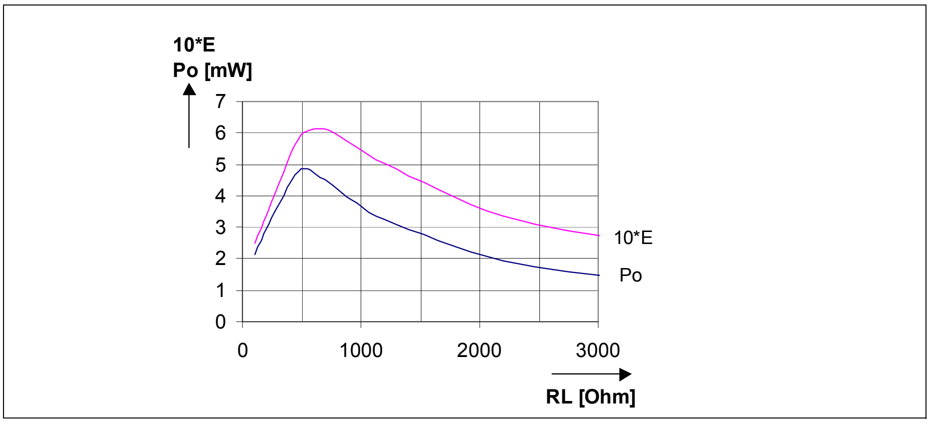


Figure 17 Output power P_o (mW) and collector efficiency E vs. load resistor R_L.

The DC collector current I_c of the power amplifier and the RF output power P_o vary with the load resistor R_L. This is typical for overcritical operation of class C amplifiers. The collector current will show a characteristic dip at the resonance frequency for this type of “overcritical” operation. The depth of this dip will increase with higher values of R_L.

4 Reference

4.1 Electrical Data

4.1.1 Absolute Maximum Ratings

***Attention:** The maximum ratings must not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the IC will result.*

Table 10 Absolute Maximum Ratings, T_{amb} = -20 °C … +70 °C

Parameter	**Symbol**	**Limit Values**		**Unit**	**Remarks**
		min.	**max.**		
Junction Temperature	T_J	–40	+150	°C	
Storage Temperature	T_s	–40	+125	°C	
Thermal Resistance	R_{thJA}		220	K/W	
Supply voltage	V_S	–0.3	+4.0	V	
Voltage at any pin excluding pin 9	V_{pins}	-0.3	V_S + 0.3	V	
Voltage at pin 9	V_{pin9}	-0.3	2 * V_S	V	No ESD-Diode to V_S
ESD integrity, all pins	V_{ESD}	-1	+1	kV	JEDEC Standard JESD22-A114-B
ESD integrity, all pins excluding pin 9	V_{ESD}	-2	+2	kV	JEDEC Standard JESD22-A114-B

Ambient Temperature under bias: T_A = –20°C to +70°C

Note: All voltages referred to ground (pins) unless stated otherwise.

Pins 3 and 8 are grounded.

4.2 Operating Ratings

Within the operational range the IC operates as described in the circuit description.

Table 11 Operating Ratings

Parameter	Symbol	Limit Values		Unit	Test Conditions
		min.	max.		
Supply voltage	V_S	2.1	4.0	V	
Ambient temperature	T_A	-20	70	°C	

4.3 AC/DC Characteristics

AC/DC characteristics involve the spread of values guaranteed within the specified supply voltage and ambient temperature. Typical charcateristics are the median of the production.

4.3.1 AC/DC Characteristic at 3V, 25°C

Table 12 Supply Voltage V_S=3V, Ambient temperature T_{amb}=25°C

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Current consumption						
Power Down mode	$I_{S\ PDWN}$		0.3	100	nA	V (Pins 10, 6 and 7) < 0.2 V
PLL Enable mode	$I_{S\ PLL\_EN}$		3.5	4.2	mA	
Transmit mode 434 MHz	$I_{S\ TRANSM}$		7.5		mA	
Output frequency						
Output frequency	f_{OUT}	427	434	442	MHz	f_{OUT} = 32 * f_{COSC}
Clock Driver Output (Pin 1)						
Output current (High)	I_{CLKOUT}			5	µA	V_{CLKOUT} = V_S
Saturation Voltage (Low)$^{1)}$	V_{SATL}			0.56	V	I_{CLKOUT} = 1 mA

Table 12 Supply Voltage V_S=3V, Ambient temperature T_{amb}=25°C (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
FSK Switch Output (Pin 4)						
On resistance	R_{FSKOUT}			250	Ω	V_{FSKDTA} = 0 V
On capacitance	C_{FSKOUT}			6	pF	V_{FSKDTA} = 0 V
Off resistance	R_{FSKOUT}	10			kΩ	V_{FSKDTA} = V_S
Off capacitance	C_{FSKOUT}			1.5	pF	V_{FSKDTA} = V_S
Crystal Oscillator Input (Pin 5)						
Load capacitance	$C_{COSCmax}$			5	pF	
Serial Resistance of the crystal				100	Ω	f = 13.56 MHz
Input inductance of the COSC pin			4.6		µH	f = 13.56 MHz
ASK Modulation Data Input (Pin 6)						
ASK Transmit disabled	V_{ASKDTA}	0		0.5	V	
ASK Transmit enabled	V_{ASKDTA}	1.5		V_S	V	
Input bias current ASKDTA	I_{ASKDTA}			30	µA	V_{ASKDTA} = V_S
Input bias current ASKDTA	I_{ASKDTA}	-20			µA	V_{ASKDTA} = 0 V
ASK data rate	f_{ASKDTA}			20	kHz	
FSK Modulation Data Input (Pin 7)						
FSK Switch on	V_{FSKDTA}	0		0.5	V	
FSK Switch off	V_{FSKDTA}	1.5		V_S	V	
Input bias current FSKDTA	I_{FSKDTA}			30	µA	V_{FSKDTA} = V_S
Input bias current FSKDTA	I_{FSKDTA}	-20			µA	V_{FSKDTA} = 0 V
FSK data rate	f_{FSKDTA}			20	kHz	
Power Amplifier Output (Pin 9)						
Output Power$^{2)}$ at 434 MHz transformed to 50 Ohm	P_{OUT434}		5.2		dBm	

Table 12 Supply Voltage V_S=3V, Ambient temperature T_{amb}=25°C (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Power Down Mode Control (Pin 10)						
Power Down mode	V_{PDWN}	0		0.7	V	$V_{ASKDTA} < 0.2$ V $V_{FSKDTA} < 0.2$ V
PLL Enable mode	V_{PDWN}	1.5		V_S	V	$V_{ASKDTA} < 0.5$ V
Transmit mode	V_{PDWN}	1.5		V_S	V	$V_{ASKDTA} > 1.5$ V
Input bias current PDWN	I_{PDWN}			30	µA	$V_{PDWN} = V_S$

1) Derating linearly to a saturation voltage of max. 140 mV at I_{CLKOUT} = 0 mA

2) Power amplifier in overcritical C-operation
Matching circuitry as used in the 50 Ohm-Output Testboard at the specified frequency.
Tolerances of the passive elements not taken into account.

4.3.2 AC/DC Characteristic at 2.1V ...4.0 V, -20°C ...+70°C

Table 13 Supply Voltage V_S=2.1V ... 4.0V, T_{amb}=-20°C ... +70°C

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Current consumption						
Power Down mode	$I_{S\ PDWN}$			4	µA	V (Pins 10, 6 and 7) < 0.2 V
PLL Enable mode	$I_{S\ PLL\_EN}$		3.5	4.6	mA	
Transmit mode	$I_{S\ TRANSM}$		7.5		mA	
Output frequency						
Output frequency	f_{OUT}	432	434	437	MHz	$f_{OUT} = 32 * f_{COSC}$
Clock Driver Output (Pin 1)						
Output current (High)	I_{CLKOUT}			5	µA	$V_{CLKOUT} = V_S$
Saturation Voltage (Low)[1]	V_{SATL}			0.5	V	I_{CLKOUT} = 0.6 mA

Table 13 Supply Voltage V_S=2.1V ... 4.0V, T_{amb}=-20°C ... +70°C (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
FSK Switch Output (Pin 4)						
On resistance	R_{FSKOUT}			280	Ω	V_{FSKDTA} = 0 V
On capacitance	C_{FSKOUT}			6	pF	V_{FSKDTA} = 0 V
Off resistance	R_{FSKOUT}	10			kΩ	$V_{FSKDTA} = V_S$
Off capacitance	C_{FSKOUT}			1.5	pF	$V_{FSKDTA} = V_S$
Crystal Oscillator Input (Pin 5)						
Load capacitance	$C_{COSCmax}$			5	pF	
Serial Resistance of the crystal				100	Ω	f = 13.56 MHz
Input inductance of the COSC pin			4.6		µH	f = 13.56 MHz
ASK Modulation Data Input (Pin 6)						
ASK Transmit disabled	V_{ASKDTA}	0		0.5	V	
ASK Transmit enabled	V_{ASKDTA}	1.5		V_S	V	
Input bias current ASKDTA	I_{ASKDTA}			33	µA	$V_{ASKDTA} = V_S$
Input bias current ASKDTA	I_{ASKDTA}	-20			µA	V_{ASKDTA} = 0 V
ASK data rate	f_{ASKDTA}			20	kHz	
FSK Modulation Data Input (Pin 7)						
FSK Switch on	V_{FSKDTA}	0		0.5	V	
FSK Switch off	V_{FSKDTA}	1.5		V_S	V	
Input bias current FSKDTA	I_{FSKDTA}			33	µA	$V_{FSKDTA} = V_S$
Input bias current FSKDTA	I_{FSKDTA}	-20			µA	V_{FSKDTA} = 0 V
FSK data rate	f_{FSKDTA}			20	kHz	

Table 13 Supply Voltage V_S=2.1V ... 4.0V, T_{amb}=-20°C ... +70°C (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Power Amplifier Output (Pin 9)						
Output Power [2] at 434 MHz transformed to 50 Ohm.	$P_{OUT, 434}$		2.5		dBm	V_S = 2.1 V
	$P_{OUT, 434}$		5.2		dBm	V_S = 3.0 V
	$P_{OUT, 434}$		6.9		dBm	V_S = 4.0 V
Power Down Mode Control (Pin 10)						
Power Down mode	V_{PDWN}	0		0.5	V	V_{ASKDTA} < 0.2 V V_{FSKDTA} < 0.2 V
PLL Enable mode	V_{PDWN}	1.5		V_S	V	V_{ASKDTA} < 0.5 V
Transmit mode	V_{PDWN}	1.5		V_S	V	V_{ASKDTA} > 1.5 V
Input bias current PDWN	I_{PDWN}			38	µA	V_{PDWN} = V_S

1) Derating linearly to a saturation voltage of max. 140 mV at I_{CLKOUT} = 0 mA

2) Matching circuitry as used in the 50 Ohm-Output Testboard.

Tolerances of the passive elements not taken into account.

Typ. temperature dependency at 2.1 V: +0.3 dBm@-20°C and -0.5 dBm@+70°C, reference +25°C

Typ. temperature dependency at 3.0 V: +0.35 dBm@-20°C and -0.7 dBm@+70°C, reference +25°C

Typ. temperature dependency at 4.0 V: +0.7 dBm@-20°C and -1.1 dBm@+70°C, reference +25°C

5 Package Outlines

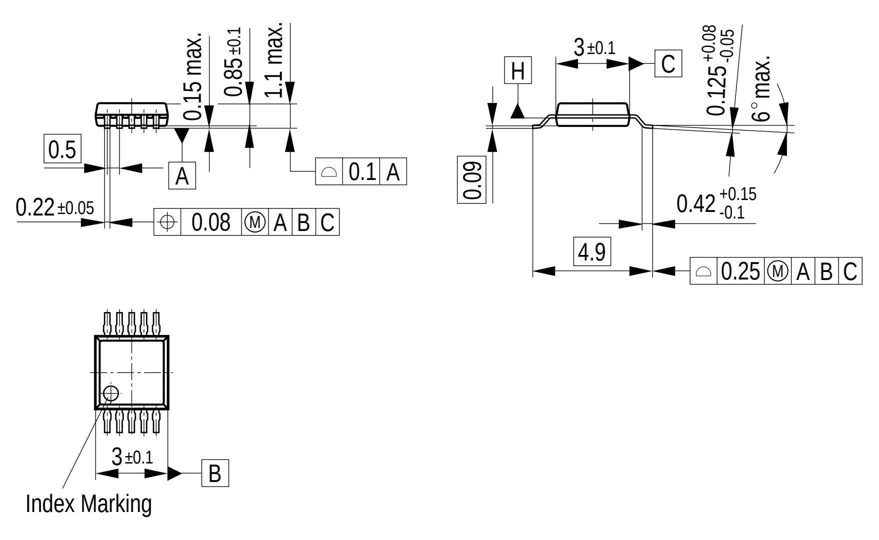

0.15 max.
0.85±0.1
1.1 max.
0.5
A
0.1 A
0.22±0.05
0.08 Ⓜ A B C
3±0.1
C
H
0.125 +0.08 -0.05
6° max.
0.09
0.42 +0.15 -0.1
4.9
0.25 Ⓜ A B C
3±0.1
B
Index Marking

Figure 18 PG-TSSOP-10

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SMD = Surface Mounted Device

Dimensions in mm

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