4. Block Diagram

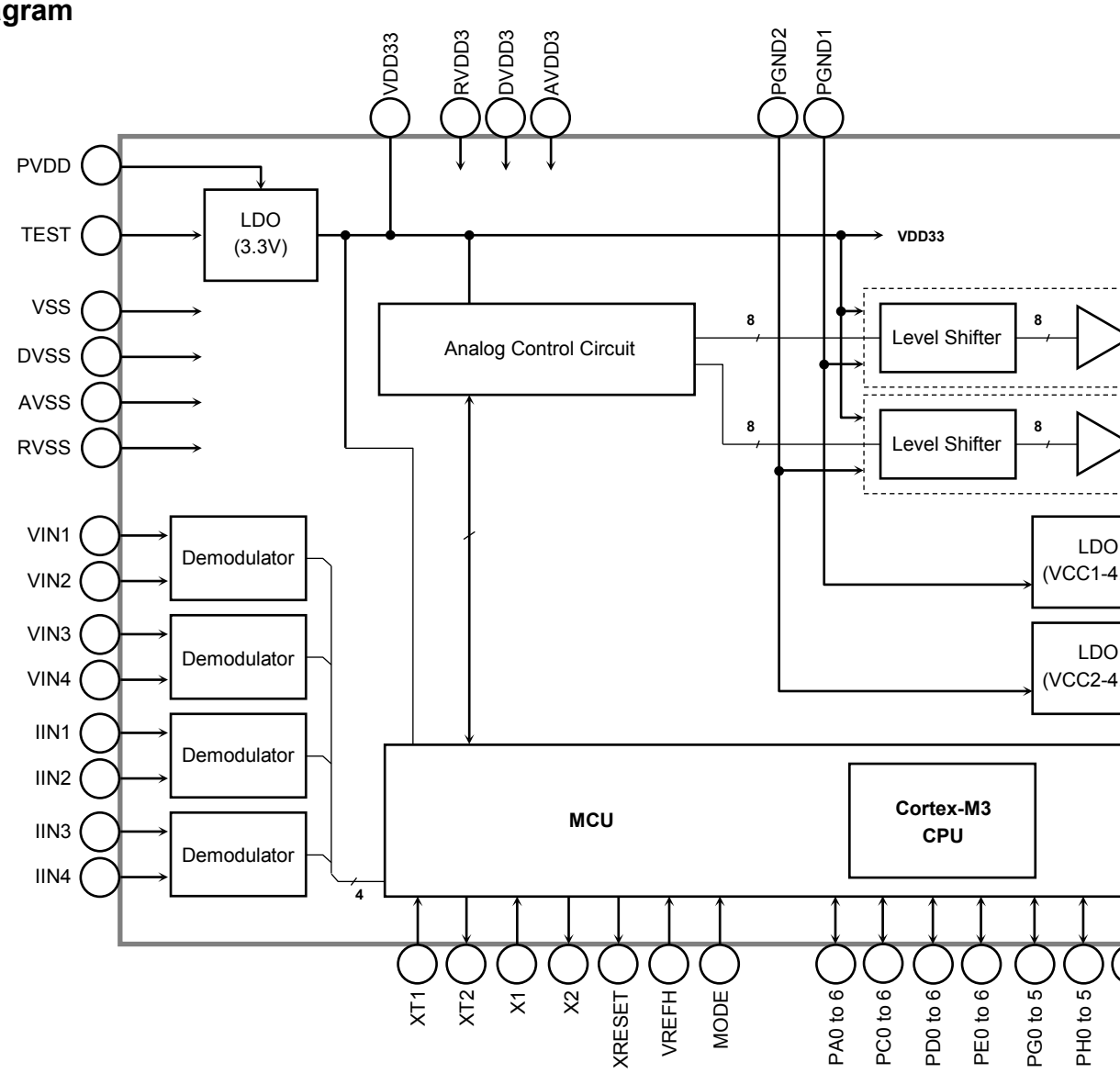


Figure 4.1 Block Diagram

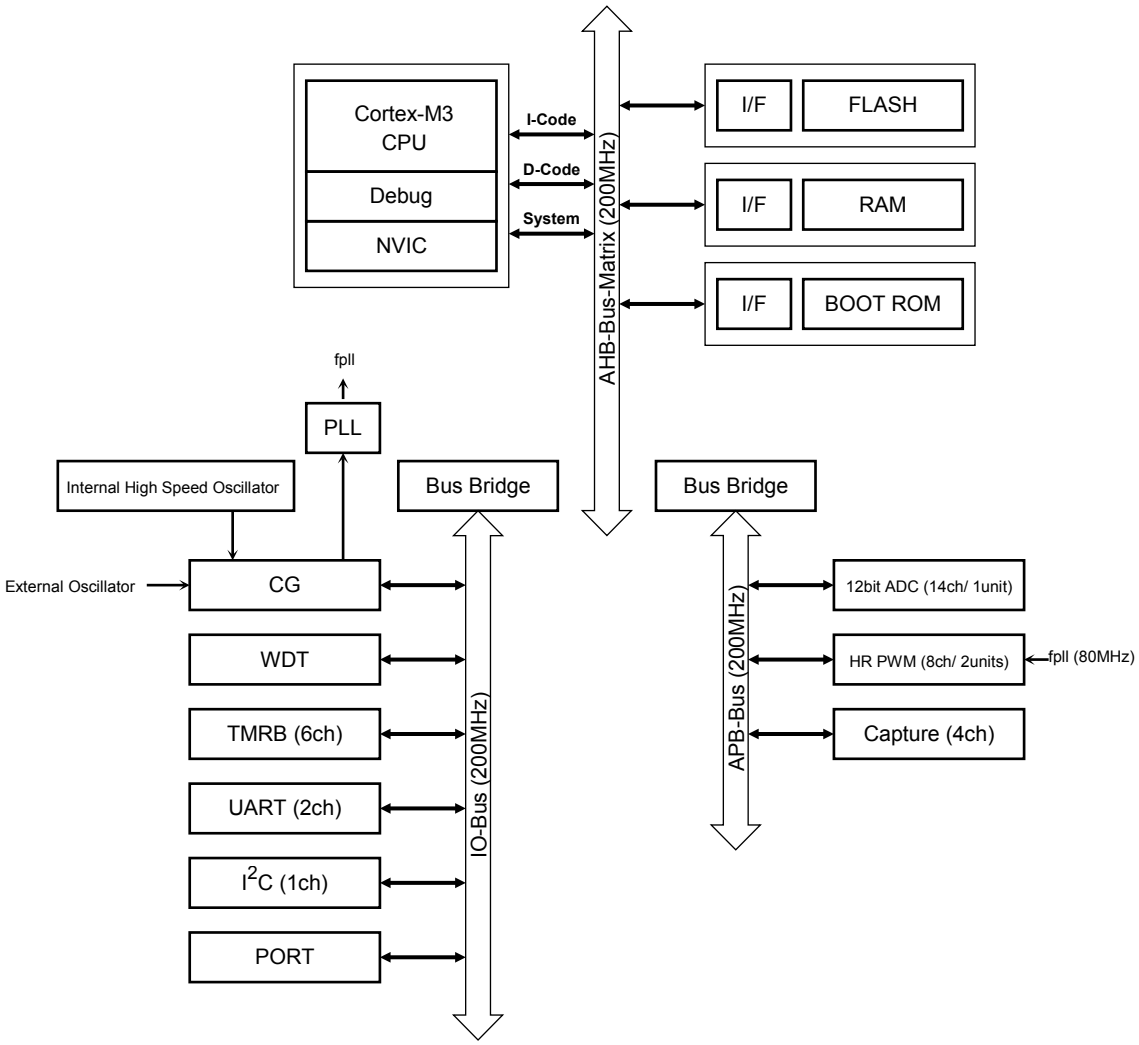


Figure 4.2 Block Diagram (CPU Core)

5. Pin Assignment

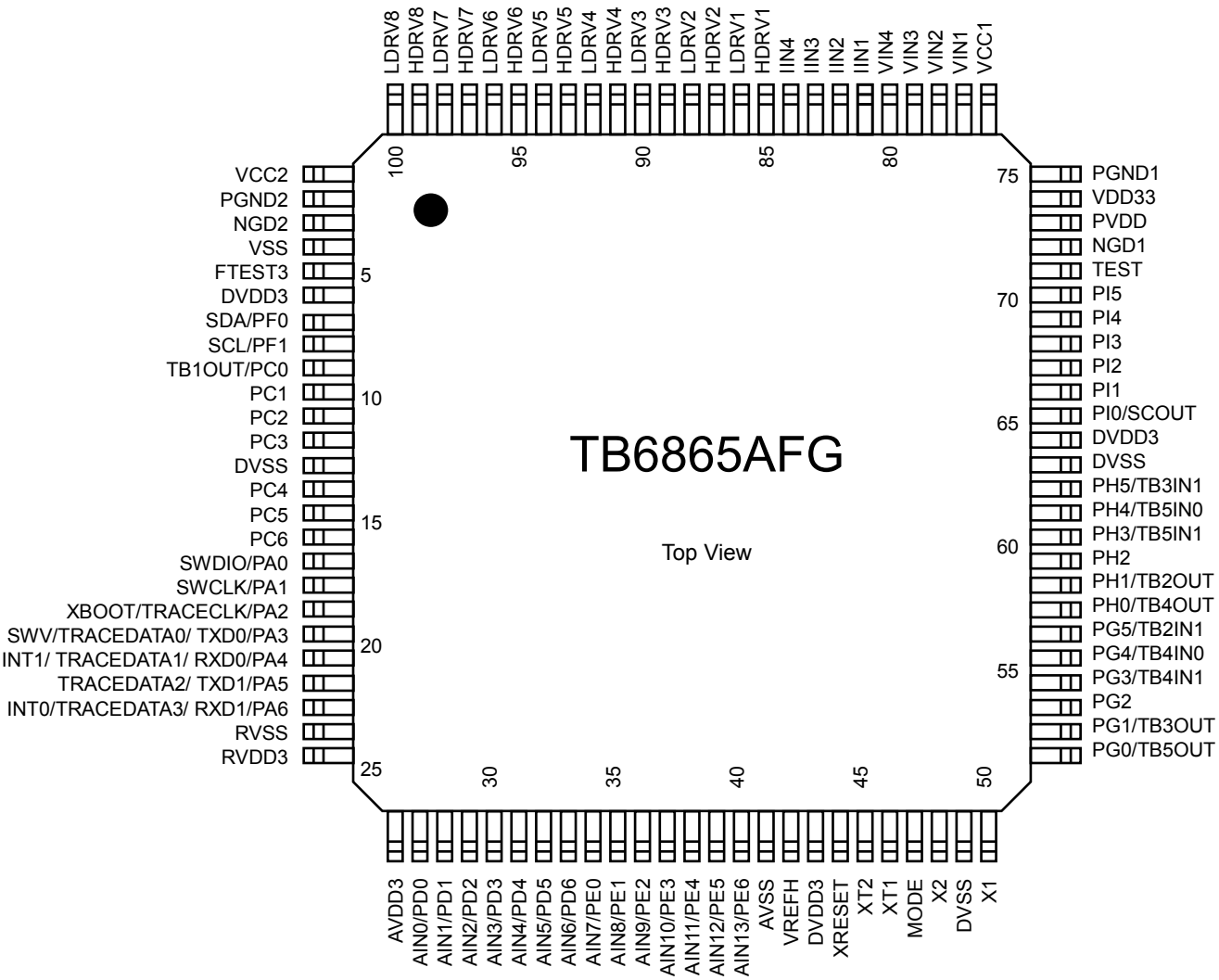


Figure 5.1 Pin Assignment

6. Pin Function

Table 6.1 Pin Function

Pin Number	Pin symbol	I/O	Description	Comment
1	VCC2	-	Power supply pin for CH5 to CH8 pre-drivers 2	(Note 1)
2	PGND2	-	Power GND pin for Analog circuit	(Note 2)
3	NGD2	O	VCC2-4.5V LDO output pin for internal circuit 2	(Note 3)
4	VSS	-	Analog GND pin	(Note 2)
5	FTEST3	I	TEST pin	(Note 4)
6	DVDD3	-	Power supply pin for Digital circuit	
7	PF0 SDA	I/O	Input Output Port	
		I/O	Serial data input output	I^2C bus(SDA)
8	PF1 SCL	I/O	Input Output Port	
		I/O	Serial clock input output	I^2C bus(SCL)
9	PC0 TB1OUT	I/O	Input Output Port	
		O	TMRB1 Output	Control for Buzzer
10	PC1	I/O	Input Output Port	Large current for LED drive
11	PC2	I/O	Input Output Port	Large current for LED drive
12	PC3	I/O	Input Output Port	Large current for LED drive
13	DVSS	-	GND pin	(Note 2)
14	PC4	I/O	Input Output Port	Large current for LED drive
15	PC5	I/O	Input Output Port	Large current for LED drive
16	PC6	I/O	Input Output Port	Large current for LED drive
17	PA0 SWDIO	I/O	Input Output Port	
		I/O	Serial Wire debug port	Debug port
18	PA1 SWCLK	I/O	Input Output Port	
		I	Serial Wire clock	Debug port
19	PA2 TRACECLK XBOOT	I/O	Input Output Port	
		O	TRACE clock output	Debug port
		I	Single boot mode	
20	PA3 TXD0 TRACEDATA0 SWV	I/O	Input Output Port	
		O	TXD0	
		O	TRACE data output 0	Debug port
		O	Serial Wire Viewer output	
21	PA4 RXD0 TRACEDATA1 INT1	I/O	Input Output Port	
		I	RXD0	
		O	TRACE data output 1	Debug port
		I	External Interrupt 1	

Note 1: When it's not in use, connect to GND.

Note 2: Connect to common ground(GND).

Note 3: It is impossible to supply power to external parts. Connect capacitor ($0.01\mu F$) between NGD2 and VCC2.

Note 4: Must be open.

Table 6.2 Pin Function

Pin Number	Pin symbol	I/O	Description	Comment
22	PA5 TXD1 TRACEDATA2	I/O	Input Output Port	
		O	TXD1	UART(TXD)
		O	TRACE data output 2	Debug port
23	PA6 RXD1 TRACEDATA3 INT0	I/O	Input Output Port	
		I	RXD1	UART(RXD)
		O	TRACE data output 3	Debug port
		I	External Interrupt 0	
24	RVSS	-	GND pin	(Note 2)
25	RVDD3	-	Power supply pin for Regulator	
26	AVDD3	-	Power supply pin for ADC	
27	PD0 AIN0	I/O	Input Output Port	
		I	ADC input	
28	PD1 AIN1	I/O	Input Output Port	
		I	ADC input	
29	PD2 AIN2	I/O	Input Output Port	
		I	ADC input	
30	PD3 AIN3	I/O	Input Output Port	
		I	ADC input	
31	PD4 AIN4	I/O	Input Output Port	
		I	ADC input	
32	PD5 AIN5	I/O	Input Output Port	
		I	ADC input	
33	PD6 AIN6	I/O	Input Output Port	
		I	ADC input	
34	PE0 AIN7	I/O	Input Output Port	
		I	ADC input	
35	PE1 AIN8	I/O	Input Output Port	
		I	ADC input	
36	PE2 AIN9	I/O	Input Output Port	
		I	ADC input	
37	PE3 AIN10	I/O	Input Output Port	
		I	ADC input	
38	PE4 AIN11	I/O	Input Output Port	
		I	ADC input	
39	PE5 AIN12	I/O	Input Output Port	
		I	ADC input	
40	PE6 AIN13	I/O	Input Output Port	
		I	ADC input	
41	AVSS	-	GND pin	(Note 2)
42	VREFH	I	Analog reference input pin for A/D conversion	
43	DVDD3	-	Power supply pin for Digital circuit	

Table 6.3 Pin Function

Pin Number	Pin symbol	I/O	Description	Comment
44	XRESET	I	External RESET input	
45	XT2	O	Low frequency oscillator output	(Note 5)
46	XT1	I	Low frequency oscillator input	
47	MODE	I	TEST pin	(Note 6)
48	X2	O	High frequency oscillator output	(Note 7)
49	DVSS	-	GND pin	(Note 2)
50	X1	I	High frequency oscillator input	(Note 7)
51	PG0 TB5OUT	I/O	Input Output Port	
		O	TMRB5 Output	
52	PG1 TB3OUT	I/O	Input Output Port	
		O	TMRB3 Output	
53	PG2	I/O	Input Output Port	
54	PG3 TB4IN1	I/O	Input Output Port	
		I	TMRB4 Input1	
55	PG4 TB4IN0	I/O	Input Output Port	
		I	TMRB4 Input0	
56	PG5 TB2IN1	I/O	Input Output Port	
		I	TMRB2 Input1	
57	PH0 TB4OUT	I/O	Input Output Port	
		O	TMRB4 Output	
58	PH1 TB2OUT	I/O	Input Output Port	
		O	TMRB2 Output	
59	PH2	I/O	Input Output Port	
60	PH3 TB5IN1	I/O	Input Output Port	
		I	TMRB5 Input1	
61	PH4 TB5IN0	I/O	Input Output Port	
		I	TMRB5 Input0	
62	PH5 TB3IN1	I/O	Input Output Port	
		I	TMRB3 Input1	
63	DVSS	-	GND pin	(Note 2)
64	DVDD3	-	Power supply pin for Digital circuit	

Note 5: Connect with low frequency X'tal resonator. If low frequency X'tal resonator is not connected, XT1 must be pull-up with resistor (10kΩ) and XT2 must be open.

Note 6: Must be connected GND.

Note 7: Connect with High frequency X'tal resonator for high accuracy clock.

Table 6.4 Pin Function

Pin Number	Pin symbol	I/O	Description	Comment
65	PI0 SCOUT	I/O	Input Output Port	
		O	Clock output	
66	PI1	I/O	Input Output Port	
67	PI2	I/O	Input Output Port	
68	PI3	I/O	Input Output Port	
69	PI4	I/O	Input Output Port	
70	PI5	I/O	Input Output Port	
71	TEST	I	TEST pin (pull-up)	(Note 8)
72	NGD1	O	VCC1-4.5V LDO output pin for internal circuit 1	(Note 9)
73	PVDD	-	System power supply pin	
74	VDD33	I/O	3.3V LDO Output or Input pin	
75	PGND1	-	GND pin	(Note 2)
76	VCC1	-	Power supply pin for CH1 to CH4 Pre-drivers 1	(Note 10)
77	VIN1	I	Capture input: Voltage1	
78	VIN2	I	Capture input: Voltage2	
79	VIN3	I	Capture input: Voltage3	
80	VIN4	I	Capture input: Voltage4	
81	IIN1	I	Capture input: Current1	
82	IIN2	I	Capture input: Current2	
83	IIN3	I	Capture input: Current3	
84	IIN4	I	Capture input: Current4	
85	HDRV1	O	High Gate driving force 1	
86	LDRV1	O	Low Gate driving force 1	
87	HDRV2	O	High Gate driving force 2	
88	LDRV2	O	Low Gate driving force 2	
89	HDRV3	O	High Gate driving force 3	
90	LDRV3	O	Low Gate driving force 3	
91	HDRV4	O	High Gate driving force 4	
92	LDRV4	O	Low Gate driving force 4	
93	HDRV5	O	High Gate driving force 5	
94	LDRV5	O	Low Gate driving force 5	
95	HDRV6	O	High Gate driving force 6	
96	LDRV6	O	Low Gate driving force 6	
97	HDRV7	O	High Gate driving force 7	
98	LDRV7	O	Low Gate driving force 7	
99	HDRV8	O	High Gate driving force 8	
100	LDRV8	O	Low Gate driving force 8	

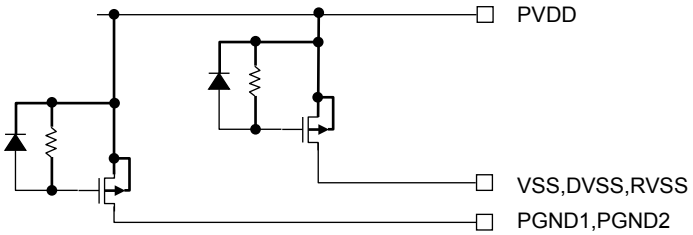
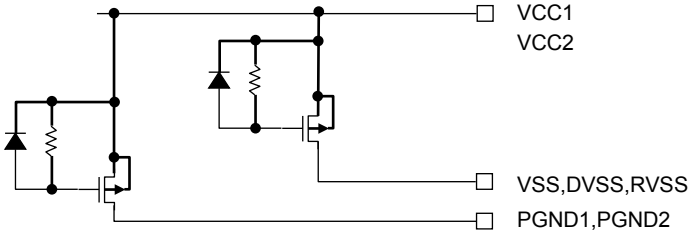
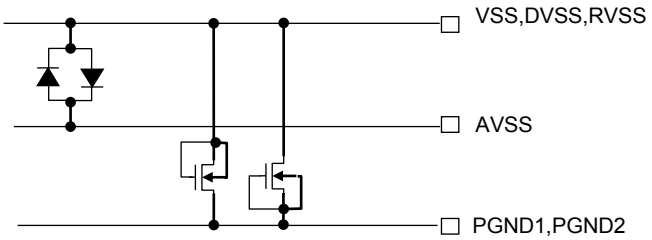
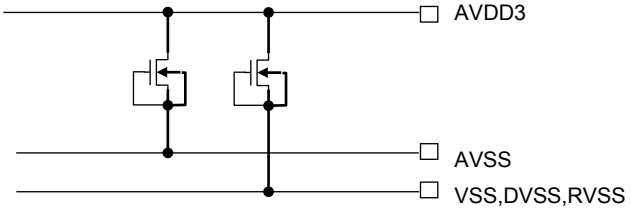
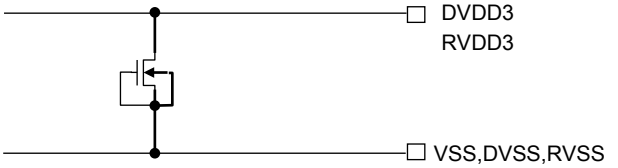
Note 8: Control input/output VDD33. When using external power supply for VDD33, set TEST="L" level.

Note 9: It is impossible to supply power to external parts. Connect capacitor (0.01μF) between NGD1 and VCC1.

Note 10: When it's not in use, connect to GND.

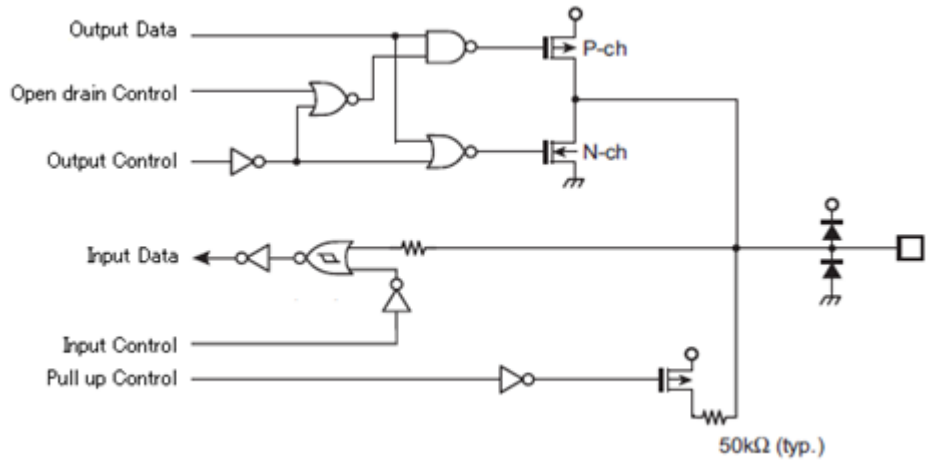
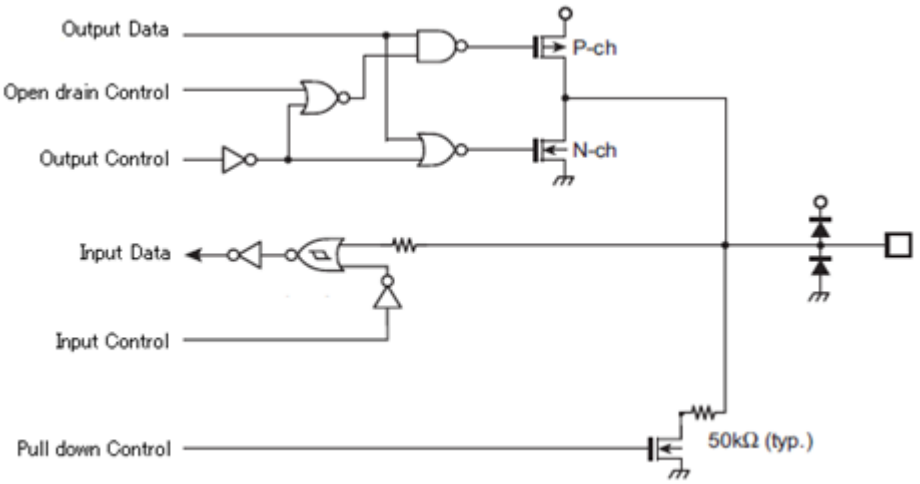
7. Equivalent circuits for input/output/power supply terminals

Table 7.1 Equivalent circuits for power supply terminals

Pin name	Equivalent circuit
PVDD-VSS,DVSS,RVSS PVDD-PGND1,2	
VCC1-VSS,DVSS,RVSS VCC2-VSS,DVSS,RVSS VCC1-PGND1,2 VCC2-PGND1,2	
VSS,DVSS,RVSS-AVSS VSS,DVSS,RVSS-PGND1,2	
AVDD3-AVSS AVDD3-VSS,DVSS,RVSS	
DVDD3-VSS,DVSS,RVSS RVDD3-VSS,DVSS,RVSS	

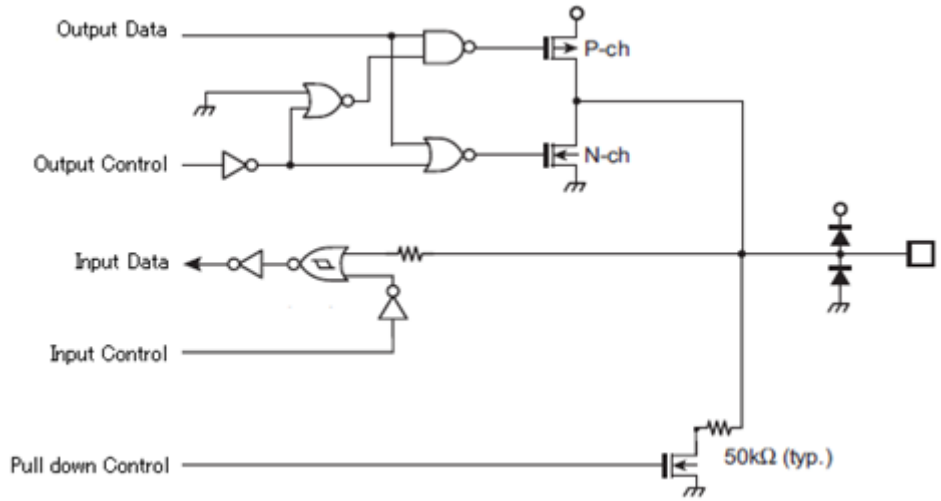
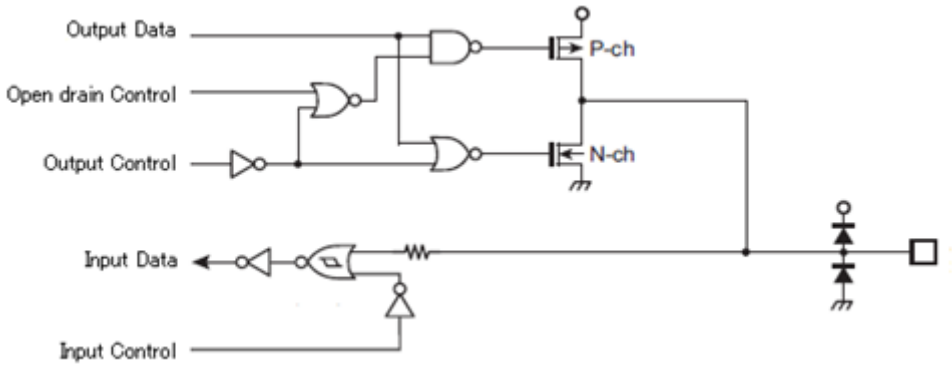
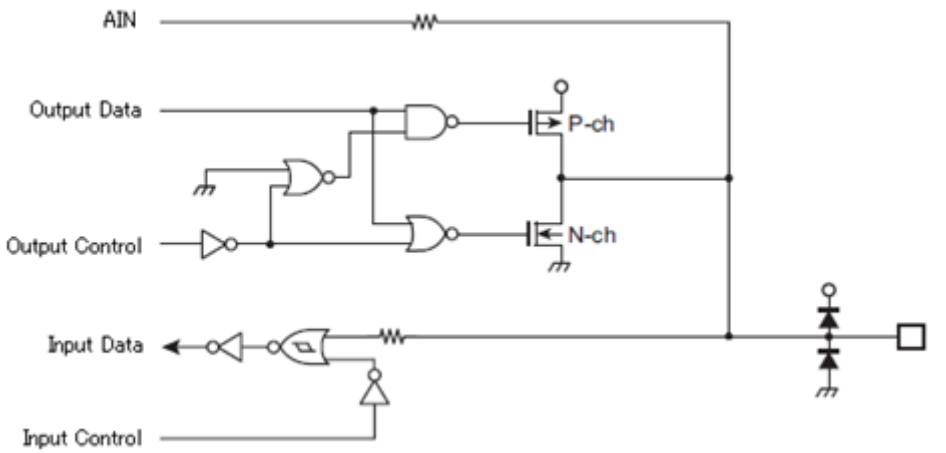
Note: Equivalent circuits may be simplified to illustrate circuits.

Table 7.2 Equivalent circuits of Input / Output terminals

Pin name	Equivalent circuit
PA0 PA2-PA6 PF0 PF1	
PA1	

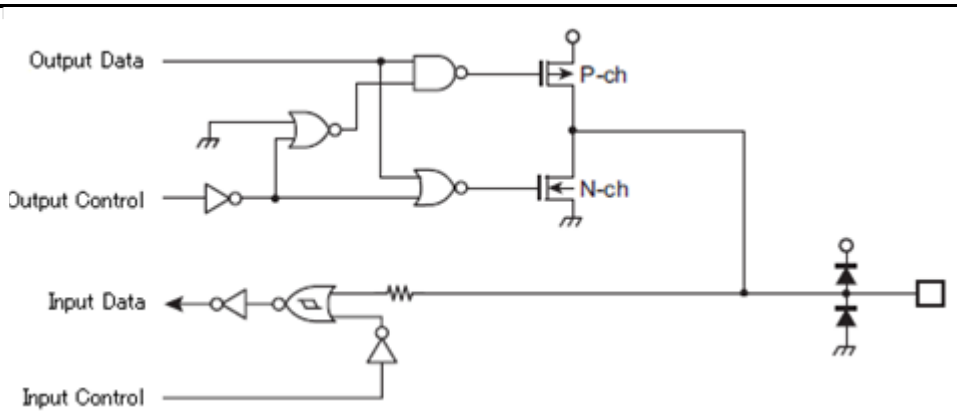
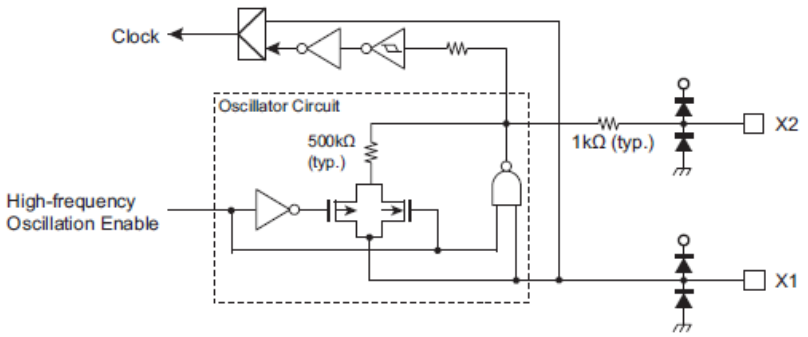
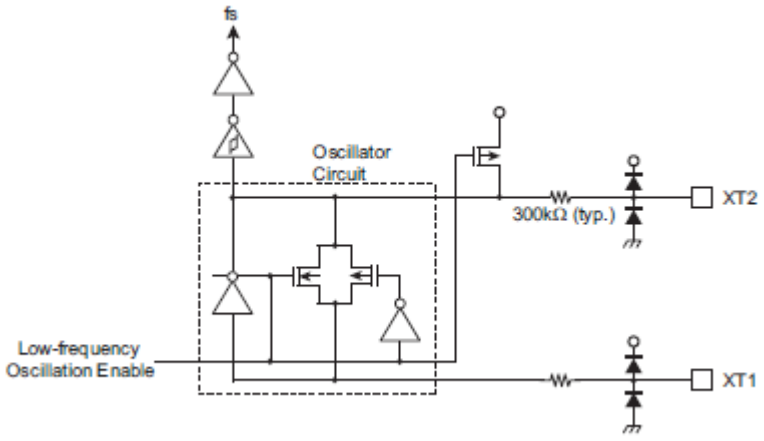
Note: Equivalent circuits may be simplified to illustrate circuits.

Table 7.3 Equivalent circuits of Input / Output terminals

Pin name	Equivalent circuit
PI0-PI5	
PC0-PC6	
PD0-PD6 PE0-PE6	

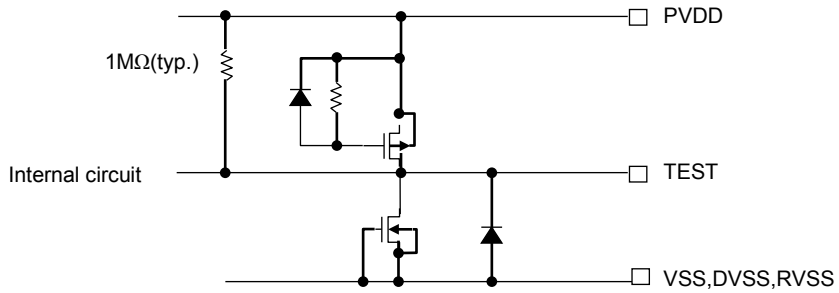
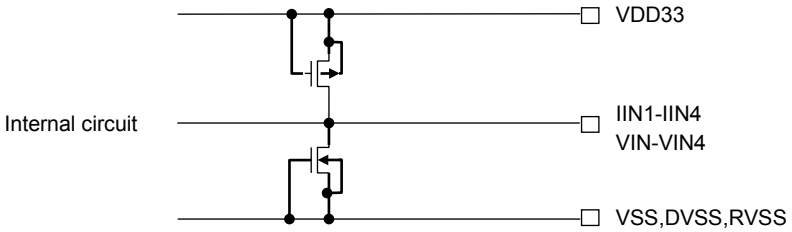
Note: Equivalent circuits may be simplified to illustrate circuits.

Table 7.4 Equivalent circuits of Input / Output terminals

Pin name	Equivalent circuit
PG0-PG5 PH0-PH5	
X1 X2	
XT1 XT2	
XRESET	

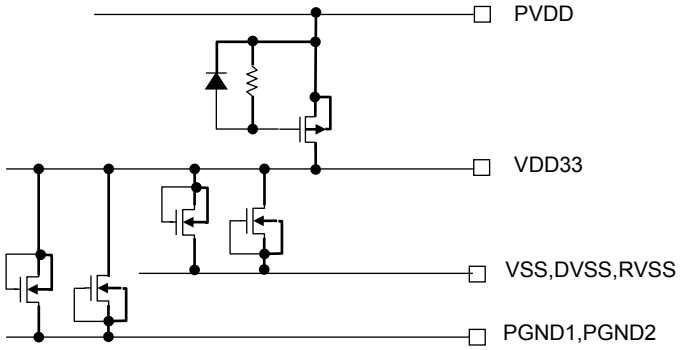
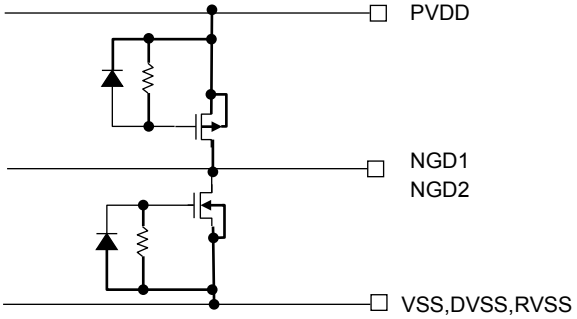
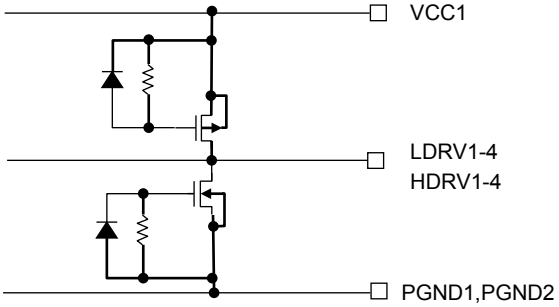
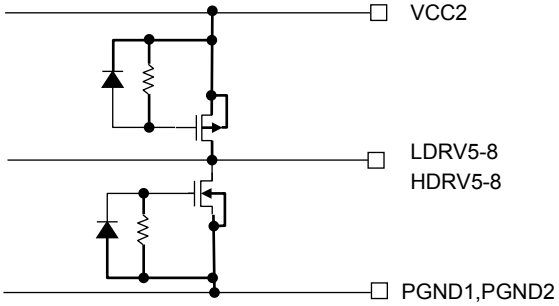
Note: Equivalent circuits may be simplified to illustrate circuits.

Table 7.5 Equivalent circuits of Input terminals

Pin name	Equivalent circuit
MODE	 (Note)MODE pin is fixed to GND.
FTEST3	 (Note)FTEST3 pin is fixed to Open.
TEST	
IIN1-IIN4 VIN1-VIN4	

Note: Equivalent circuits may be simplified to illustrate circuits.

Table 7.6 Equivalent circuits of Output terminals

Pin name	Equivalent circuit
VDD33	
NGD1	
LDRV1-4 HDRV1-4	
LDRV5-8 HDRV5-8	

Note: Equivalent circuits may be simplified to illustrate circuits.

8. Function

8.1 General outline of wireless power system

Qi compliant wireless power system consists of the first side (TX) which transmits power and the second side (RX) which receives power. Power is transmitted by adjoining coils included in TX and RX and by sharing and combining flux. RX controls the power by monitoring receiving power and sending feedback signal to TX. TX controls the power by controlling transmitting power with feedback signal which is received from RX. Configuration example of wireless power system is shown in Figure 8.1.

Communication signal from RX to TX is transmitted (modulated) by ASK modulation. The communication rate and its packet in this communication are defined by Qi compliant. Communication rate is 2kbps. Packets are ID, identification signal, error information, receive power, and stop signal.TX stops its operation in normal mode. It is powered on intermittently and confirms the existence of RX on the TX pad. When TX recognizes RX and succeeds the identification, transmit operation starts. TX continues transmit operation until TX cannot recognize the existence of RX or receives transmit stop signal from RX.

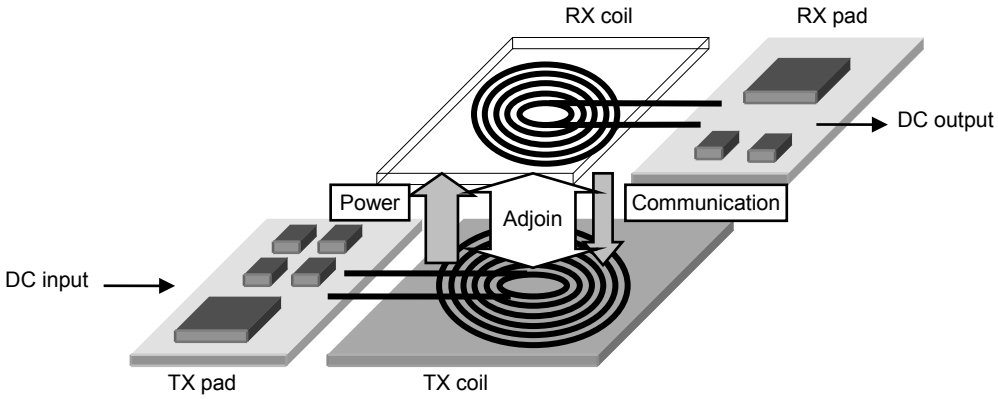


Figure 8.1 General outline of Wireless power system

8.2 Processor Core

The TB6865AFG has a high-performance 32-bit processor core (the ARM Cortex-M3 processor core). For information on the operations of this processor core, please refer to the "Cortex-M3 Technical Reference Manual" issued by ARM Limited. This chapter describes the functions unique to the TB6865AFG that are not explained in that document.

8.2.1 Information on the processor core

The following table shows the revision of the processor core in the TB6865AFG.
Refer to the detailed information about the CPU core and architecture; refer to the ARM manual "Cortex-M series processors" in the following URL: http://infocenter.arm.com/help/index.jsp

Product Name	Core Revision
TB6865AFG	r2p1

8.2.2 Configurable Options

The Cortex-M3 core has optional blocks. The following table shows the configurable options in the TB6865AFG.

Table 8.1 Option

Configurable Options	Implementation
FPB	Two Internal comparators Six Instruction comparators
DWT	Four comparators
ITM	Implementable
MPU	Not implementable
ETM	Implementable
AHB-AP	Implementable
AHB Trace Macro cell Interface	Implementable
TPIU	Implementable
WIC	Not implementable
Debug Port	JTAG / Serial Wire
Bit Band	Present
Constant AHB control	Absent

8.3 Reset

The TB6865AFG has four reset sources: an external reset pin (XRESET), a low voltage detection reset (LVD) and the setting <SYSRESETREQ> in the Application Interrupt and Reset Control Register.
For reset from the LVD, refer to the 8.10 LVD.

For reset from <SYSRESETREQ>, refer to "Cortex-M3 Technical Reference Manual".

8.4 High Resolution PWM Output: (HRPWM)

HRPWM unit consists of four PWM outputs and TB6865AFG has two units of this HRPWM. The functions are as follows.

- Outputs : Eight channels (four channels x two unit)
  - Unit1: PWMOUT1/2, PWMOUT3/4, Unit2: PWMOUT5/6, PWMOUT7/8
  - It can connect Full Bridge Inverter
- PWM Frequency : 90kHz to 205kHz and 250kHz
- Frequency step : Under 100Hz
- Dead time generator : 50ns to10μs, 50ns step

8.5 Capture Communication port

Capture Communication Port is use for communication from RX to TX that is defined by Wireless Power Consortium(WPC). (Note)

This IC has four channels of Capture Communication Port. And they can be used independently.

Their features are given in the following.

- Automatic decoding with backscatter modulation signal
- It can be busy to up to ten words

Note: Please refer to WPC document that is “System Description, Wireless Power Transfer, Volume I: Low Power, Part 1: Interface Definition, Version 1.0.3, September 2011”.

8.6 Pre driver

TB6865AFG has 16 pre-drivers for full-bridge invertor.

8.6.1 Configuration

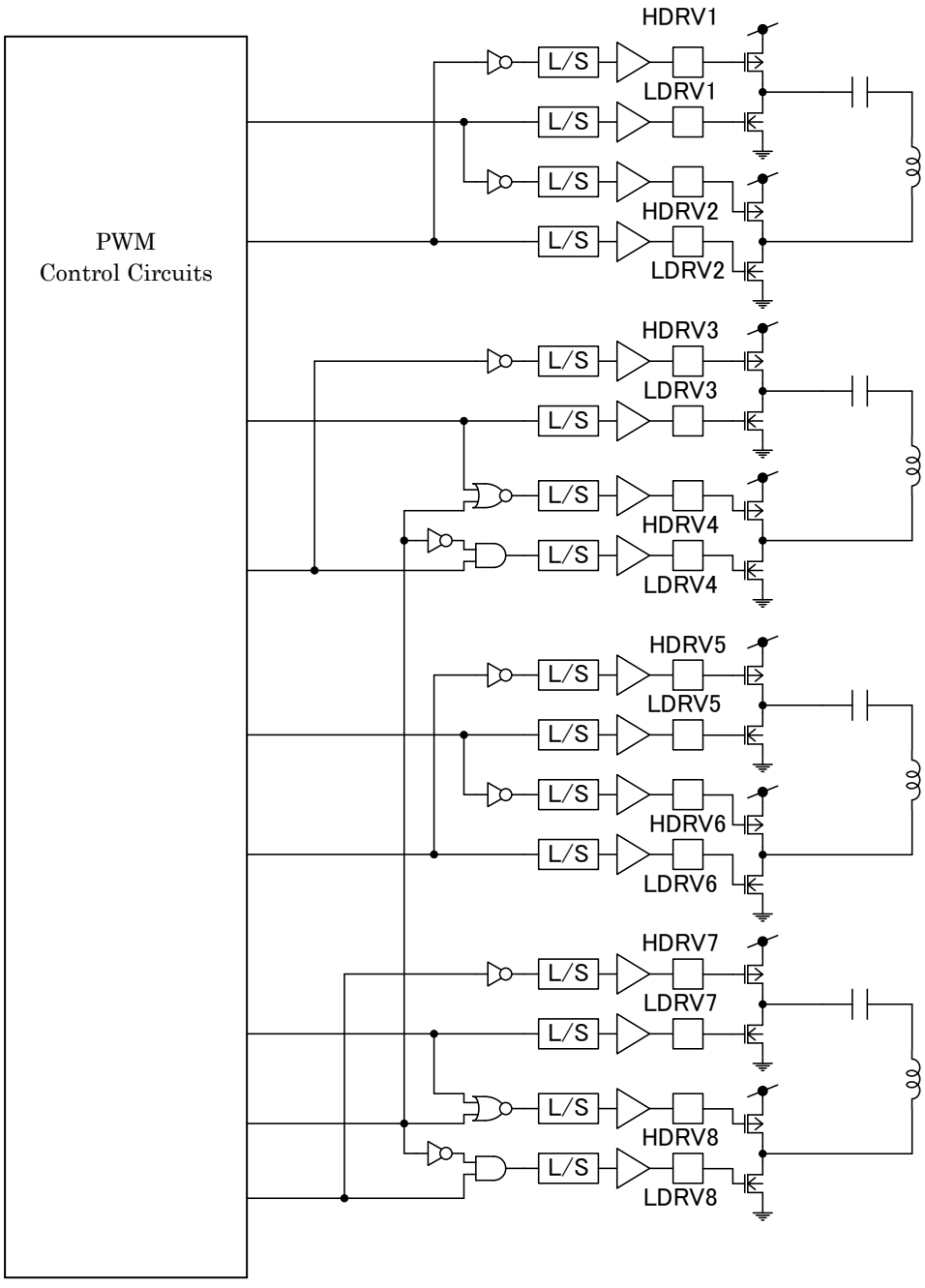


Figure 8.2 Pre-driver circuit

8.7 LDO

TB6865AFG has three LDOs. VDD33 is for MCU block and NGD1, NGD2 are for Pre driver. User cannot use these LDOs output since they are only used for inside circuit of this product.

8.7.1 VDD33 (Output pin mode)

VDD33 is 3.3V voltage source for MCU block. Connect capacitor of 1μF to GND.

8.7.2 NGD1,NGD2

NGD1 and NGD2 are LDOs which are used in pre-driver block.
Note: Connect capacitor of 0.01μF to VCC.

8.8 Analog/Digital Converter (ADC)

TB6865AFG contains a 12-bit, sequential-conversion analog/digital converter (ADC) with 14 analog input channels.

These 14 analog input channels (pins AIN00 through AIN13) are also used as input/output ports.

8.9 Power on reset (POR)

The power-on-reset circuit (POR) generates a power-on reset signal when power-on.
Power supply voltage is indicated as DVDD3(=AVDD3=RVDD3).

8.9.1 Configuration

Power-on-reset circuit consists of the reference voltage generation circuit, comparators, the LVD reset circuit and the power-on counter.

This circuit compares a voltage divided by the ladder resistor with a reference voltage generated in the reference voltage generation circuit in the comparator.

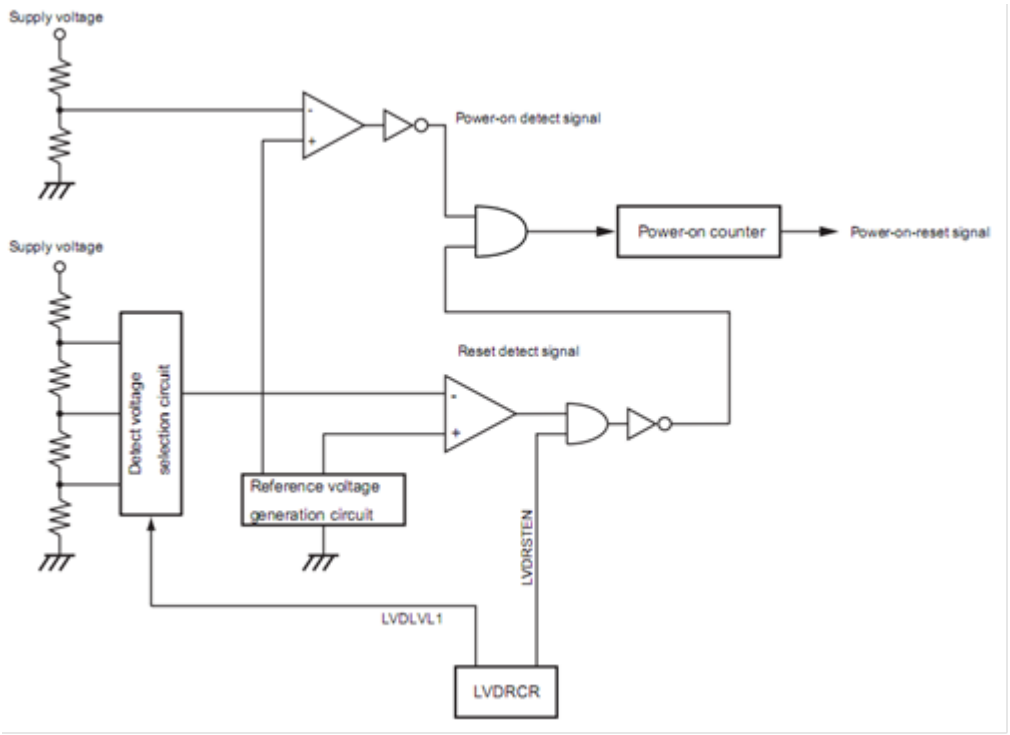


Figure 8.3 Power-on-reset circuit

For details of LVDRCR in LVD reset circuit, refer to Section "Low Voltage Detection Circuit (LVD)".

8.10 Low Voltage Detection Circuit (LVD)

Voltage detection circuit generates a reset signal or an interrupt signal (NMI) by detecting a decreasing/increasing voltage.

Supply voltage is indicated as DVDD3(=AVDD3=RVDD3).

Note: Due to the fluctuation of supply voltage, the power-on reset circuit may not operate properly. Users should give due consideration based on the electrical characteristic in the device designing.

8.10.1 Configuration

The voltage detection circuit consists of a reference voltage generation circuit, comparators and control registers.

Supply voltage is divided by a ladder resistor and input to the voltage selection circuit. In the voltage selection circuit, a voltage is chosen according to the detected voltage then compared with the reference voltage in the comparator. If the supply voltage is upper/lower than the detected voltage, a reset/interrupt signal occurs.

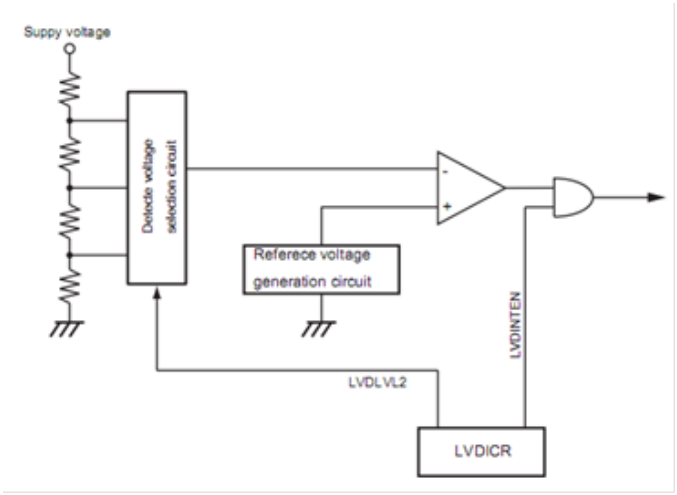


Figure8.4 Block diagram of LVD (LVD interrupt circuit)

8.10.2 Power On and Power Off sequence

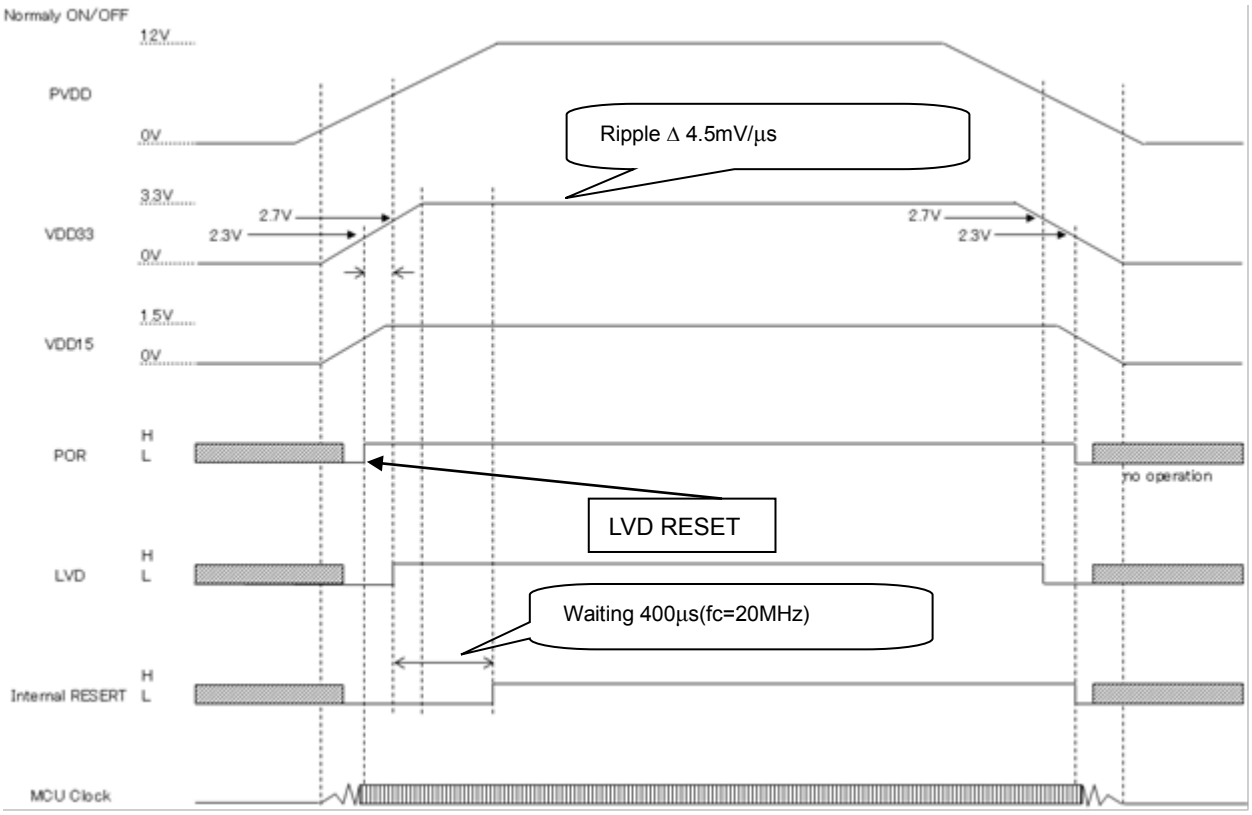


Figure8.5 Power on Power off sequence

Note: POR, LVD, Internal RESET are “low” active.

9. Absolute Maximum Ratings (Ta= 25°C)

Table 9.1 Absolute Maximum Ratings

Characteristics		Symbol	Rating	Unit
Supply Voltage		DVDD3	-0.3 to 3.9	V
		AVDD3		
		RVDD3		
		PVDD	-0.3 to 24	V
		VCC1		
		VCC2		
Input Voltage 0 (Note 1)		V_{IN}	-0.3 to 3.9	V
Input Voltage 2 (Note 2)		V_{IN2}	-0.3 to min(5.5, PVDD+0.3)	V
Input Voltage 3 (Note 3)		V_{IN3}	-0.3 to VIN2+0.3	V
Low-level Output Current	Per pin	I_{OL}	5	mA
	Total	ΣI_{OL}	50	
Low-level Large Output Current	Per pin	I_{OL}	16	
	Total	ΣI_{OL}	50	
High-level Output Current	Per pin	I_{OH}	-5	
	Total	ΣI_{OH}	-50	
Output Voltage 1 (Note 4)		V_{OUT1}	-0.3 to VCC1+0.3	V
Output Voltage 2 (Note 5)		V_{OUT2}	-0.3 to VCC2+0.3	V
Output Current (Note 6)		I_{OUT1}	500	mA
Power Consumption (Except during Flash W/E, Ta=25°C)		PD1	2780	mW
Power Consumption (During Flash W/E, Ta=25°C)		PD2	1670	mW
Soldering Temperature (10s)		T_{SOLDER}	260	°C
Storage Temperature		T_{STG}	-40 to 125	°C
Operating Temperature	Expect during Flash W/E	T_{OPR}	-40 to 85	°C
	During Flash W/E		0 to 70	

Note: The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating (s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
Please use the IC within the specified operating ranges.

Note 1: Apply to input terminals except Note 2, 3.

Note 2: Apply to VDD33 terminal (when TEST=0).
A = min(A, B) when A≦B. B = min(A, B) when A>B.

Note 3: Apply to VIN[4:1] and IIN[4:1] terminals.

Note 4: Apply to HDRV[4:1] and LDRV[4:1] terminals.

Note 5: Apply to HDRV[8:5] and LDRV[8:5] terminals.

Note 6: Apply to HDRV[8:1] and LDRV[8:1] terminals.

10. DC Electrical Characteristics

10.1 DC Electrical Characteristics(MPU part)(1/3)

Table 10.1 DC Electrical Characteristics (MPU part)(1/3)

(Unless otherwise specified, DVSS=AVSS=RVSS=0V, Ta= -40 to 85°C)

Characteristics		Symbol	Test condition	Min	Typ. (Note 1)	Max	Unit
Supply voltage	DVDD3 AVDD3 RVDD3 (Note 2)	DVDD3 AVDD3 RVDD3	fosc = 20MHz fsys = 1 to 20MHz	2.7	-	3.6	V
Low-level input voltage		V_{IL1}	2.7V ≦DVDD3 ≦3.6V	-0.3	-	0.25× DVDD3	V
High-level input voltage		V_{IH1}	2.7V ≦DVDD3 ≦3.6V	0.75× DVDD3	-	DVDD3+0.3	V
Low-level output voltage		V_{OL1}	IOL=2mA 2.7V ≦DVDD3 ≦3.6V <Except PC1 to PC6>	-	-	0.4	V
		V_{OL2}	IOL=10mA 2.7V ≦DVDD3 ≦3.6V <PC1 to PC6 >	-	-	0.4	V
High-level output voltage		V_{OH}	IOH=-2mA 2.7V ≦DVDD3 ≦3.6V	2.4	-	-	V
Input leakage current		I_{LI}	0.0V ≦VIN ≦DVDD3 0.0V ≦VIN ≦AVDD3	-	0.02	± 5	μA
Output leakage current		I_{LO}	0.2V ≦VIN≦ (DVDD3-0.2) 0.2V ≦VIN≦ (AVDD3-0.2)	-	0.05	± 10	
Pull-up resistance (RESET pin)		R_{RST}	DVDD3 =2.7V to 3.6V	-	50	150	kΩ
Schmitt triggered port		V_{TH1}	2.7V ≦DVDD3 ≦3.6V	0.3	0.6	-	V
Programmable pull-up/pull-down resistance		P_{KH}	DVDD3=2.7V to 3.6V	-	50	150	kΩ
Pin capacitance (except power supply pins)		C_{IO}	fc =1MHz	-	-	10	pF

Note 1: Unless otherwise specified, Ta=25°C, DVDD3=RVDD3=AVDD3=3.3 V

Note 2: The same voltage must be supplied to DVDD3, AVDD3 and RVDD3.

Note 3: Ensure that all power supply source is power-off and then power-on again when DVDD3, RVDD3 and AVDD3 falls below 2.7V which is minimum operating voltage

10.2 DC Electrical Characteristics(MPU part) (2/3)

Table 10.2 DC Electrical Characteristics(MPU part) (2/3)

Characteristics	Symbol	Test condition	Min	Typ. (Note 1)	Max	Unit
Low-level output current	I_{OL1}	2.7V ≦DVDD3 ≦3.6V < Except PC1 to PC6> per pin	-	-	2	mA
	I_{OL2}	2.7V ≦DVDD3 ≦3.6V <PC1 to PC6> per pin	-	-	10	mA
	ΣI_{OL}	Total	-	-	35	
High-level output current	I_{OH}	2.7V ≦DVDD3 ≦3.6V Per pin	-	-	-2.0	mA
	ΣI_{OH}	Total	-	-	-35	

Note 1: Unless otherwise specified, Ta=25°C, DVDD3=RVDD3=AVDD3=3.3 V

10.3 DC Electrical Characteristics(MPU part) (3/3)

Table 10.3 DC Electrical Characteristics(MPU part) (3/3)

Characteristics	Symbol	Test condition	Min	Typ. (Note 1)	Max	Unit
NORMAL(Note 2) Gear1/1	I_{DD}	fsys = 20 MHz	-	15	20	mA
IDLE (Note 3)			-	7	12	
STOP1		fs = 32.768kHz	-	150	650	μA

Note 1: Unless otherwise specified, Ta=25°C, DVDD3=RVDD3=AVDD3=3.3 V.

Note 2: IDD NORMAL: Measured with Dhrystone ver.2.1 operated in FLASH. All functions operate excluding A/DC and D/AC.

Note 3: IDD IDLE: Measured with all functions stopped. The currents flow through DVDD3, AVDD3 and RVDD3 are included.

10.4 DC Electrical Characteristics(Analog part)

Table 10.4 LDO33

(Unless otherwise specified, COUT=1.0μF, PVDD=12V, Ta = 25°C)

Characteristics	Symbol	Test condition	Min	Typ.	Max	Unit
Supply voltage	PVDD		4.5	-	14	V
Output voltage	VDD33		2.7	-	3.6	V
Output current	Iout33		-	60	-	mA
Line regulation	Line33	PVDD=5V→14V Iout33=1mA	-	-	33	mV
Load regulation	Load33	PVDD=5V Iout33=0mA→60mA	-	-	165	mV

Table 10.5 NGD1, NGD2

(Unless otherwise specified, COUT=0.1μF, PVDD=12V, Ta=25°C)

Characteristics	Symbol	Test condition	Min	Typ.	Max	Unit
Supply voltage	VCC1 VCC2		4.5	-	14	V
Output voltage	NGD1		-	VCC1-4.5	-	V
	NGD2		-	VCC2-4.5	-	
Output current	IoutNGD1	NGD1=VCC1-4.5V	-	15	-	mA
	IoutNGD2	NGD2=VCC2-4.5V	-	15	-	

Table 10.6 Pre driver

(Unless otherwise specified, PVDD=12V, Ta=25°C)

Characteristics	Symbol	Test condition	Min	Typ.	Max	Unit
Supply voltage	VCC1 VCC2		4.5	-	14	V
High side MOS Ron	RonH	Ids=0.1A	-	-	10	Ω
Low side MOS Ron	RonL	Ids=0.1A	-	-	10	Ω
Slew rate rise	Tr	Output capacitor=1000pF	-	-	100	ns
Slew rate fall	Tf	Output capacitor=1000pF	-	-	100	ns

Table 10.7 Filter

(Unless otherwise specified, PVDD=12V, Ta=25°C)

Characteristics	Symbol	Test condition	Min	Typ.	Max	Unit
Supply voltage	VDD33		2.7	-	3.6	V
Cutoff frequency (LPF)	FcLPF		2.9	5	7.5	kHz
Differential input range	Rdiff		-	20	VDD33	mV

10.5 12-bit ADC Electric Characteristics

Table 10.8 12-bit ADC Electric Characteristics

DVDD3=AVDD3=RVDD3=VREFH=2.7V to 3.6V, AVSS=DVSS, Ta= -40 to 85°C
AVDD3 load capacitance≧3.3μF, VREF load capacitance≧3.3 μF

Characteristics		Symbol	Test condition	Min	Typ.	Max	Unit
Analog reference voltage(+)		AV_{REFH}	-	2.7	3.3	3.6	V
Analog input voltage		V_{AIN}	-	AVSS	-	VREFH	V
Power supply current of analog reference voltage	AD conversion	I_{REF}	DVSS = AVSS	-	2.0	2.5	mA
	Non-AD conversion			-	-	5	μA
Supply current	AD conversion	ADIcc	Except IREF	-	1.0	2.0	mA
INL error		-	AIN resistance ≦ 1 kΩ AIN load capacitance ≦ 0.1 μF Conversion time ≧ 2.0 μs (ADCLK=20MHz)	-	-	±9	LSB
DNL error				-	-	±9	
Offset error				-	-	±9	
Full-scale error				-	-	±9	
Total error				-	-	±9	
Conversion time		Tconv	ADCLK=20MHz	2	-	10	μs

Note: 1LSB = (AVREFH - AVSS)/4096 [V]

Note: Peripheral functions are disabled.

±9LSB@12bit -> ±2.25LSB@10bit

10.6 On chip oscillator

Table 10.9 On chip oscillator

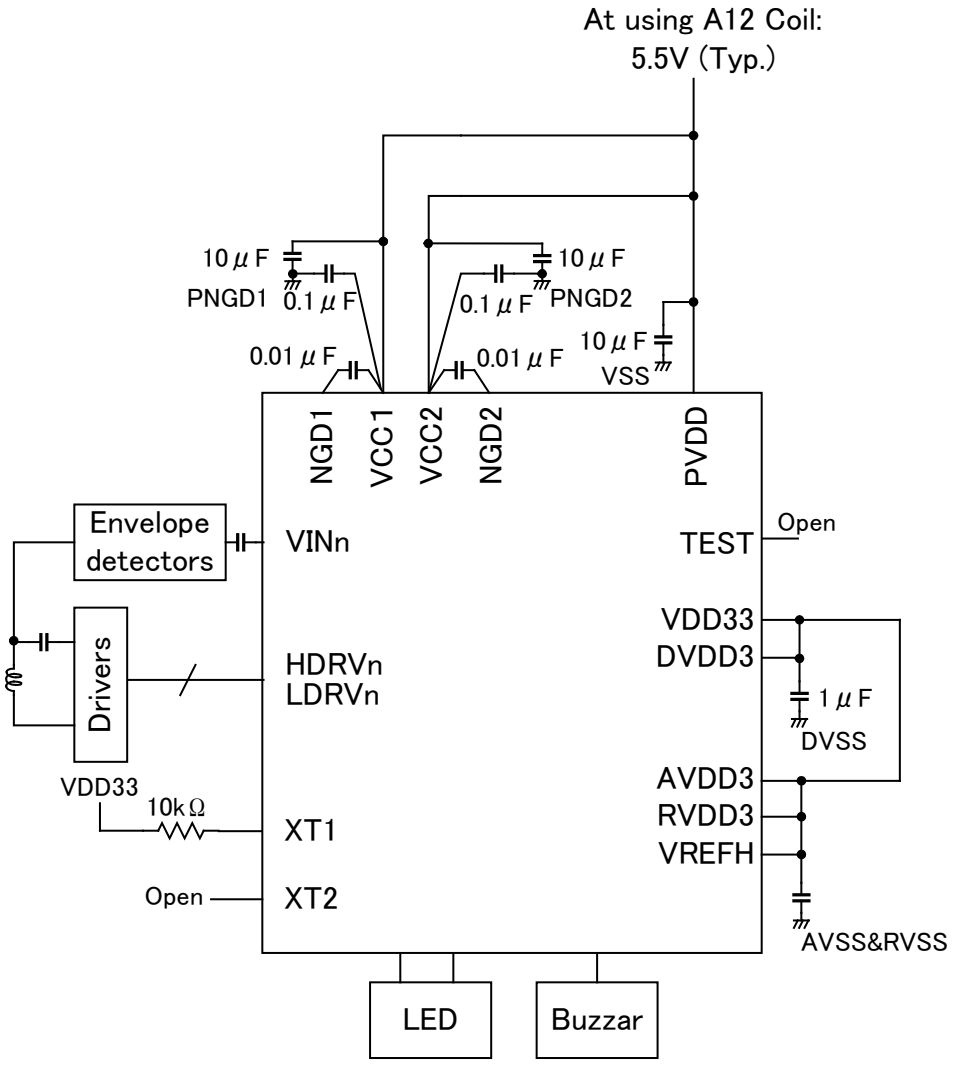
Characteristics	Symbol	Test condition	Min	Typ.	Max	Unit
Oscillating frequency	I_{HOSC}	Ta = 0 to 85°C	-	20	-	MHz

Note: ±3%

10.7 Electrostatic Discharge(ESD)

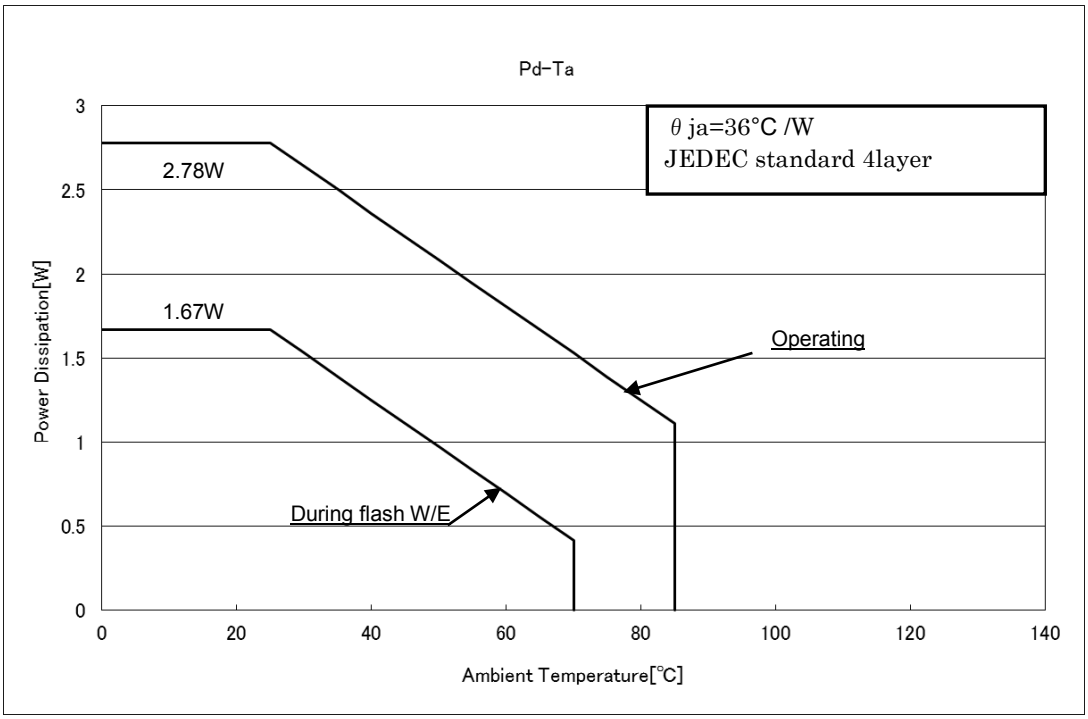
Note: Caution about the electric discharge(ESD) sensitivity of this product.
For ESD test data of this product, please contact your local Toshiba sales representative.

11. Application circuit



12. Thermal Estimation

This figure is allowable power dissipation graph of TB6865AFG.



You have to design PCB layout so that power loss does not go beyond this Pd-Ta line in this graph.

This graph is based on JEDEC standard 4 layers PCB. Thermal resistance strongly depends on the size of PCB, the pattern layout, and the number of layer of PCB.

You can thermal calculation with following formulas.

- Using built-in 3.3V LDO.

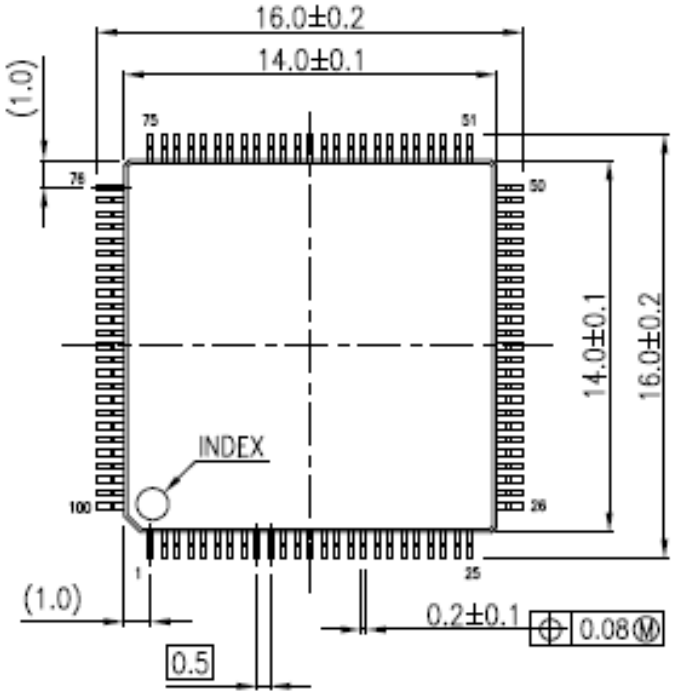
$$\Delta T = \theta ja \times \left(Vpvdd \times Ipvdd + Vvcc \times Ivcc + Vpvdd \times Ivdd \right)$$

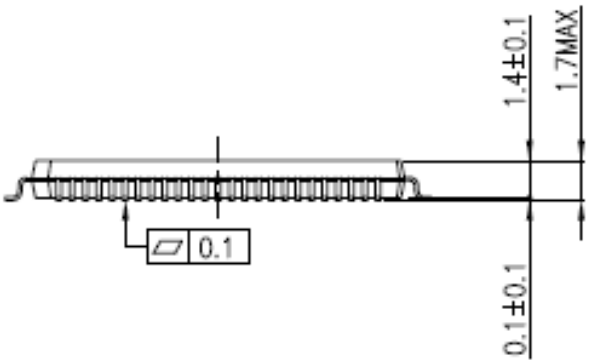
Vpvdd =PVDD voltage
Ipvdd =PVDD current
Vvcc=VCC1 voltage=VCC2 voltage
Ivcc=VCC1 current + VCC2 current
Vvdd=VDD33 voltage=DVDD3 voltage=AVDD3 voltage=RVDD3 voltage
Ivdd33=VDD33 current
Imcu=MCU current
Iled= Indicator LED current
Ivdd=Ivdd33+Imcu+Iled

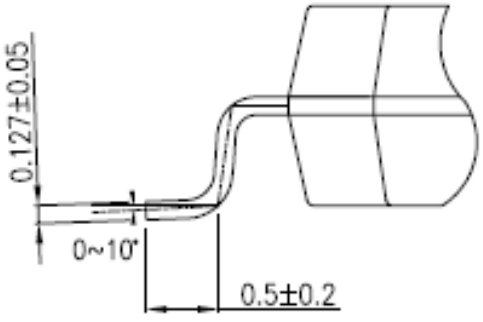
13. Package Dimensions

LQFP100-P-1414-0.50G

Unit: mm







Weight: 0.62g (typ.)

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