Ordering Information⁽¹⁾

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY898530UTZ	TQFP-48	Commercial	SY898530UTZ with Pb-Free bar-line indicator	Matte-Sn
SY898530UTZTR ⁽²⁾	TQFP-48	Commercial	SY898530UTZ with Pb-Free bar-line indicator	Matte-Sn
SY898530UTZTX ^(2, 3)	TQFP-48	Commercial	SY898530UTZ with Pb-Free bar-line indicator	Matte-Sn

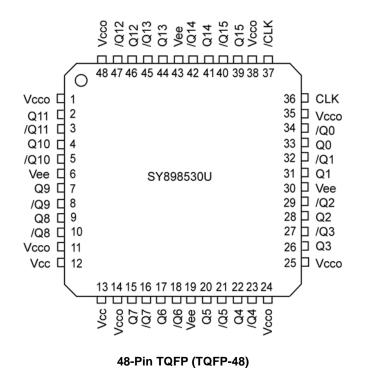
Notes:

1. Contact factory for die availability. Dice are guaranteed at $T_A = 25^{\circ}C$, DC Electricals only.

2. Tape and Reel.

3. EIA specification orientation.

Pin Configuration



Pin Description

Pin Number	Pin Name	Pin Function
36, 37	CLK, /CLK	Differential Clock Inputs. Accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL logic levels. CLK is internally connected to a pull-down resistor, /CLK is internally connected to a pull- up resistor. See "Pin Characteristics" for typical values.
33, 34	Q0, /Q0	
31, 32	Q1, /Q1	
28, 29	Q2, /Q2	
26, 27	Q3, /Q3	
22, 23	Q4, /Q4	
20, 21	Q5, /Q5	
17, 18	Q6, /Q6	
15, 16	Q7, /Q7	LVPECL Differential Output Pairs. Differential buffered copies of the input signal. The
9, 10	Q8, /Q8	output swing is typically 740mV. See Interface Applications for termination information.
7, 8	Q9, /Q9	
4, 5	Q10, /Q10	
2, 3	Q11, /Q11	
46, 47	Q12, /Q12	
44, 45	Q13, /Q13	
41, 42	Q14, /Q14	
39, 40	Q15, /Q15	
1, 11, 14, 24,	1/000	Output Power Supply: Bypass with 0.1µF//0.01µF low ESR capacitors as close to the
25, 35, 38, 48	VCCO	V_{CCO} pins as possible. Supplies the output buffers.
12, 13	VCC	Core Power Supply: Bypass with $0.1\mu F//0.01\mu F$ low ESR capacitors as close to the V _{CC} pins as possible. Supplies input and core circuitry.
6, 19, 30, 43	VEE	Ground

Pin Characteristics

Symbol	Description	Min.	Тур.	Max.	Units
CIN	Input Capacitance		4		pF
R _{PULLUP}	Input Pull Up Resistor		50		KΩ
R _{PULLDOWN}	Input Pull Down Resistor		30		KΩ

Clock Input Function Table

Inj	outs	Out	puts	Innut to Output Mode	Delerity
CLK	/CLK	Qx	/Qx	Input to Output Mode	Polarity
0	1	Low	High	Differential to Differential	Non-Inverting
1	0	High	Low	Differential to Differential	Non-Inverting
0	Biased ⁽¹⁾	Low	High	Single-Ended to Differential	Non-Inverting
1	Biased ⁽¹⁾	High	Low	Single-Ended to Differential	Non-Inverting
Biased ⁽¹⁾	0	High	Low	Single-Ended to Differential	Inverting
Biased ⁽¹⁾	1	Low	High	Single-Ended to Differential	Inverting

Note:

1. Refer to Interface Applications for Single-Ended Interfaces.

Absolute Maximum Ratings⁽¹⁾

Supply Voltage (V _{CC})4.6V
Input Voltage (V_{IN})–0.5V to V_{CC} + 0.5V
LVPECL Output Current (I _{OUT})
Continuous50mA
Surge100mA
Lead Temperature (soldering, 20sec.)
Storage Temperature (T_s) –65°C to +150°C

Operating Ratings⁽²⁾

Supply Voltage (V _{CC})	3.135V to 3.465V
Output Supply Voltage (V _{CCO})	2.375V to 3.465V
Ambient Temperature (T _A)	0°C to +70°C
Package Thermal Resistance ⁽³⁾	
TQFP	
Still-air (θ_{JA})	48°C/W
Junction-to-Case (θ_{JC})	13°C/W

DC Electrical Characteristics⁽⁶⁾

Symbol	Parameter Power Supply Voltage Range		Condition	Min.	Тур.	Max.	Units
Vcc			Power Supply Voltage Range	3.135	3.3	3.465	V
V _{CCO}	Output Power Supply			2.375		3.465	V
I _{EE}	Power Supply Current		Max. V _{CC} , V _{CCO}			125	mA
I _{IH} Input HIGH Curren		CLK	- V _{CC} = V _{IN} = 3.465V			150	uA
		/CLK				5	uA
IIL Input LOW Current			-5			uA	
		$-V_{\rm CC} = 3.465 V, V_{\rm IN} = 0.5 V$	-150			uA	
V_{PP}	Peak-to-Peak Input Sv	ving		0.15		1.3	V
V _{CMR}	Common Mode Input	Voltage	Note 4, 5	0.5		V _{cc} - 0.85	V

 V_{CC} = 3.135V to 3.465V, V_{CCO} = 2.375V to 3.465V, T_A = 0°C to +70°C, unless otherwise stated.

PECL Outputs DC Electrical Characteristics⁽⁶⁾

 V_{CC} = 3.135V to 3.465V, V_{CCO} = 2.375V to 3.465V, T_A = 0°C to +70°C, Outputs terminated with 50 Ω to V_{CCO} -2V unless otherwise stated.

Symbol	Parameter	Condition	Min.	Тур.	Max.	Units
V _{OH}	Output HIGH Voltage		V _{CCO} – 1.1		$V_{\text{CCO}} - 0.7$	V
V _{OL}	Output LOW Voltage		$V_{\text{CCO}}-2.0$		$V_{CCO}-1.4$	V
V _{OUT}	Output Voltage Swing		0.55		0.93	V

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

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2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

3. θ_{JA} and θ_{JC} values are determined for a 4-layer board in still-air.

4. For single-ended applications, the maximum input voltage for CLK, /CLK is V_{CC} +0.3V.

5. Common mode voltage is defined as $V_{\mbox{\scriptsize IH}}.$

6. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC Electrical Characteristics

 V_{CC} = 3.135V to 3.465V, V_{CCO} = 2.375V to 3.465V, T_A = 0°C to +70°C, unless otherwise stated.

Symbol	Parameter	Condition	Min.	Тур.	Max.	Units
f _{MAX}	Maximum Frequency		500			MHz
t _{PD}	Propagation Delay	Note 7	1		2	ns
	Output-to-Output skew	Note 8, 10		26	50	ps
t _{Skew}	Part-to-Part Skew	Notes 9, 10			250	ps
t _{JITTER}	Integration Range = 12kHz – 20MHz	Output = 500MHz		127		fs _{RMS}
t _R , t _F	Output Rise/Fall Times (20% to 80%)	At full output swing.	300		700	ps
	Duty Cycle		47	50	53	%

Notes:

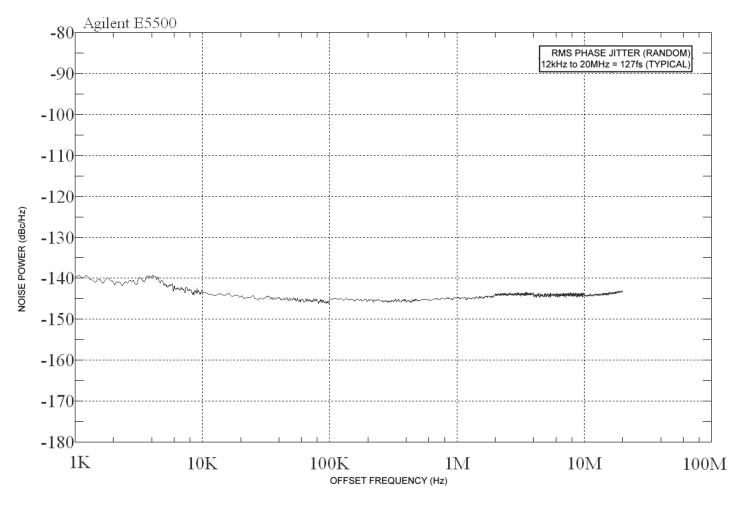
8. Output-to-Output skew is the difference in time between outputs, receiving data from the same input, for the same temperature, voltage and transition.

9. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and no skew at the edges at the respective inputs.

10. This parameter is defined in accordance with JEDEC Standard 65.

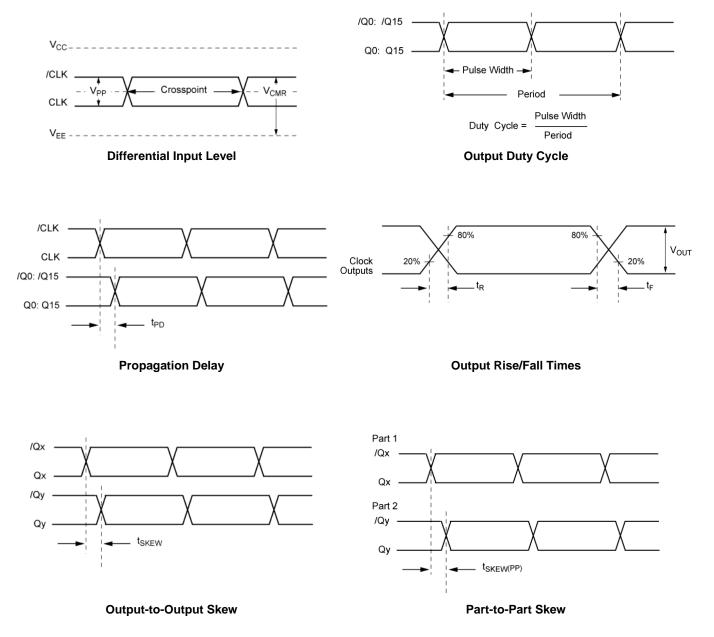
^{7.} Measured from the differential input crossing point to the differential output crossing point.

Phase Noise Graph



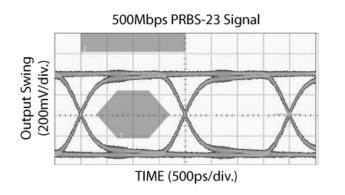
Phase Noise Plot: 500MHz @ 3.3V

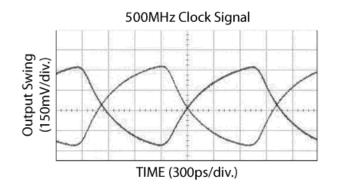
Test Circuit



Typical Characteristics

 V_{CC} = 3.3V, V_{CCO} = 2.5V or 3.3V, T_A = 25°C, Input Signal = 800mV





Junction Temperature

The maximum recommended junction temperature is $T_J = 125$ °C. The outputs are terminated with 50 ohms to Vcco - 2V. Below is a calculation of the worst case scenario with zero airflow:

 T_J = Junction Temperature T_A = Ambient Temperature Θ_{JA} = Junction-to-Ambient Thermal Resistance P_d = Power Dissipation

 $P_{d} = P_{d_core} + P_{d_outputs}$ $P_{d_core} = V_{cc_max} * I_{ee_max}$ $P_{d_core} = 3.465V * 125mA = 433mW$

$$\begin{split} & P_{d_output} = Pd_h + Pd_I \\ & P_{d_h} = [(V_{oh} - (V_{cco} - 2V))/R_L] * (V_{cco} - V_{oh_max}) \\ & P_{d_h} = [(2V - 0.7V)/50\Omega] * 0.7V \\ & P_{d_h} = 18.2mW \\ & P_{d_1} = [(V_{ol} - (V_{cco} - 2V))/R_L] * (V_{cco} - V_{ol_max}) \\ & P_{d_1} = [(2V - 1.4V)/50\Omega] * 1.4V \\ & P_{d_1} = 16.8mW \\ & P_{d_output} = 35mW \\ & P_{d_outputs} = 16 * 35mW \\ & P_{d_outputs} = 560mW \end{split}$$

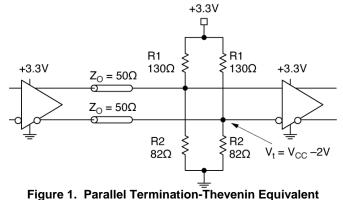
 $P_d = 433 \text{mW} + 560 \text{mW}$ $P_d = 0.993 \text{W}$ $T_J = T_A + \Theta_{JA} * P_d$ $T_{J_worst_case} = 70^{\circ}\text{C} + 0.993 \text{W} * 48^{\circ}\text{C/W}$

 $T_{J_worst_case}$ = 118 °C in still air.

The worst case junction temperature is below 125 C.

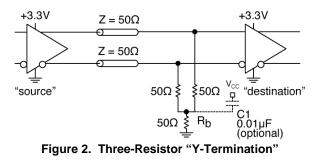
9

Output Interface Applications



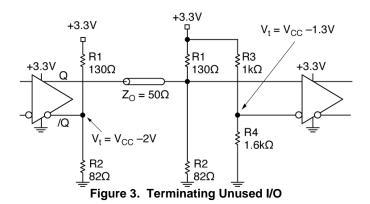
Notes:

1. For +2.5V systems: R1 = 250Ω, R2 = 82.5Ω.



Notes:

- 1. Power-saving alternatives to Thevenin termination.
- 2. Place termination resistors as close to destination inputs as possible.
- 3. For +2.5V systems, R_b = 19 Ω . R_b resistor sets the DC bias voltage, equal to V_t.



Notes:

- 1. Unused output (/Q) must be terminated to balance the output.
- 2. For 2.5V systems: R1 = 250 Ω , R2 = 62.5 Ω , R3 = 1.25k Ω , R4 = 1.2k Ω .

November 2011

Input Interface Applications

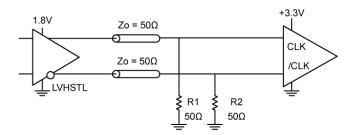


Figure 4. CLK and /CLK Input Driven By 1.8V LVHSTL

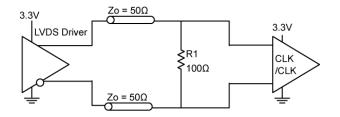


Figure 5. CLK and /CLK Input Driven By 3.3V LVDS Driver

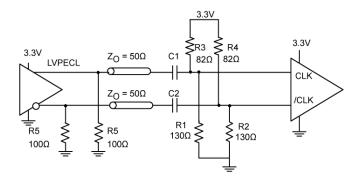
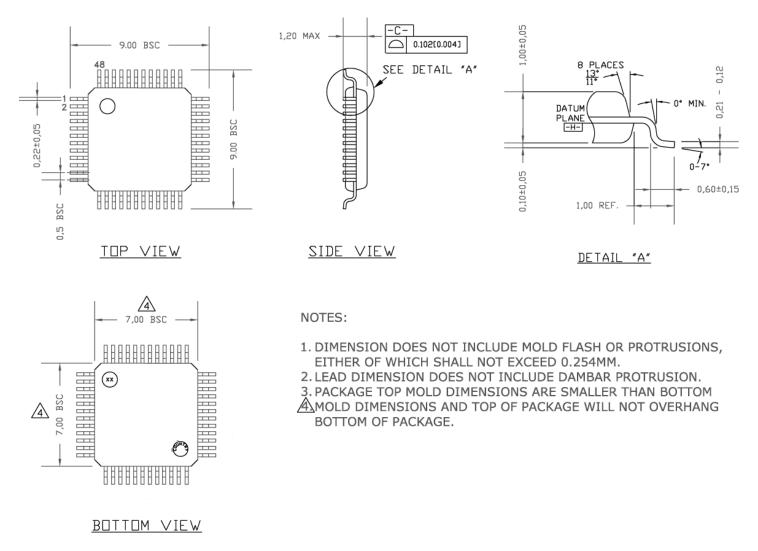


Figure 6. CLK and /CLK Input Driven By 3.3V LVPECL Driver with AC Couple

Notes:

1. For +2.5V systems: R5 = 50 Ω . R1 & R2 = 220 Ω , R3 & R4 = 68 Ω .

Package Information



48-Pin TQFP (TQFP-48)

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