Ordering Information[1]

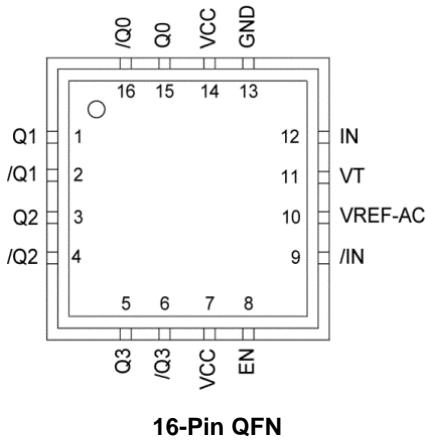| Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89832UMG	QFN-16	Industrial	832U with Pb-Free bar line indicator	NiPdAu Pb-Free
SY89832UMG TR[2]	QFN-16	Industrial	832U with Pb-Free bar line indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.

Truth Table

IN	/IN	EN	Q	/Q
0	1	1	0	1
1	0	1	1	0
X	X	0	0[3]	1[3]

Note:

3. On next negative transition of the input signal (IN).

Pin Configuration

16-Pin QFN

Pin Description

Pin Number	Pin Name	Pin Function
15, 16 1, 2 3, 4 5, 6	Q0, /Q0 Q1, /Q1 Q2, /Q2 Q3, /Q3	LVDS Differential (Outputs): Normally terminated with 100Ω across the pair (Q, /Q). See LVDS Outputs section for more details.Unused outputs should be terminated with a 100Ω resistor across each pair.
8	EN	The single-ended, TTL/CMOS-compatible input functions as a synchronous output enable. The synchronous enable ensures that enable/disable will only occur when the outputs are in a logic LOW state. Note that this input is internally connected to a 25kΩ pull-up resistor and will default to logic HIGH state (enabled) if left open.
9, 12	/IN, IN	Differential Inputs: These input pairs are the differential signal inputs to the device. Inputs accept AC- or DC-Coupled differential signs as small as 100mV. Each pin of a pair internally terminates to a VT pin through 50Ω. Note that these inputs will default to an intermediate state if left open. See Input Interface Applications section for more details.
10	VREF-AC	Reference Voltage: These outputs bias to VCC–1.4V. They are used when AC coupling the inputs (IN, /IN). For AC-Coupled applications, connect VREF-AC to VT pin and bypass with 0.01µF low ESR capacitor to VCC. See Input Interface Applications section for more details. Maximum sink/source current is ±1.5mA. Due to the limited drive capability, each VREF-AC pin is only intended to drive its respective VT pin.
11	VT	Input Termination Center-Tap: Each side of the differential input pair terminates to a VT pin. The VT pins provide a center-tap to a termination network for maximum interface flexibility. See Input Interface Applications section for more details.
13	GND	Ground. GND pins and exposed pad must be connected to the most negative potential of the device ground.
7, 14	VCC	Positive Power Supply: Bypass with 0.1µF//0.01µF low ESR capacitors and place as close to each VCC pin as possible.

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Absolute Maximum Ratings[4]

Supply Voltage (V_{CC})..................................... −0.5V to +4.0V
Input Voltage (V_{IN}). ....−0.5V to V_{CC} +0.3V
LVDS Output Current (I_{OUT}).......................................±10mA
Input Current
    Source or Sink Current on (IN, /IN) ....±50mA
VREF-AC Current
    Source or Sink Current on (I_{VT})............................±2mA
Lead Temperature (soldering, 20s)........................... 260°C
Storage Temperature (T_S).........................−65°C to +150°C

Operating Ratings[5]

Supply Voltage Range (V_{IN}) .... +2.375V to +2.675V
Ambient Temperature (T_A) ....−40°C to +85°C
Package Thermal Resistance[6]
    QFN
    (θ_{JA}) Still-Air ....60°C/W
    (Ψ_{JB})..32°C/W

DC Electrical Characteristics[7]

T_A = -40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power Supply		2.375	2.5	2.625	V
I_{CC}	Power Supply Current	No load, maximum V_{CC}.		75	100	mA
R_{IN}	Input Resistance (IN-to-VT)		45	50	55	Ω
R_{DIFF_IN}	Differential Input Resistance (IN-to-/IN)		90	100	110	Ω
V_{IH}	Input HIGH Voltage (IN, /IN)		0.1		V_{CC}+0.3	V
V_{IL}	Input LOW Voltage (IN, /IN)		−0.3		V_{IH}-0.1	V
V_{IN}	Input Voltage Swing (IN, /IN)	See Figure 4.	0.1		V_{CC}	V
V_{DIFF_IN}	Differential Input Voltage Swing |IN − /IN|	See Figure 5.	0.2			V
$\|I_{IN}\|$	Input Current (IN, /IN)	Note 8			45	mA
$V_{REF\text{-}AC}$	Output Reference Voltage		$V_{CC} - 1.525$	$V_{CC} - 1.425$	$V_{CC} - 1.325$	V

Notes:

4. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

6. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. ψ_{JB} and θ_{JA} values are determined for a 4-layer board in still-air number, unless otherwise stated.

7. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

8. Due to the internal termination the input current depends on the applied voltages at IN, /IN and VT inputs. Do not apply a combination of voltages that causes the input current to exceed the maximum limit!

LVDS Outputs DC Electrical Characteristics[7]

V_{CC} = 2.5V ±5%, R_L = 100Ω across the outputs; T_A = −40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{OUT}	Output Voltage Swing	See Figure 4.	250	325		mV
V_{DIFF_OUT}	Differential Output Voltage Swing	See Figure 5.	500	650		mV
V_{OCM}	Output Common Mode Voltage		1.125		1.275	V
ΔV_{OCM}	Change in Common Mode Voltage		−50		50	mV

LVTTL/CMOS DC Electrical Characteristics[7]

V_{CC} = 2.5V ±5%, T_A = −40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input HIGH Voltage		2.0		V_{CC}	V
V_{IL}	Input LOW Voltage		0		0.8	V
I_{IH}	Input HIGH Current		−125		30	µA
I_{IL}	Input LOW Current		−300			µA

AC Electrical Characteristics[9]

V_{CC} = 2.5V ±5% or 3.3V ±10%, R_L = 100Ω across the outputs; T_A = −40°C to +85°C unless otherwise stated.

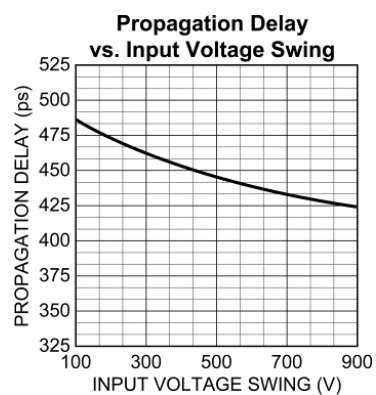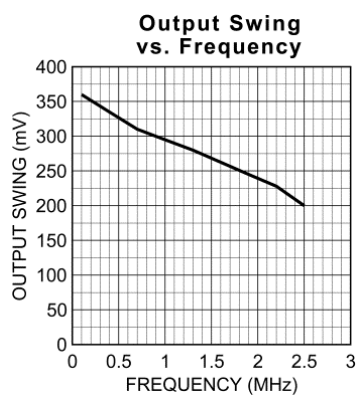| Symbol	Parameter		Condition	Min.	Typ.	Max.	Units
f_{MAX}	Maximum Frequency		V_{OUT} ≥ 200mV	2.0	2.5		GHz
t_{pd}	Propagation Delay IN-to-Q		V_{IN} < 400mV	370	470	570	ps
			V_{IN} ≥ 400mV	300	410	500	ps
t_{SKEW}	Within-Device Skew		Note 10		5	20	ps
	Part-to-Part Skew		Note 11			200	ps
t_S	Set-Up Time	EN to IN, /IN	Note 12	300			ps
t_H	Hold Time	EN to IN, /IN	Note 12	500			ps
t_{JITTER}	Additive Phase Jitter		Carrier = 622MHz Integration Range: 12kHz – 20MHz		81		fs
			Carrier = 250MHz Integration Range: 12kHz – 20MHz		195		fs
t_r, t_f	Output Rise/Fall Times (20% to 80%)		At full output swing.	70	150	200	ps

Notes:

9. High-frequency AC parameters are guaranteed by design and characterization.

10. Within device skew is measured between two different outputs under identical input transitions.

11. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and no skew at the edges at the respective inputs.

12. Set-up and hold times apply to synchronous applications that intend to enable/disable before the next clock cycle. For asynchronous applications, set-up and hold times do not apply.
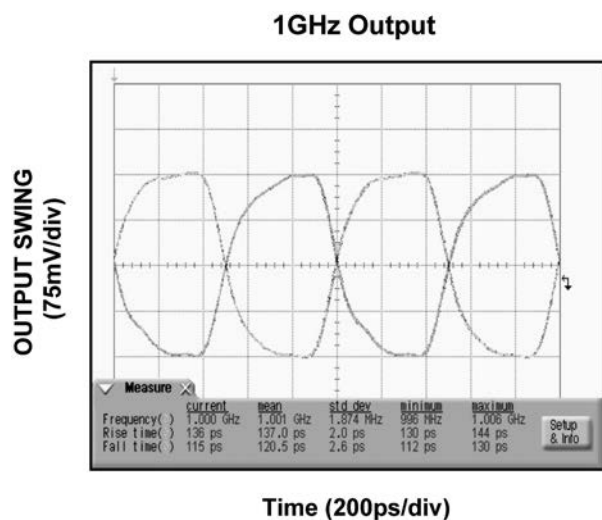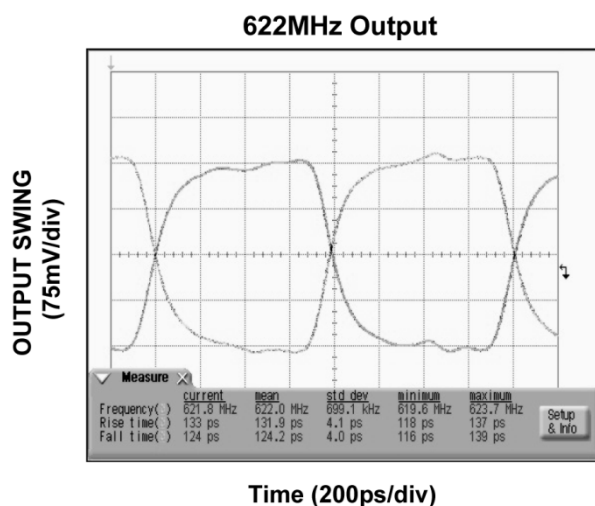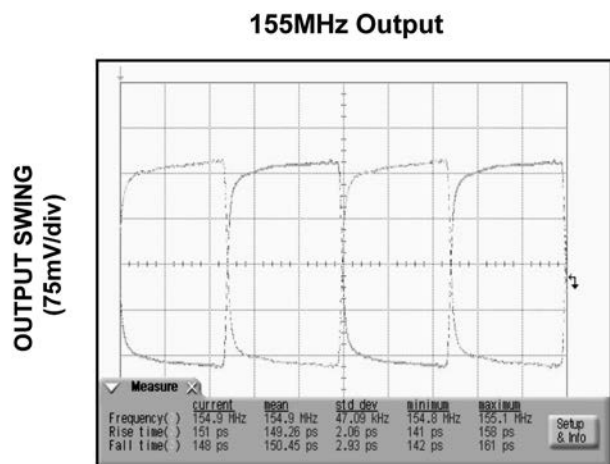
Timing Diagram
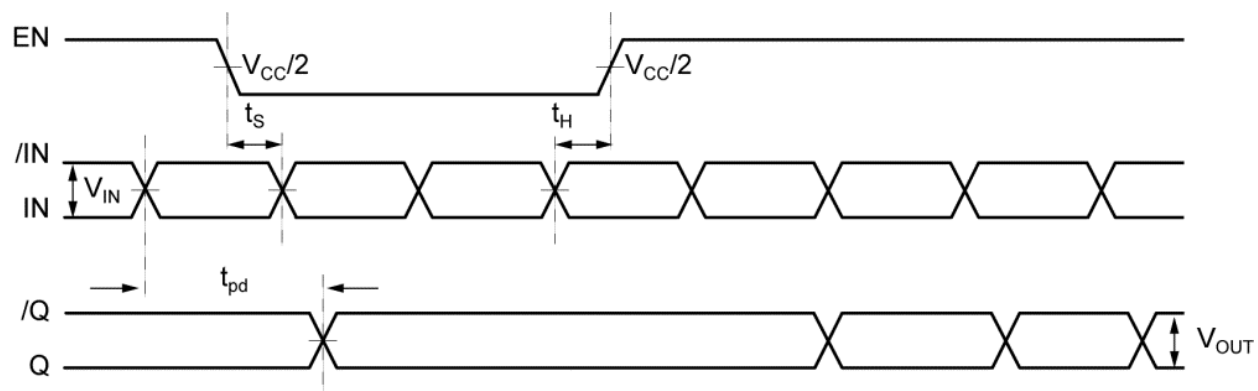
Typical Operating Characteristics

V_{CC} = 2.5V, GND = 0V, V_{IN} = 400mV, R_L = 100Ω across the outputs; T_A = 25°C, unless otherwise stated.

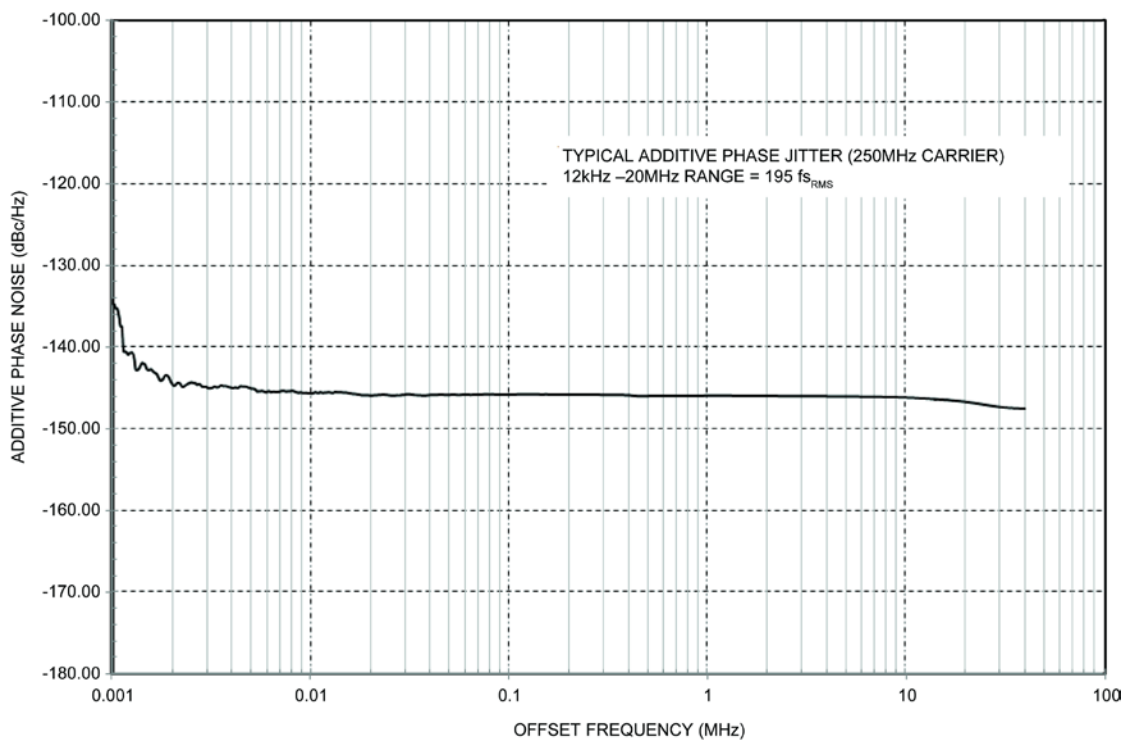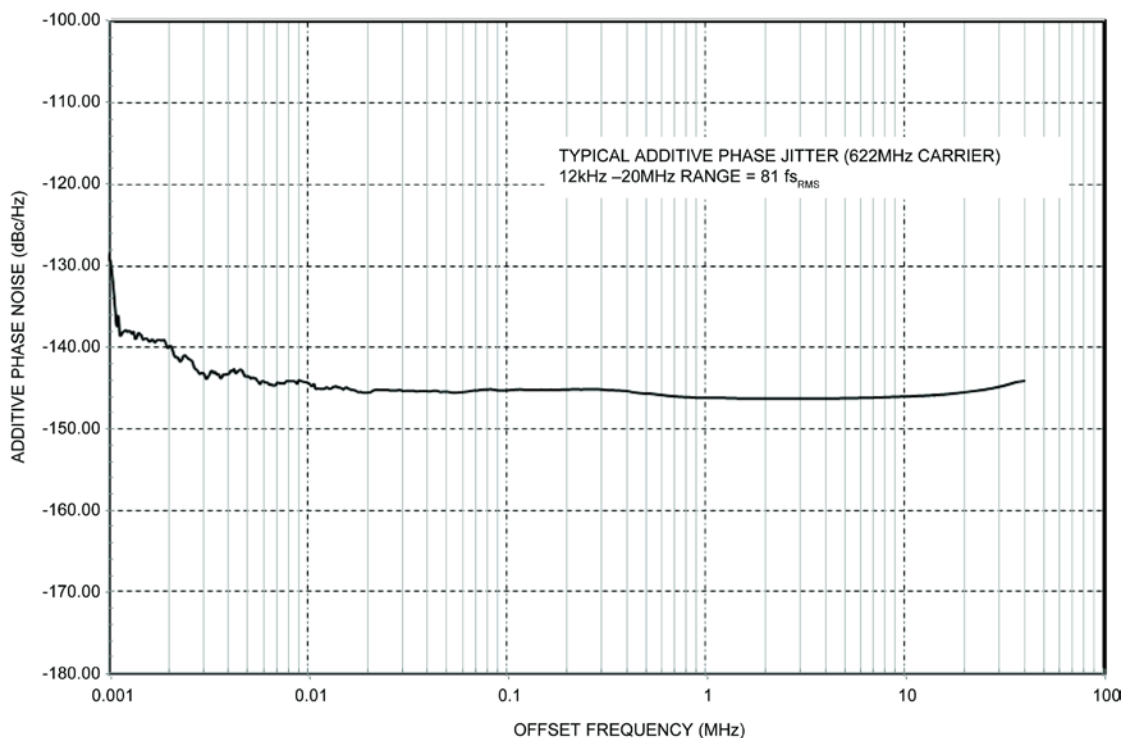**Output Swing vs. Frequency**

Propagation Delay vs. Input Voltage Swing

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Functional Characteristics

V_{CC} = 2.5V, GND = 0V, V_{IN} = 400mV, R_L = 100Ω across the outputs; T_A = 25°C, unless otherwise stated.

155MHz Output

Time (1.3ns/div)

622MHz Output

Time (200ps/div)

1GHz Output

Time (200ps/div)

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Additive Phase Noise Plots

V_{CC} = +3.3V, GND = 0, T_A = 25°C

TYPICAL ADDITIVE PHASE JITTER (622MHz CARRIER)
12kHz –20MHz RANGE = 81 fs_{RMS}

TYPICAL ADDITIVE PHASE JITTER (250MHz CARRIER)
12kHz –20MHz RANGE = 195 fs_{RMS}

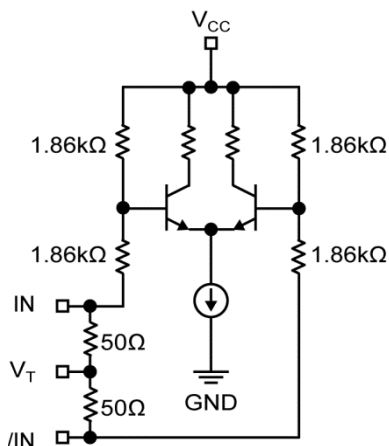tcghelp@micrel.com or (408) 955-1690

Input Stage

Figure 1. Simplified Differential Input Buffer

LVDS Outputs

LVDS specifies a small swing of 325mV typical, on a nominal 1.2V common-mode above ground.

The common-mode voltage has tight limits to permit large variations in ground noise between an LVDS driver and receiver.
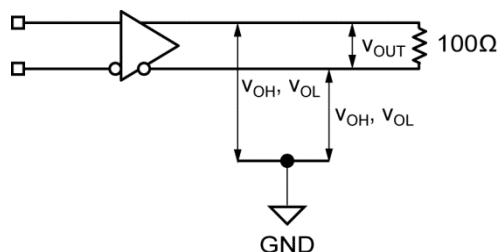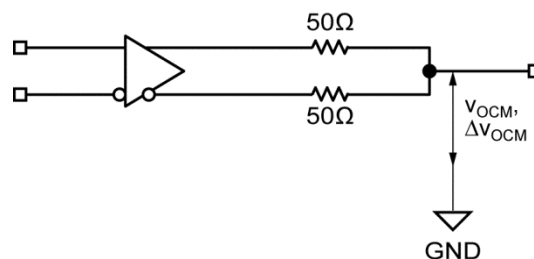

Figure 2. LVDS Differential Measurement

Figure 3. LVDS Common Mode Measurement
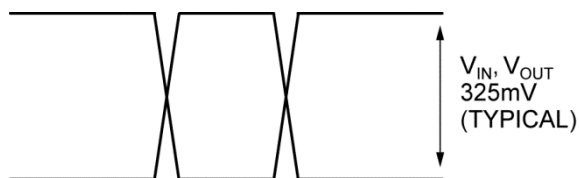
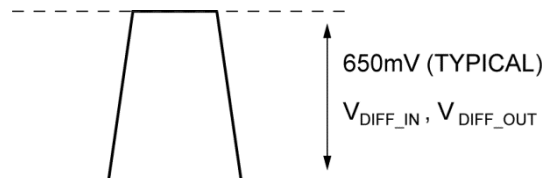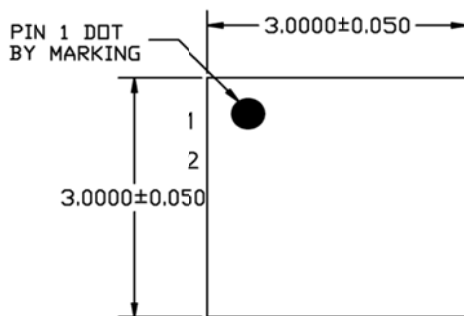## Single-Ended and Differential Swings
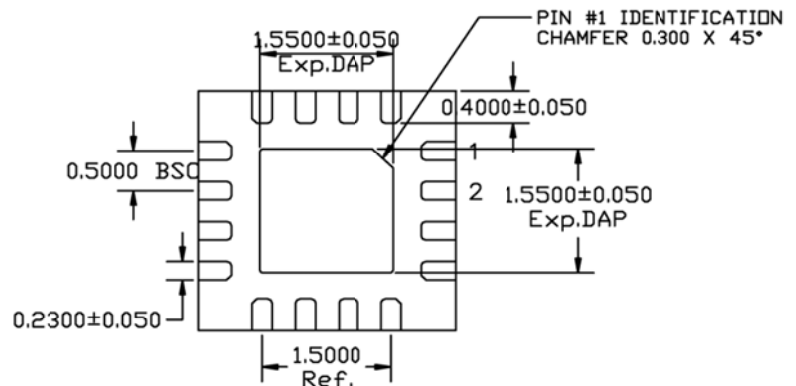

Figure 4. Single-Ended Swing

Figure 5. Differential Swing

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Input Interface Applications

**Figure 6. DC-Coupled CML
Input Interface**

**Figure 7. AC-Coupled CML
Input Interface**

**Figure 8. DC-Coupled LVPECL
Input Interface**
(*Bypass with 0.01µF to GND)

**Figure 9. AC-Coupled LVPECL
Input Interface**

Figure 10. LVDS Input Interface

**Figure 11. AC-Coupled LVDS
Input Interface**

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Package Information and Recommended Land Pattern[13]

PIN 1 DOT BY MARKING

3.0000±0.050

3.0000±0.050

1
2

TOP VIEW
NOTE: 1, 2, 3

1.5500±0.050
Exp.DAP

PIN #1 IDENTIFICATION
CHAMFER 0.300 X 45°

0.4000±0.050

0.5000 BSC

0.2300±0.050

1
2 1.5500±0.050
Exp.DAP

1.5000
Ref.

BOTTOM VIEW
NOTE: 1, 2, 3

0.850±0.050

0.000-0.050

0.2030±0.025

SIDE VIEW
NOTE: 1, 2, 3

0.48±0.05

0.23±0.05

0.50 BSC

1.60±0.05

1.60±0.05

2.72±0.05

2.72±0.05
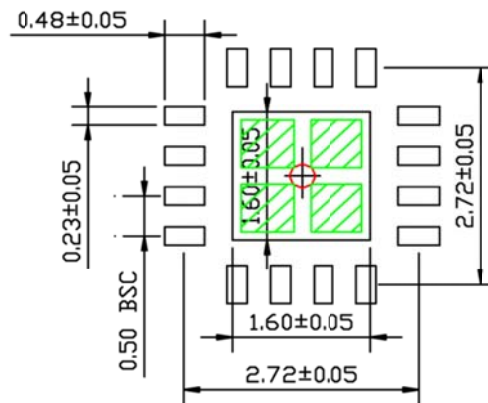
RECOMMENDED LAND PATTERN
NOTE: 4, 5

NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA.
SIZE SHOULD BE 0.30-0.3M IN DIAMETER AND SHOULD BE
CONNECTED TO GND FOR MAX THERMAL PERFORMANCE
5. GREEN RECTANGLES (SHADED AREA) indicate SOLDER
STENCIL OPENING ON EXPOSED PAD AREA.   SIZE SHOULD BE
0.60x0.60 MM IN SIZE, 0.20 MM SPACING.

16-Pin 3mm × 3mm QFN (MM)

Note:
13. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

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