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# 1 Electrical characteristics

**Table 1. Absolute maximum ratings (limiting value)**

| Symbol | Parameter | Rating | Unit |
|---|---|---|---|
| $AV_{DD}$ | Analog supply voltage | -0.3 to +5.5 | V |
| VIO | Digital supply voltage | -0.3 to +3.3 | V |
| $V_{I/O}$ | Input voltage logic lines (DATA, CLK, CS) | -0.5 to VIO + 0.5 | V |
| $V_{ESD\ (HBM)}$ | Human body model, JESD22-A114-B, All I/O | 2 | kV |
| $V_{ESD\ (CDM)}$ | Charge device model, JESD22-C101-C, All I/O | 500 | V |
| $T_{stg}$ | Storage temperature range | -55 to +150 | °C |
| $T_j$ | Maximum junction temperature | 150 | °C |

**Table 2. Recommended operating conditions**

| Symbol | Parameter | Rating | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| $T_{AMB\_oP}$ | Operating ambient temperature | -30 | - | +85 | °C |
| $AV_{DD}$ | Analog supply voltage | 2.3 | - | 5 | V |
| $V_{I/O}$ | Digital supply voltage | 1.65 | - | 1.95 | V |
| $V_{IH}$ | Input voltage logic level HIGH (DATA, CLK, CS) | $0.7*V_{I/O}$ | - | $V_{I/O}$ + 0.3 | V |
| $V_{IL}$ | Input voltage logic level LOW (DATA, CLK, CS) | -0.3 | - | $0.35*V_{I/O}$ | V |

**Table 3. High voltage DAC output characteristics**

| Conditions: $AV_{DD}$ from 2.5 to 5 V, VIO from 1.65 to 1.95 V, $T_{amb}$ from -30 °C to +85 °C, OUTA-C, unless otherwise specified | | | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min.** | **Typ.** | **Max.** | **Unit** |
| Shutdown mode | | | | | | |
| $R_{PD}$ | OUTA-OUTC set in pull down mode | | | | 500 | Ω |
| Active mode | | | | | | |
| $V_{OH}$ | OUTA-OUTC maximum output voltage | DAC = 7Fh, $I_{LOAD}$ < 1 µA | 24 | | | V |
| $V_{OL}$ | OUTA-OUTC minimum output voltage | DAC = 01h, $I_{LOAD}$ < 1 µA | | | 1 | V |
| Resolution | Voltage resolution / OUTA, OUTC | 7 bits DAC 01h to 3Ch range (< 6V) | | 100 | | mV |
| | | 7 bits DAC, 3Dh to 48h range ( 6 V-8,4 V) | | 200 | | mV |
| | | 7 bits DAC, 49h to 7Fh range ( (>8,4 V) | | 300 | | mV |
| ERROR | | $V_{OUT}$ 2 to 25 V | -3.5 | | +3.5 | $\%V_{OUT}$ |
| $I_{SC}$ | Over current protection | Any DAC output | | | 50 | mA |

**Table 4. DC characteristics**

| Conditions: $AV_{DD}$ 3.3 V, $V_{IO}$ from 1.65 to 1.95 V, $T_{amb}$ from -30 °C to +85 °C, $L_{BOOST}$ = 15 µH unless otherwise specified | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | | **Conditions** | **Min.** | **Typ.** | **Max.** | **Unit** |
| $I_{LBOOST}$ | Boost inductor supply current:<br>L = 15 µA<br>$AV_{DD}$ = 3.3 V | Low power mode or shutdown | | | 0.3 | | µA |
| | | $I_{LBOOST\_SS2}$ | Active mode, 1 output steady state 2 V | | 130 | | |
| | | | Active mode, 3outputs steady state 2 V | | 300 | 570 | |
| | | $I_{LBOOST\_SS20}$ | Active mode, 1 output steady state 20 V | | 150 | | |
| | | | Active mode, 3outputs steady state 20 V | | 370 | 750 | |
| $I_{AVDD}$ | $AV_{DD}$ supply current<br>$AV_{DD}$ = 3.3 V | Low power mode or shutdown | | | 1.35 | 4 | µA |
| | | $I_{AVDD\_SS2}$ | Active mode, 1 output steady state 2 V | | 590 | 670 | |
| | | | Active mode, 3outputs steady state 2 V | | 700 | 780 | |
| | | $I_{AVDD\_SS2}$ | Active mode, 1 output steady state 20 V | | 590 | 670 | |
| | | | Active mode, 3outputs steady state 20 V | | 700 | 780 | |
| $I_{vio}$ | $V_{dig}$ supply current | Low power mode | | | 1.8 | 4 | µA |
| | | Active mode: (3 outputs active)<br>No activity on CLK, $V_{IO}$ = 1.8 V<br>FCLK = 13 MHz<br>FCLK = 26 MHz | | | 27 | 40<br>315<br>585 | |
| $I_{IH}$ | Input current logic level high | DATA, CLK, SELSID pins | | -1 | | 1 | µA |
| $I_{IL}$ | Input current logic level LOW | DATA, CLK , SELSID pins | | -1 | | 1 | µA |
| $V_{IORST}$ | $V_{IO}$ low threshold | | | | | 0.2 | V |

# 2 Functional block diagram

**Figure 2. HVDAC functional block diagram**

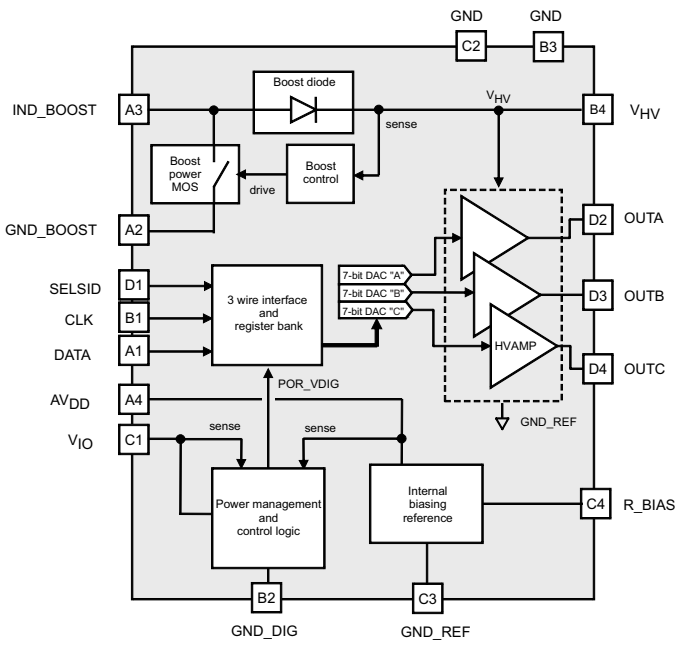



**Table 5. Signal descriptions**

| Pin number | Pin name | Description |
|---|---|---|
| A1 | DATA | RFFE interface / serial DATA |
| A2 | GND_BOOST | Power ground for BOOST |
| A3 | IND_BOOST | Boost inductance |
| A4 | $AV_{DD}$ | Analog supply |
| B1 | CLK | RFFE interface / serial clock |
| B2 | GND_DIG | Ground reference |
| B3 | GND | Tie to GND plane on PCB |
| B4 | $V_{HV}$ | Boost high voltage output |
| C1 | $V_{IO}$ | RFFE interface / Serial I/O supply |
| C2 | GND | Tie to GND plane on PCB |
| C3 | GND_REF | Ground reference |
| C4 | $R_{bias}$ | Biasing reference resistance |
| D1 | SELSID | RFFE interface / SELSID |
| D2 | OUTA | High voltage output A |
| D3 | OUTB | High voltage output B |
| D4 | OUTC | High voltage output C |

# 3 Theory of operation

## 3.1 HVDAC output voltages

The HVDAC outputs are directly controlled by programming the 7-bit DAC (DAC A, DAC B and DAC C) through the RFFE serial interface.

The DAC stages are driven from a reference voltage, generating an analog output voltage driving a high voltage amplifier supplied from the boost converter (see HVDAC block diagram - *Figure 2*).

The HVDAC output voltages are scaled from 0 to 25 V, with 128 steps. The device resolution is automatically adjusted depending on the voltage output range so that it will match the CV curve of tunable BST capacitors.

From 0 to 6 V the resolution is 100 mV, from 6 V to 8.4 V the resolution is 200 mV, from 8.4 V to 25 V the resolution is 300 mV.

If DAC value is set to 00 h, then the corresponding output is directly connected to GND through a pull-down resistor (500 Ω). See *Table 6* for DAC settings correspondence table.

**Table 6. DAC settings correspondence table**

| DEC | HEX | BIN | Volts | DEC | HEX | BIN | Volts | DEC | HEX | BIN | Volts |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 00000000 | 0 | 19 | 13 | 00010011 | 1.9 | 38 | 26 | 00100110 | 3.8 |
| 1 | 1 | 00000001 | 0.56 | 20 | 14 | 00010100 | 2 | 39 | 27 | 00100111 | 3.9 |
| 2 | 2 | 00000010 | 0.56 | 21 | 15 | 00010101 | 2.1 | 40 | 28 | 00101000 | 4 |
| 3 | 3 | 00000011 | 0.56 | 22 | 16 | 00010110 | 2.2 | 41 | 29 | 00101001 | 4.1 |
| 4 | 4 | 00000100 | 0.57 | 23 | 17 | 00010111 | 2.3 | 42 | 2A | 00101010 | 4.2 |
| 5 | 5 | 00000101 | 0.58 | 24 | 18 | 00011000 | 2.4 | 43 | 2B | 00101011 | 4.3 |
| 6 | 6 | 00000110 | 0.62 | 25 | 19 | 00011001 | 2.5 | 44 | 2C | 00101100 | 4.4 |
| 7 | 7 | 00000111 | 0.7 | 26 | 1A | 00011010 | 2.6 | 45 | 2D | 00101101 | 4.5 |
| 8 | 8 | 00001000 | 0.8 | 27 | 1B | 00011011 | 2.7 | 46 | 2E | 00101110 | 4.6 |
| 9 | 9 | 00001001 | 0.9 | 28 | 1C | 00011100 | 2.8 | 47 | 2F | 00101111 | 4.7 |
| 10 | A | 00001010 | 1 | 29 | 1D | 00011101 | 2.9 | 48 | 30 | 00110000 | 4.8 |
| 11 | B | 00001011 | 1.1 | 30 | 1E | 00011110 | 3 | 49 | 31 | 00110001 | 4.9 |
| 12 | C | 00001100 | 1.2 | 31 | 1F | 00011111 | 3.1 | 50 | 32 | 00110010 | 5 |
| 13 | D | 00001101 | 1.3 | 32 | 20 | 00100000 | 3.2 | 51 | 33 | 00110011 | 5.1 |
| 14 | E | 00001110 | 1.4 | 33 | 21 | 00100001 | 3.3 | 52 | 34 | 00110100 | 5.2 |
| 15 | F | 00001111 | 1.5 | 34 | 22 | 00100010 | 3.4 | 53 | 35 | 00110101 | 5.3 |
| 16 | 10 | 00010000 | 1.6 | 35 | 23 | 00100011 | 3.5 | 54 | 36 | 00110110 | 5.4 |
| 17 | 11 | 00010001 | 1.7 | 36 | 24 | 00100100 | 3.6 | 55 | 37 | 00110111 | 5.5 |
| 18 | 12 | 00010010 | 1.8 | 37 | 25 | 00100101 | 3.7 | 56 | 38 | 00111000 | 5.6 |
| 57 | 39 | 00111001 | 5.7 | 81 | 51 | 01010001 | 11.1 | 105 | 69 | 01101001 | 18.3 |

**Table 6. DAC settings correspondence table**

| DEC | HEX | BIN | Volts | DEC | HEX | BIN | Volts | DEC | HEX | BIN | Volts |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 58 | 3A | 00111010 | 5.8 | 82 | 52 | 01010010 | 11.4 | 106 | 6A | 01101010 | 18.6 |
| 59 | 3B | 00111011 | 5.9 | 83 | 53 | 01010011 | 11.7 | 107 | 6B | 01101011 | 18.9 |
| 60 | 3C | 00111100 | 6 | 84 | 54 | 01010100 | 12 | 108 | 6C | 01101100 | 19.2 |
| 61 | 3D | 00111101 | 6.2 | 85 | 55 | 01010101 | 12.3 | 109 | 6D | 01101101 | 19.5 |
| 62 | 3E | 00111110 | 6.4 | 86 | 56 | 01010110 | 12.6 | 110 | 6E | 01101110 | 19,8 |
| 63 | 3F | 00111111 | 6.6 | 87 | 57 | 01010111 | 12.9 | 111 | 6F | 01101111 | 20.1 |
| 64 | 40 | 01000000 | 6.8 | 88 | 58 | 01011000 | 13.2 | 112 | 70 | 01110000 | 20.4 |
| 65 | 41 | 01000001 | 7 | 89 | 59 | 01011001 | 13.5 | 113 | 71 | 01110001 | 20.7 |
| 66 | 42 | 01000010 | 7.2 | 90 | 5A | 01011010 | 13.8 | 114 | 72 | 01110010 | 21 |
| 67 | 43 | 01000011 | 7.4 | 91 | 5B | 01011011 | 14.1 | 115 | 73 | 01110011 | 21.3 |
| 68 | 44 | 01000100 | 7.6 | 92 | 5C | 01011100 | 14.4 | 116 | 74 | 01110100 | 21.6 |
| 69 | 45 | 01000101 | 7.8 | 93 | 5D | 01011101 | 14.7 | 117 | 75 | 01110101 | 21.9 |
| 70 | 46 | 01000110 | 8 | 94 | 5E | 01011110 | 15 | 118 | 76 | 01110110 | 22.2 |
| 71 | 47 | 01000111 | 8.2 | 95 | 5F | 01011111 | 15.3 | 119 | 77 | 01110111 | 22.5 |
| 72 | 48 | 01001000 | 8.4 | 96 | 60 | 01100000 | 15.6 | 120 | 78 | 01111000 | 22.8 |
| 73 | 49 | 01001001 | 8.7 | 97 | 61 | 01100001 | 15.9 | 121 | 79 | 01111001 | 23.1 |
| 74 | 4A | 01001010 | 9 | 98 | 62 | 01100010 | 16.2 | 122 | 7A | 01111010 | 23.4 |
| 75 | 4B | 01001011 | 9.3 | 99 | 63 | 01100011 | 16.5 | 123 | 7B | 01111011 | 23.7 |
| 76 | 4C | 01001100 | 9.6 | 100 | 64 | 01100100 | 16.8 | 124 | 7C | 01111100 | 24 |
| 77 | 4D | 01001101 | 9.9 | 101 | 65 | 01100101 | 17.1 | 125 | 7D | 01111101 | 24.3 |
| 78 | 4E | 01001110 | 10.2 | 102 | 66 | 01100110 | 17.4 | 126 | 7E | 01111110 | 24.6 |
| 79 | 4F | 01001111 | 10.5 | 103 | 67 | 01100111 | 17.7 | 127 | 7F | 01111111 | 24.9 |
| 80 | 50 | 01010000 | 10.8 | 104 | 68 | 01101000 | 18 | | | | |

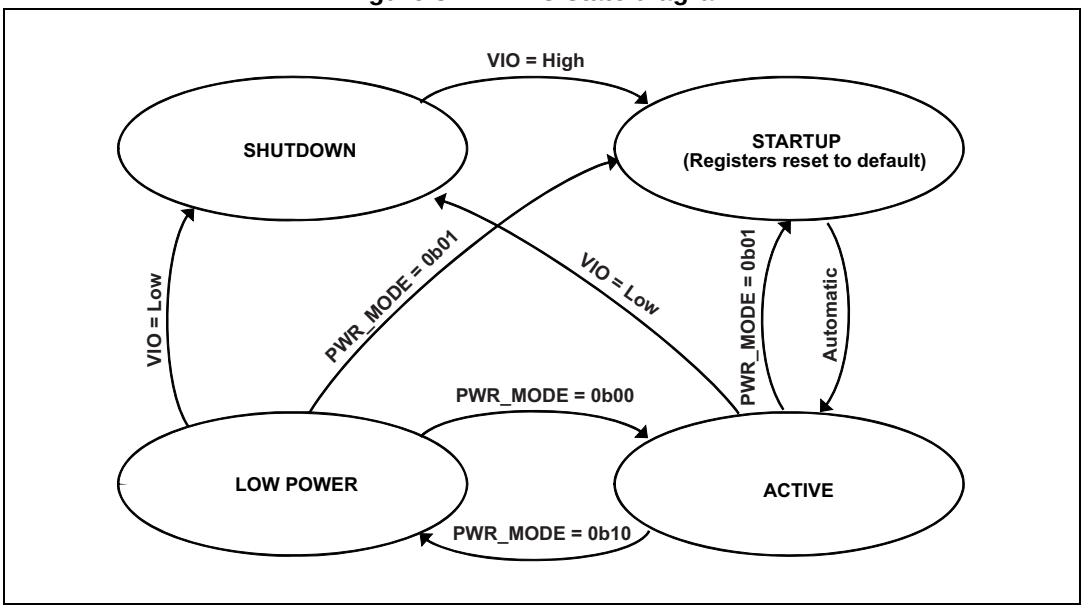
– From 0 to 6 V the resolution is 100 mV.
– From 6.20 to 8.40 V the resolution is 200 mV.
– From 8.70 to 24.90 V the resolution is 300 mV.

## 3.2 Operating modes

The following operating modes are accessible through the serial interface:

- **Shutdown mode:** The HVDAC is switched off, and all the blocks in the control ASIC are switched off. Power consumption is almost zero in this mode, the DAC outputs are pulled down. The shutdown mode is set by driving VIO to low level.
- **Active mode:** The HVDAC is switched on and the DAC outputs are fully controlled through the RFFE serial interface. The DAC settings can be dynamically modified and the HV outputs will be adjusted according to the specified timing diagrams. Each DAC can be individually controlled and/or switched off according to application requirements. Boost is active in this mode.The device is directly set into this mode after startup (VIO supply switched on, or power mode bits set to 01b).
- **Low power mode:** The HVDAC is switched OFF except the RFFE interface. This mode is set by driving PWR_MODE bits to 10b.

**Figure 3. HVDAC state diagram**




## 3.3 Device reset

Power-On Reset is implemented on the VIO supply input, ensuring the HVDAC will be reset to default mode once VIO supply line rises above a given threshold $V_{IORST}$. This trigger will force all registers to their default value.

Soft Reset is also implemented as defined in the MIPI RFFE specification. Setting PWR_MODE bits to 01b will force the device to reset all registers to their default value, and switch into active mode.

## 3.4 RFFE serial interface

The HVDAC is fully controlled through RFFE serial interface (DATA, VIO, CLK).

This interface is further described in the next sections of this document and is made compliant to the MIPI alliance Specification for RF Front End control Interface version 1.10 (26 July 2011)

Sequence Start Condition (SSC): One rising edge followed by falling edge on DATA while CLK remains at logic level low. This is used by the Master to identify the start of a Command frame.

Parity (P): Each frame shall end with a single parity bit. The parity bit shall be driven such that the total number of bits in the frame that are driven to logic level one, including the parity bit, is odd.

Bus Park Cycle (BP): The slave releasing DATA will drive the DATA to logic level zero during the first half of the CLK clock cycle. This is used by the Master as the indication of the end of Frame.

## 3.5 RFFE register and write command sequence

Register #0 is a specific register that can be programmed without sending the register address. Output C is associated to Register #0 so that when there is only one tunable capacitor to control a simple register#0 write command is sufficient. Please refer to *Figure 12* for Register #0 Write sequence. The Sequence Starts with an Start Sequence command (SSC) followed by the Register #0 Write Command frame containing the slave address, a logic one and a seven bit word to be written to Register #0.

## 3.6 RFFE serial interface extended mode

All the registers in the device can be addressed in extended mode, by sending appropriate command sequences as per MIPI RFFE specification (see *Figure 11*).

## 3.7 RFFE serial interface broadcast capability

Registers 27 to 31 can be addressed in broadcast mode, by sending appropriate command sequences as per MIPI RFFE specification.

## 3.8 Power-up / down sequence

*Table 7* and *Figure 4* describe the HVDAC settling time requirements and recommended timing diagrams.

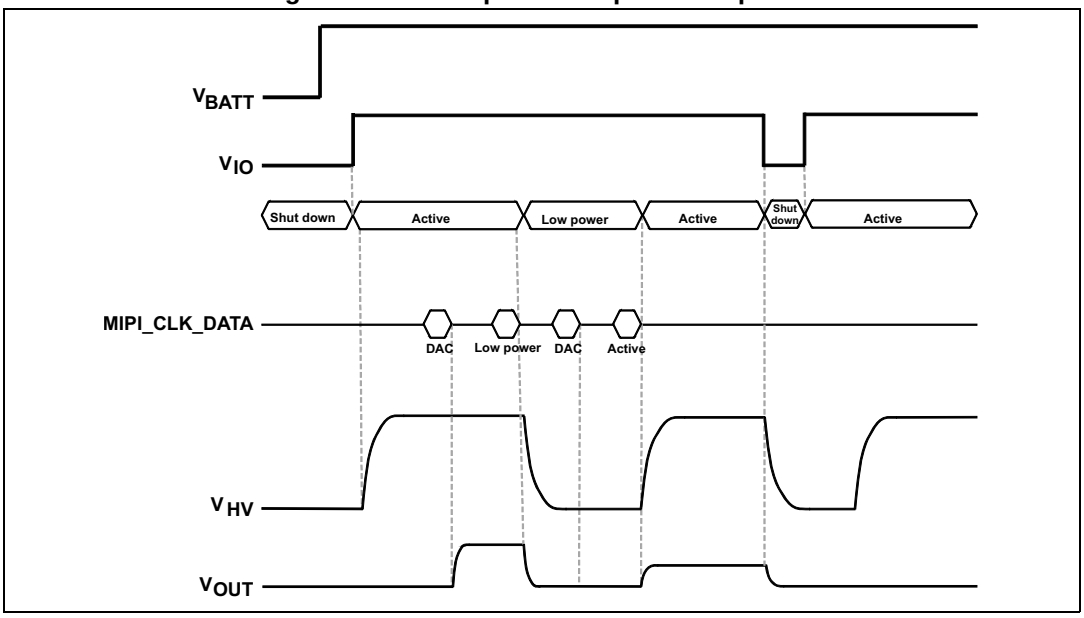
Switching from shutdown to active mode is triggered by setting VIO to high level.

Switching from active to low power mode will occur by setting PWR_MODE bits to 10b in register 28.

Switching from low power to active mode will occur by setting power mode bits to 01b in register 28

Following active mode command (from Shutdown or from Low power), the HVDAC will be operational after $T_{active}$ (typ. 100 µs). Once in Active mode, a settling time of 10 µs typical ($T_{set}$) is required following each DAC command in active mode. During this settling time the HVDAC output voltages will vary from the initial to the updated DAC command.

**Figure 4. Power up and low power sequence**




## 3.9 Power supply sequencing

It is assumed that the $AV_{DD}$ input will be directly supplied from the battery and will then be the first ON.

VIO should then be switched as described in previous sections.

## 3.10 Trigger Mode

To meet precise timing requirements and avoid RFFE interface traffic congestion at critical timing, trigger mode has been implemented in the RFFE interface.

Two triggers (TRIG0 and TRIG1) are available and can be controlled through the RFFE interface.

Registers 0 and 1 (DAC C and DAC B) are associated to TRIG0, and register 2 (DAC A) is associated to TRIG1. Each trigger can be activated independently.

### 3.10.1 Trigger mode enabled:

The different triggers are enabled unsetting corresponding trigger mask bits in register 28.

In this case, once in ACTIVE mode, the following sequence must be followed to control the HVDAC outputs:

Send any valid register 0/1/2 write command sequence. The new register values will be temporarily stored in shadow registers.

Send a register28 write command sequence, setting trigger bits and keeping Trigger mask bits low. The shadow registers will be loaded to destination registers and this will trigger the corresponding DAC outputs to their new values (see *Figure 5*).

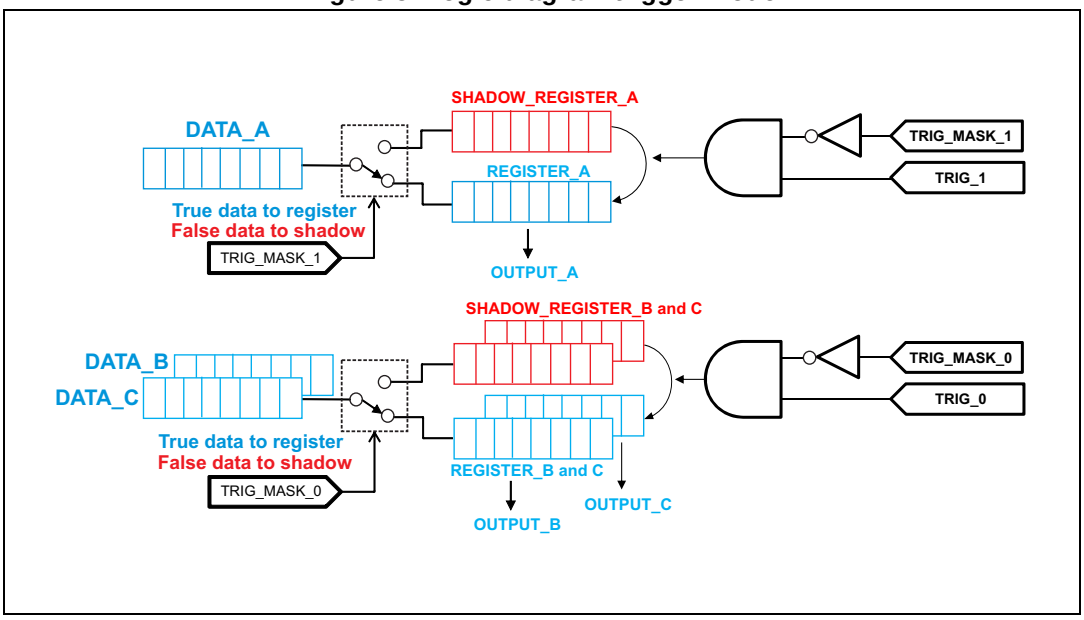
### 3.10.2 Trigger mode disabled (default mode):

The different triggers are disabled setting corresponding trigger mask bits in register 28.

In this case, any valid register write command sequence is directly loaded to the destination register, directly triggering the corresponding DAC output to its new value.

The following logic diagram illustrates the trigger mode function. By default the trigger mode is disable and the data are directly sent to the register in order to change the outputs without Trigger.

**Figure 5. Logic diagram trigger mode**



## 3.11 Settling time

The ST HVDAC will set the bias voltage of the tuner within 10µs typical after

- Bus Park (BP) of register28 write sequence data frame if trigger mode is enabled
- Bus Park (BP) of register 0/1/2/3 write sequence data frame if trigger mode is disabled

**Table 7. Timing**

| Conditions: $AV_{DD}$ from 2.3 to 5 V, VIO from 1.65 to 1.95 V, $T_{amb}$ from -30 °C to +85 °C, OUTA-OUTC unless otherwise specified | | | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Condition** | **min** | **typ (1)** | **max** | **unit** |
| $T_{active}$ | activation time | Activation time from shutdown to active mode | | 100 | 300 | µs |
| $T_{set+}$ | Output positive settling time at 95% | Vout = 2 V to 20 V<br>equivalent load of 15 Kohms and 1 nF | | 10 | 35 | µs |
| $T_{set-}$ | Output negative settling time at 95% | Vout = 20 V to 2 V<br>equivalent load of 15 Kohms and 1 nF | | 10 | 35 | µs |

1. Typical value are provided for IND = 15 µH

## 3.12 Operation with 1 to 3 tunable capacitors

With triggers:

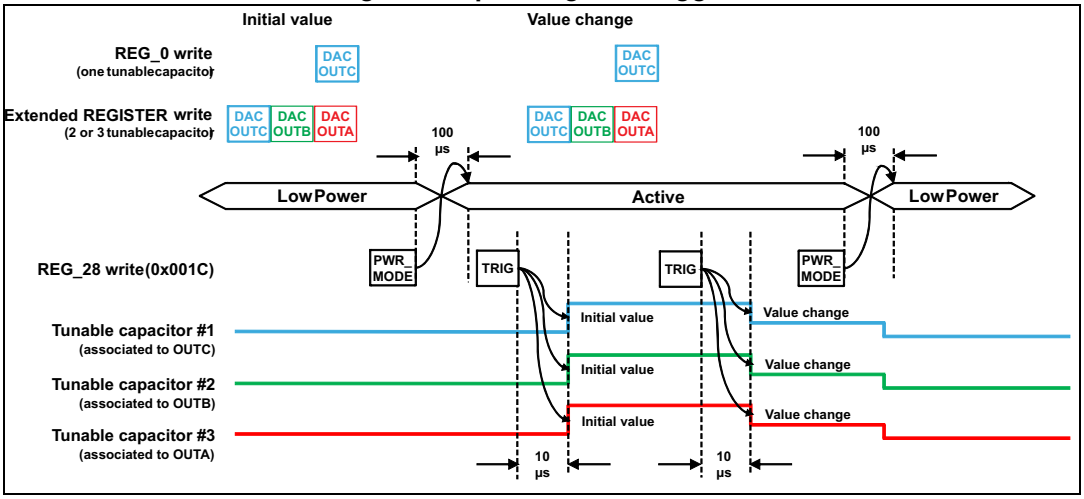
It is recommended to use trigger so that outputs will be activated by write to REG_28. In order to use the trigger, it is required to change the TRIG_MASK to 0.

When only one tunable capacitor is required it is recommended to use the REG_0 associated to OUTC.

When several tunable capacitors are required it is recommended to use extended register write so that all DAC registers can be programmed with only one command.

The *Figure 6* below represents operation when trigger and extended write are in use.

**Figure 6. Operating with triggers**

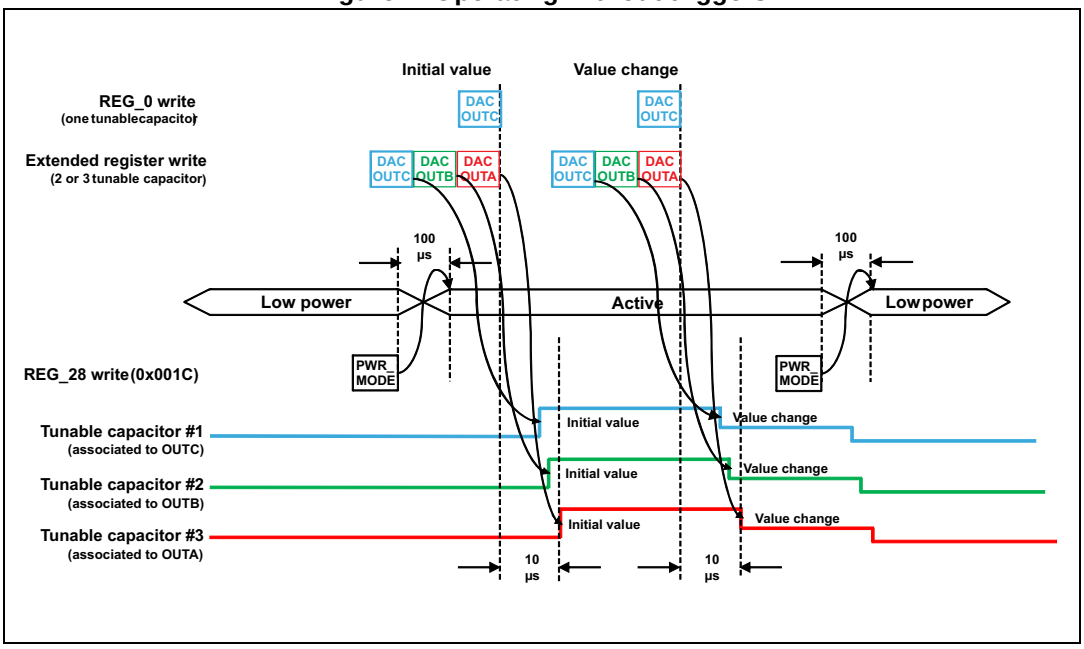


Without triggers:

When the TRIG_MASK are set to 1 (disable) the outputs will change after the DAC are set. When using the extended write all output will changed at the same time.

The *Figure 7* below represents operation without trigger and using extended write.

**Figure 7. Operating without triggers**



# 4 Register table

The HVDAC is embedding 8 bits registers. Registers content is described in *Table 8*, and registers default values are provided in *Table 9*.

**Table 8. Registers content**

| Reg | Address | D7 MSB | D6 | D5 | D4 | D3 | D2 | D1 | D0 LSB | Access type | Triggered |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | [00000] | 0 | DAC C | | | | | | | RW | TRIG0 |
| 1 | [00001] | 0 | DAC B | | | | | | | RW | TRIG0 |
| 2 | [00010] | 0 | DAC A | | | | | | | RW | TRIG1 |
| 28 | [11100] | PWR_MODE | | Trig mask2 | Trig mask1 | Trig mask0 | TRIG2 | TRIG1 | TRIG0 | RW | no |
| 29 | [11101] | Product ID | | | | | | | | R | no |
| 30 | [11110] | Manufacturer ID | | | | | | | | R | no |
| 31 | [11111] | Spare | | Manufacturer ID | | USID | | | | RW | no |

**Table 9. Registers default values**

| Reg | Address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | [00000] | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | [00001] | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 2 | [00010] | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 28 | [11100] | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 29 | [11101] | (*)(1) | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 30 | [11110] | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 31 | [11111] | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |

1. (*) Reg #29 - D7 (MSB DEVICE ID) default value is directly tied to SELSID pin. This bit is set to 1 if SELSID pin is tied to VIO, and set to 0 if SELSID pin is tied to GND.This will allow to have two HVDAC with specific product ID on the same mobile phone.

## 4.1 RFFE interface-register content description

Registers content and control are further described in *Table 10* to *Table 12*.

**Table 10. HVDAC mode selection-REG#28**

| D7 | D6 | Comments |
|---|---|---|
| PWR_MODE | | |
| 0 | 0 | Active mode |
| 0 | 1 | Startup / registers reset to default |
| 1 | 0 | Low power |
| 1 | 1 | n/a |

**Table 11. HVDAC trigger control register - REG#28**

| D5 | D4 | D3 | D2 | D1 | D0 | comments |
|---|---|---|---|---|---|---|
| Trig mask2 | Trig mask1 | Trig mask0 | TRIG2 | TRIG1 | TRIG0 | |
| 0 | 0 | 0 | 0 | 0 | 0 | Triggers 2, 1 and 0 are unmasked and disable |
| 0 | 0 | 0 | 1 | 1 | 1 | Triggers 2, 1 and 0 are unmasked and enable |
| 1 | 1 | 1 | 0 | 0 | 0 | Triggers 2, 1 and 0 are masked (default) |

**Table 12. HVDAC unique slave identifier control - REG31**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | comments |
|---|---|---|---|---|---|---|---|---|
| spare | | Manufacturer_ID[9,8] | | USID | | | | |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | default value |
| 0 | 0 | 0 | 1 | x | x | x | x | USID can be modified by RFFE master, see detailed programming procedure in MIPI RFFE specification |

## 4.2 RFFE interface, command and data frame structure

The STHVDAC-253M RFFE interface has been implemented to support the following command sequences:

- Register WRITE
- Register READ
- Extended Register Write

These supported command sequences are described in *Table 13*.

**Table 13. Support command sequences**

| | SSC (1) | | | Command frame | | | | | | | | | Data frame | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Register write | 0 | 1 | 0 | USID (2) | 0 | 1 | 0 | Reg adress [4,0] | | | | P (3) | DATA[7,0] | P | BP (4) | | | | | | | |
| Register read | 0 | 1 | 0 | USID | 0 | 1 | 1 | Reg adress [4,0] | | | | P | BP | DATA [7,0] | P | BP | | | | | | |
| Extended register write | 0 | 1 | 0 | USID | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | P | Adress[7,0] | P | Up to 4 bytes of data with parity | | | | | | BP |
| | | | | | | | | | BC(5)[3,0] | | | | | | | | | | | | | |
| | | | | | | | | | 1 | 1 | 1 | 1 | | | | | | | | | | |

1. Sequence start condition
2. Unique slave identifier
3. Parity bit
4. Bus park cycle
5. Byte count

All frames are required to end with a single parity bit. The parity bit shall be driven such that the total number of bits in the frame that are driven to logic level 1, including the parity bit, is odd. In case the device detects a parity error, the frame is considered not valid and is ignored.

*Table 14* is showing a typical set of command sequences, to start up and initialize the device, control the HVDAC outputs, and then switch off the device. Command sequences #2,3 & 4 can also be sent at once using an extended mode command sequence.

**Table 14. Typical command sequences**

| CS# | Description | SSC | | | Command frame | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 0 | 1 | 0 | USID | | | | R/W | | | Reg adress [4,0] | | | | | P | DATA [7,0] | | | | | | | | P | BP | | | | | | |
| 1 | Write Reg28 - switch to active mode | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | BP | | | | | | |
| 2 | Write Reg0 - program DAC C | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | BP | | | | | | |
| | | | | | | | | | | | | | | | | | | DAC C value | | | | | | | | P | BP | | | | | | |
| | | | | | | | | | | | | | | | | | | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | BP | | | | | | |
| 3 | Write Reg1 - program DAC B | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | BP | | | | | | |
| | | | | | | | | | | | | | | | | | | DAC B value | | | | | | | | P | BP | | | | | | |
| | | | | | | | | | | | | | | | | | | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | BP | | | | | | |
| 4 | Write Reg2 - program DAC C | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | BP | | | | | | |
| | | | | | | | | | | | | | | | | | | DAC A value | | | | | | | | P | BP | | | | | | |
| | | | | | | | | | | | | | | | | | | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | BP | | | | | | |
| Back to CS#2 to run in loop mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5 | Write Reg28 - switch to shutdown mode | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | BP | | | | | | |

## 4.3 Changing USID

The USID programming method is compliant with MIPI RFFE interface 1.10 (26 July 2011).

This task is achieved writing consecutively registers 29 (Product ID), 30 (Manufacturer ID) and 31 (Manufacturer ID and USID definition).

Note that while reprogramming USID:

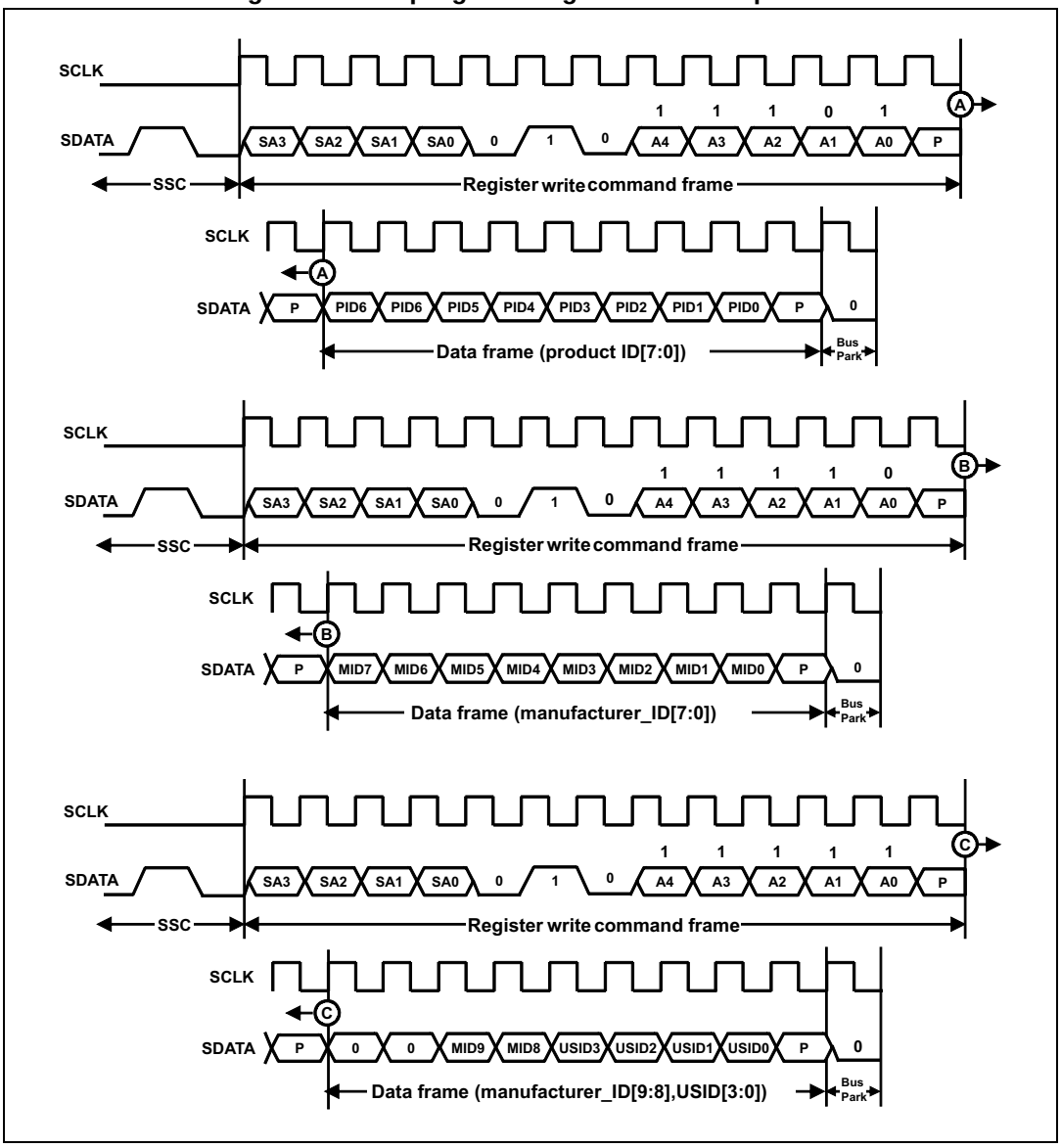
- Bits SA3, SA2, SA1 and SA0 remain old USID value.

- Register 29, D7 (MSB) corresponds to pin SELSID logic level

- New USID is defined by the register 30 last four bits.

After the USID reprogramming, SA3, SA2, SA1 and SA0 values correspond to New USID respective values (see *Figure 8*).

**Figure 8. USID programming command sequence**



## 4.4 Serial interface specification

**Table 15. Interface specification**

| Conditions: $AV_{DD}$ from 2.3 to 5 V, VIO from 1.65 to 1.95 V, $T_{amb}$ from -30 °C to +85 °C, unless otherwise specified | | | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Condition** | **min** | **typ** | **max** | **unit** |
| $F_{CLK}$ | Clock frequency | | | | 26 | MHz |
| $T_{CLK}$ | Clock period | | 38,4 | | | ns |
| $T_{HIGH}$ | Clock high time | | 11,25 | | | ns |
| $T_{LOW}$ | Clock low time | | 11,25 | | | ns |
| $TD_{setup}$ | DATA setup time | Relative to 30% of CLK failing edge | 1 | | | ns |
| $TD_{hold}$ | DATA hold time | Relative to 70% of CLK failing edge | 5 | | | ns |
| $C_{CLK}$ | CLK pin input capacitance | | | | 5 | pF |
| $C_{DATA}$ | DATA pin input capacitance | | | | 8 | pF |

**Figure 9. Register write command sequence**

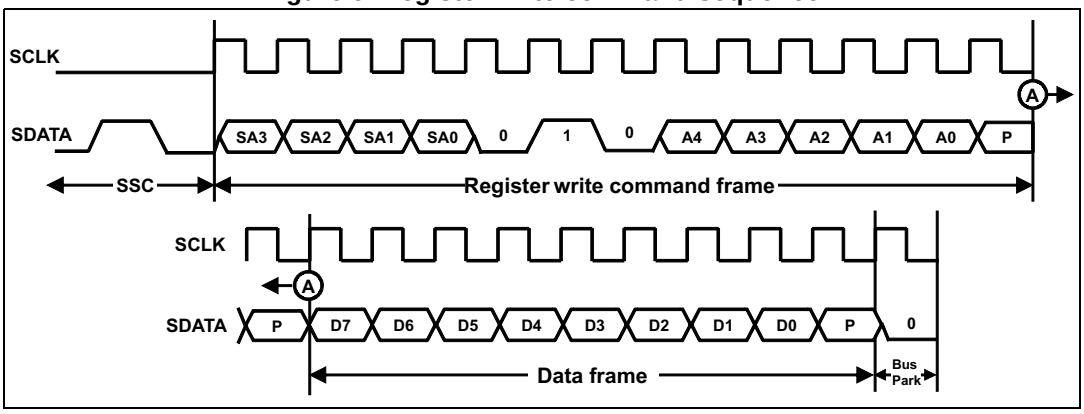



**Figure 10. Register read command sequence**

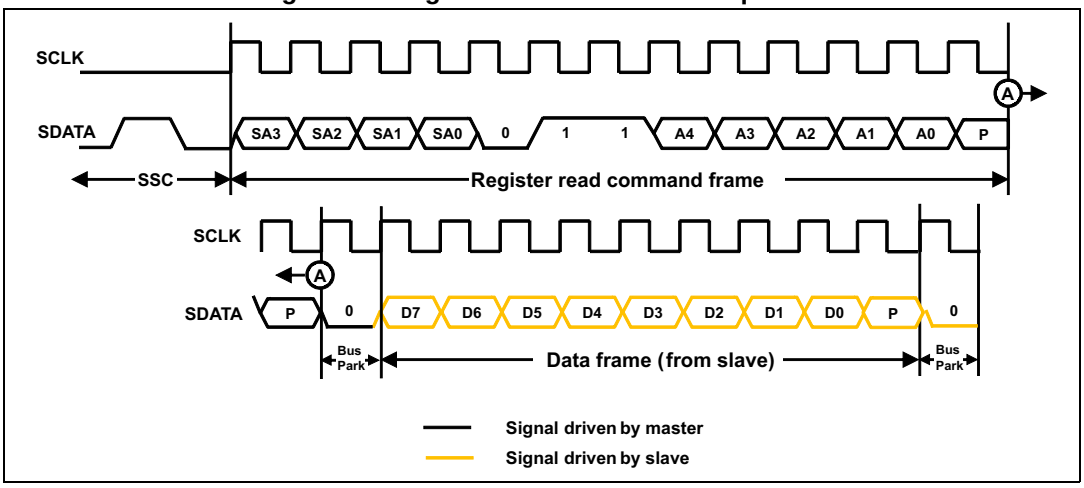


**Figure 11. Extended register write command sequence**

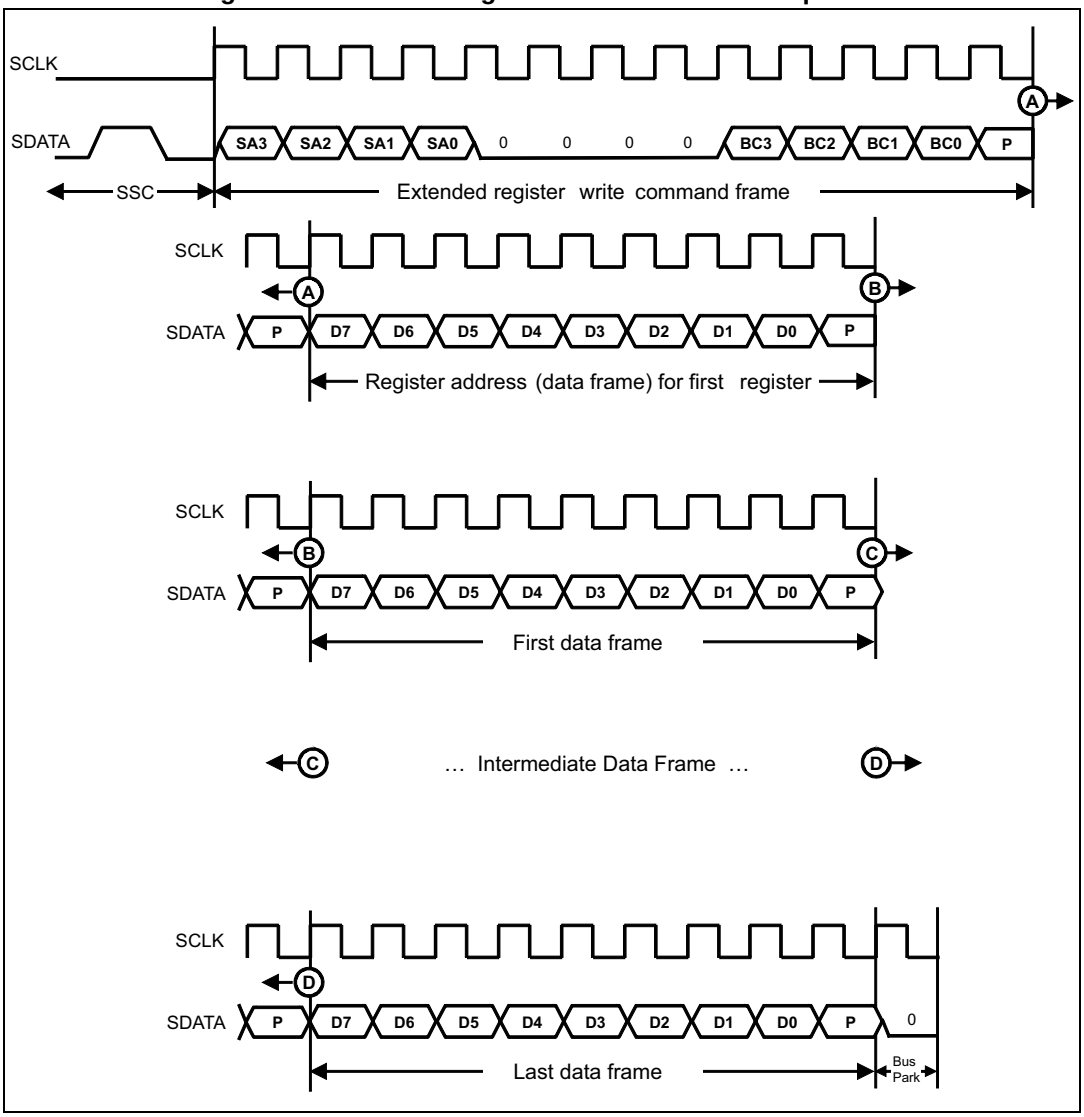
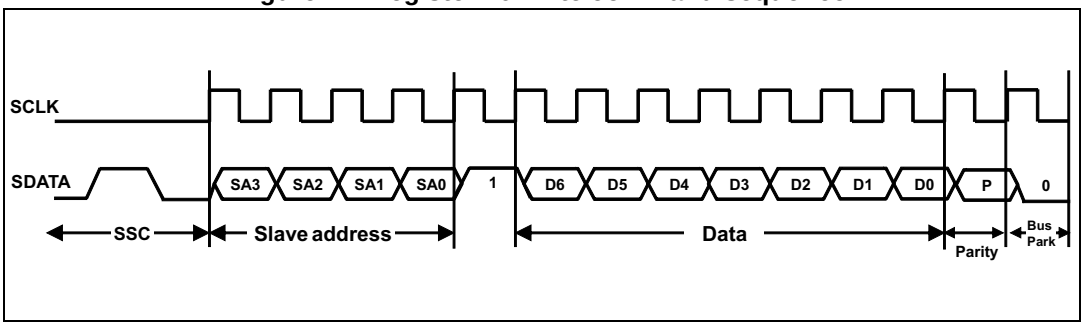



**Figure 12. Register #0 write command sequence**



# 5 Application schematic

Figure 13. Recommended application schematic

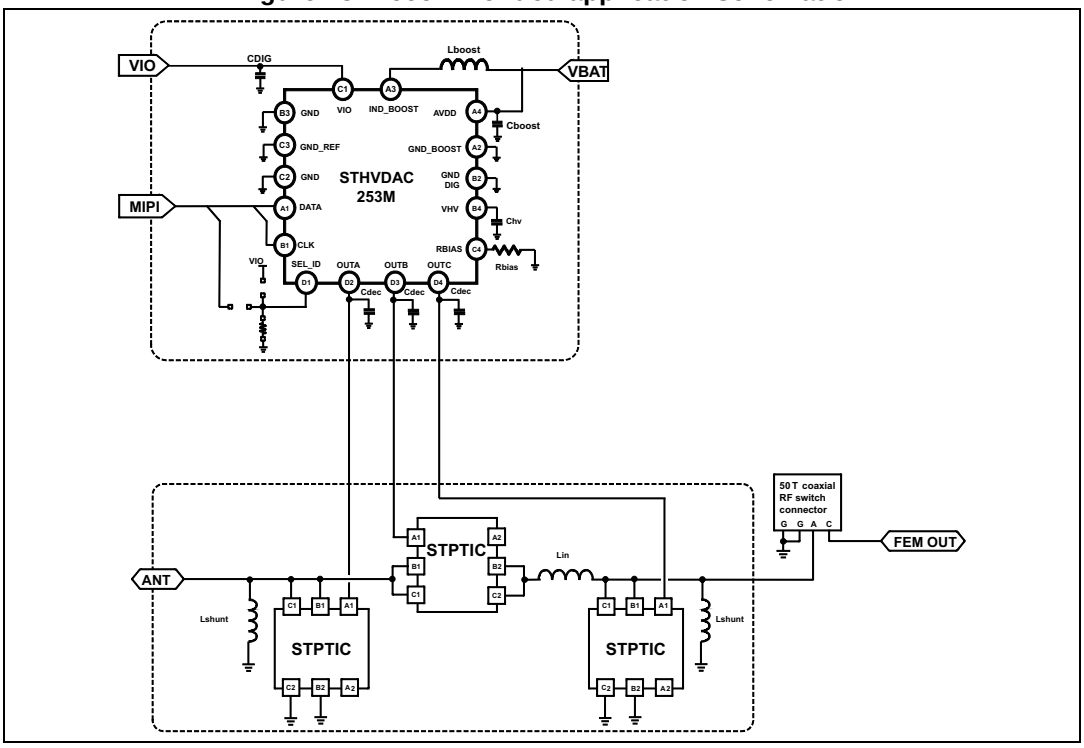



Figure 14. Evaluation board

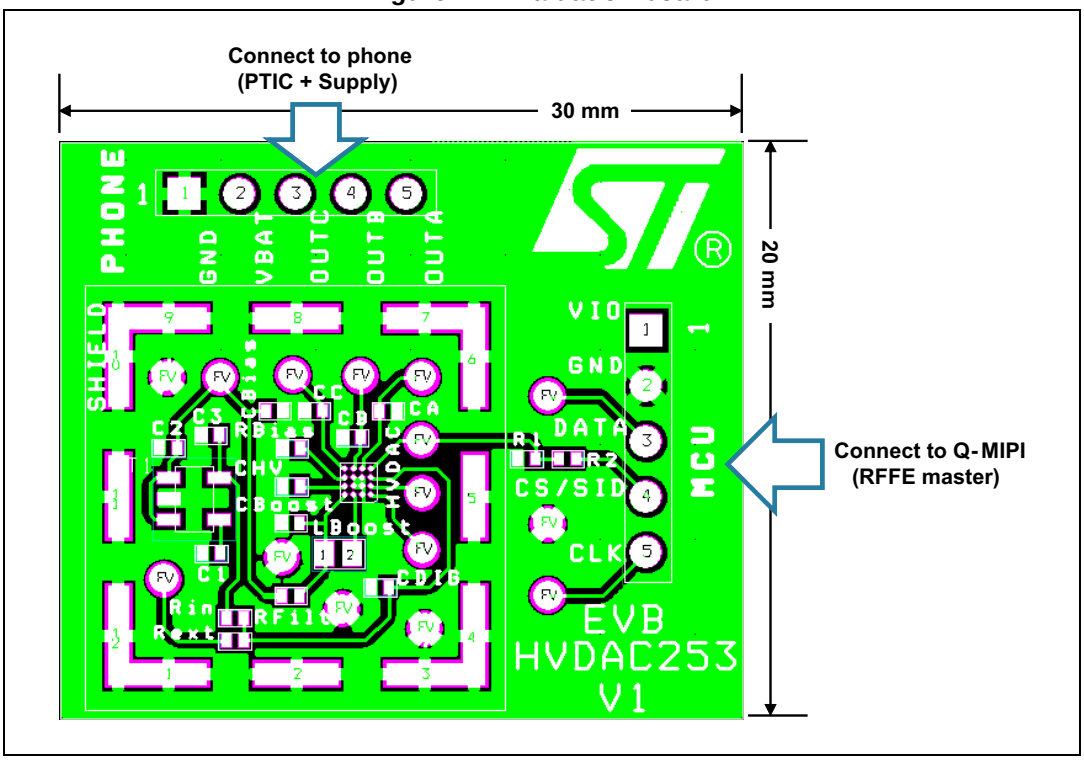


Figure 15. Recommended PCB layout

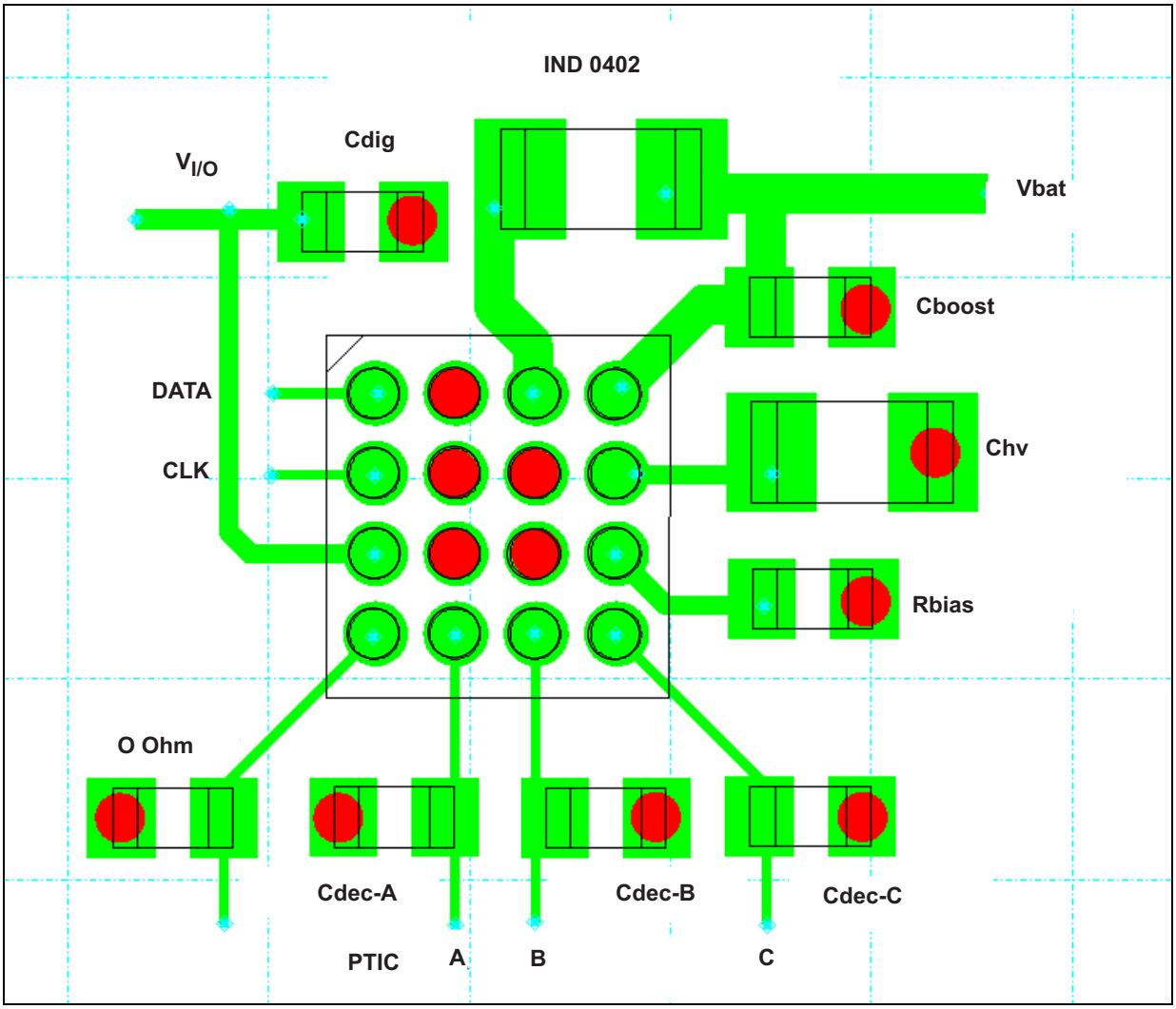



Table 16. Recommended external BOM

| Component | Description | Nominal value | Package (inch) | Package (mm) | Recommended P/N |
|---|---|---|---|---|---|
| $C_{boost}$ | Boost supply capacitor | 1 µF | 0201 | 0603 | AVX: 02016D105MAT2A |
| $L_{boost}$ | Boost inductance | 15 µH | 0603 | 1608 | COILCRAFT: 0603LS-153XGL |
| | | 10 µH | 0402 | 1005 | Murata: LQW15CN100K10 |
| | | | | 2016 | TDK: VLS2016ET-100M |
| $R_{bias}$ | Reference bias resistor, 1% | 110 kΩ | 0201 | 0603 | Multicomp: MC0.0625W0402 |
| $C_{hv}$ | Boost output capacitance, 50 V | 22 nF | 0402 | 1005 | Murata: GRM155R71H223KA12<br>Semco: CL21B223KBCNNNC |
| $C_{dec}$ | Decoupling capacitance, 50 V | 100 pF | 0201 | 0603 | TDK: C0603COG1H101J |

# 6 Package information

- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

**Figure 16. Package dimensions**

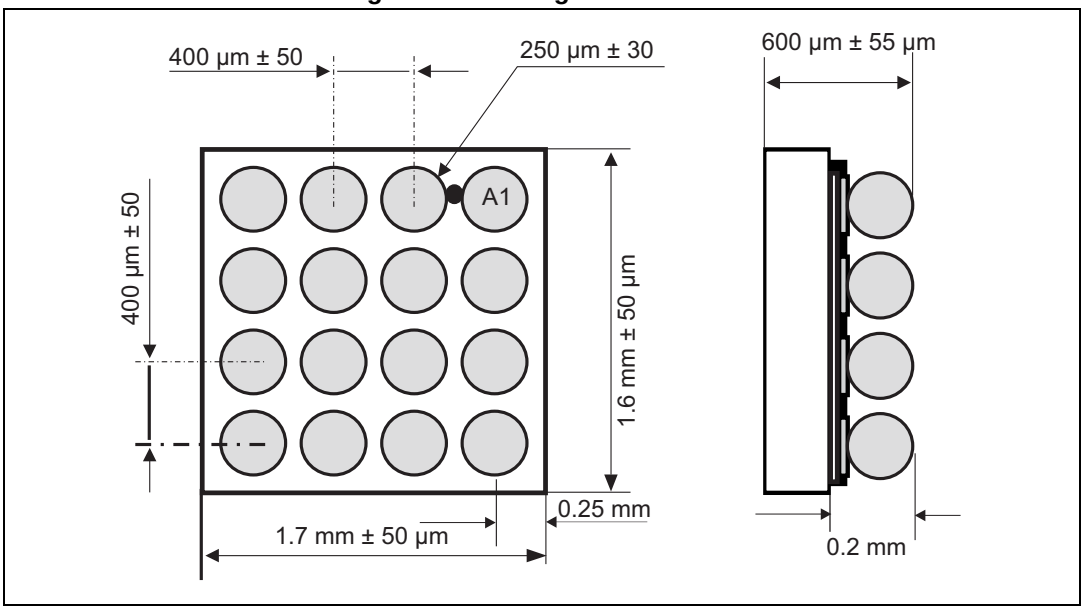



**Figure 17. Footprint**

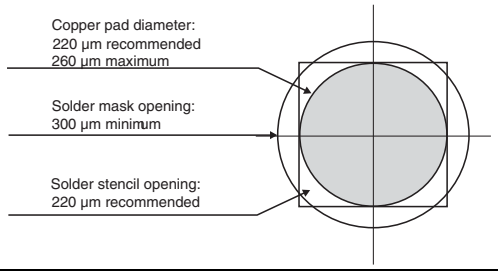



**Figure 18. Marking**

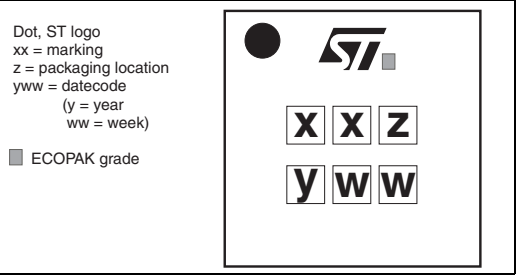
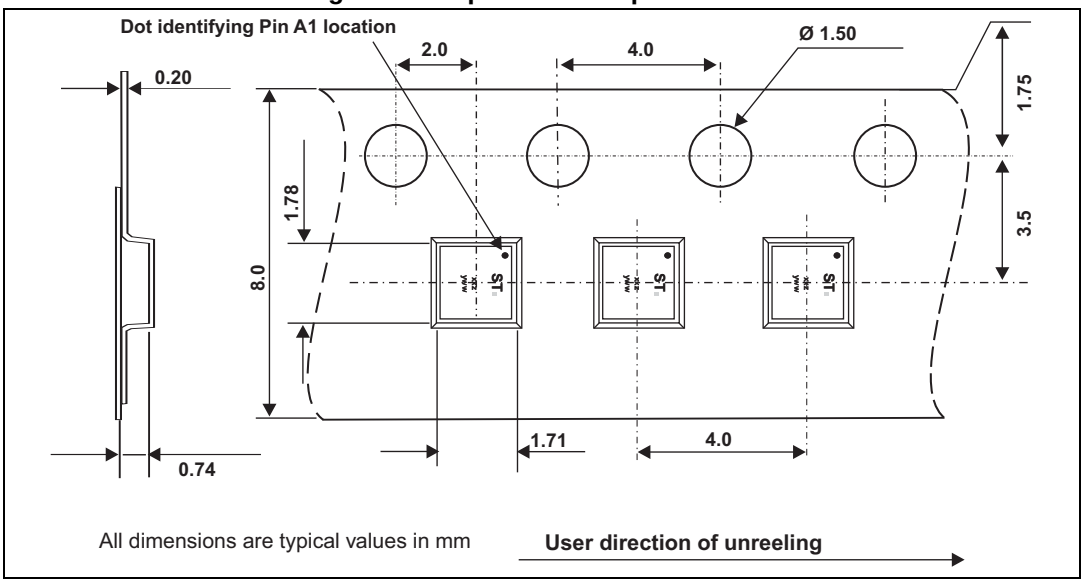


**Figure 19. Tape and reel specification**



# 7 Ordering information

**Table 17. Ordering information**

| Order code | Marking | Package | Weight | Base qty | Delivery mode |
|---|---|---|---|---|---|
| STHVDAC-253MF3 | PP | Flip Chip | 2.7 mg | 5000 | Tape and reel |

*Note: More information is available in the STMicroelectonics Application note: AN1235: "Flip Chip: Package description and recommendations for use"*

# 8 Revision history

**Table 18. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 19-Feb-2014 | 1 | Initial release. |

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