ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{CC} ..... -0.3V to 6.5V
RESET, $\overline{\text{RESET}}$ ..... -0.3V to V_{CC}+0.3V
Output Current (RESET, $\overline{\text{RESET}}$) 20mA
Power Dissipation (T_A=70°C) 320mW
Junction Temperature ..... 125°C
Storage Temperature ..... -65°C to 150°C

OPERATING RATINGS

Input Voltage Range V_{CC} ..... 0.9V to 6V
Junction Temperature Range ..... -40°C to 85°C

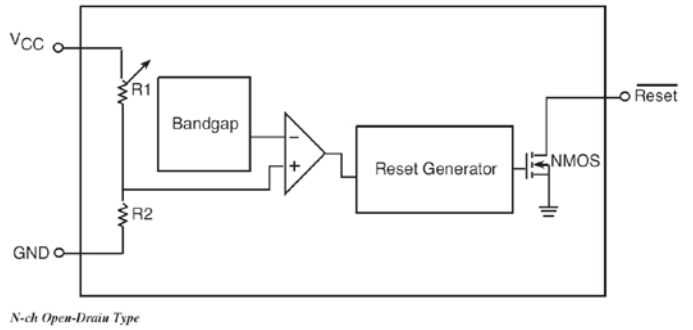
ELECTRICAL SPECIFICATIONS

Specifications with standard type are for an Operating Temperature of T_A = 25°C only; limits applying over the full Operating Temperature range are denoted by a "•". Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_A = 25°C, and are provided for reference purposes only. Unless otherwise indicated, T_A= 25°C.

Parameter	Min.	Typ.	Max.	Units		Conditions
Operating Voltage Range V_{CC}	0.9		6.0	V		
Supply Current I_{CC}		1.0	3.0	µA		$V_{CC}=V_{TH}+0.1V$
Reset Threshold V_{TH}	2.265	2.3	2.335	V		T_A=+25°C
	2.254		2.346		•	T_A=-40°C to 85°C
	2.561	2.6	2.639			T_A=+25°C
	2.548		2.652		•	T_A=-40°C to 85°C
	2.857	2.9	2.944			T_A=+25°C
	2.842		2.958		•	T_A=-40°C to 85°C
	3.054	3.1	3.147			T_A=+25°C
	3.038		3.162		•	T_A=-40°C to 85°C
	4.334	4.4	4.466			T_A=+25°C
	4.312		4.488		•	T_A=-40°C to 85°C
	4.531	4.6	4.669			T_A=+25°C
	4.508		4.692		•	T_A=-40°C to 85°C
V_{CC} Reset Delay t_{TRIP}		20		µs		$V_{CC}=V_{TH}$ to (V_{TH} - 0.1V), V_{TH}=3.1V
Reset Active Timeout Period t_{RP}	140	230	560	ms		T_A=+25°C
	100		1030		•	T_A=-40°C to 85°C
RESET Output Voltage V_{OH}	0.8V_{CC}			V		$V_{CC}=V_{TH}$ - 0.1V, I_{SOURCE} = 1.2mA
RESET Output Voltage V_{OL}			0.3			$V_{CC}=V_{TH}$ + 0.1V, I_{SINK} = 1.2mA
$\overline{\text{RESET}}$ Output Voltage V_{OH}	0.8V_{CC}			V		$V_{CC}=V_{TH}$ + 0.1V, I_{SOURCE} = 1.2mA
$\overline{\text{RESET}}$ Output Voltage V_{OL}			0.3			$V_{CC}=V_{TH}$ - 0.1V, I_{SINK} = 1.2mA

Note 1: $\overline{\text{RESET}}$ output is for SP809; RESET output is for SP810.

BLOCK DIAGRAM



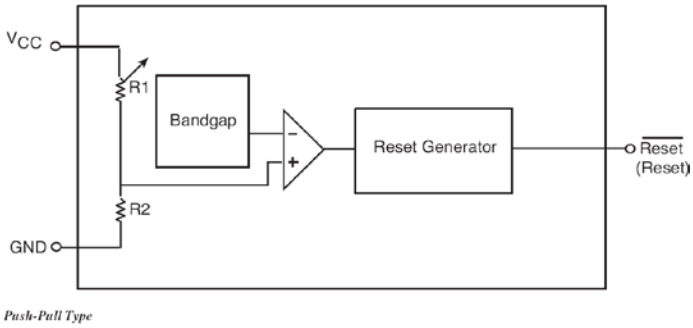


Fig. 2: SP809 / SP810 Block Diagram

PIN ASSIGNMENT

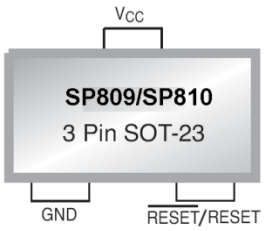


Fig. 3: SP809 / SP810 Pin Assignment

PIN DESCRIPTION

Name	Pin Number	Description
GND	1	Ground Signal
$\overline{\text{RESET}}$	2	Active Low Output Pin. $\overline{\text{RESET}}$ Output remains high while VCC is below the reset threshold
RESET		Active High Output Pin. RESET Output remains high while VCC is below the reset threshold
V_{CC}	3	Supply Voltage

ORDERING INFORMATION(1)

Part Number	Operating Temperature Range	Lead-Free	Package	Packing Method
SP809EK-L-2-3/TR	-40°C≤T_A≤+85°C	Yes(2)	SOT23-3	Tape & Reel
SP809EK-L-2-6/TR				
SP809EK-L-2-9/TR				
SP809EK-L-3-1/TR(3)				
SP809EK-L-4-6/TR(3)				
SP809NEK-L-2-3/TR(3)				
SP809NEK-L-2-9/TR(3)				
SP809NEK-L-3-1/TR				
SP809NEK-L-4-6/TR(3)				
SP810EK-L-4-4/TR(3)				

NOTES:

1. Refer to www.exar.com/SP809 and www.exar.com/SP810 for most up-to-date Ordering Information.
2. Visit www.exar.com for additional information on Environmental Rating.
3. NRND – Not Recommended for New Designs.

TYPICAL PERFORMANCE CHARACTERISTICS

All data taken at T_A = 25°C, unless otherwise specified - Schematic and BOM from Application Information section of this datasheet.

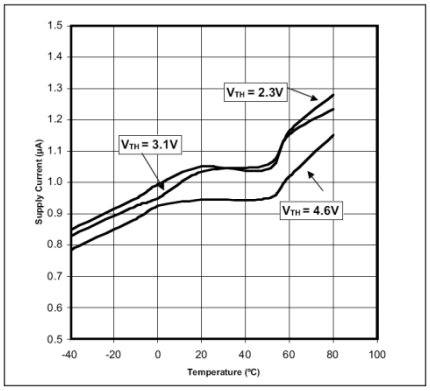


Fig. 4: Supply Current versus Temperature

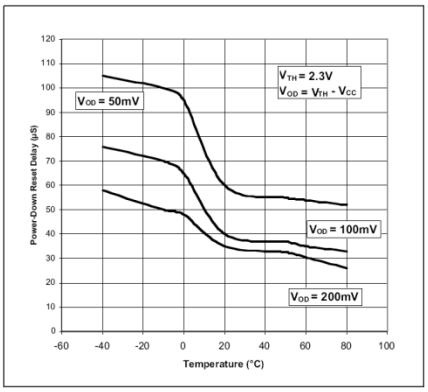


Fig. 5: Power-Down Reset Delay versus Temperature

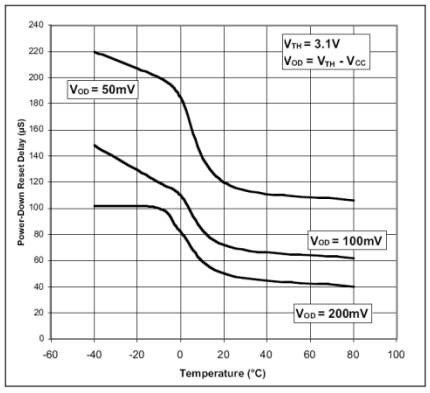


Fig. 6: Power-Down Reset Delay versus Temperature

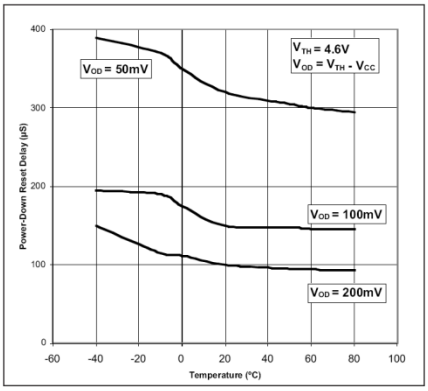


Fig. 7: Power-Down Reset Delay versus Temperature

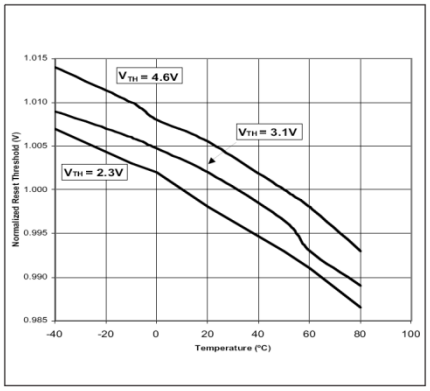


Fig. 8: Normalized Reset Threshold versus Temperature

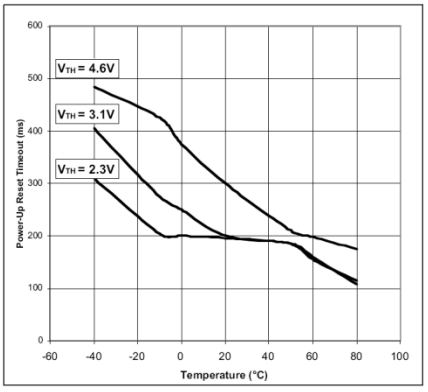


Fig. 9: Power-Up Reset Time-out versus Temperature

THEORY OF OPERATION

µP will be activated at a valid reset state. These µP supervisory circuits assert reset to prevent code execution errors during power-up, power-down, or brownout conditions.

Reset is guaranteed to be a logic low for $V_{TH}>V_{CC}>0.9V$. Once V_{CC} exceeded the reset threshold, an internal timer keeps $\overline{RESET}$ low for the reset timeout period; after this interval, $\overline{RESET}$ goes high.

If a brownout condition occurs (V_{CC} drops below the reset threshold), $\overline{RESET}$ goes low. Any time V_{CC} goes below the reset threshold, the internal timer resets to zero, and $\overline{RESET}$ goes low. The internal timer is activated after V_{CC} returns above the reset threshold, and $\overline{RESET}$ remains low for the reset timeout period.

BENEFIT OF HIGHLY ACCURATE RESET THRESHOLD

SP809/810 with specified voltage as 5V±10% or 3V±10% are ideal for systems using a 5V±5% or 3V±5% power supply. The reset is guaranteed to assert after the power supply falls below the minimum specified operating voltage range of the system ICs. The pre-trimmed thresholds are reducing the range over which an undesirable reset may occur.

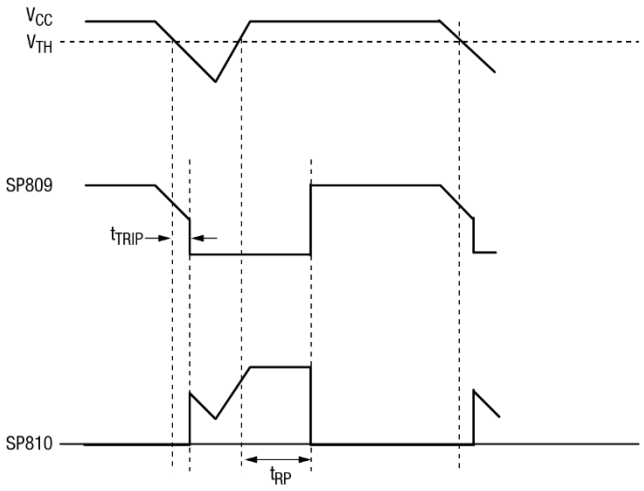


Fig. 10: Timing Waveforms

APPLICATION INFORMATION

NEGATIVE GOING V_{CC} TRANSIENTS

In addition to issuing a reset to the µP during power-up, power-down, and brownout conditions, SP809 series are relatively resistant to short-duration negative-going V_{CC} transient.

ENSURING A VALID RESET OUTPUT DOWN TO $V_{CC}=0$

When V_{CC} falls below 0.9V, SP809 $\overline{RESET}$ output no longer sinks current; it becomes an open circuit. In this case, high-impedance CMOS logic inputs connecting to $\overline{RESET}$ can drift to undetermined voltages. Therefore, SP809/810 with CMOS is perfect for most applications of V_{CC} down to 0.9V.

However in applications where $\overline{RESET}$ must be valid down to 0V, adding a pull-down resistor to $\overline{RESET}$ causes any leakage currents to flow to ground, holding $\overline{RESET}$ low.

INTERFACING TO µP WITH BIDIRECTIONAL RESET PINS

The $\overline{RESET}$ output on the SP809N is open drain, this device interfaces easily with µPs that have bidirectional reset pins. Connecting the µP supervisor's $\overline{RESET}$ output directly to the microcontroller's RESET pin with a single pull-up resistor allows either device to assert reset.

TEST CIRCUIT

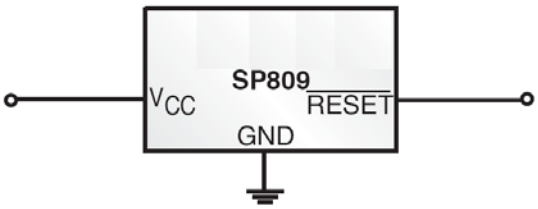
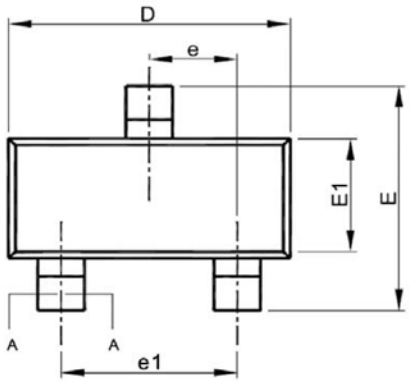


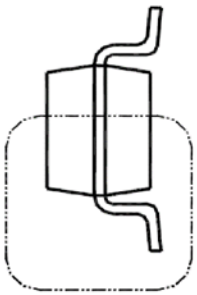
Fig. 11: Test Circuit

PACKAGE SPECIFICATION

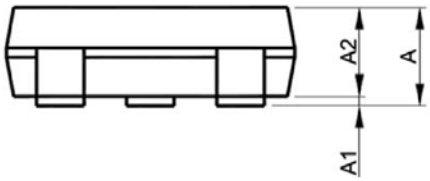
3-PIN SOT23



TOP VIEW



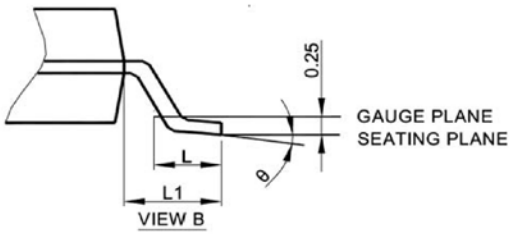
BOTTOM VIEW



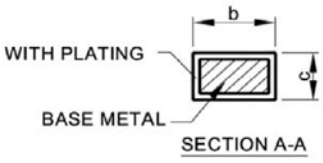
SIDE VIEW

SYMBOL	SOT-23	
	MILLIMETERS	
	MIN.	MAX.
A	0.95	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.30	0.50
c	0.08	0.22
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.70
e	0.95 BSC	
e1	1.90 BSC	
L	0.30	0.60
L1	0.60 REF	
θ	0°	8°

TERMINAL DETAILS



VIEW B



SECTION A-A

1. Refer to Jedec MO-178
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 10mils per side.
3. Dimension "E1" does not include inter lead flash or protursions.
4. All dimensions are milimeters.

Drawing No : POD - 00000128

Revision: A

REVISION HISTORY

Revision	Date	Description
2.0.0	2011	Reformat of Datasheet Correction of package drawing
2.0.1	August 2017	Correct Reset Delay conditions. Updated to MaxLinear logo. Updated format and ordering information table.
2.0.2	November 2017	Corrected typo from rev 2.0.1, added 2 missing overlines to RESET in Electrical Specifications.

Corporate Headquarters:
5966 La Place Court
Suite 100
Carlsbad, CA 92008
Tel.:+1 (760) 692-0711
Fax: +1 (760) 444-8598
www.maxlinear.com

High Performance Analog:
1060 Rincon Circle
San Jose, CA 95131
Tel.: +1 (669) 265-6100
Fax: +1 (669) 265-6101
Email: powertechsupport@exar.com
www.exar.com