- Cold start power up time in less than 1 ms
- Programmable via USB, UART, SPI, Over-The-Air
- 23 GPIOs, USB 2.0, UART, SPI
- 4 channel 12 bit rail-to-rail ADC
- 88-key matrix scan hardware
- Dimmer and PWM generators
- IR code generator and learning HW
- 4 channel LED PWM generator

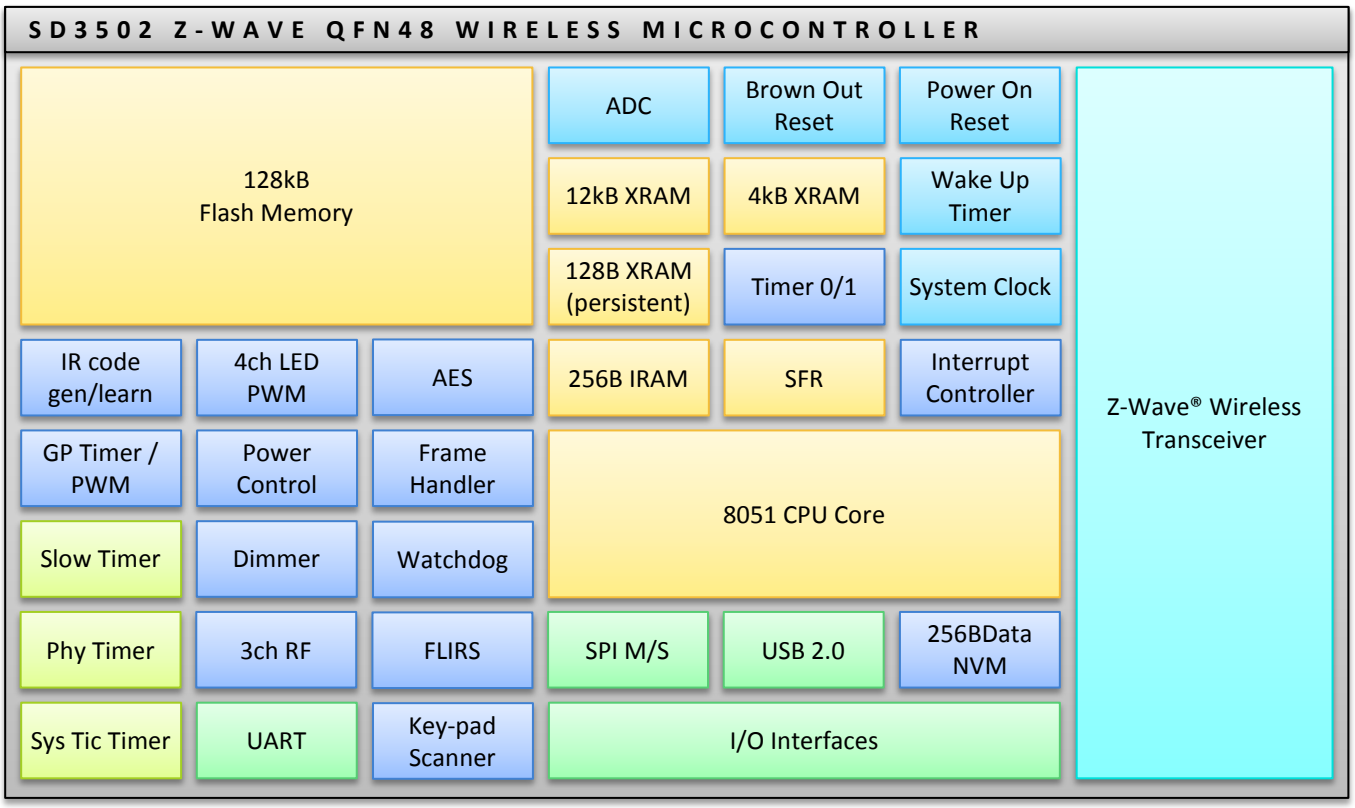


Figure 1: Architecture (kB=1024 byte)

DESCRIPTION

The SD3502 Z-Wave® chip is a complete wireless solution for applications in home control, home security monitoring, home energy management, and AV control, consisting of an integrated multi-band, multi-channel, multi-speed RF transceiver, an 8051 microcontroller, a comprehensive set of peripherals, SRAM, 128k-byte FLASH, and data-NVM memory for sharing between a user application and the Z-Wave® protocol.

Thanks to its patented multi-channel support and excellent interference blocking performance, the SD3502 provides superior robustness. The Z-Wave system uses frequency agility, frame acknowledgement, retransmission, collision avoidance, frame checksum check, and sophisticated mesh routing for reliable full-home coverage. Products based on the SD3502 are fully interoperable with existing Z-Wave solutions.

The SD3502 provides lowest power consumption in a wide range of supply voltages, starting at only 2.3V, enabling multi-year operation on just two AAA batteries. It enables advanced battery-to-battery applications in networks at an average current of only 50 µA.

Through an integrated HW key matrix scanner, on-chip IR coding support, IR learning features, low power design, and advanced power management, the SD3502 is well-matched to the requirements of low cost universal and meta-data remote controls with years of battery life.

Thanks to its integrated full-speed USB 2.0 interface, the cost of integrating Z-Wave into PC designs, PDAs, smart phones, and other peripherals is reduced. The UART and SPI interfaces on the SD3502 further simplify integration into other host devices, such as CE and AV devices. The SD3502 provides a high-performance AES-128 hardware processor plus a hardware random number generator that are fully compatible with the security solution in Z-Wave.

The SD3502 provides four PWM's for interfacing to external LED drivers.

CONTENTS

ELECTRICAL SPECIFICATIONS

NOTES

For Absolute Maximum Ratings, refer to page 9.
For Qualification Test Conditions, T_A = -40 to 90°C, V_{DD} = 2.3 to 3.6V, refer to page 10.
For Production Test Conditions, refer to page 10.

POWER CONSUMPTION

Supply Voltage Range T_A = -40 to +90°C		Min	Max	Units
V_{DD}	Supply Voltage	2.3	3.6	V
$V_{DD\ USB}$	Supply Voltage when the USB PHY is used	3.0	3.6	V
V_{BOR}	The supply voltage at which the Brown Out Detector (BOR) resets the chip. The BOR will reset the device if the supply is inadequate to guarantee correct behavior.		2.3	V

System consumption, Z-Wave FLIRS Node, V_{DD} = 2.3 to 3.6V, T_A = -40 to +90°C		Typ	Units
$I_{VDD\ FLIRS\ 1}$	Average current drawn by a frequently listening SDK 6.51.01 slave sensor to keep the RF link active, EU/US, 1 sec max latency, measured	44	µA
$I_{VDD\ FLIRS\ 2}$	Same as above, 3-channel mode (use depends on actual region), 1 sec max latency	76	µA

Power Saving Modes, V_{DD}= 3.3V, T_A = 25°C		Typ	Max	Units
$I_{VDD\ SLEEP}$	Interruptible sleep mode	1.0	1.6	µA
$\Delta I_{VDD\ WUT}$	Enabling Wake-up Timer when in sleep mode increments current by	0.7		µA
$\Delta I_{VDD\ RAM}$	Enabling SRAM data persistency in a sleep mode adds	0.1		µA
$I_{USB\ SLEEP}$	USB sleep mode with full data & state persistency, Wake-up Timer, and system clock	1.9	2.1	mA

Power Saving Modes, V_{DD} = 3.0 to 3.6V, T_A = -40 to +90°C		Max	Units
$I_{USB\ SLEEP}$	USB suspend mode with full data and state persistency, Wake-up Timer, and system clock	2.3	mA

Active Modes, V_{DD}= 3.3V, T_A = 25°C		Typ	Max	Units
$I_{VDD\ MCU}$	MCU running at 32MHz	15	16	mA
$I_{VDD\ MCU\ RX}$	MCU and receiver (RX mode)	32	34	mA
$I_{VDD\ MCU\ TX\ 0.5}$	MCU and transmitter (TX mode), 0.5 dBm	34	36	mA
$I_{VDD\ MCU\ TX\ 3.5}$	MCU and transmitter (TX mode), 3.5 dBm	36	38	mA
$\Delta I_{VDD\ ADC}$	Using the ADC adds	0.15	0.25	mA

Programming modes, V_{DD}= 3.3V, T_A = 25°C		Typ	Max	Units
$I_{VDD\ PGM\ USB}$	Programming via USB	15		mA
$I_{VDD\ PGM\ SPI}$	Programming via SPI	15		mA
$I_{VDD\ PGM\ UART}$	Programming via UART	15	16	mA

SYSTEM TIMING

System Start-Up Time, V_{DD} = 2.3 to 3.6V, T_A = -40 to +90°C		Max	Units
$T_{POWER\ UP}$	The System Start-Up delay from the supply voltage (VDD) exceeds 2.3V to the MCU responds, using qualification schematic and a power rise time not exceeding 10µs.	1	ms

	Note 1: This value applies identically for recovery after brown-out events. Note 2: There is no restriction on the supply rise time. But an increase in power rise time will increase the Start-Up time proportionally.

Wake-up Timer precision, V_{DD} = 2.3 to 3.6V, T_A = -40 to +90°C		Max	Units
$T_{WUT\ OFFSET}$	Wake-up Timer accuracy, max offset deviation	40	ms
$T_{WUT\ SCALE}$	Wake-up Timer accuracy, max scale deviation	2%	

Reset and Interrupt timing requirements, V_{DD} = 2.3 to 3.6V, T_A = -40 to +90°C		Max	Units
T_{RST_PULSE}	Minimum time RESET_N must be held low to guarantee a full system reset	20	ns
T_{INT_PULSE}	To guarantee recognition of an external interrupt pulse, an input pin, if configured to sample external interrupts, must be held low two complete clock cycles.	65	ns

NON-VOLATILE MEMORIES

The Flash and the NVM Data Array are built with SuperFlash® technology.

Endurance and Retention	Min	Units
FLASH (code) endurance	10k	cycle
Data NVM endurance	100k	cycle
Retention, data and code, at room temperature	100	year
Retention, data and code, at junction temperature -40°C to 105°C	10	year

RF TRANSCEIVER CHARACTERISTICS

Transmit Power, V_{DD} = 2.3 to 3.6V, T_A = -40 to +90°C		Min	Max	Units
P_{0x3F}	RF output power delivered to 50 Ω at max software setting	4.3	6.5	dBm
P_{0x01}	Same as above, but at min software setting	-24.5	-22	dBm
$P_{h2,odBm}$	2nd harmonics content, PA setting 0x14 ~ 0dBm		-50	dBc
$P_{h2,5dBm}$	2nd harmonics content, PA setting 63 ~ 5dBm		-30	dBc
$P_{h3,0dBm}$	3rd harmonics content, PA setting 20 ~ 0dBm		-30	dBc
$P_{h3,5dBm}$	3rd harmonics content, PA setting 63 ~ 5dBm		-20	dBc

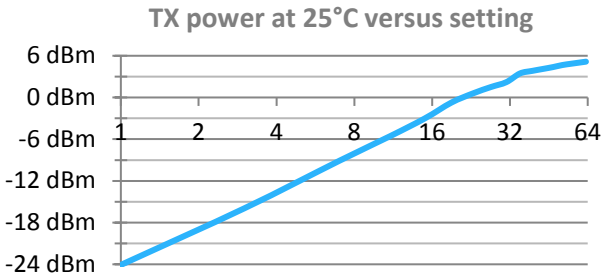


Figure 2: Typical Transmit Power versus Digital Setting

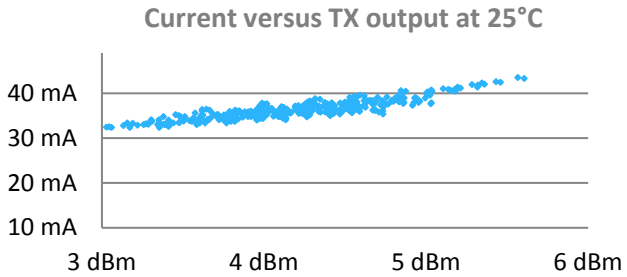


Figure 3: Typical current consumption versus TX power

Receiver Sensitivity, V_{DD} = 2.3 to 3.6V, T_A = -40 to +90°C		Max	Units
$P_{9.6}$	Sensitivity at 9.6 kbit/s. Defined as the lowest power at which the frame error rate is less than 1%	-104	dBm
P_{40}	Sensitivity at 40 kbit/s, defined as above	-99	dBm
P_{100}	Sensitivity at 100 kbit/s, defined as above	-92	dBm

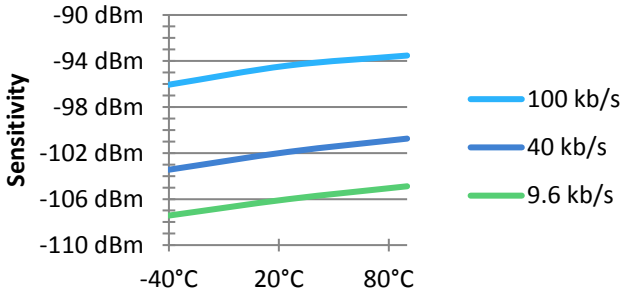


Figure 4: Typical Sensitivity (average over process corners)

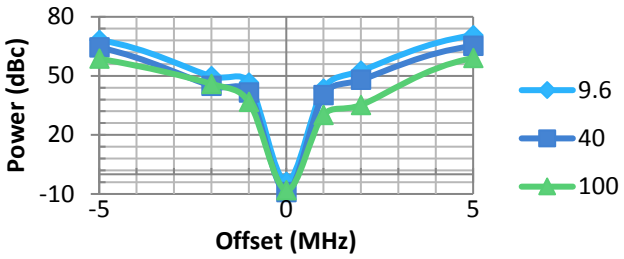


Figure 5: Typical Blocking performance

Blocking @40kbit/s, RSSI, LO leakage, intermodulation at V_{DD}= 3.3V, T_A = 25°C		Typ	Units
$P_{BLOCK\ 1MHz}$	Blocking at Δf=1MHz. Blocker level is defined relative to a wanted signal and measured with the wanted signal 3 dB above the sensitivity level	34	dBc
$P_{BLOCK\ 2MHz}$	Blocking at Δf=2MHz. Defined as above	38	dBc
$P_{BLOCK\ 5MHz}$	Blocking at Δf=5MHz. Defined as above	60	dBc
$P_{BLOCK\ 10MHz}$	Blocking at Δf=10MHz. Defined as above	63	dBc
$P_{BLOCK\ 100MHz}$	Blocking at Δf=100MHz. Defined as above	68	dBc
$RSSI_{RANGE}$	RSSI Dynamic Range	70	dB
$RSSI_{LSB}$	RSSI Resolution	1.5	dB
P_L	LO leakage	-80	dBm
IIP3	Intermodulation distortion product, third order interception point	-12	dBm

NOTES

- All Z-Wave frequencies and modulation forms apply, unless noted otherwise. Z-Wave frequencies currently span from 865.2MHz (IN) to 926MHz (Japan).
- Crystal must be rated or calibrated to 32MHz ±25ppm.
- Region-specific impedance matching circuits according to reference designs applies.
- Power level specifications are valid at the RF pin of the chip.

DIGITAL IO CHARACTERISTICS

GPIO pins have a nominal drive capability of 8mA (or 16mA) at the nominal 3.3V supply conditions. They are however fully functional down to 2.3V. Digital input pins, including all GPIO pins, features Schmitt trigger input hysteresis.

3.3V SYSTEMS

Output Pins, V_{DD} = 3.0V to 3.6V, T_A = -40 to +90°C		Min	Max	Units
V_{OH}	High level output voltage, sourcing 8mA (pins P3.4 – P3.7 16mA)	2.4		V
V_{OL}	Low level output voltage, sinking 8mA (pins P3.4 – P3.7 16mA)		0.4	V
T_{RISE}	Rise Time, 10% to 90%, 2pF external load		10	ns
T_{FALL}	Fall Time, 90% to 10%, 2pF external load		10	ns

Input Pins, V_{DD} = 3.0V to 3.6V, T_A = -40 to +90°C		Min	Max	Units
V_{IF}	Falling input trigger threshold	0.9	1.3	V
V_{IR}	Rising edge trigger threshold	1.6	2.1	V
ΔV_I	Hysteresis	0.65	0.95	V
I_{IN}	Input current, 0V ≤ V_{IN} ≤ VDD when internal pull-up is not available	-10	10	µA
$I_{PULL\ UP}$	Input current at V_{IN}=0V when internal pull-up is available	40	120	µA
C_{IN}	Input capacitance		10	pF

SUB 3V SYSTEMS

Output Pins, V_{DD}= 2.3V to 3.0V, T_A = -40 to +90°C		Min	Max	Units
V_{OH}	High level output voltage, sourcing 6mA (pins P3.4 – P3.7 12mA)	1.9		V
V_{OL}	Low level output voltage, sinking 6mA (pins P3.4 – P3.7 12mA)		0.4	V

Input Pins, V_{DD}= 2.3V to 3.0V, T_A = -40 to +90°C		Min	Max	Units
V_{IF}	Falling input trigger threshold	0.75	1.05	V
V_{IR}	Rising edge trigger threshold	1.35	1.85	V
ΔV_I	Hysteresis	0.55	0.85	V
I_{IN}	Input current, 0V ≤ V_{IN} ≤ VDD when internal pull-up is not available	-7	7	µA
$I_{PULL\ UP}$	Input current at V_{IN}=0V when internal pull-up is available	35	90	µA

TYPICAL IO CHARACTERISTICS, V_{DD}= 2.3V TO 3.6V, T_A = -40 TO +90°C

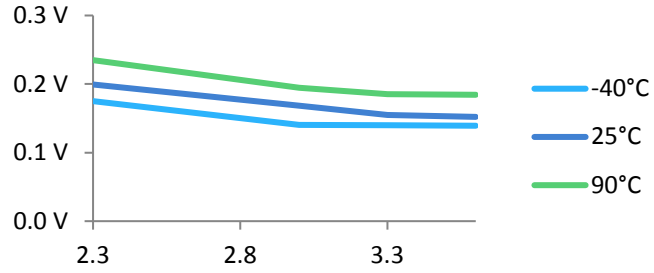


Figure 6: Output Voltage versus supply voltage when sinking 8mA

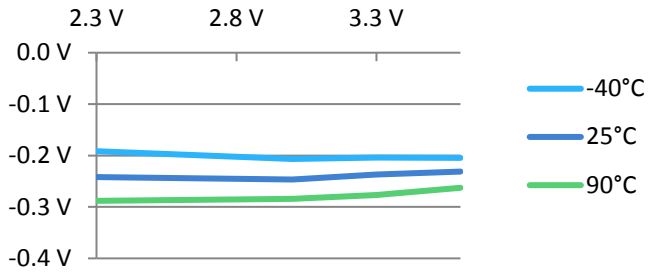


Figure 7: Output Voltage – VDD versus supply voltage when sourcing 8mA

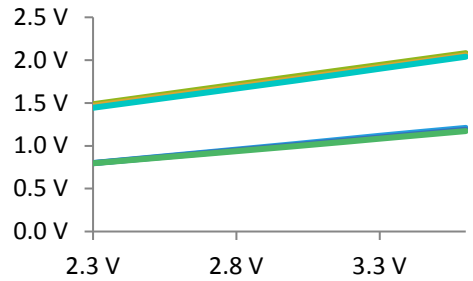


Figure 8: Input threshold voltages incl. hysteresis, versus supply voltage

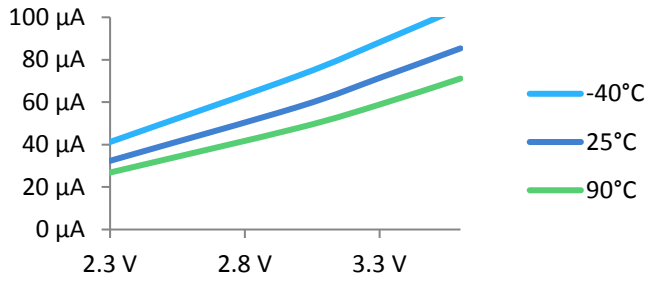


Figure 9: Input current at V_{IN}=0V with pull-up activated, versus supply voltage

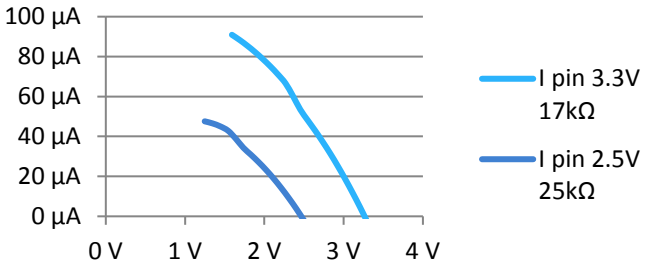


Figure 10: Internal pull up current versus pin voltage, 25°C, V_{DD}=3.3V and V_{DD}=2.5V

Pull up resistance ranges 17kΩ to 25kΩ at 25°C.

ADC CHARACTERISTICS

12 bit A to D converter, V_{DD} = 2.3 to 3.6V, T_A = -40 to +90°C		Min	Max	Units
V_{BG}	Internal Voltage Reference, referenced to GND	1.2	1.3	V
	Converter used with external bipolar voltage reference:			
$V_{REF\ NEG}$	Lower reference input voltage	0	1.2	V
$V_{REF\ POS}$	Upper reference input voltage	VDD-0.9	VDD	V
	Differential non-linearity	-1	1	LSB
	Accuracy at sampling 10k samples per second at 12 bit resolution	-5	5	LSB
	Accuracy at sampling 20k samples per second at 8 bit resolution	-2	2	LSB
$I_{IN\ ADC}$[1]	Input current, 0V ≤ V_{IN} ≤ VDD	-10	10	µA

ABSOLUTE MAXIMUM RATINGS

Max Ratings		Min	Max	Units
V_{DD}	Supply voltage and other 3.3V rated pins as indicated in the Pin Descriptions section, page 24	-0.3	3.6	V
V_{IO}	Voltage applied on GPIO and other digital output pins	-0.3	3.6	V
V_{CORE}	Voltage applied on low-voltage analogue pins and other 1.5 V rated pins as indicated in the Pin Descriptions section, page 24	-0.3	1.8	V
P_{RF-IN}	RX input power		10	dBm
T_J	Operating Junction Temperature Range	-55	125	°C
$T_{STORAGE}$	Storage temperature range	-40	85	°C
$I_{VDD\ MAX}$	Max total continuous supply consumption		120	mA
$V_{ESD-HBM}$	All pins tested according to JESD22-A114 JEDEC Human Body Model JESD22-A114		2k	V
$V_{ESD-CDM}$	All pins tested according to JEDEC Charged Device Model JESD22-C101		500	V
$I_{LatchUp}$	IO pins Latch-Up Test JESD78, current stress		100	mA
$V_{LatchUp}$	Supply pins Latch-Up Test JESD78, voltage stress		5.4	V

NOTES

- Stresses beyond those listed under "Max Ratings" may cause permanent damages to the device.

[1] Refer to document INS12213 "Instruction: 500 Series Integration Guide" for details.

- These are stress ratings only. Functional operation of these devices beyond the ratings stated in the operational sections of the specifications is not implied.
- Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
- TX matching network design will influence $TX_{VRF\ PEAK}$ on TX output pin.
- Caution: ESD-sensitive device

PRODUCTION TEST CONDITIONS

The following conditions apply for the production final test, unless noted otherwise.

1. Ambient temperature T_A = 25°C
2. Supply voltage V_{DD} = 3.3V
3. Crystal frequency = 32MHz
4. TX output power is measured at 900MHz
5. RX sensitivity is measured at 900.2MHz
6. All RF input and output levels referred to the pins of the chip (not the RF module).
7. Conditions include using production test schematic

QUALIFICATION TEST CONDITIONS

The following conditions apply for the qualification test, unless noted otherwise.

1. Ambient temperature T_A = -40 to +90°C
2. Supply voltage V_{DD} = 2.3 to 3.6V
3. Crystal frequency = 32MHz
4. RF performance is measured across the span of Z-Wave frequencies
5. All RF input and output levels refer to the pins of the chip (not the RF module)
6. Conditions include using qualification test schematic
7. Conditions include using Z-Wave qualified RF drivers

OVERVIEW

With the Z-Wave protocol embedded, and a range of manufacturing blueprints of PCB circuitry that achieve proven RF performance at a low BOM, the SD3502 provides a low-effort, low-risk solution for adding reliable and interoperable wireless RF-based communications technology to your product.

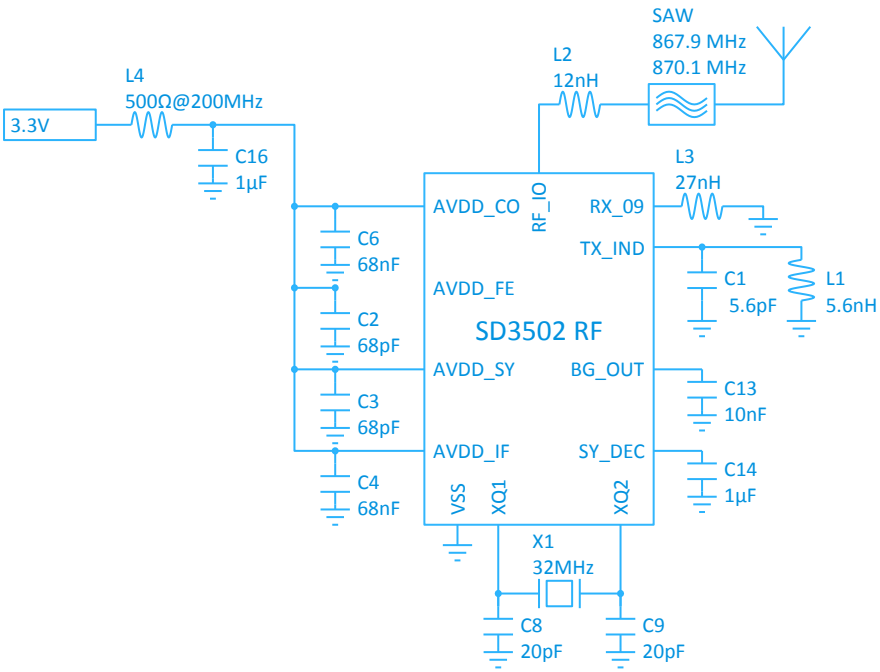


Figure 11 Example Schematic: Z Wave RF supply and EU impedance matching components.

On-chip Flash memory and a rich selection of peripherals help you to further reduce the complexity, cost, and effort of building your product.

WIRELESS TRANSCEIVER

The wireless Transceiver comprises a 3-channel 1GHz ISM FSK narrowband radio covering all currently used and projected Z-Wave frequencies, a modem, and a baseband controller.

This architecture provides an all-digital direct synthesis transmitter and a low-IF digital receiver. The Z-Wave protocol currently utilizes two key FSK/GFSK modulation schemes and 9.6 / 40 / 100 kbit/s data rates throughout a span of carrier frequencies from 865.2 to 926 MHz.

The software-controlled digital radio offers a wide selection of features: One, two, or three channel use, a frequency agility strategy applied to enhance network robustness, and power-saving RSSI usage. Regional enforced listen-before-talk constraints, data rate selection sets, signaling formats, and carrier frequencies can be configured to match the geographical region and product type targeted by your product build. This set of features expands gradually with new Z-Wave software releases to closely match the expanding diversity of products being added to the home control market group. For details, refer to the API documentation for the Z-Wave software applicable for your products.

Seen from an application builder's perspective, the complexity of handling all these features, while ensuring full interoperability with existing products, are conveniently concealed behind the simple interface presented by the Z-Wave API.

INTERFACING THE FRONT-END

The output power of the transmitter covers a range of -21dBm to 5dBm, as set by your application, valid for V_{DD} = 2.3 to 3.6V, T_A = -40 to +90°C. Increased transmit power is easily achieved through the API and HW support for an external PA, or even a complete external front-end (PA, LNA, switch). Request the application note and reference design for further details.

The reference designs include a few external components to optimally match the impedance of the PA (transmitter) and the LNA (receiver) to the 50 Ω antenna to be connected to the single-ended chip pin, "RF_IO" . The SD3502 can be used with various types of antennas. Refer to the document: 'Antennas for Short Range Devices'. Suitable PCB wires often serve directly as the antenna, while helical, whip, and other antenna types are commonly seen where performance is emphasized.

Request manufacturing PCB blueprints for your target region and antenna choice.

Z-WAVE FREQUENCY COVERAGE

Region	Standard	Z-Wave Frequency
Australia	AS/NZS 4268	921.4 MHz
Brazil	ANATEL Resolution 506	921.4 MHz
CEPT[2]	EN 300 220	868.4 MHz
Chile	FCC CFR47 Part 15.249	908.4 MHz
China	CNAS/EN 300 220	868.4 MHz
Hong Kong	HKTA 1035	919.8 MHz
India	N/A	865.2 MHz
Japan 950[3]	ARIB T96	951-956 MHz
Japan 920	ARIB STD-T108	922-926 MHz
Korea		919-923 MHz
Malaysia	SKMM WTS SRD/EN 300 220	868.1 MHz
Mexico	FCC CFR47 Part 15.249	908.4 MHz
New Zealand	AS/NZS 4268	921.4 MHz
Russia	GKRCh/EN 300 220	869.0 MHz
Singapore	TS SRD/EN 300 220	868.4 MHz
South Africa	ICASA/EN 300 220	868.4 MHz
Taiwan	NCC/LP0002	922-926 MHz
UAE	EN 300 220	868.4 MHz
USA/Canada	FCC CFR47 Part 15.249	908.4 MHz

CPU AND MEMORY

The CPU is binary compatible with the industry standard 803x/805x CPU and is operated at 32MHz. Its cycle performance is improved by 6:1 to the standard 8051 implementation.

The CPU processing power is shared between the Z-Wave MAC, higher level protocols, and the user application. An available Z-Wave Developer's Kit contains all the software and detailed documentation necessary to design and write application software

[2] CEPT is the European regional organization dealing with postal and telecommunications issues and presently has 45 Members: Albania, Andorra, Austria, Azerbaijan, Belarus, Belgium, Bosnia and Herzegovina, Bulgaria, Croatia, Cyprus, Czech Republic, Denmark, Estonia, Finland, France, Germany, Greece, Hungary, Iceland, Ireland, Italy, Latvia, Liechtenstein, Lithuania, Luxembourg, Malta, Moldova, Monaco, Netherlands, Norway, Poland, Portugal, Romania, Russian Federation, San Marino, Serbia and Montenegro, Slovakia, Slovenia, Spain, Sweden, Switzerland, The former Yugoslav Republic of Macedonia, Turkey, Ukraine, United Kingdom, and Vatican.

[3] In February 2012, Japanese regulatory body ARIB (Association of Radio Industries and Businesses) released new 920 MHz frequency band for radio equipment, due to LTE rollout.
The 950 MHz frequency band will be obsolete by end of 2015.

on top of the Z-Wave protocol API, and to test and debug the final product. The Keil® µVision4 Integrated Development Environment is fully supported.

MEMORY LAYOUT

Memory is shared between the user application and the Z-Wave stack as depicted in Figure 12. Additional ROM and NVR areas are used for lock bits, calibration data, and USB boot code.

ID	Memory Item	Address method	Exposed via programmer	Description
I1-I4	128 k byte program memory	Program Memory	YES	Flash memory, mapped in 3 banks of 32k-byte slices over a 32k byte common block, one read access per 2 clock cycles.
I5, I6	16 k byte data	XRAM	YES	SRAMs is split into 4k and 12k contiguous blocks
I7	256 byte SRAM	IRAM		Bit addressable SRAM
I8	128 byte SRAM	XRAM		SRAM allows for persistency of data through power-down
I9	256 byte data NVM	(API)		Cached high endurance non-volatile data memory
I10	256 byte data NVM	(API)	YES	Flash area reserved the Z-Wave protocol, calibration data and memory lock bits

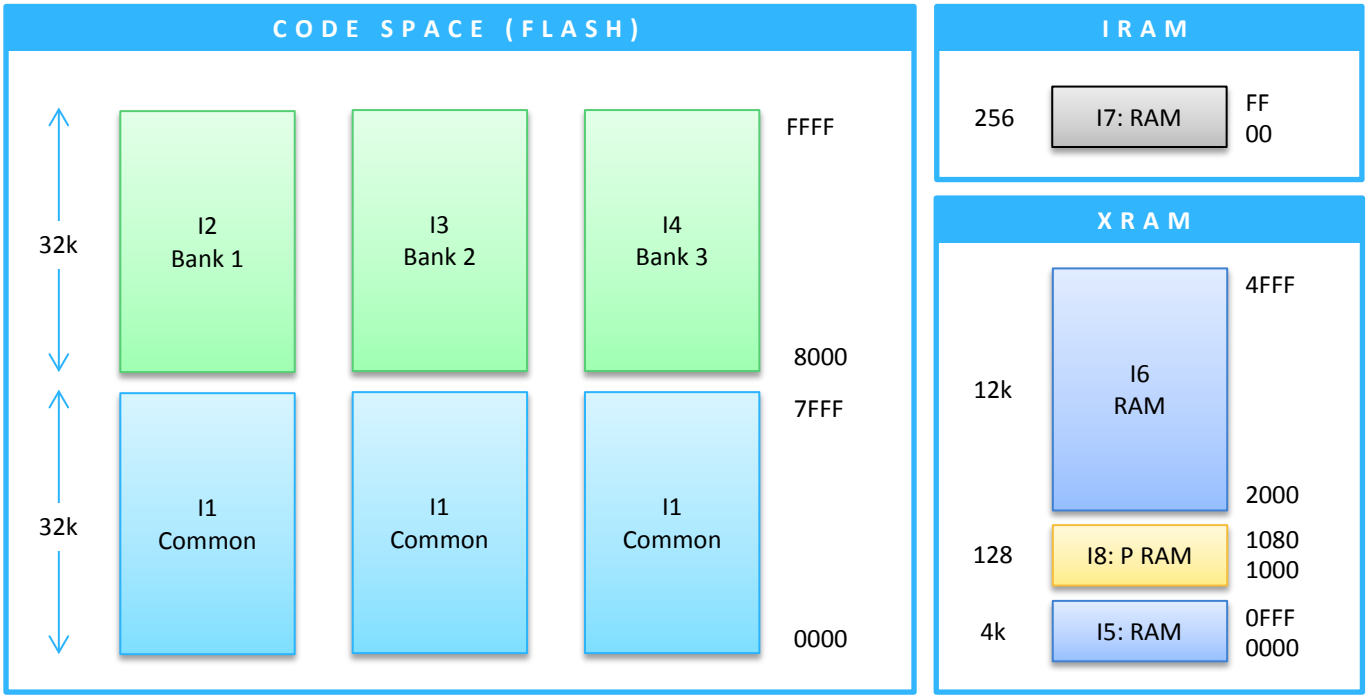


Figure 12 Memory Map, 8 bit words, block sizes indicated on left side, address ranges on right side

MODES

The following modes of operations are supported:

ACTIVE	• Code is executed • Peripherals are available • All I/O's are resistively pulled high • Use a short (up to 4ms) reset-low pulse to enter the reset of active state
SLEEP	• Wake-up timer available • Critical memory retention available • I/O's states according to user configuration • Use API call to enter from ACTIVE mode
PROGRAMMING DURING SUSTAINED RESET	• Used to program the internal FLASH via UART or SPI • Code is not executed • All I/O's are resistively pulled high • Programming requires external control of the RESET pin plus either the UART or the SPI port
APM PROGRAMMING	• Used to program the internal FLASH via USB, UART, or SPI, often initiated from an API call • All I/O's are resistively pulled high • Access to the RESET pin is not required • The chip can be configured to reset into this state either using an API call or instructed via the programming interface.
EXTERNAL NVM PROGRAMMING	• Used to program an external NVM (FLASH/EPROM) (optionally) wired to the SPI port • Code is not executed • All I/O's are resistively pulled high • External NVM programming requires external control of the RESET pin (plus the NVM-SPI port)

PROGRAMMING MODE

The code space and the NVR pages of the flash can be read and programmed through the UART, the SPI, and the USB interface. With proper (optional) Z-Wave software loaded into the Flash, Over-The-Air reprogramming will be available to your application.

ENTERING PROGRAMMING MODE

To enter programming mode, assert the RESET_N pin low for 5.2ms. The chip will then listen on the UART and SPI port for a correct initiating command.

Additionally, an API function is available that configures the chip to enter programming mode after next reset (hardware- or software-initiated). In this state only, the chip begins listening for the initiating string on the USB port as well as on the UART and SPI ports.

PERIPHERALS AND AUXILIARY BLOCKS

The peripherals and auxiliary blocks, other than the Z-Wave radio outlined on page 11, are explained in the following sections.

SUPPLY SYSTEM

The chip is powered from a single 2.3 – 3.6 V supply.

As shown in the schematic in Figure 13, an internal Power-On-Reset circuit guarantees that execution never begins unless the supply voltage is sufficient. The internal Brown-Out-Reset (BOR) circuit guarantees that the chip is always reset before

insufficient voltage levels cause execution to fail. These guarantees apply equally in all active- and power-down modes. Further, there is no restriction on power-up rise time to consider when designing an application.

On-chip supply regulators derive all the 1.5 V and 2.5 V internal supplies needed by MCU core logic, data persistency registers, Flash, and the analogue circuitry. Decoupling capacitors are required as shown in Figure 13.

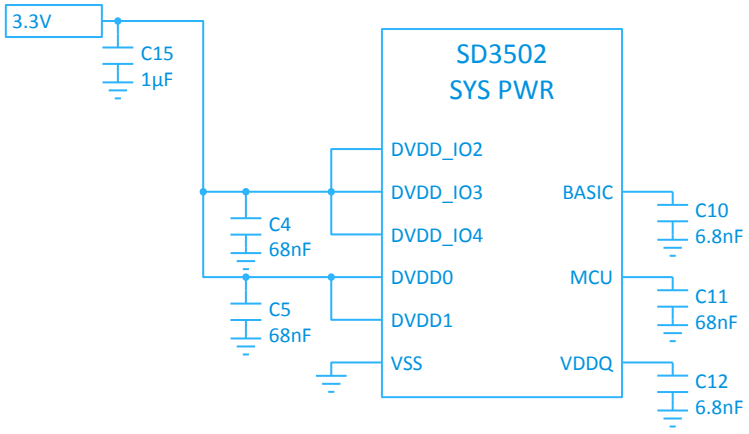


Figure 13: Supply related external components

Note that digital IO circuits are powered unregulated via the supply pins. As a consequence, for the internal USB PHY to be signaling level-compliant when in use, the supply must be set to 3.0 – 3.6 V.

XTAL AND SYSTEM CLOCK

The SD3502 derives RF frequencies and MCU clocks from an external 32MHz crystal (XTAL) as shown in Figure 11 on page 11.

Refer to your crystal component supplier for suitable load capacitance values, or refer to the BOM on our published reference designs.

PRODUCTION CONSIDERATIONS

Silicon Labs specifies application of a reference clock during the system test/calibration step to guarantee initial frequency precision. Request the applicable application note. A built-in frequency calibration circuit compensates for initial crystal frequency offsets of up to ±100 ppm.

The temperature and 5 years aging margin for the 32MHz crystal is 15 ppm.

To ensure frequency shift keying is kept within the 10% accuracy range specified by ITU-T G.9959, the device should be allowed to self-calibrate using a procedure built into all supported programmers.

TIMERS

GENERAL PURPOSE TIMER

This 16 bit General Purpose Timer is an auto-reload interval timer incrementing at 4 MHz or (approx.) 32 kHz, and may be polled or programmed to generate interrupts on wrap around. It also serves as a PWM (Pulse Width Modulating) generator on pin P3.7. High and low periods are set individually using two 8 bit registers.

Using just a few passive external components, a simple low frequency DAC may be built.

8051 LIKE TIMER0/TIMER1

Two 16 bit counters are available for use as interval or event timers, either counting a fixed clock source or counting external events. The full set of classic 8051 T0/T1 features, except the use of external gating signals, is available.

Counter sources:

Timer unit	Interval Counter Source	Event Counter Source
Timer 0	16 MHz	P3.4 (pin 47)
Timer 1	16 MHz	P3.5 (pin 46)

WAKE-UP-TIMER

The max 700nA built-in WUT (Wake Up Timer) plays an important role in maximizing battery life of applications like Frequently Listening Routing Slave (FLIRS) Z-Wave nodes. The WUT is also available to customer applications, and may be programmed to wake a sleeping node after 0 to 256 seconds of sleep. The programming resolution equals 8 bit fractions of 2 seconds, alternatively 8 bit fractions of 256 seconds.

The WUT is autonomously calibrated to the system clock (whenever this is running) and maintains a better than 1% precision.

SFR REGISTERS

Loyal to the 8051 architecture, the built-in peripherals are controlled and monitored via SFR (Special Function Register) circuits. Most of these are conveniently but safely exposed via the API.

INTERRUPT CONTROLLER

The chip supports 15 interrupt sources, including external interrupt sources on the General Purpose I/O port 1 pins 0 and 1.

External interrupts (in ACTIVE mode) is level sensitive high/low per configuration.

The interrupt system is shared between the user application and the Z-Wave software. Priority assignment is preset by the Z-Wave protocol implementation. User application constraints apply.

Vector	Interrupt Name	Priority	Resources served[4]
0	External interrupt 0	1	External interrupt via P1.0/INT0 (pin 18) and via the RESET pin
1	Timer 0	2	Timer 0
2	External interrupt 1	3	External interrupt via P1.1/INT1 (pin 19) or P1.* active low per configuration. Key scanner.
3	Timer 1	4	Timer 1
4	UART	5	UART
5	Multi	6	AES, SPI, and many more reserved resources
6	ZEROX	7	External interrupt via P3.7/ZEROX. Supported by the Dimmer API
7	General Purpose Timer	8	General Purpose Timer
8	ADC	9	Battery monitor, ADC low and high monitor
9	RF	10	RF DMA
10		11	

[4] The Z-Wave API serves additional resources that are not exposed to the user application nor listed in the table. More constraints may apply, based on the library selected for the application.

Vector	Interrupt Name	Priority	Resources served[4]
11	USB	12	USB
12	IR	13	IR API (IR Rx data ready or Tx done)
13		14	
14	NMI	0	Non maskable interrupt for debugger and more

DIMMER

The SD3502 Dimmer allows you to build **LEADING EDGE** or **TRAILING EDGE** dimmers to cover dimming applications with electronic transformers, halogen or incandescent lamps, wire-wound transformers, etc.

The classic **LEADING EDGE** method requires an external TRIAC while the more versatile and electronic transformer friendly **TRAILING EDGE** method requires external FET's or IGBT's.

The Dimmer regulates the power-on duration with a precision of 1000 steps in each 50 Hz or 60 Hz half-period. Once the Dimmer has been initialized, it will run at the requested power setting without any assistance from the MCU.

LEADING EDGE MODE

This is the classic TRIAC mode. Based on the dim-level requested, the Dimmer determines *when* and *how* the power is switched on. To ensure reliable handling in presence of inductive loads, multiple trigger pulses are automatically appended when needed.

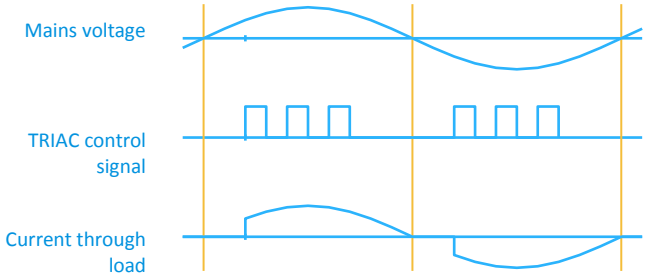


Figure 14: Leading Edge Mode (TRIAC)

TRAILING EDGE MODE

When FET/IGBT Mode is enabled the Dimmer will operate as a Trailing Edge dimmer. This method allows power to grow softly with each voltage zero crossing events. The Dimmer controls the turn-off time (or angle) by switching of the FET/IGBT.

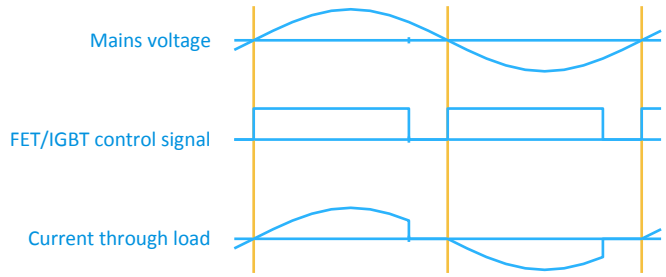


Figure 15: Trailing Edge Mode (FET/IGBT)

ZERO CROSSING SYNCHRONIZATION

The Dimmer detects and synchronizes to the AC voltage via a zero-crossing acquisition signal provided by the dimming application. This signal must be GPIO input level compliant and connects to pin P3.7.

Multiple single and dual event-per-cycle formats are supported, and fixed phase delays and skews are accepted and easily compensated for through the API.

ADC

The ADC samples one of 5 input voltage sources and returns an 8 or 12 bit unsigned fractional representation of the selected input scaled relative to the selected reference voltage, as in the formula:

$$ADC_{OUT} = \frac{V_{IN}}{V_{REF}}, \qquad \text{where } V_{REF} = V_{REF+} - V_{REF-} \text{ and } V_{REF-} \leq V_{IN} \leq V_{REF+}$$

Operation is rail to rail as indicated in the formula.

The following input configurations apply (V_{BG} = built-in Band-gap 1.25V, V_{DD}= supply voltage, P3.*n*= GPIO port 3 pin *n*):

Configuration Options		Physical pin, configuration options
V_{IN}	The value being converted	P3.7, P3.6, P3.5, P3.4, V_{BG}
V_{REF+}	The positive node of the reference voltage	P3.7, V_{BG}, V_{DD}. Constraints on P3.7 apply; refer to section ADC Characteristics on page 9.
V_{REF-}	The negative node of the reference voltage	P3.6, GND. Constraints on P3.6 apply; refer to section ADC Characteristics on page 9.

The sample rate versus accuracy tradeoff options (in continuous mode) are:

- 20 kHz 8 bit mode
- 10 kHz 12 bit mode

The ADC raises an interrupt if a lower or an upper warning threshold is exceeded by the converter. Setting V_{IN} = V_{BG} and V_{RFE+} = V_{DD} implements a battery monitor.

All inputs (V_{IN}, V_{REF+}, V_{REF-}) must be driven by low impedance voltage sources, preferably not exceeding 200Ω, to accurately handle the load current of the ADC input pins. Select R_{OUT} so that $log_2(8\mu A \cdot R_{OUT}/V_{REF})$ is not less than the number of significant bits required.

SPI

A Serial Peripheral Interface (SPI) is available on port 2 pins 2-4. The SPI enables synchronous data transfers between this and other SPI devices.

Pin	SPI Pin	SPI Function, master	SPI Function, slave
P2.2	MOSI	Data output	Data input
P2.3	MISO	Data input	Data output
P2.4	SCK	Clock output	Clock input

During data transmission, the SCK pin act as a clock. 8 bit of data will be exchanged between the two devices after 8 cycles of SCK as shown in Figure 16.

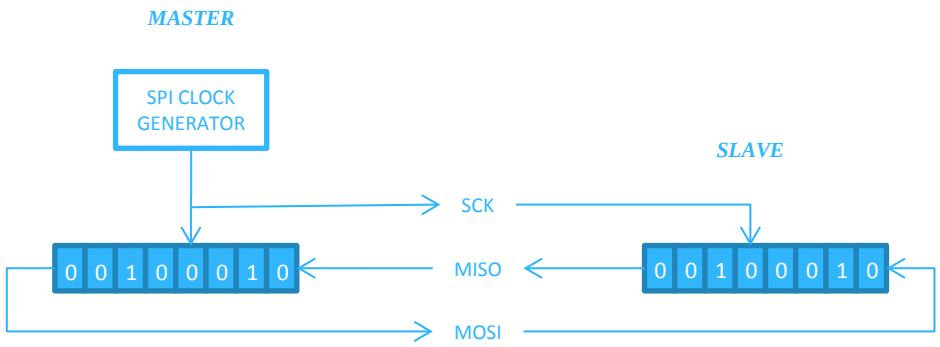


Figure 16 Flow of data between master and slave when correctly connected

The chip operates as a SPI master when controlling an external EEPROM and likewise. An EEPROM enable (Slave Select) pin may be driven by an available GPIO pin.

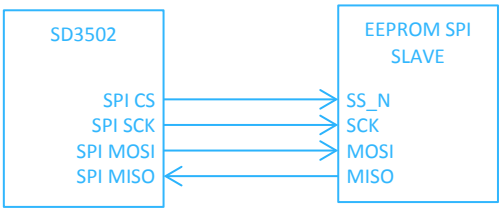


Figure 17: Typical interface to EEPROM

The chip operates as a SPI slave when being programmed or controlled from an externally device.

UART

The chip has a full duplex 9.6 to 230.4 kbit/s UART hardware block operating independently of the CPU (and not using timer resources as in the classic 8051 MCU).

The UART interface is available on P2.0 and P2.1. Figure 18 shows a typical RS232 UART application.

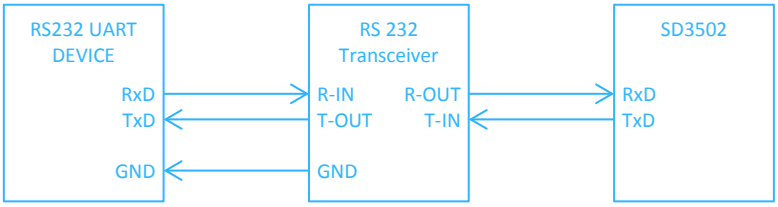


Figure 18: UART application example

The UART shifts data in/out in the following order: start bit, data bits (LSB first) and stop bit. Figure 19 gives the waveform of a serial byte.

Figure 19 UART waveform

It is possible to program the device using the USB interface.

USB

The built-in USB2.0 device controller and PHY support 12Mbit/s. Three resistors should be inserted between the USB connector and the chip as shown in Figure 20.

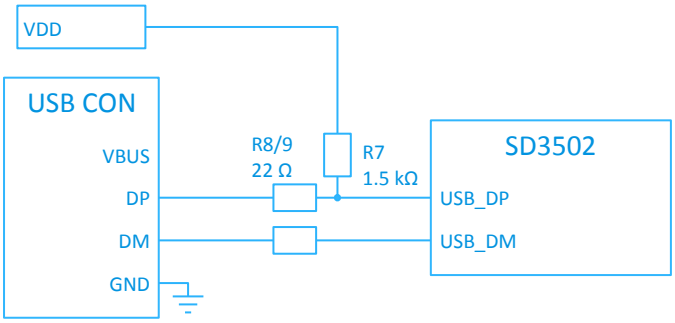


Figure 20: USB interface

The USB controller implements an interface with two CDC/ACM compliant ports, and can be setup to use the built-in drivers of Windows etc. It supports a custom USB string for helping the driver doing predictable identification. Setup and enumeration is handled in hardware, and data access is sent to predefined memory buffers in the 4K SRAM using DMA. The data is CRC protected, and automatically retransmitted on error, buffer full etc.

It is possible to program the device using the USB interface.

USB-BUS-POWERED AND SUSPEND-MODE SUPPORT

The USB controller supports suspend mode and remote wakeup. The XTAL remains powered and the CPU may continue to run during suspend at a reduced clock frequency.

The USB 2.0 spec allows connected devices to be powered via the USB. Devices are each allowed a minimum of 100mA during non-suspend periods, and 2.5mA (average) (after proper enumeration) during suspend periods. The USB 2.0 supply ranges from 4.4 V to 5.25 V. This allows SD3502 based systems to be entirely powered by the USB using simple linear regulators. The power budget margin even allows such systems to resume full Z-Wave network presence on a frequent basis even when placed in USB suspend state.

IR CONTROLLER

The IR Controller is a DMA enabled peripheral that implements a transmitter and a learning functionality at minimal MCU load.

A rich set of functions is exposed through the API. This simplifies the task of writing applications that detects and generates most of the IR coding formats used in existing AV equipment.

IR TRANSMITTER

As an IR Transmitter, the controller generates and streams a data modulated carrier via a GPIO port to an external IR LED driver, or via up to 3 GPIO's (16mA/pin) directly to an IR LED unit.

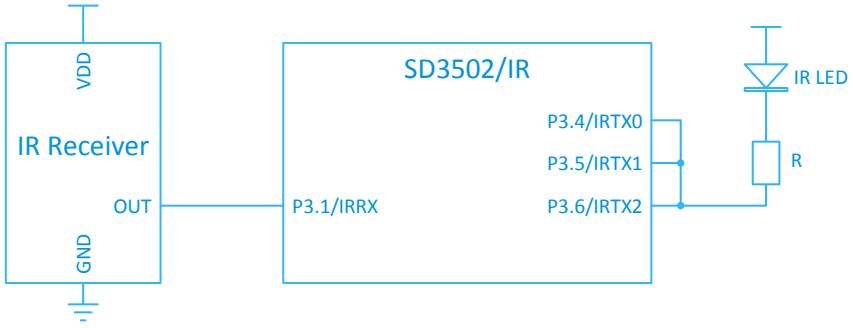


Figure 21: SD3502 with IR transmitter and receiver devices

Data is kept in a compact pre-scaled format and fetched from SRAM using DMA.

IR RECEIVE/LEARN

The controller listens via GPIO port P3.1 for signals received via an external IR Receiver device or circuit as shown in Figure 21. The status is made available to the application via polling and via the interrupt system.

Incoming pre-scaled 'base-band' data is streamed into SRAM using DMA, and the carrier properties will be acquired in IR Learn Mode.

LED CONTROLLER

A 4 channel PWM generator is fitted on GPIO port 0 pins 4 to 7. This hardware setup makes it easy to enable control and dimming of your 4 channels current controlled LED supply via any Z-Wave home control network. Basic operation as well as detailed fine tuning is available via the API.

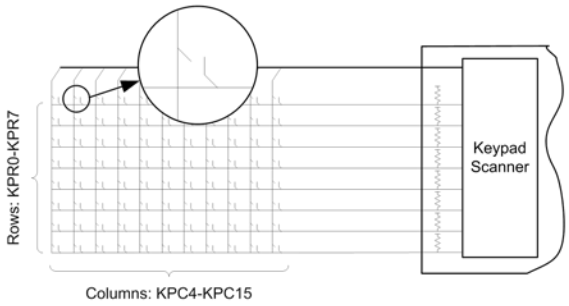
Parameter	Value	Description
Pulse width resolution	16 bit	
Frequency	488 Hz	
No Channels	1-4	
Pulse turn-on placement method	Normal mode	All pulses start at the beginning of the period.
	Skewed mode	Channels are started individually. Delay between starts equals 25% of a period.
Pins	Port 0 pins 4-7	5 volt compliant 16mA GPIO drivers

KEYPAD SCANNER

The chip includes a key scanner to service up to 88 keys. 11 GPIO outputs and 8 GPIO inputs provide all the pull-up resistors and Schmitt trigger inputs required by the full setup.

Parameter	Value/Description
Key array size	8 rows by 11 columns.
Number of concurrent key press detections	Min 2, up to 8.

Hardware setup	8 horizontal wires are resistively pulled high by 8 GPIO inputs. 11 vertical wires are set by 11 GPIO's as driven-low or resistively-pulled-high. A pressed key at a wire intersection will shorten the wires thus forming a signal path from a driver to an input.
Detection method	A '0' forced by an output GPIO will propagate to input pins via intersection points being shorted by a key being pressed. Frequently scheduled walking-zero output patterns allows the hardware to scan the state of all keys. Detected activity will be latched and an interrupt generated.
Interrupts	Key press and key release events each cause a notification through the interrupt system.
De-bounce filtering	The scanner discards glitches and rapid key state transitions. Glitch black-out and minimum key press duration thresholds are configured through the API in 2ms steps.
Wake-up	The scanner can be configured to wake up the chip in sleep mode following any key press. Enabling this feature will not increase the power consumption in sleep mode.



AES SECURITY PROCESSOR

The Z-Wave protocol specifies the use of AES 128-bit block encryption in secured applications.

The built-in Security Processor is a hardware accelerator that encrypts and decrypts data at a rate of 1 byte per 1.5µs. It encodes the frame payload and the message authentication code to ensure privacy, integrity, and authenticity on messages.

The processor supports OFB, CBC (and ECB) modes to target variable length messages. Payload data is streamed in OFB mode, and authentication data is processed in CBC mode as required by the Z-Wave protocol.

The processor implements two efficient access methods: DMA and streaming through SFR ports. The processor is exposed via the API for additional custom use.

GPIO INTERFACES

The SD3502 has 23 configurable General Purpose I/O (GPIO) pins grouped as four ports. Many functions are mapped into these groups. All ports have a drive capability of at least 8 mA, inputs featuring Schmitt trigger feedbacks, and an internal pull-up that can be disabled via software when preferred.

General GPIO property	Value/Description
Total count	23
Configurability	1. CMOS output, min 8mA drive capability 2. Schmitt trigger input with internal pull-up resistor 3. Schmitt trigger input with no pull-up
State after RESET	Schmitt trigger input with internal pull-up resistor
State after wake-up	State is preserved.
Wake-up	The Key-scanner peripheral can be configured to wake up the chip in sleep mode by any key press. Enabling this feature will not increase the power consumption in sleep mode.

8051 GPIO pin locations

GPIO	Pin Names	Package Pin	Description
Port 0	P0.4-7	14, 15, 16, 17	8051 GPIO port # 0, 4 bits
Port 1	P1.0-7	18, 19, 20, 21, 22, 23, 24, 25	8051 GPIO port # 1, 8 bits
Port 2	P2.0-5	31, 30, 29, 28, 27, 26	8051 GPIO port # 2, 6 bits
Port 3	P3.1, P3.4-7	48, 47, 46, 45, 44	8051 GPIO port # 3, 5 bits

Other functions mapped onto the GPIO pins

Mapped Function	Pin Names	Package Pin	Description
SPI	SCK MISO MOSI	27, 28, 29	
UART	TXD RXD	30, 31	
DIMMER	TRIAC ZEROX	45, 44	TRIAC/FET output, Phase detector input
Key scanner	KS_ROW0-7	18, 19, 20, 21, 22, 23, 24, 25	Inputs with pull-up
	KS_COL4-7	14, 15, 16, 17	Drivers for walking-zero scan
	KS_COL8-12	44, 45, 46, 47, 48	
	KS_COL14-15	30, 31	
IR	IRRX IRTX0-2	48, 47, 46, 45	IR receiver input, IR driver (3 pins) output
LED	LED0-3	14, 15, 16, 17	PWM output, 4 channels
ADC	ADC0-3	47, 46, 45, 44	Analogue inputs
External Interrupts	INT0 INT1	18, 19	These pins may be configured to request an interrupt when the system is running, and a wake-up reset when the system is in power down mode.
General Purpose PWM	PWM	44	General Purpose PWM output
T0/T1 Counter	T0_EXT_CLK T1_EXT_CLK	47, 46	Counter inputs to Timer0 and Timer 1

RESET

A RESET causes the MCU to be powered, clocked, initialized, and started.

The delay associated with a RESET is less than 1 ms using any of our reference designs, and is mostly spent on charging the supply capacitances (internal as well as external) and bringing the XTAL clock into a stable and confirmed oscillation.

Multiple events may cause a reset of the chip. The actual cause is latched by hardware and may be retrieved via SW when the system resumes operation. The table lists the supported reset methods.

Some reset methods deliberately leaves the state of GPIO pins untouched. Other GPIO pins are reset to its input state with pull-up activated.

Reset Cause	Description	Effect on GPIO state	May be masked
POR	Reset request generated by Power-On-Reset hardware	Reset	NO
BOR	Reset request generated by Brown-Out-Reset hardware	Reset	NO
RESET_N	Reset request generated by the RESET_N pin being de-asserted	Reset	NO
WUT	Reset request generated by the Wake-Up-Timer timing out	Untouched	YES
WATCHDOG	Reset request generated by the WATCHDOG Timer timing out	Reset	YES
INT1	Reset request generated when a signal is	Reset	YES

Reset Cause	Description	Effect on GPIO state	May be masked
	received on pin INT1, when the chip is in power down mode. INT1 is a dual function of GPIO P1.1		
Software	Reset by software	Untouched	YES
Key pad scanner	Reset request generated when any of the KS_ROW pins are being held low, and the chip is in power down mode. This happens when a key is pressed.	Reset	YES

PIN DESCRIPTIONS

No	Name	Type	Description
pin 1	XOSC_Q1	1.5V analogue	Clock Oscillator (input)
pin 2	XOSC_Q2	1.5V analogue	Clock Oscillator (output)
pin 3	AVDD_AC	3.3V supply input	Power for Analog core
pin 4	AVDD_FE	3.3V supply input	Power for RF front end
pin 5	TX_IND	1.5V RF analogue	RF Tx inductor
pin 6	RF_IO	1.5V RF analogue	RF IO
pin 7	RX_09	1.5V RF analogue	RF RX 900MHz inductor
pin 8	N.A.		Not connected
pin 9	AVDD_SY	3.3V supply input	Power for synthesizer and bandgap
pin 10	SY_DECOUP	1.5V RF analogue	Synthesizer Decoupling capacitor
pin 11	BG_OUT	1.5V analogue	Bandgap voltage OUT
Pin 12	NC		Not connected
pin 13	AVDD_IF	3.3V supply input	Power for analog IF
pin 14	P0_4	3.3 V Digital IO	GPIO 0.4 / KS COL4 / PWM LED0
pin 15	P0_5	3.3 V Digital IO	GPIO 0.5 / KS COL5 / PWM LED1
pin 16	P0_6	3.3 V Digital IO	GPIO 0.6 / KS COL6 / PWM LED2
pin 17	P0_7	3.3 V Digital IO	GPIO 0.7 / KS COL7 / PWM LED3
pin 18	P1_0	3.3 V Digital IO	GPIO 1.0 / INT1 / INT0 / KS ROW0 / PWM
pin 19	P1_1	3.3 V Digital IO	GPIO 1.1 / INT1 / KS ROW1
pin 20	P1_2	3.3 V Digital IO	GPIO 1.2 / INT1 / KS ROW2
pin 21	P1_3	3.3 V Digital IO	GPIO 1.3 / INT1 / KS ROW3
pin 22	P1_4	3.3 V Digital IO	GPIO 1.4 / INT1 / KS ROW4
pin 23	P1_5	3.3 V Digital IO	GPIO 1.5 / INT1 / KS ROW5
pin 24	P1_6	3.3 V Digital IO	GPIO 1.6 / INT1 / KS ROW6
pin 25	P1_7	3.3 V Digital IO	GPIO 1.7 / INT1 / KS ROW7
pin 26	P2_5	3.3 V Digital IO	GPIO 2.5
pin 27	P2_4	3.3 V Digital IO	GPIO 2.4 / SPI SCK / pgm interface[5]
pin 28	P2_3	3.3 V Digital IO	GPIO 2.3 / SPI MISO / pgm interface
pin 29	P2_2	3.3 V Digital IO	GPIO 2.2 / SPI MOSI / pgm interface
pin 30	P2_1	3.3 V Digital IO	GPIO 2.1 / KS COL14 / UART TX / pgm interface
pin 31	P2_0	3.3 V Digital IO	GPIO 2.0 / KS COL15 / UART RX / pgm interface
pin 32	RESET_N	3.3 V CMOS Input	System reset / pgm interface
pin 33	N.A.	IO	Reserved pin for test purposes. Do not connect!
pin 34	DVDD_IO	3.3 V supply input	Digital IO power
pin 35	DVDD_IO	3.3 V supply input	Digital IO power
pin 36	VDDQ	2.5 V	Power for Flash (output of charge pump)
pin 37	USB_DM	3.3 V USB 2.0 PHY	USB negative diff IO
pin 38	USB_DP	3.3 V USB 2.0 PHY	USB positive diff IO

[5] The pins marked "/ pgm interface" constitute the programming and debugging interface. This interface must be exposed to the programmer if In-System Programming is required. Please refer to INS12213 Instruction: 500 Series Integration Guide.

No	Name	Type	Description
pin 39	DVDD_IO	3.3 V supply input	Digital IO power / pgm interface
pin 40	DVDD	3.3 V supply input	Digital domain power
pin 41	DVDD	3.3 V supply input	Digital domain power
pin 42	MCU	1.5 V	Internal Power 1.5V (MCU)
pin 43	BASIC	1.5 V	Internal Power 1.5V (BASIC)
pin 44	P3_7	3.3 V Digital IO	GPIO 3.7 / ADC3 / KS COL08 / ZEROX / PWM
pin 45	P3_6	3.3 V Digital IO	GPIO 3.6 / ADC2 / KS COL09 / IR TX2 / TRIAC
pin 46	P3_5	3.3 V Digital IO	GPIO 3.5 / T1 EXT CLK / ADC1 / KS COL10 / IR TX1 / UART0 TX
pin 47	P3_4	3.3 V Digital IO	GPIO 3.4 / T0 EXT CLK / ADC0 / KS COL11 / IR TX0
pin 48	P3_1	3.3 V Digital IO	GPIO 3.1 / KS COL12 / IR RX
Exposed pad	GND	Ground	GND / pgm interface

PROCESS SPECIFICATION

Specification	Description
MSL 3	Moisture Sensitivity Level tested according to JEDEC J-STD-020C
REACH	REACH is a European Community Regulation on chemicals and their safe use (EC 1907/2006). It deals with the Registration, Evaluation, Authorisation and Restriction of Chemical substances
RoHS	Designed in compliance with The Restriction of Hazardous Substances Directive (RoHS)

PCB MOUNTING AND SOLDERING

RECOMMENDED PCB MOUNTING PATTERN

Please follow standard QFN mounting pattern.

SOLDERING INFORMATION

The soldering details to properly solder the SD3502 module on standard PCBs are described below. The information provided is intended only as a guideline and Silicon Labs is not liable if a selected profile does not work.

See IPC/JEDEC J-STD-020D.1 for more information.

PCB solder mask expansion from landing pad edge	0.1 mm
PCB paste mask expansion from landing pad edge	0.0 mm
PCB process	Pb-free (Lead free for RoHS [6]compliance)
PCB finish	Defined by the manufacturing facility (EMS) or customer
Stencil aperture	Defined by the manufacturing facility (EMS) or customer
Stencil thickness	Defined by the manufacturing facility (EMS) or customer
Solder paste used	Defined by the manufacturing facility (EMS) or customer
Flux cleaning process	Defined by the manufacturing facility (EMS) or customer

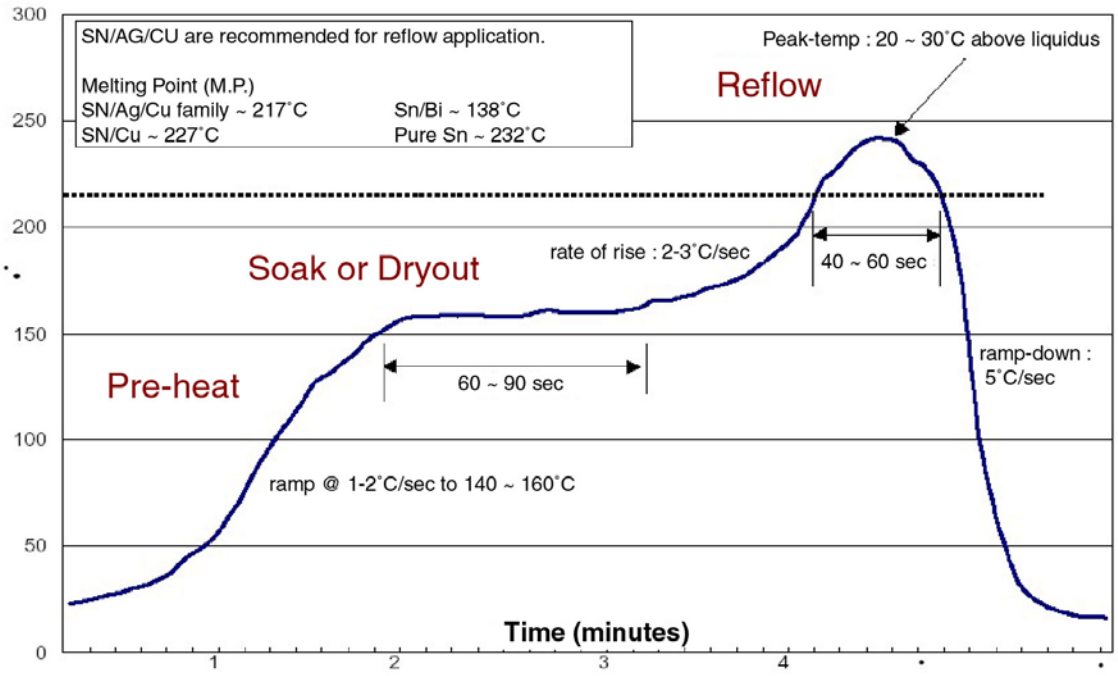


Figure 22 Recommended Reflow Temperature Profile

ORDERING INFORMATION

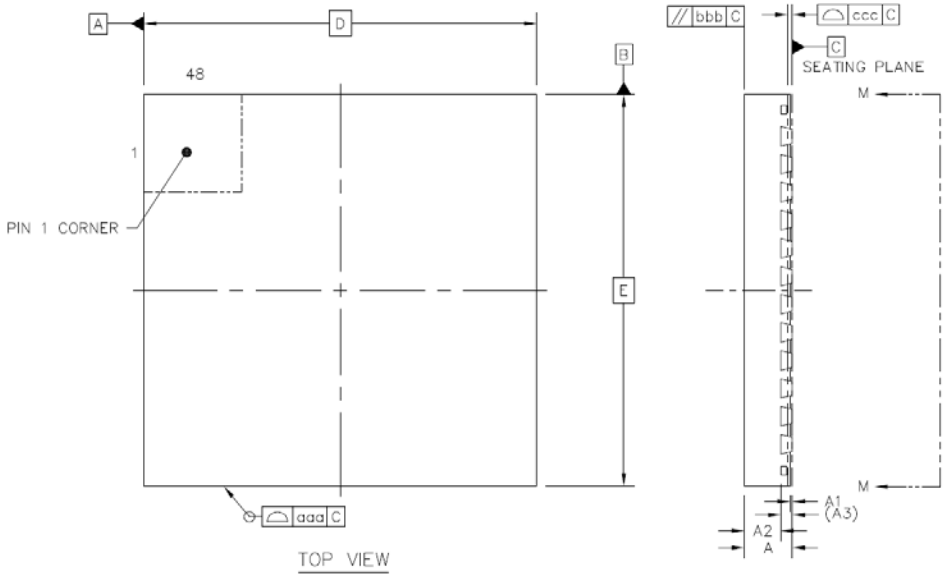
Part Number	Product Description
SD3502A-CNE3R	2000 pcs QFN 48 pins 7x7 mm on reel

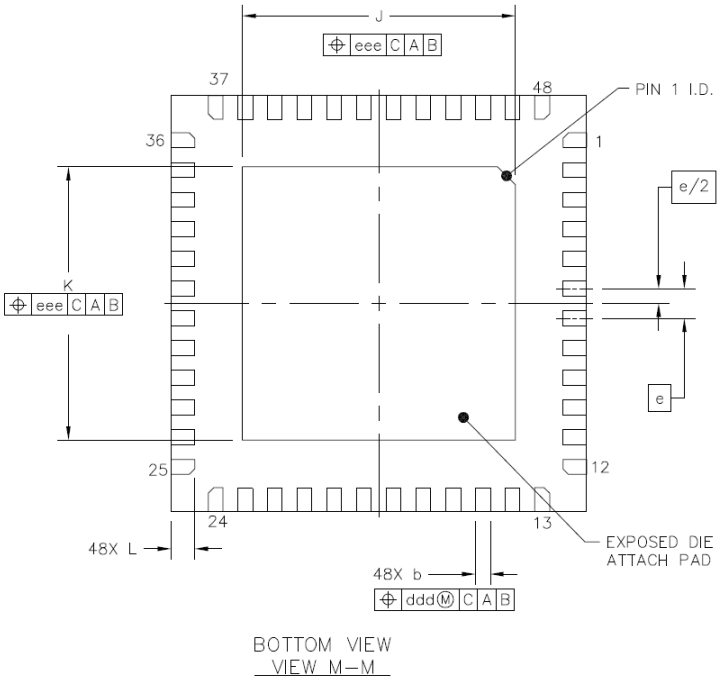
PACKAGE

QFN 48 PINS 7X7 MM

Caution: Moisture sensitive device MSL-3 defined by IPC/JEDEC J-STD-020. May require bake before mounting after bag is opened.

[6] RoHS = Restriction of Hazardous Substances Directive, EU

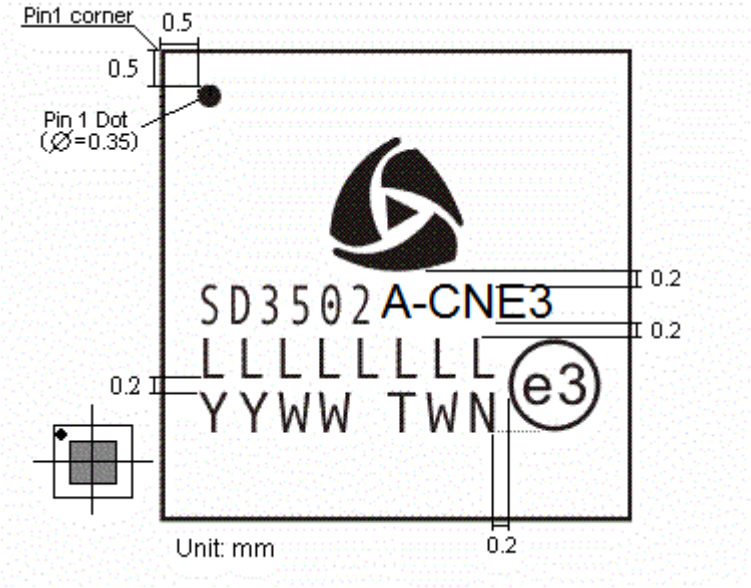




	Symbol	Min	Nom	Max
Total thickness	A	0.8	0.85	0.9
Stand off	A1	0	0.035	0.05
Mold thickness	A2	---	0.65	0.67
L/F thickness	A3		0.203 REF	
Leak width	b	0.2	0.25	0.3
Body size	D (x)		7 BSC	
	E (y)		7 BSC	
Lead pitch	e		0.5 BSC	
EP size	J (x)	4.5	4.6	4.7
	K (y)	4.5	4.6	4.7
Lead length	L	0.35	0.4	0.45
Package edge tolerance	aaa		0.1	
Mold flatness	bbb		0.1	

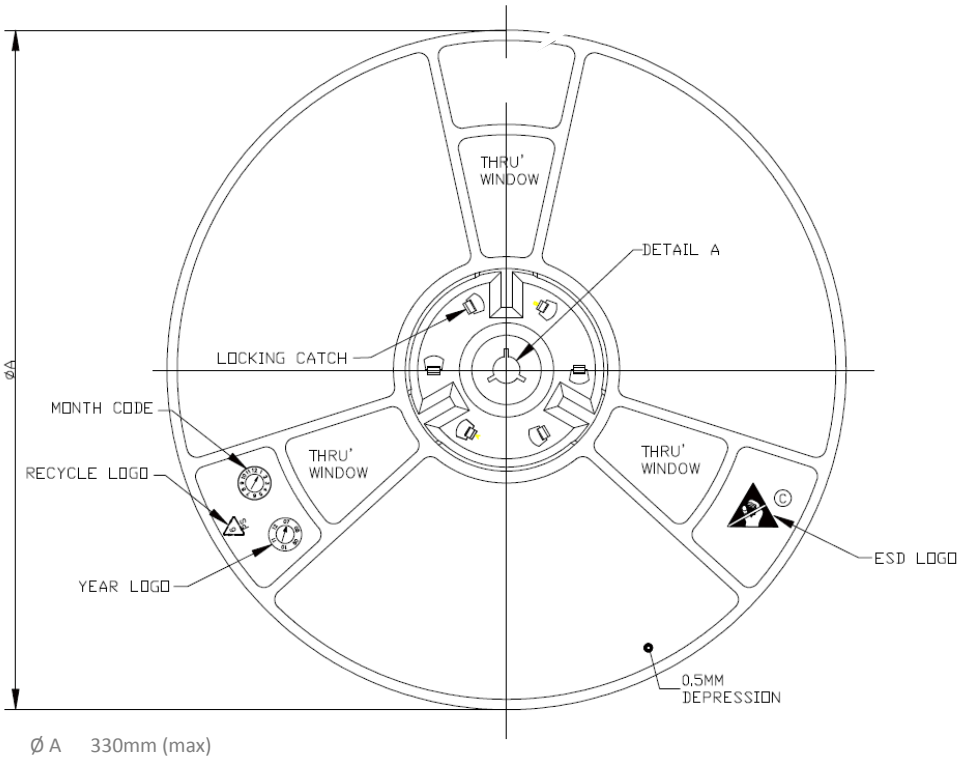
	Symbol	Min	Nom	Max
Co-planarity	ccc		0.08	
Lead offset	ddd		0.1	
Exposed pad offset	eee		0.1	

TOP MARKING



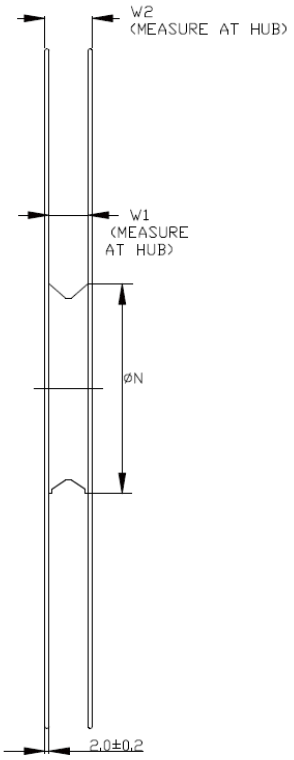
Marking	Meaning
SD3502	Product Number
A	Product revision
C	Commercial temperature range
N	QFN package
E3	Green BOM
LLLL…	Wafer lot
YYWW TWN	YY [year]
	WW [week]
	TWN [Country of Origin]

REEL



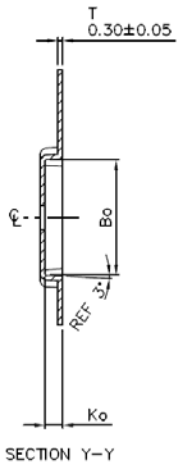
Ø A 330mm (max)

FRONT VIEW

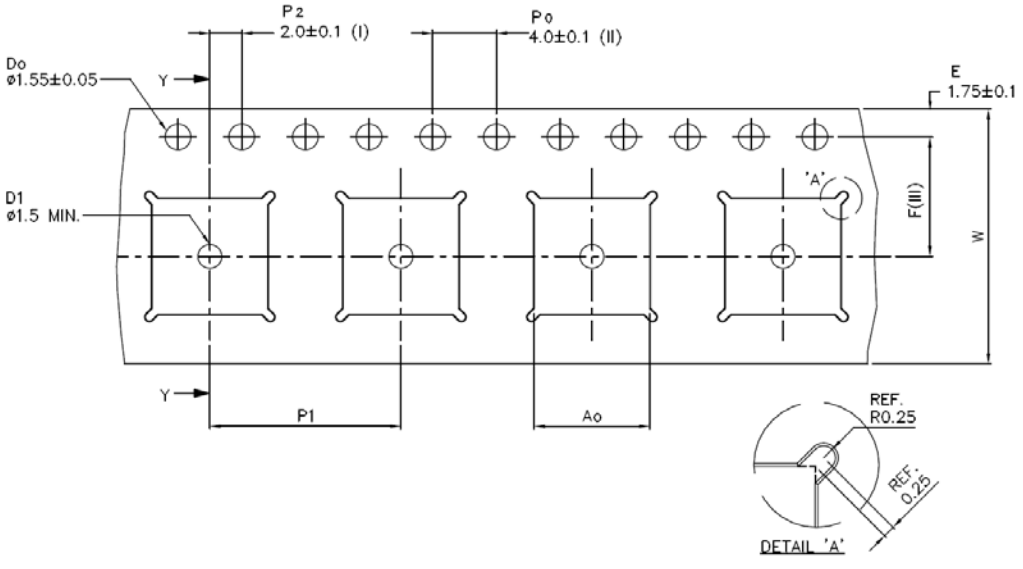


SIDE VIEW

W116.4mm – 16.6mm
W222.4mm (max)
Ø N 100mm (min)



SECTION Y-Y

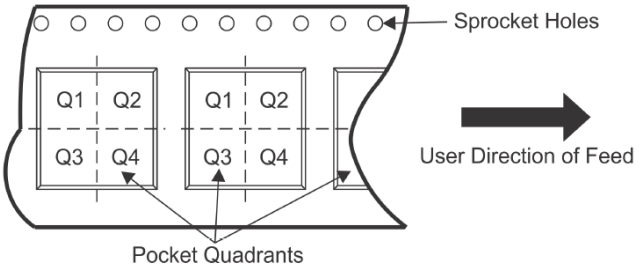


Ao	7.25 +/−0.1
Bo	7.25 +/−0.1
Ko	1.10 +/−0.1
F	7.50 +/−0.1
P1	12.00 +/−0.1
W	16.00 +0.3/−0.0

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

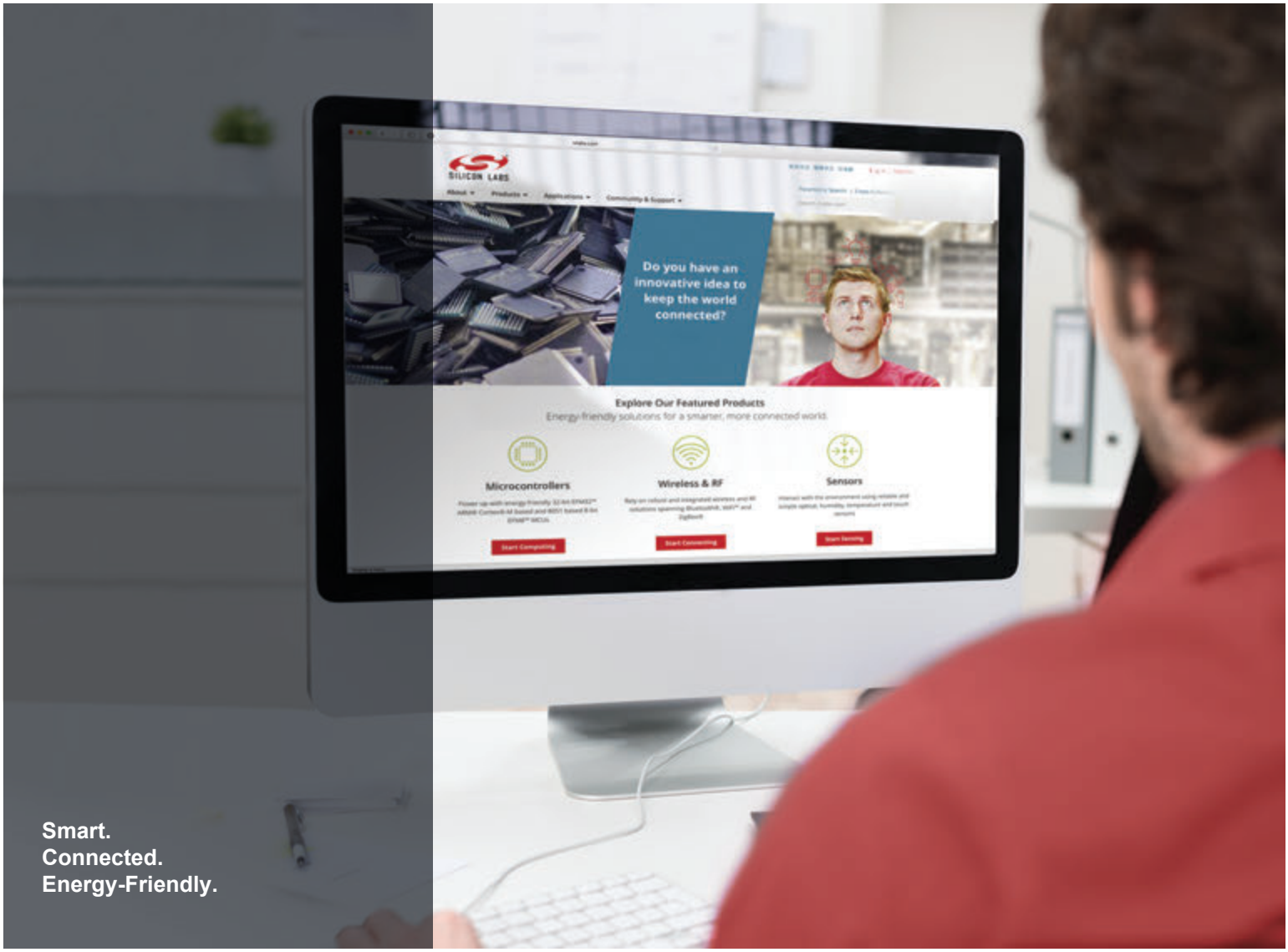
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Parameter	Value
Pin 1 Quadrant	Pocket Quadrant Q1

DOCUMENT CHANGE LIST

Version	Date	By	Pages affected	Description of changes
1	2013-02-19	PNI	All	Initial draft
2	2013-05-13	PNI	7	Sensitivity versus Temperature graph added
3	2013-05-14	PNI	7	Added typical current consumption versus TX power
4	2013-05-17	PNI	All	Edits from technical writer committed
5	2013-05-31	PNI	8-9	Section “DIGITAL IO CHARACTERISTICS“ updated. New values on schematics
5	2013-06-03	PNI	2,13,10	Figure 1, figure 10 text, use of units in table Part no changed
6	2013-08-16	PNI	26-29	Ordering info changed to reel, reel drawing added
7	2013-09-13	PNI	25	Pin list type designations changed in VDDA
8	2013-09-30	Pni	10,15,17-20,23	Pull up graph added, CPU Modes added, interrupt controller and ADC descriptions extended
9	2013-11-29	PNI	7	Added typical blocking versus bit rate
10	2013-11-12	PNI	13-14	Operating modes section updated
11	2014-03-11	PNI	25	P/N now appended with an R (to emphasize the Reel packaging)
12	2014-04-22	PNI	9, 24-25	Storage temperature added, programming pin notifications, MSL3 specified
12	2014-04-28	PNI	12	Table “Z WAVE FREQUENCY COVERAGE” updated
12	2014-06-18	PNI	5	FLIRS power consumption updated
13	2015-03-27	MHANSEN	25	Added section PCB mounting and soldering
			25	Added section Process Specification
			30	Added orientation of component in tape



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