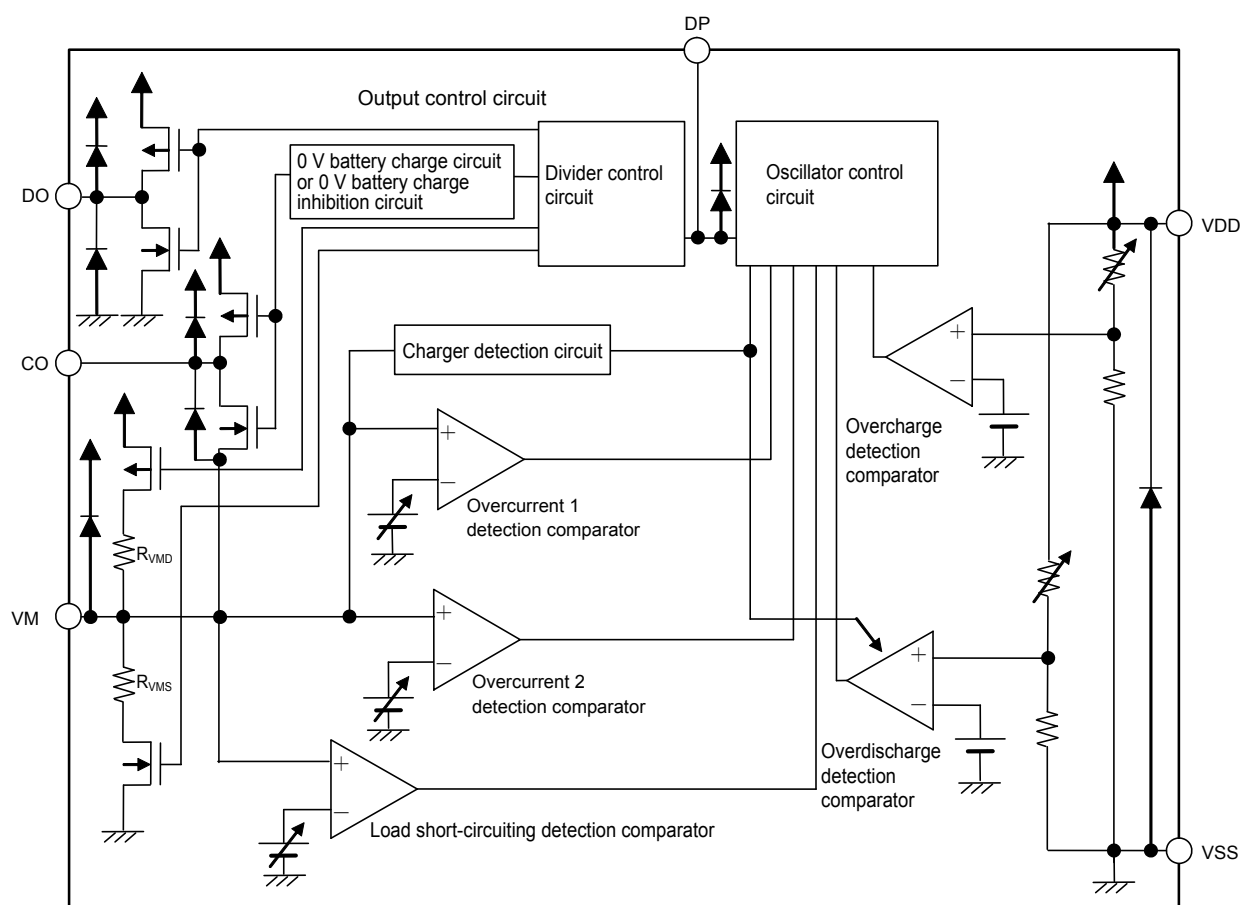


■ **Block Diagram**

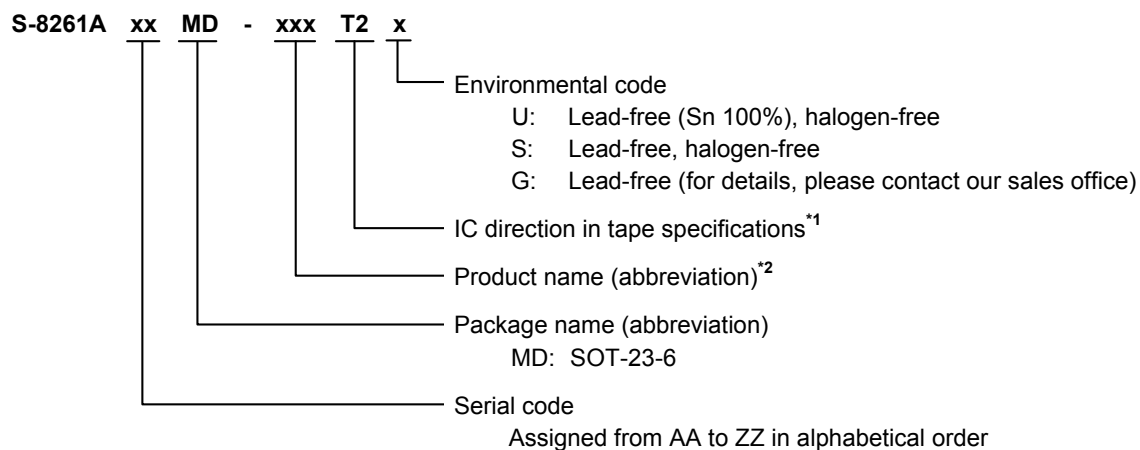


Remark All the diodes shown in the figure are parasitic diodes.

Figure 1

■ Product Name Structure

1. Product Name



*1. Refer to the tape drawing.

*2. Refer to "3. Product Name List".

2. Package

Package name	Drawing code		
	Package	Tape	Reel
SOT-23-6	MP006-A-P-SD	MP006-A-C-SD	MP006-A-R-SD

3. Product Name List

Table 1 (1 / 2)

Product name	Overcharge detection voltage [V _{CU}]	Overcharge hysteresis voltage [V _{HC}]	Overdischarge detection voltage [V _{DL}]	Overdischarge hysteresis voltage [V _{HD}]	Overcurrent 1 detection voltage [V _{IOV1}]	0 V battery charge function	Delay time combination ^{*1}	Power-down function
S-8261AAGMD-G2GT2x	4.280 V	0.20 V	2.300 V	0 V	0.160 V	Available	(1)	Yes
S-8261AAHMD-G2HT2x	4.280 V	0.20 V	2.300 V	0 V	0.080 V	Available	(1)	Yes
S-8261AAJMD-G2JT2x	4.325 V	0.25 V	2.500 V	0.4 V	0.150 V	Unavailable	(1)	Yes
S-8261AALMD-G2LT2x	4.300 V	0.10 V	2.300 V	0 V	0.080 V	Unavailable	(1)	Yes
S-8261AAMMD-G2MT2x	4.300 V	0.10 V	2.300 V	0 V	0.200 V	Unavailable	(1)	Yes
S-8261AANMD-G2NT2x	4.275 V	0.10 V	2.300 V	0.1 V	0.100 V	Available	(1)	Yes
S-8261AAOMD-G2OT2x	4.280 V	0.20 V	2.300 V	0 V	0.130 V	Unavailable	(1)	Yes
S-8261AAPMD-G2PT2x	4.325 V	0.25 V	2.500 V	0.4 V	0.100 V	Unavailable	(1)	Yes
S-8261AARMMD-G2RT2x	4.280 V	0.20 V	2.300 V	0 V	0.100 V	Available	(1)	Yes
S-8261AASMD-G2ST2x	4.280 V	0.20 V	2.300 V	0 V	0.150 V	Unavailable	(2)	Yes
S-8261AATMD-G2TT2x	4.300 V	0.10 V	2.300 V	0 V	0.080 V	Available	(3)	Yes
S-8261AAUMD-G2UT2x	4.275 V	0.10 V	2.300 V	0.1 V	0.100 V	Available	(4)	Yes
S-8261AAXMD-G2XT2x	4.350 V	0.10 V	2.300 V	0.1 V	0.100 V	Available	(4)	Yes
S-8261AAZMD-G2ZT2x	4.280 V	0.25 V	2.500 V	0.4 V	0.100 V	Unavailable	(1)	Yes
S-8261ABAMD-G3AT2x	4.350 V	0.20 V	2.500 V	0 V	0.200 V	Available	(4)	Yes
S-8261ABBMD-G3BT2x	4.275 V	0.20 V	2.300 V	0 V	0.130 V	Available	(1)	Yes
S-8261ABCMD-G3CT2x	4.300 V	0.20 V	2.300 V	0 V	0.130 V	Available	(1)	Yes
S-8261ABIMD-G3IT2x	4.275 V	0.20 V	2.300 V	0 V	0.200 V	Unavailable	(5)	Yes
S-8261ABJMD-G3JT2x	4.280 V	0.20 V	3.000 V	0 V	0.080 V	Available	(1)	Yes
S-8261ABKMD-G3KT2x	4.100 V	0.25 V	2.500 V	0.4 V	0.150 V	Unavailable	(1)	Yes
S-8261ABLMD-G3LT2x	4.275 V	0.20 V	2.300 V	0 V	0.050 V	Unavailable	(5)	Yes
S-8261ABMMD-G3MT2x	4.280 V	0.20 V	2.800 V	0 V	0.100 V	Available	(1)	Yes
S-8261ABNMD-G3NT2x	4.300 V	0.20 V	2.300 V	0 V	0.060 V	Available	(1)	Yes
S-8261ABPMD-G3PT2x	4.200 V	0.10 V	2.800 V	0.1 V	0.150 V	Unavailable	(1)	Yes
S-8261ABRMD-G3RT2x	4.275 V	0.20 V	2.500 V	0.4 V	0.150 V	Unavailable	(1)	Yes
S-8261ABSMD-G3ST2x	4.280 V	0.10 V	2.500 V	0.5 V	0.180 V	Unavailable	(1)	Yes
S-8261ABTMD-G3TT2x	4.280 V	0.20 V	3.000 V	0.4 V	0.080 V	Available	(5)	Yes
S-8261ABYMD-G3YT2x	4.275 V	0.10 V	2.300 V	0.1 V	0.100 V	Available	(6)	Yes
S-8261ABZMD-G3ZT2x	4.325 V	0.25 V	2.500 V	0.4 V	0.150 V	Unavailable	(6)	Yes
S-8261ACAMD-G4AT2x	4.280 V	0.20 V	2.300 V	0 V	0.130 V	Unavailable	(6)	Yes
S-8261ACBMD-G4BT2x	4.250 V	0.20 V	2.600 V	0.3 V	0.120 V	Unavailable	(1)	No
S-8261ACDMD-G4DT2x	4.350 V	0.25 V	2.300 V	0.7 V	0.250 V	Available	(7)	Yes
S-8261ACEMD-G4ET2x	3.900 V	0.10 V	2.000 V	0.3 V	0.100 V	Available	(1)	Yes
S-8261ACFMD-G4FT2x	4.280 V	0.20 V	2.300 V	0 V	0.100 V	Available	(8)	Yes
S-8261ACHMD-G4HT2x	4.465 V	0.30 V	2.100 V	0 V	0.150 V	Available	(9)	Yes
S-8261ACIMD-G4IT2x	4.250 V	0.20 V	2.400 V	0.5 V	0.100 V	Available	(1)	No
S-8261ACJMD-G4JT2x	4.275 V	0.10 V	2.300 V	0.1 V	0.150 V	Available	(1)	Yes
S-8261ACKMD-G4KT2x	4.280 V	0.20 V	2.800 V	0 V	0.130 V	Available	(1)	Yes

*1. Refer to the **Table 2** about the details of the delay time combinations (1) to (9).

- Remark 1.** Please contact our sales office for the products with detection voltage value other than those specified above.
2. x: G or U
 3. Please select products of environmental code = U for Sn 100%, halogen-free products.

Table 1 (2 / 2)

Product name	Overcharge detection voltage [V _{CU}]	Overcharge hysteresis voltage [V _{HC}]	Overdischarge detection voltage [V _{DL}]	Overdischarge hysteresis voltage [V _{HD}]	Overcurrent 1 detection voltage [V _{IOV1}]	0 V battery charge function	Delay time combination *1	Power-down function
S-8261ACMMD-G4MT2x	4.325 V	0.20 V	3.000 V	0.4 V	0.060 V	Unavailable	(1)	Yes
S-8261ACNMD-G4NT2x	4.215 V	0.10 V	2.300 V	0.1 V	0.130 V	Unavailable	(1)	Yes
S-8261ACSMD-G4ST2y	4.350 V	0.10 V	2.300 V	0.1 V	0.150 V	Available	(6)	Yes

*1. Refer to the **Table 2** about the details of the delay time combinations (1) to (9).

Remark 1. Please contact our sales office for the products with detection voltage value other than those specified above.

2. x: G or U

3. y: S or U

4. Please select products of environmental code = U for Sn 100%, halogen-free products.

Table 2

Delay time combination	Overcharge detection delay time [t _{CU}]	Overdischarge detection delay time [t _{DL}]	Overcurrent 1 detection delay time [t _{IOV1}]	Overcurrent 2 detection delay time [t _{IOV2}]	Load short-circuiting detection delay time [t _{SHORT}]
(1)	1.2 s	144 ms	9 ms	2.24 ms	320 μs
(2)	1.2 s	144 ms	4.5 ms	2.24 ms	320 μs
(3)	4.6 s	36 ms	18 ms	9 ms	320 μs
(4)	4.6 s	144 ms	9 ms	2.24 ms	320 μs
(5)	1.2 s	36 ms	9 ms	2.24 ms	320 μs
(6)	1.2 s	144 ms	9 ms	1.12 ms	320 μs
(7)	1.2 s	290 ms	18 ms	2.24 ms	320 μs
(8)	1.2 s	144 ms	18 ms	2.24 ms	320 μs
(9)	0.3 s	36 ms	9 ms	1.12 ms	320 μs

Remark The delay times can be changed within the range listed **Table 3**. For details, please contact our sales office.

Table 3

Delay time	Symbol	Selection range			Remarks
Overcharge detection delay time	t _{CU}	0.15 s	1.2 s ^{*1}	4.6 s	Choose from the left.
Overdischarge detection delay time	t _{DL}	36 ms	144 ms ^{*1}	290 ms	Choose from the left.
Overcurrent 1 detection delay time	t _{IOV1}	4.5 ms	9 ms ^{*1}	18 ms	Choose from the left.
Overcurrent 2 detection delay time	t _{IOV1}	1.12 ms	2.24 ms ^{*1}	—	Choose from the left.
Load short-circuiting detection delay time	t _{SHORT}	—	320 μs ^{*1}	600 μs	Choose from the left.

*1. The value is the delay time of the standard products.

■ Pin Configuration

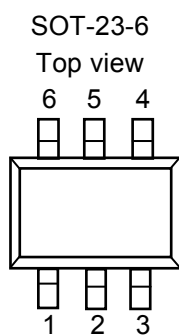


Figure 2

Table 4

Pin No.	Symbol	Description
1	DO	FET gate control pin for discharge (CMOS output)
2	VM	Voltage detection pin between VM and VSS (Overcurrent detection pin)
3	CO	FET gate control pin for charge (CMOS output)
4	DP	Test pin for delay time measurement
5	VDD	Positive power supply input pin
6	VSS	Negative power supply input pin

■ Absolute Maximum Ratings

Table 5

(Ta = 25°C unless otherwise specified)

Item	Symbol	Applied pin	Absolute Maximum Rating	Unit
Input voltage between VDD and VSS	V _{DS}	VDD	V _{SS} -0.3 to V _{SS} +12	V
Input pin voltage for VM	V _{VM}	VM	V _{DD} -28 to V _{DD} +0.3	V
Output pin voltage for CO	V _{CO}	CO	V _{VM} -0.3 to V _{DD} +0.3	V
Output pin voltage for DO	V _{DO}	DO	V _{SS} -0.3 to V _{DD} +0.3	V
Power dissipation	P _D	—	250 (When not mounted on board)	mW
			650 ^{*1}	mW
Operating ambient temperature	T _{opr}	—	-40 to +85	°C
Storage temperature	T _{stg}	—	-55 to +125	°C

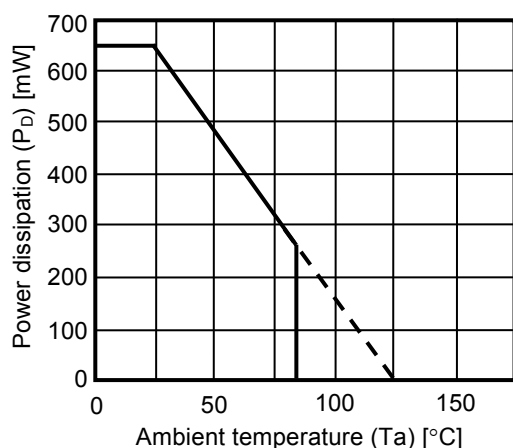
*1. When mounted on board

[Mounted board]

- (1) Board size : 114.3 mm × 76.2 mm × t1.6 mm
 (2) Board name : JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

(1) When mounted on board



(2) When not mounted on board

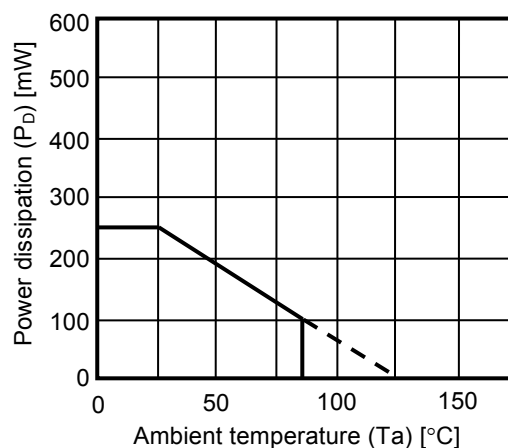


Figure 3 Power Dissipation of Package

■ Electrical Characteristics

1. Except Detection Delay Time (25°C)

Table 6

(Ta = 25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Condition	Test Circuit
DETECTION VOLTAGE								
Overcharge detection voltage V _{CU} = 3.900 V to 4.500 V, 5 mV Step	V _{CU}	—	V _{CU} −0.025	V _{CU}	V _{CU} +0.025	V	1	1
		Ta = −5°C to 55°C*1	V _{CU} −0.030	V _{CU}	V _{CU} +0.030	V	1	1
Overcharge hysteresis voltage V _{HC} = 0.1 V to 0.4 V, 50 mV Step	V _{HC}	—	V _{HC} −0.025	V _{HC}	V _{HC} +0.025	V	1	1
Overdischarge detection voltage V _{DL} = 2.000 V to 3.000 V, 10 mV Step	V _{DL}	—	V _{DL} −0.050	V _{DL}	V _{DL} +0.050	V	2	2
Overdischarge hysteresis voltage V _{HD} = 0.0 V to 0.7 V, 100 mV Step	V _{HD}	—	V _{HD} −0.050	V _{HD}	V _{HD} +0.050	V	2	2
Overcurrent 1 detection voltage V _{IOV1} = 0.050 V to 0.300 V, 10 mV Step	V _{IOV1}	—	V _{IOV1} −0.015	V _{IOV1}	V _{IOV1} +0.015	V	3	2
Overcurrent 2 detection voltage	V _{IOV2}	—	0.400	0.500	0.600	V	3	2
Load short-circuiting detection voltage	V _{SHORT}	—	0.900	1.200	1.500	V	3	2
Charger detection voltage	V _{CHA}	—	−1.0	−0.7	−0.4	V	4	2
INPUT VOLTAGE, OPERATION VOLTAGE								
Operation voltage between VDD and VSS	V _{DSOP1}	Internal circuit operating voltage	1.5	—	8	V	—	—
Operation voltage between VDD and VM	V _{DSOP2}	Internal circuit operating voltage	1.5	—	28	V	—	—
CURRENT CONSUMPTION (with power-down function)								
Current consumption in normal operation	I _{OPE}	V _{DD} = 3.5 V, V _{VM} = 0 V	1.0	3.5	7.0	μA	5	2
Current consumption at power down	I _{PDN}	V _{DD} = V _{VM} = 1.5 V	—	—	0.1	μA	5	2
CURRENT CONSUMPTION (without power-down function)								
Current consumption in normal operation	I _{OPE}	V _{DD} = 3.5 V, V _{VM} = 0 V	1.0	3.5	7.0	μA	5	2
Overdischarge current consumption	I _{OPED}	V _{DD} = V _{VM} = 1.5 V	1.0	3.0	5.5	μA	5	2
OUTPUT RESISTANCE								
CO pin resistance "H"	R _{COH}	V _{CO} = 3.0 V, V _{DD} = 3.5 V, V _{VM} = 0 V	2.5	5	10	kΩ	7	4
CO pin resistance "L"	R _{COL}	V _{CO} = 0.5 V, V _{DD} = 4.5 V, V _{VM} = 0 V	2.5	5	10	kΩ	7	4
DO pin resistance "H"	R _{DOH}	V _{DO} = 3.0 V, V _{DD} = 3.5 V, V _{VM} = 0 V	2.5	5	10	kΩ	8	4
DO pin resistance "L"	R _{DOL}	V _{DO} = 0.5 V, V _{DD} = V _{VM} = 1.8 V	2.5	5	10	kΩ	8	4
VM INTERNAL RESISTANCE								
Internal resistance between VM and VDD	R _{VMD}	V _{DD} = 1.8 V, V _{VM} = 0 V	100	300	900	kΩ	6	3
Internal resistance between VM and VSS	R _{VMS}	V _{DD} = 3.5 V, V _{VM} = 1.0 V	10	20	40	kΩ	6	3
0 V BATTERY CHARGE FUNCTION								
0 V battery charge starting charger voltage	V _{OCHA}	0 V battery charge "available"	1.2	—	—	V	11	2
0 V battery charge inhibition battery voltage	V _{OINH}	0 V battery charge "unavailable"	—	—	0.5	V	12	2

*1. Since products are not screened at high and low temperatures, the specification for this temperature range is guaranteed by design, not tested in production.

2. Except Detection Delay Time (–40°C to +85°C^{*1})

Table 7

(Ta = –40°C to +85°C^{*1} unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Condition	Test Circuit
DETECTION VOLTAGE								
Overcharge detection voltage V _{CU} = 3.900 V to 4.500 V, 5 mV Step	V _{CU}	—	V _{CU} –0.055	V _{CU}	V _{CU} +0.040	V	1	1
Overcharge hysteresis voltage V _{HC} = 0.1 V to 0.4 V, 50 mV Step	V _{HC}	—	V _{HC} –0.025	V _{HC}	V _{HC} +0.025	V	1	1
Overdischarge detection voltage V _{DL} = 2.000 V to 3.000 V, 10 mV Step	V _{DL}	—	V _{DL} –0.080	V _{DL}	V _{DL} +0.080	V	2	2
Overdischarge hysteresis voltage V _{HD} = 0.0 V to 0.7 V, 100 mV Step	V _{HD}	—	V _{HD} –0.050	V _{HD}	V _{HD} +0.050	V	2	2
Overcurrent 1 detection voltage V _{IOV1} = 0.050 V to 0.300 V, 10 mV Step	V _{IOV1}	—	V _{IOV1} –0.021	V _{IOV1}	V _{IOV1} +0.021	V	3	2
Overcurrent 2 detection voltage	V _{IOV2}	—	0.370	0.500	0.630	V	3	2
Load short-circuiting detection voltage	V _{SHORT}	—	0.700	1.200	1.700	V	3	2
Charger detection voltage	V _{CHA}	—	–1.2	–0.7	–0.2	V	4	2
INPUT VOLTAGE, OPERATION VOLTAGE								
Operation voltage between VDD and VSS	V _{DSOP1}	Internal circuit operating voltage	1.5	—	8	V	—	—
Operation voltage between VDD and VM	V _{DSOP2}	Internal circuit operating voltage	1.5	—	28	V	—	—
CURRENT CONSUMPTION (with power-down function)								
Current consumption in normal operation	I _{OP}	V _{DD} = 3.5 V, V _{VM} = 0 V	0.7	3.5	8.0	μA	5	2
Current consumption at power down	I _{PDN}	V _{DD} = V _{VM} = 1.5 V	—	—	0.1	μA	5	2
CURRENT CONSUMPTION (without power-down function)								
Current consumption in normal operation	I _{OP}	V _{DD} = 3.5 V, V _{VM} = 0 V	0.7	3.5	8.0	μA	5	2
Overdischarge current consumption	I _{OPED}	V _{DD} = V _{VM} = 1.5 V	0.7	3.0	6.0	μA	5	2
OUTPUT RESISTANCE								
CO pin resistance "H"	R _{COH}	V _{CO} = 3.0 V, V _{DD} = 3.5 V, V _{VM} = 0 V	1.2	5	15	kΩ	7	4
CO pin resistance "L"	R _{COL}	V _{CO} = 0.5 V, V _{DD} = 4.5 V, V _{VM} = 0 V	1.2	5	15	kΩ	7	4
DO pin resistance "H"	R _{DOH}	V _{DO} = 3.0 V, V _{DD} = 3.5 V, V _{VM} = 0 V	1.2	5	15	kΩ	8	4
DO pin resistance "L"	R _{DOL}	V _{DO} = 0.5 V, V _{DD} = V _{VM} = 1.8 V	1.2	5	15	kΩ	8	4
VM INTERNAL RESISTANCE								
Internal resistance between VM and VDD	R _{VMD}	V _{DD} = 1.8 V, V _{VM} = 0 V	78	300	1310	kΩ	6	3
Internal resistance between VM and VSS	R _{VMS}	V _{DD} = 3.5 V, V _{VM} = 1.0 V	7.2	20	44	kΩ	6	3
0 V BATTERY CHARGE FUNCTION								
0 V battery charge starting charger voltage	V _{0CHA}	0 V battery charge "available"	1.7	—	—	V	11	2
0 V battery charge inhibition battery voltage	V _{0INH}	0 V battery charge "unavailable"	—	—	0.3	V	12	2

*1. Since products are not screened at high and low temperatures, the specification for this temperature range is guaranteed by design, not tested in production.

3. Detection Delay Time

- (1) S-8261AAG, S-8261AAH, S-8261AAJ, S-8261AAL, S-8261AAM, S-8261AAN, S-8261AAO, S-8261AAP, S-8261AAR, S-8261AAZ, S-8261ABB, S-8261ABC, S-8261ABJ, S-8261ABK, S-8261ABM, S-8261ABN, S-8261ABP, S-8261ABR, S-8261ABS, S-8261ACB, S-8261ACE, S-8261ACI, S-8261ACK, S-8261ACM, S-8261ACJ, S-8261ACN

Table 8

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Condition	Test Circuit
DELAY TIME (Ta = 25°C)								
Overcharge detection delay time	t _{CU}	—	0.96	1.2	1.4	s	9	5
Overdischarge detection delay time	t _{DL}	—	115	144	173	ms	9	5
Overcurrent 1 detection delay time	t _{IOV1}	—	7.2	9	11	ms	10	5
Overcurrent 2 detection delay time	t _{IOV2}	—	1.8	2.24	2.7	ms	10	5
Load short-circuiting detection delay time	t _{SHORT}	—	220	320	380	μs	10	5
DELAY TIME (Ta = -40°C to +85°C) *1								
Overcharge detection delay time	t _{CU}	—	0.7	1.2	2.0	s	9	5
Overdischarge detection delay time	t _{DL}	—	80	144	245	ms	9	5
Overcurrent 1 detection delay time	t _{IOV1}	—	5	9	15	ms	10	5
Overcurrent 2 detection delay time	t _{IOV2}	—	1.2	2.24	3.8	ms	10	5
Load short-circuiting detection delay time	t _{SHORT}	—	150	320	540	μs	10	5

*1. Since products are not screened at high and low temperatures, the specification for this temperature range is guaranteed by design, not tested in production.

- (2) S-8261AAS

Table 9

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Condition	Test Circuit
DELAY TIME (Ta = 25°C)								
Overcharge detection delay time	t _{CU}	—	0.96	1.2	1.4	s	9	5
Overdischarge detection delay time	t _{DL}	—	115	144	173	ms	9	5
Overcurrent 1 detection delay time	t _{IOV1}	—	3.6	4.5	5.4	ms	10	5
Overcurrent 2 detection delay time	t _{IOV2}	—	1.8	2.24	2.7	ms	10	5
Load short-circuiting detection delay time	t _{SHORT}	—	220	320	380	μs	10	5
DELAY TIME (Ta = -40°C to +85°C) *1								
Overcharge detection delay time	t _{CU}	—	0.7	1.2	2.0	s	9	5
Overdischarge detection delay time	t _{DL}	—	80	144	245	ms	9	5
Overcurrent 1 detection delay time	t _{IOV1}	—	2.5	4.5	7.7	ms	10	5
Overcurrent 2 detection delay time	t _{IOV2}	—	1.2	2.24	3.8	ms	10	5
Load short-circuiting detection delay time	t _{SHORT}	—	150	320	540	μs	10	5

*1. Since products are not screened at high and low temperatures, the specification for this temperature range is guaranteed by design, not tested in production.

(3) S-8261AAT**Table 10**

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Condition	Test Circuit
DELAY TIME (Ta = 25°C)								
Overcharge detection delay time	t _{CU}	—	3.7	4.6	5.5	s	9	5
Overdischarge detection delay time	t _{DL}	—	29	36	43	ms	9	5
Overcurrent 1 detection delay time	t _{IOV1}	—	14	18	22	ms	10	5
Overcurrent 2 detection delay time	t _{IOV2}	—	7.2	9	11	ms	10	5
Load short-circuiting detection delay time	t _{SHORT}	—	220	320	380	μs	10	5
DELAY TIME (Ta = -40°C to +85°C) *1								
Overcharge detection delay time	t _{CU}	—	2.5	4.6	7.8	s	9	5
Overdischarge detection delay time	t _{DL}	—	20	36	61	ms	9	5
Overcurrent 1 detection delay time	t _{IOV1}	—	10	18	31	ms	10	5
Overcurrent 2 detection delay time	t _{IOV2}	—	5	9	15	ms	10	5
Load short-circuiting detection delay time	t _{SHORT}	—	150	320	540	μs	10	5

*1. Since products are not screened at high and low temperatures, the specification for this temperature range is guaranteed by design, not tested in production.

(4) S-8261AAU, S-8261AAX, S-8261ABA**Table 11**

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Condition	Test Circuit
DELAY TIME (Ta = 25°C)								
Overcharge detection delay time	t _{CU}	—	3.7	4.6	5.5	s	9	5
Overdischarge detection delay time	t _{DL}	—	115	144	173	ms	9	5
Overcurrent 1 detection delay time	t _{IOV1}	—	7.2	9	11	ms	10	5
Overcurrent 2 detection delay time	t _{IOV2}	—	1.8	2.24	2.7	ms	10	5
Load short-circuiting detection delay time	t _{SHORT}	—	220	320	380	μs	10	5
DELAY TIME (Ta = -40°C to +85°C) *1								
Overcharge detection delay time	t _{CU}	—	2.5	4.6	7.8	s	9	5
Overdischarge detection delay time	t _{DL}	—	80	144	245	ms	9	5
Overcurrent 1 detection delay time	t _{IOV1}	—	5	9	15	ms	10	5
Overcurrent 2 detection delay time	t _{IOV2}	—	1.2	2.24	3.8	ms	10	5
Load short-circuiting detection delay time	t _{SHORT}	—	150	320	540	μs	10	5

*1. Since products are not screened at high and low temperatures, the specification for this temperature range is guaranteed by design, not tested in production.

(5) S-8261ABI, S-8261ABL, S-8261ABT

Table 12

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test condition	Test circuit
DELAY TIME (Ta = 25°C)								
Overcharge detection delay time	t _{CU}	—	0.96	1.2	1.4	s	9	5
Overdischarge detection delay time	t _{DL}	—	29	36	43	ms	9	5
Overcurrent 1 detection delay time	t _{IOV1}	—	7.2	9	11	ms	10	5
Overcurrent 2 detection delay time	t _{IOV2}	—	1.8	2.24	2.7	ms	10	5
Load short-circuiting detection delay time	t _{SHORT}	—	220	320	380	μs	10	5
DELAY TIME (Ta = -40°C to +85°C) *1								
Overcharge detection delay time	t _{CU}	—	0.7	1.2	2.0	s	9	5
Overdischarge detection delay time	t _{DL}	—	20	36	61	ms	9	5
Overcurrent 1 detection delay time	t _{IOV1}	—	5	9	15	ms	10	5
Overcurrent 2 detection delay time	t _{IOV2}	—	1.2	2.24	3.8	ms	10	5
Load short-circuiting detection delay time	t _{SHORT}	—	150	320	540	μs	10	5

*1. Since products are not screened at high and low temperatures, the specification for this temperature range is guaranteed by design, not tested in production.

(6) S-8261ABY, S-8261ABZ, S-8261ACA, S-8261ACS

Table 13

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Condition	Test Circuit
DELAY TIME (Ta = 25°C)								
Overcharge detection delay time	t _{CU}	—	0.96	1.2	1.4	s	9	5
Overdischarge detection delay time	t _{DL}	—	115	144	173	ms	9	5
Overcurrent 1 detection delay time	t _{IOV1}	—	7.2	9	11	ms	10	5
Overcurrent 2 detection delay time	t _{IOV2}	—	0.89	1.12	1.35	ms	10	5
Load short-circuiting detection delay time	t _{SHORT}	—	220	320	380	μs	10	5
DELAY TIME (Ta = -40°C to +85°C) *1								
Overcharge detection delay time	t _{CU}	—	0.7	1.2	2.0	s	9	5
Overdischarge detection delay time	t _{DL}	—	80	144	245	ms	9	5
Overcurrent 1 detection delay time	t _{IOV1}	—	5	9	15	ms	10	5
Overcurrent 2 detection delay time	t _{IOV2}	—	0.61	1.12	1.91	ms	10	5
Load short-circuiting detection delay time	t _{SHORT}	—	150	320	540	μs	10	5

*1. Since products are not screened at high and low temperatures, the specification for this temperature range is guaranteed by design, not tested in production.

(7) S-8261ACD**Table 14**

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Condition	Test Circuit
DELAY TIME (Ta = 25°C)								
Overcharge detection delay time	t _{CU}	—	0.96	1.2	1.4	s	9	5
Overdischarge detection delay time	t _{DL}	—	232	290	348	ms	9	5
Overcurrent 1 detection delay time	t _{IOV1}	—	14	18	22	ms	10	5
Overcurrent 2 detection delay time	t _{IOV2}	—	1.8	2.24	2.7	ms	10	5
Load short-circuiting detection delay time	t _{SHORT}	—	220	320	380	μs	10	5
DELAY TIME (Ta = -40°C to +85°C) *1								
Overcharge detection delay time	t _{CU}	—	0.7	1.2	2.0	s	9	5
Overdischarge detection delay time	t _{DL}	—	160	290	493	ms	9	5
Overcurrent 1 detection delay time	t _{IOV1}	—	10	18	31	ms	10	5
Overcurrent 2 detection delay time	t _{IOV2}	—	1.2	2.24	3.8	ms	10	5
Load short-circuiting detection delay time	t _{SHORT}	—	150	320	540	μs	10	5

*1. Since products are not screened at high and low temperatures, the specification for this temperature range is guaranteed by design, not tested in production.

(8) S-8261ACF**Table 15**

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Condition	Test Circuit
DELAY TIME (Ta = 25°C)								
Overcharge detection delay time	t _{CU}	—	0.96	1.2	1.4	s	9	5
Overdischarge detection delay time	t _{DL}	—	115	144	173	ms	9	5
Overcurrent 1 detection delay time	t _{IOV1}	—	14	18	22	ms	10	5
Overcurrent 2 detection delay time	t _{IOV2}	—	1.8	2.24	2.7	ms	10	5
Load short-circuiting detection delay time	t _{SHORT}	—	220	320	380	μs	10	5
DELAY TIME (Ta = -40°C to +85°C) *1								
Overcharge detection delay time	t _{CU}	—	0.7	1.2	2.0	s	9	5
Overdischarge detection delay time	t _{DL}	—	80	144	245	ms	9	5
Overcurrent 1 detection delay time	t _{IOV1}	—	10	18	31	ms	10	5
Overcurrent 2 detection delay time	t _{IOV2}	—	1.2	2.24	3.8	ms	10	5
Load short-circuiting detection delay time	t _{SHORT}	—	150	320	540	μs	10	5

*1. Since products are not screened at high and low temperatures, the specification for this temperature range is guaranteed by design, not tested in production.

(9) S-8261ACH

Table 16

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Condition	Test Circuit
DELAY TIME (Ta = 25°C)								
Overcharge detection delay time	t _{CU}	—	0.24	0.3	0.36	s	9	5
Overdischarge detection delay time	t _{DL}	—	29	36	43	ms	9	5
Overcurrent 1 detection delay time	t _{IOV1}	—	7.2	9	11	ms	10	5
Overcurrent 2 detection delay time	t _{IOV2}	—	0.89	1.12	1.35	ms	10	5
Load short-circuiting detection delay time	t _{SHORT}	—	220	320	380	μs	10	5
DELAY TIME (Ta = -40°C to +85°C) **1								
Overcharge detection delay time	t _{CU}	—	0.17	0.3	0.51	s	9	5
Overdischarge detection delay time	t _{DL}	—	20	36	61	ms	9	5
Overcurrent 1 detection delay time	t _{IOV1}	—	5	9	15	ms	10	5
Overcurrent 2 detection delay time	t _{IOV2}	—	0.61	1.12	1.91	ms	10	5
Load short-circuiting detection delay time	t _{SHORT}	—	150	320	540	μs	10	5

*1. Since products are not screened at high and low temperatures, the specification for this temperature range is guaranteed by design, not tested in production.

■ Test Circuits

Caution Unless otherwise specified, the output voltage levels “H” and “L” at CO pin (V_{CO}) and DO pin (V_{DO}) are judged by the threshold voltage (1.0 V) of the N-channel FET. Judge the CO pin level with respect to V_{VM} and the DO pin level with respect to V_{SS} .

(1) Test Condition 1, Test Circuit 1

(Overcharge Detection Voltage, Overcharge Hysteresis Voltage)

The overcharge detection voltage (V_{CU}) is defined as the voltage between VDD and VSS at which V_{CO} goes from “H” to “L” when the voltage V_1 is gradually increased from the starting condition of $V_1 = 3.5$ V. The overcharge hysteresis voltage (V_{HC}) is then defined as the difference between the overcharge detection voltage (V_{CU}) and the voltage between VDD and VSS at which V_{CO} goes from “L” to “H” when the voltage V_1 is gradually decreased.

(2) Test Condition 2, Test Circuit 2

(Overdischarge Detection Voltage, Overdischarge Hysteresis Voltage)

The overdischarge detection voltage (V_{DL}) is defined as the voltage between VDD and VSS at which V_{DO} goes from “H” to “L” when the voltage V_1 is gradually decreased from the starting condition of $V_1 = 3.5$ V and $V_2 = 0$ V. The overdischarge hysteresis voltage (V_{HD}) is then defined as the difference between the overdischarge detection voltage (V_{DL}) and the voltage between VDD and VSS at which V_{DO} goes from “L” to “H” when the voltage V_1 is gradually increased.

(3) Test Condition 3, Test Circuit 2

(Overcurrent 1 Detection Voltage, Overcurrent 2 Detection Voltage, Load Short-Circuiting Detection Voltage)

The overcurrent 1 detection voltage (V_{IOV1}) is defined as the voltage between VM and VSS whose delay time for changing V_{DO} from “H” to “L” lies between the minimum and the maximum value of the overcurrent 1 detection delay time when the voltage V_2 is increased rapidly (within 10 μ s) from the starting condition $V_1 = 3.5$ V and $V_2 = 0$ V.

The overcurrent 2 detection voltage (V_{IOV2}) is defined as the voltage between VM and VSS whose delay time for changing V_{DO} from “H” to “L” lies between the minimum and the maximum value of the overcurrent 2 detection delay time when the voltage V_2 is increased rapidly (within 10 μ s) from the starting condition $V_1 = 3.5$ V and $V_2 = 0$ V.

The load short-circuiting detection voltage (V_{SHORT}) is defined as the voltage between VM and VSS whose delay time for changing V_{DO} from “H” to “L” lies between the minimum and the maximum value of the load short-circuiting detection delay time when the voltage V_2 is increased rapidly (within 10 μ s) from the starting condition $V_1 = 3.5$ V and $V_2 = 0$ V.

(4) Test Condition 4, Test Circuit 2

(Charger Detection Voltage, Abnormal Charge Current Detection Voltage)

The charger detection voltage (V_{CHA}) is defined as the voltage between VM and VSS at which V_{DO} goes from “L” to “H” when the voltage V_2 is gradually decreased from 0 V after the voltage V_1 is gradually increased from the starting condition of $V_1 = 1.8$ V and $V_2 = 0$ V until the voltage V_1 becomes $V_1 = V_{DL} + (V_{HD} / 2)$.

The charger detection voltage can be measured only in the product whose overdischarge hysteresis $V_{HD} \neq 0$.

Set $V_1 = 3.5$ V and $V_2 = 0$ V. Decrease V_2 from 0 V gradually. The voltage between VM and VSS when V_{CO} goes from “H” to “L” is the abnormal charge current detection voltage. The abnormal charge current detection voltage has the same value as the charger detection voltage (V_{CHA}).

(5) Test Condition 5, Test Circuit 2

(Normal Operation Current Consumption, Power-Down Current Consumption, Overdischarge Current Consumption)

With power-down function

The operating current consumption (I_{OPE}) is the current that flows through the VDD pin (I_{DD}) under the set conditions of $V_1 = 3.5$ V and $V_2 = 0$ V (Normal status).

The power-down current consumption (I_{PDN}) is the current that flows through the VDD pin (I_{DD}) under the set conditions of $V_1 = V_2 = 1.5$ V (Overdischarge status).

Without power-down function

The operating current consumption (I_{OPE}) is the current that flows through the VDD pin (I_{DD}) under the set conditions of $V_1 = 3.5$ V and $V_2 = 0$ V (Normal status).

The Overdischarge current consumption (I_{OPED}) is the current that flows through the VDD pin (I_{DD}) under the set conditions of $V_1 = V_2 = 1.5$ V (Overdischarge status).

(6) Test Condition 6, Test Circuit 3

(Internal Resistance between VM and VDD, Internal Resistance between VM and VSS)

The resistance between VM and VDD (R_{VMD}) is the internal resistance between VM and VDD under the set conditions of $V_1 = 1.8\text{ V}$ and $V_2 = 0\text{ V}$.

The resistance between VM and VSS (R_{VMS}) is the internal resistance between VM and VSS under the set conditions of $V_1 = 3.5\text{ V}$ and $V_2 = 1.0\text{ V}$.

(7) Test Condition 7, Test Circuit 4

(CO Pin Resistance "H", CO Pin Resistance "L")

The CO pin resistance "H" (R_{COH}) is the resistance the CO pin under the set condition of $V_1 = 3.5\text{ V}$, $V_2 = 0\text{ V}$ and $V_3 = 3.0\text{ V}$.

The CO pin resistance "L" (R_{COL}) is the resistance the CO pin under the set condition of $V_1 = 4.5\text{ V}$, $V_2 = 0\text{ V}$ and $V_3 = 0.5\text{ V}$.

(8) Test Condition 8, Test Circuit 4

(DO Pin Resistance "H", DO Pin Resistance "L")

The DO pin resistance "H" (R_{DOH}) is the resistance the DO pin under the set condition of $V_1 = 3.5\text{ V}$, $V_2 = 0\text{ V}$ and $V_4 = 3.0\text{ V}$.

The DO pin resistance "L" (R_{DOL}) is the resistance the DO pin under the set condition of $V_1 = 1.8\text{ V}$, $V_2 = 0\text{ V}$ and $V_4 = 0.5\text{ V}$.

(9) Test Condition 9, Test Circuit 5

(Overcharge Detection Delay Time, Overdischarge Detection Delay Time)

The overcharge detection delay time (t_{CU}) is the time needed for V_{CO} to change from "H" to "L" just after the voltage V_1 momentarily increases (within $10\text{ }\mu\text{s}$) from the overcharge detection voltage (V_{CU}) - 0.2 V to the overcharge detection voltage (V_{CU}) + 0.2 V under the set condition of $V_2 = 0\text{ V}$.

The overdischarge detection delay time (t_{DL}) is the time needed for V_{DO} to change from "H" to "L" just after the voltage V_1 momentarily decreases (within $10\text{ }\mu\text{s}$) from the overdischarge detection voltage (V_{DL}) + 0.2 V to the overdischarge detection voltage (V_{DL}) - 0.2 V under the set condition of $V_2 = 0\text{ V}$.

(10) Test Condition 10, Test Circuit 5

(Overcurrent 1 Detection Delay Time, Overcurrent 2 Detection Delay Time, Load Short-circuiting Detection Delay Time, Abnormal Charge Current Detection Delay Time)

The overcurrent 1 detection delay time (t_{IOV1}) is the time needed for V_{DO} to go "L" after the voltage V_2 momentarily increases (within $10\text{ }\mu\text{s}$) from 0 V to 0.35 V under the set condition of $V_1 = 3.5\text{ V}$ and $V_2 = 0\text{ V}$.

The overcurrent 2 detection delay time (t_{IOV2}) is the time needed for V_{DO} to go "L" after the voltage V_2 momentarily increases (within $10\text{ }\mu\text{s}$) from 0 V to 0.7 V under the set condition of $V_1 = 3.5\text{ V}$ and $V_2 = 0\text{ V}$.

The load short-circuiting detection delay time (t_{SHORT}) is the time needed for V_{DO} to go "L" after the voltage V_2 momentarily increases (within $10\text{ }\mu\text{s}$) from 0 V to 1.6 V under the set condition of $V_1 = 3.5\text{ V}$ and $V_2 = 0\text{ V}$.

The abnormal charge current detection delay time is the time needed for V_{CO} to go from "H" to "L" after the voltage V_2 momentarily decreases (within $10\text{ }\mu\text{s}$) from 0 V to -1.1 V under the set condition of $V_1 = 3.5\text{ V}$ and $V_2 = 0\text{ V}$. The abnormal charge current detection delay time has the same value as the overcharge detection delay time.

(11) Test Condition 11, Test Circuit 2 (0 V battery charge function)

(0 V Battery Charge Starting Charger Voltage)

The 0 V battery charge starting charger voltage (V_{0CHA}) is defined as the voltage between VDD and VM at which V_{CO} goes "H" ($V_{VM} + 0.1\text{ V}$ or higher) when the voltage V_2 is gradually decreased from the starting condition of $V_1 = V_2 = 0\text{ V}$.

(12) Test Condition 12, Test Circuit 2 (0 V battery charge inhibition function)

(0 V Battery Charge Inhibition Battery Voltage)

The 0 V battery charge inhibition battery voltage (V_{0INH}) is defined as the voltage between VDD and VSS at which V_{CO} goes "H" ($V_{VM} + 0.1\text{ V}$ or higher) when the voltage V_1 is gradually increased from the starting condition of $V_1 = 0\text{ V}$ and $V_2 = -4\text{ V}$.

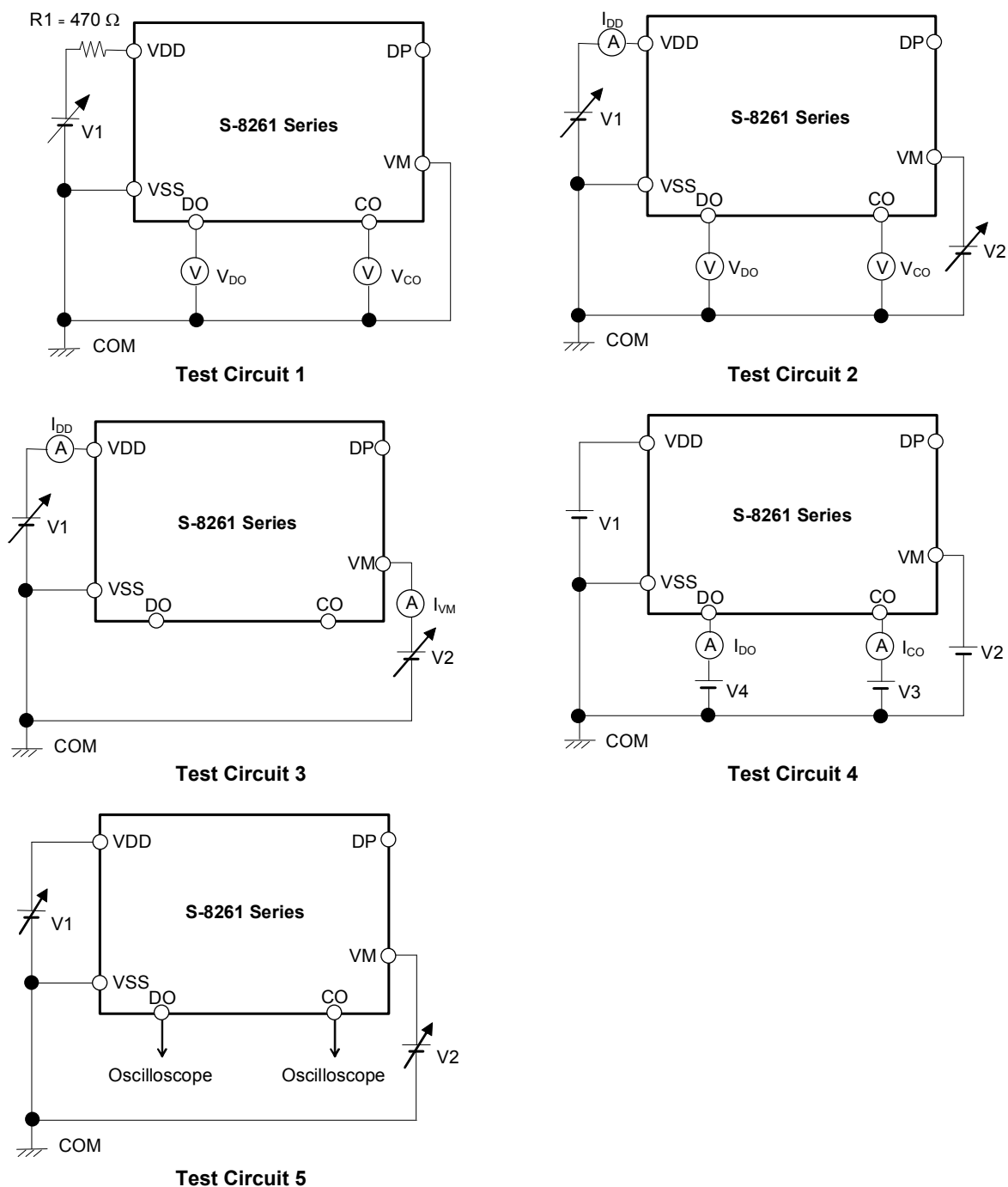


Figure 4

■ Operation

Remark Refer to “■ Battery Protection IC Connection Example”.

1. Normal Status

The S-8261 Series monitors the voltage of the battery connected between VDD pin and VSS pin and the voltage difference between VM pin and VSS pin to control charging and discharging. When the battery voltage is in the range from the overdischarge detection voltage (V_{DL}) to the overcharge detection voltage (V_{CU}), and the VM pin voltage is in the range from the charger detection voltage (V_{CHA}) to the overcurrent 1 detection voltage (V_{IOV1}), the IC turns both the charging and discharging control FETs on. This status is called the normal status, and in this status charging and discharging can be carried out freely.

Caution When a battery is connected to the IC for the first time, discharging may not be enabled. In this case, short the VM pin and VSS pin or connect the charger to restore the normal condition.

2. Overcurrent Status (Detection of Overcurrent 1, Overcurrent 2 and Load Short-circuiting)

When a battery in the normal status is in the status where the voltage of the VM pin is equal to or higher than the overcurrent detection voltage because the discharge current is higher than the specified value and the status lasts for the overcurrent detection delay time, the discharge control FET is turned off and discharging is stopped. This status is called the overcurrent status.

In the overcurrent status, the VM and VSS pins are shorted by the resistor between VM and VSS (R_{VMS}) in the IC. However, the voltage of the VM pin is at the V_{DD} potential due to the load as long as the load is connected. When the load is disconnected completely, the VM pin returns to the V_{SS} potential.

The voltage of the VM pin returns to overcurrent 1 detection voltage (V_{IOV1}) or lower and the overcurrent status is restored to the normal status.

3. Overcharge Status

When the battery voltage becomes higher than the overcharge detection voltage (V_{CU}) during charging under the normal status and the detection continues for the overcharge detection delay time (t_{CU}) or longer, the S-8261 Series turns the charging control FET off to stop charging. This status is called the overcharge status.

The overcharge status is released by the following two cases ((1) and (2)):

- (1) When the battery voltage falls below the overcharge detection voltage (V_{CU}) – overcharge hysteresis voltage (V_{HC}), the S-8261 Series turns the charging control FET on and turns to the normal status.
- (2) When a load is connected and discharging starts, the S-8261 Series turns the charging control FET on and returns to the normal status. Just after the load is connected and discharging starts, the discharging current flows through the parasitic diode in the charging control FET. At this moment the VM pin potential becomes V_f , the voltage for the parasitic diode, higher than V_{SS} level. When the battery voltage goes under the overcharge detection voltage (V_{CU}) and provided that the VM pin voltage is higher than the overcurrent 1 detection voltage, the S-8261 Series releases the overcharge status.

Caution 1. If the battery is charged to a voltage higher than the overcharge detection voltage (V_{CU}) and the battery voltage does not fall below the overcharge detection voltage (V_{CU}) even when a heavy load is connected, the detection of overcurrent 1, overcurrent 2 and load short-circuiting do not function until the battery voltage falls below overcharge detection voltage (V_{CU}). Since an actual battery has an internal impedance of several dozens of $m\Omega$, the battery voltage drops immediately after a heavy load that causes overcurrent is connected, and the detection of overcurrent 1, overcurrent 2 and load short-circuiting function.

2. When a charger is connected after the overcharge detection, the overcharge status is not released even if the battery voltage is below the overcharge release voltage (V_{CL}). The overcharge status is released when the VM pin voltage goes over the charger detection voltage (V_{CHA}) by removing the charger.

4. Overdischarge Status

With power-down function

When the battery voltage falls below the overdischarge detection voltage (V_{DL}) during discharging under the normal status and the detection continues for the overdischarge detection delay time (t_{DL}) or longer, the S-8261 Series turns the discharging control FET off to stop discharging. This status is called the overdischarge status. When the discharging control FET is turned off, the VM pin voltage is pulled up by the resistor between VM and VDD in the IC (R_{VMD}). When the voltage difference between the VM and VDD then is 1.3 V (typ.) or lower, the current consumption is reduced to the power-down current consumption (I_{PDN}). This status is called the power-down status.

The power-down status is released when a charger is connected and the voltage difference between the VM and VDD becomes 1.3 V (typ.) or higher. Moreover when the battery voltage becomes the overdischarge detection voltage (V_{DL}) or higher, the S-8261 Series turns the discharging FET on and returns to the normal status.

Without power-down function

When the battery voltage falls below the overdischarge detection voltage (V_{DL}) during discharging under the normal status and the detection continues for the overdischarge detection delay time (t_{DL}) or longer, the S-8261 Series turns the discharging control FET off to stop discharging. This status is called the overdischarge status. When the discharging control FET is turned off, the VM pin voltage is pulled up by the resistor between VM and VDD in the IC (R_{VMD}).

When the battery voltage becomes the overdischarge detection voltage (V_{DL}) + overdischarge hysteresis voltage (V_{HD}) or higher, the S-8261 Series turns the discharging FET on and returns to the normal status.

5. Charger Detection

When a battery in the overdischarge status is connected to a charger and provided that the VM pin voltage is lower than the charger detection voltage (V_{CHA}), the S-8261 Series releases the overdischarge status and turns the discharging control FET on when the battery voltage becomes equal to or higher than the overdischarge detection voltage (V_{DL}) since the charger detection function works. This action is called charger detection.

When a battery in the overdischarge status is connected to a charger and provided that the VM pin voltage is not lower than the charger detection voltage (V_{CHA}), the S-8261 Series releases the overdischarge status when the battery voltage reaches the overdischarge detection voltage (V_{DL}) + overdischarge hysteresis voltage (V_{HD}) or higher.

6. Abnormal Charge Current Detection

If the VM pin voltage falls below the charger detection voltage (V_{CHA}) during charging under normal status and it continues for the overcharge detection delay time (t_{CU}) or longer, the charging control FET turns off and charging stops. This action is called the abnormal charge current detection.

Abnormal charge current detection works when the DO pin voltage is "H" and the VM pin voltage falls below the charger detection voltage (V_{CHA}). Consequently, if an abnormal charge current flows to an over-discharged battery, the S-8261 Series turns the charging control FET off and stops charging after the battery voltage becomes higher than the overdischarge detection voltage which make the DO pin voltage "H", and still after the overcharge detection delay time (t_{CU}) elapses.

Abnormal charge current detection is released when the voltage difference between VM pin and VSS pin becomes less than charger detection voltage (V_{CHA}).

7. Delay Circuit

The detection delay times are determined by dividing a clock of the approximately 3.5 kHz with the counter.

Remark 1. The detection delay time for overcurrent 2 (t_{IOV2}) and load short-circuiting (t_{SHORT}) start when the overcurrent 1 (V_{IOV1}) is detected. When the overcurrent 2 (V_{IOV2}) or load short-circuiting (V_{SHORT}) is detected over the detection delay time for each of them ($= t_{IOV2}$ or t_{SHORT}) after the detection of overcurrent 1 (V_{IOV1}), the S-8261 Series turns the FET off within t_{IOV2} or t_{SHORT} of each detection.

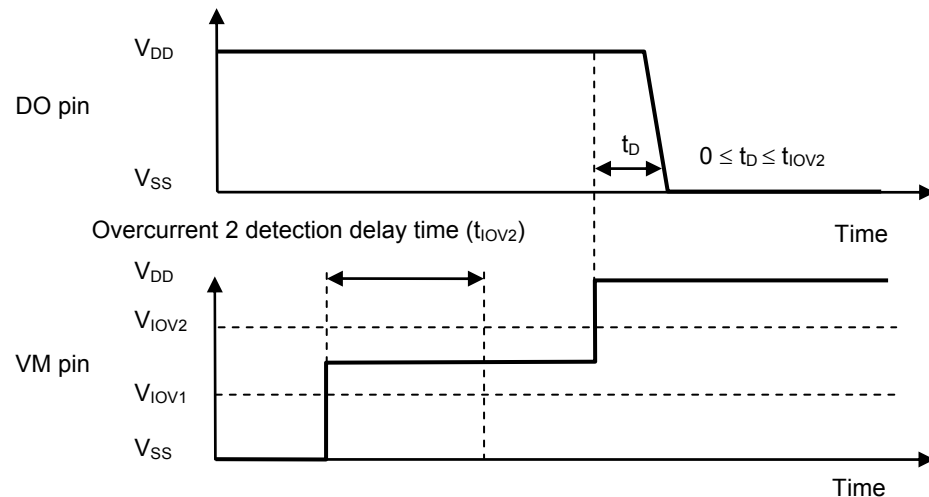


Figure 5

2. With power-down function

When the overcurrent is detected and continues for longer than the overdischarge detection delay time (t_{DL}) without releasing the load, the status changes to the power-down status when the battery voltage falls below the overdischarge detection voltage (V_{DL}). When the battery voltage falls below the overdischarge detection voltage (V_{DL}) due to the overcurrent, the S-8261 Series turns the discharging control FET off by the overcurrent detection. In this case if the recovery of the battery voltage is so slow that the battery voltage after the overdischarge detection delay time (t_{DL}) is still lower than the overdischarge detection voltage (V_{DL}), the S-8261 Series shifts to the power-down status.

Without power-down function

When the overcurrent is detected and continues for longer than the overdischarge detection delay time (t_{DL}) without released the load, the status changes to the overdischarge status when the battery voltage falls below overdischarge detection voltage (V_{DL}). When the battery voltage falls below overdischarge detection voltage (V_{DL}) due to the overcurrent, the S-8261 Series turns the discharging control FET off by the overcurrent detection. In this case, if the recovery of the battery voltage is so slow that the battery voltage after the overdischarge detection delay time (t_{DL}) is still lower than the overdischarge detection voltage (V_{DL}), the S-8261 Series shifts to the overdischarge status.

8. DP Pin

The DP pin is a test pin for delay time measurement and it should be open in the actual application. If a capacitor whose capacitance is larger than 1000 pF or a resistor whose resistance is less than 1 MΩ is connected to this pin, error may occur in the delay times or in the detection voltages.

9. 0 V Battery Charge Function “Available”

This function is used to recharge the connected battery whose voltage is 0 V due to the self-discharge. When the 0 V battery charge starting charger voltage (V_{0CHA}) or higher is applied between EB+ pin and EB– pin by connecting a charger, the charging control FET gate is fixed to VDD pin voltage. When the voltage between the gate and source of the charging control FET becomes equal to or higher than the turn-on voltage due to the charger voltage, the charging control FET is turned on to start charging. At this time, the discharging control FET is off and the charging current flows through the internal parasitic diode in the discharging control FET. When the battery voltage becomes equal to or higher than the overdischarge detection voltage (V_{DL}) and the overdischarge hysteresis voltage (V_{HD}), the S-8261 Series enters the normal status.

Caution Some battery providers do not recommend charging for completely self-discharged battery. Please ask battery providers before determine whether to enable or inhibit the 0 V battery charge function.

Remark The 0 V battery charge function has higher priority than the abnormal charge current detection function. Consequently, a product with the 0 V battery charging function is enabled charges a battery forcibly and abnormal charge current cannot be detected when the battery voltage is low.

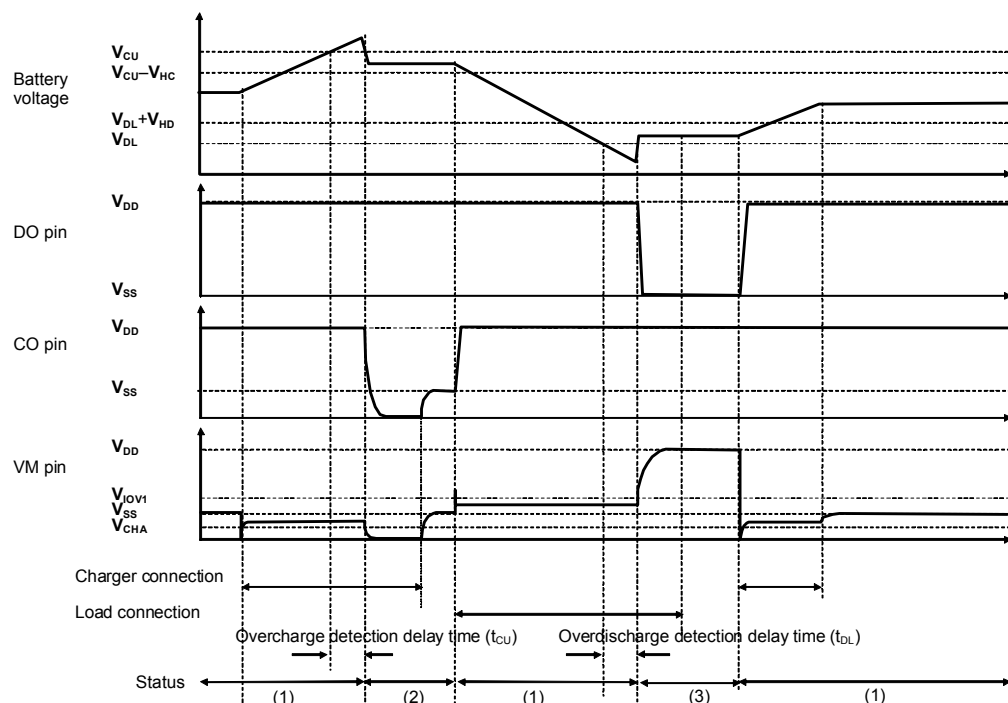
10. 0 V Battery Charge Function “Unavailable”

This function inhibits the recharging when a battery that is short-circuited (0 V battery) internally is connected. When the battery voltage is the 0 V battery charge inhibition battery voltage (V_{0INH}) or lower, the charging control FET gate is fixed to EB– pin voltage to inhibit charging. When the battery voltage is the 0 V battery charge inhibition battery voltage (V_{0INH}) or higher, charging can be performed.

Caution Some battery providers do not recommend charging for completely self-discharged battery. Please ask battery providers before determining the 0 V battery charge function.

■ Timing Chart

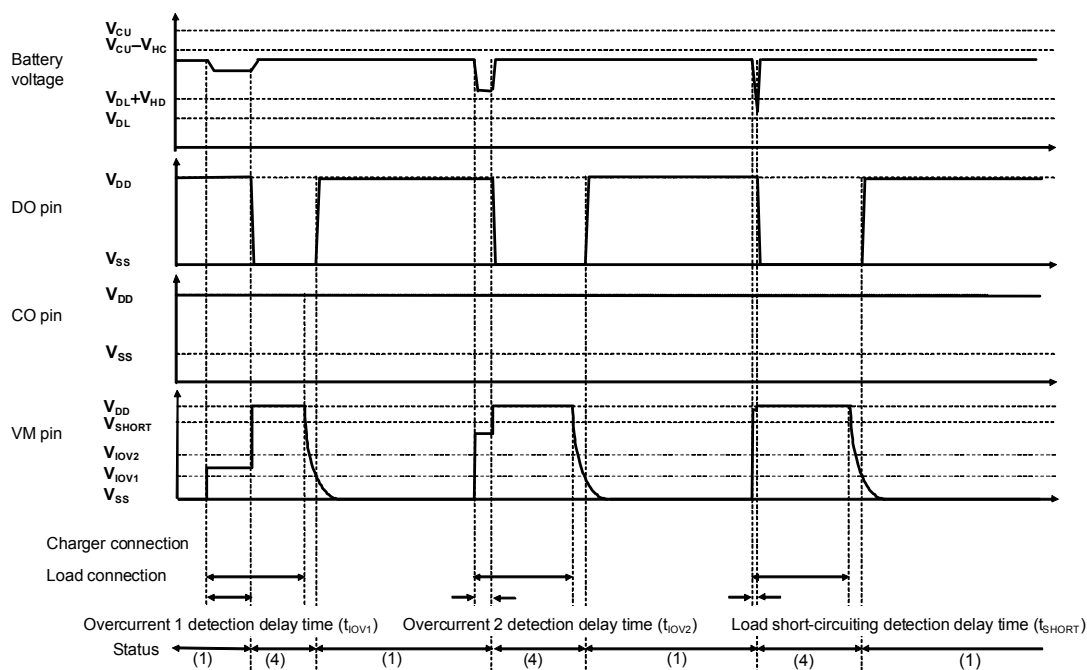
(1) Overcharge and Overdischarge Detection



Remark (1) Normal status, (2) Overcharge status, (3) Overdischarge status, (4) Overcurrent status
 The charger is supposed to charge with constant current.

Figure 6

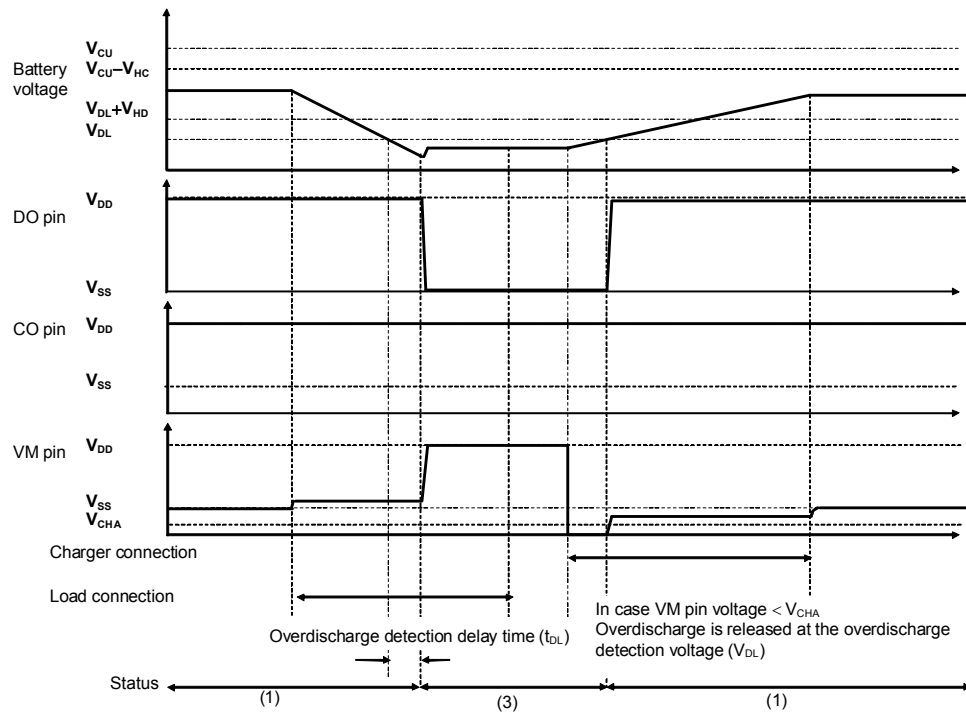
(2) Overcurrent Detection



Remark (1) Normal status, (2) Overcharge status, (3) Overdischarge status, (4) Overcurrent status
 The charger is supposed to charge with constant current.

Figure 7
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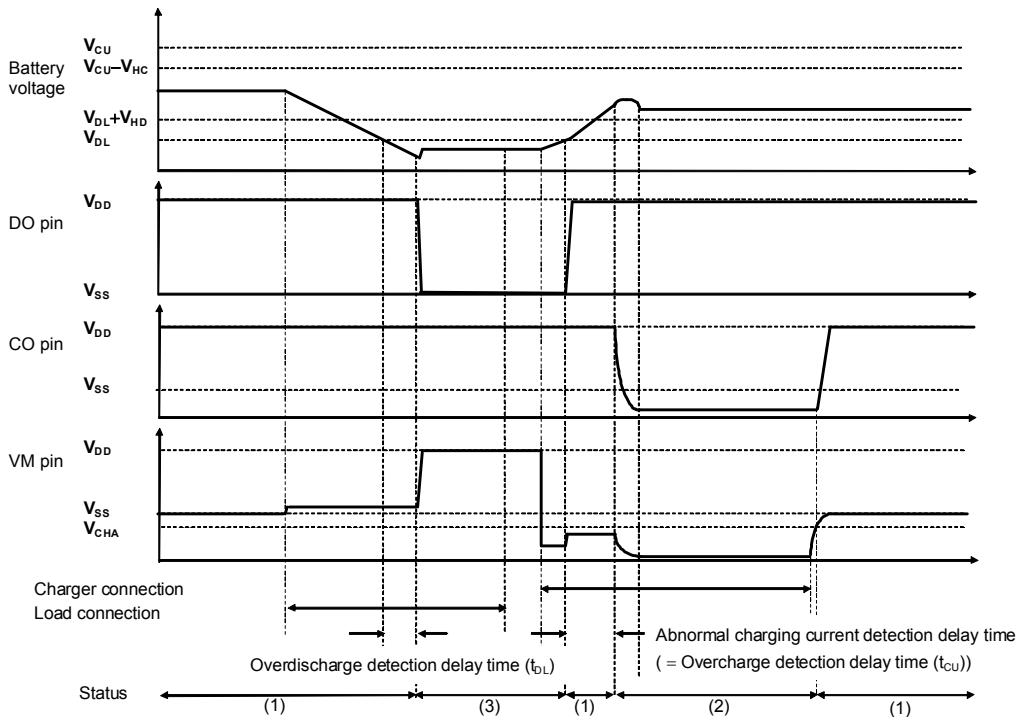
(3) Charger Detection



Remark (1) Normal status, (2) Overcharge status, (3) Overdischarge status, (4) Overcurrent status
The charger is supposed to charge with constant current.

Figure 8

(4) Abnormal Charge Current Detection



Remark (1) Normal status, (2) Overcharge status, (3) Overdischarge status, (4) Overcurrent status
The charger is supposed to charge with constant current.

Figure 9

■ Battery Protection IC Connection Example

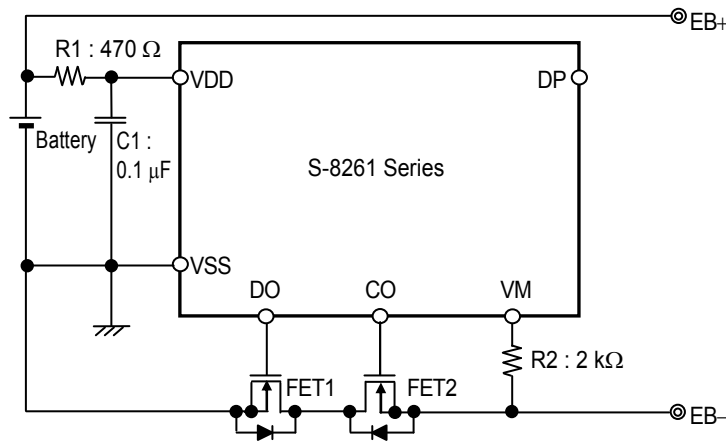


Figure 10

Table 17 Constant for External Components

Symbol	Part	Purpose	Min.	Typ.	Max.	Remarks
FET1	N-channel MOS FET	Discharge control	—	—	—	Threshold voltage $\leq$ Overdischarge detection voltage ^{*1} Gate to source withstanding voltage $\geq$ Charger voltage ^{*2}
FET2	N-channel MOS FET	Charge control	—	—	—	Threshold voltage $\leq$ Overdischarge detection voltage ^{*1} Gate to source withstanding voltage $\geq$ Charger voltage ^{*2}
R1	Resistor	ESD protection, For power fluctuation	300 Ω	470 Ω	1 k Ω	Resistance should be as small as possible to avoid lowering of the overcharge detection accuracy caused by VDD pin current. ^{*3}
C1	Capacitor	For power fluctuation	0.022 μ F	0.1 μ F	1.0 μ F	Install a capacitor of 0.022 μ F or higher between VDD and VSS. ^{*4}
R2	Resistor	Protection for reverse connection of a charger	300 Ω	2 k Ω	4 k Ω	Select a resistance as large as possible to prevent large current when a charger is connected in reverse. ^{*5}

- *1. If the threshold voltage of a FET is low, the FET may not cut the charging current.
If a FET with a threshold voltage equal to or higher than the overdischarge detection voltage is used, discharging may be stopped before overdischarge is detected.
- *2. If the withstanding voltage between the gate and source is lower than the charger voltage, the FET may be destroyed.
- *3. If R1 has a high resistance, the voltage between VDD and VSS may exceed the absolute maximum rating when a charger is connected in reverse since the current flows from the charger to the IC. Insert a resistor of 300 Ω or higher to R1 for ESD protection.
- *4. If a capacitor of less than 0.022 μ F is connected to C1, DO may oscillate when load short-circuiting is detected. Be sure to connect a capacitor of 0.022 μ F or higher to C1.
- *5. If R2 has a resistance higher than 4 k Ω , the charging current may not be cut when a high-voltage charger is connected.

Caution 1. The above constants may be changed without notice.

2. The DP pin should be open.

3. It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constant.

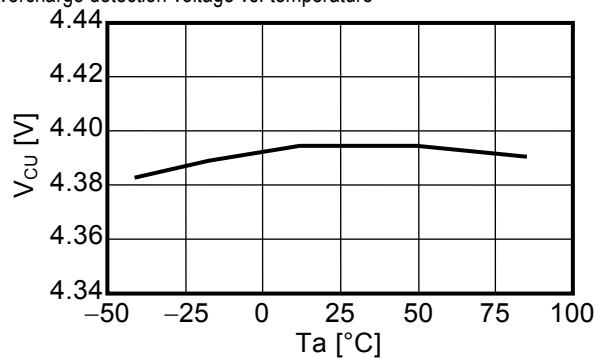
■ Precautions

- The application conditions for the input voltage, output voltage, and load current should not exceed the package power dissipation.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
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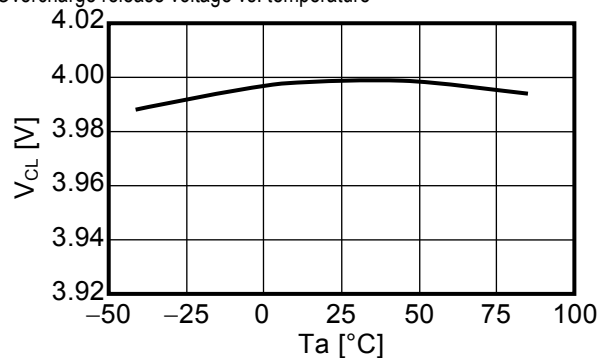
■ Characteristics (Typical Data)

1. Detection / Release Voltage Temperature Characteristics

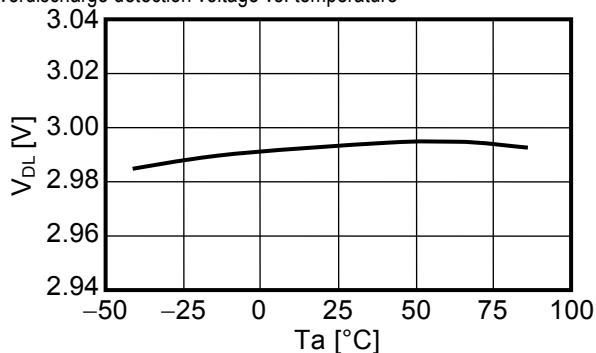
Overcharge detection voltage vs. temperature



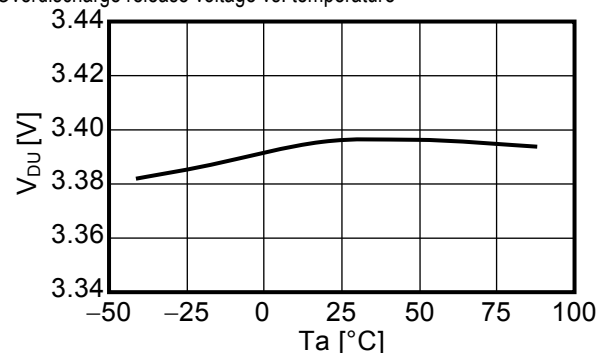
Overcharge release voltage vs. temperature



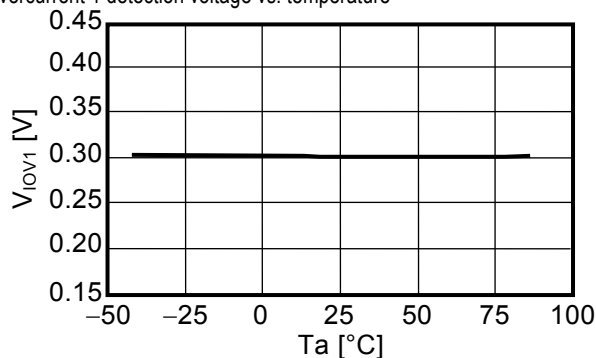
Overdischarge detection voltage vs. temperature



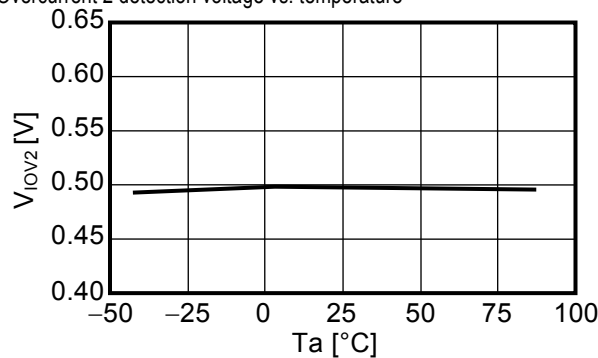
Overdischarge release voltage vs. temperature



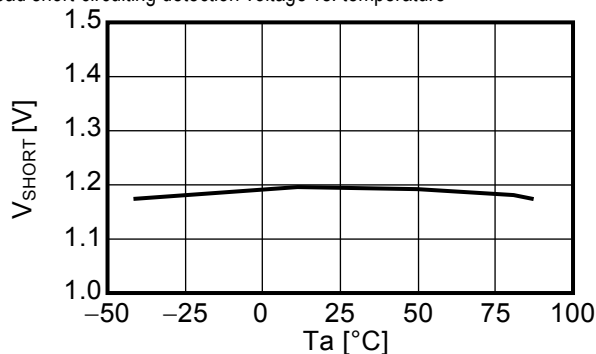
Overcurrent 1 detection voltage vs. temperature



Overcurrent 2 detection voltage vs. temperature

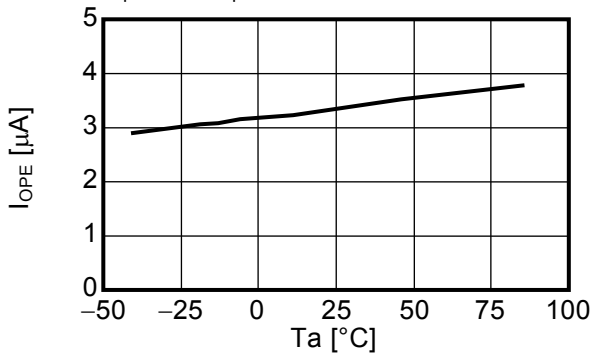


Load short-circuiting detection voltage vs. temperature

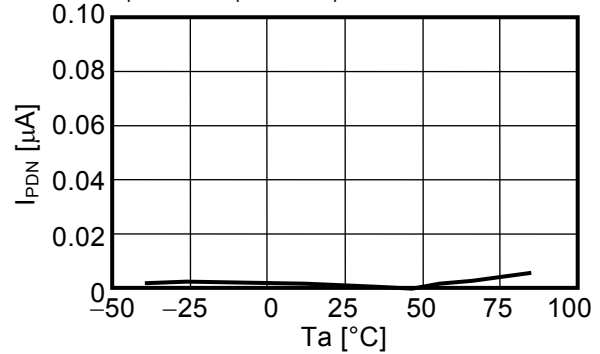


2. Current Consumption Temperature Characteristics

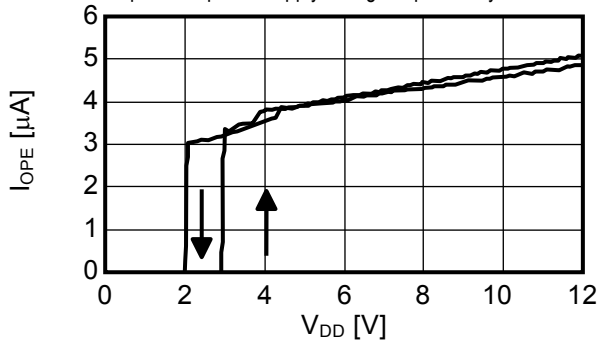
Current consumption vs. temperature in normal mode



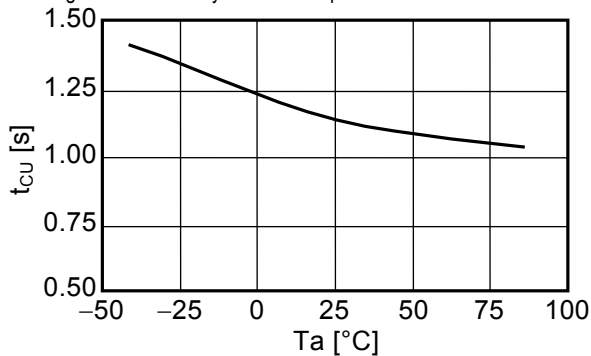
Current consumption vs. temperature in power-down mode

**3. Current Consumption Power Voltage Characteristics ($T_a = 25^{\circ}C$)**

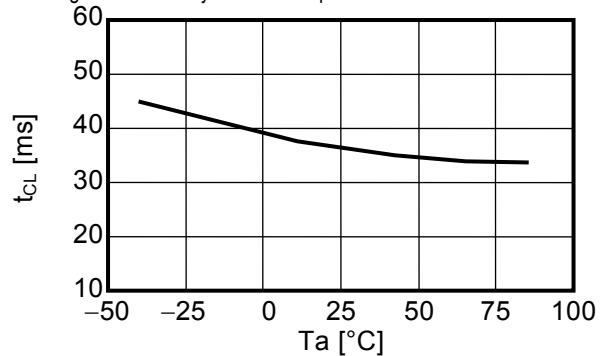
Current consumption vs. power supply voltage dependency

**4. Detection / Release Delay Time Temperature Characteristics**

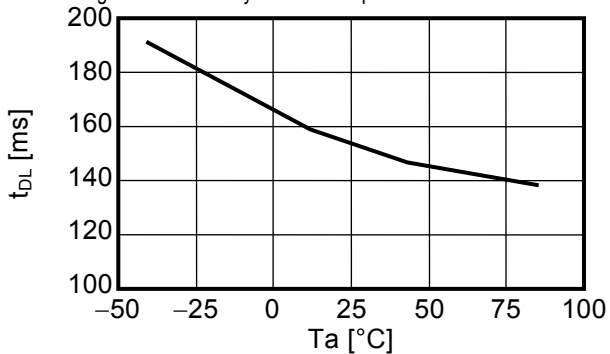
Overcharge detection delay time vs. temperature



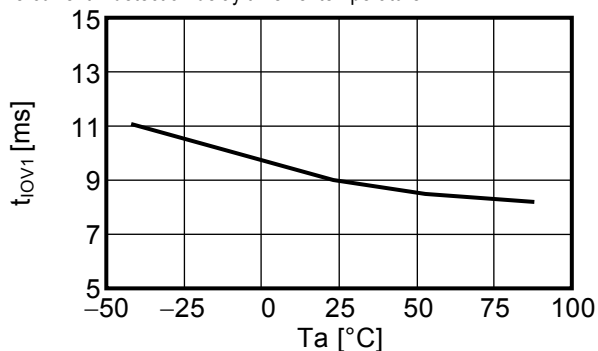
Overcharge release delay time vs. temperature



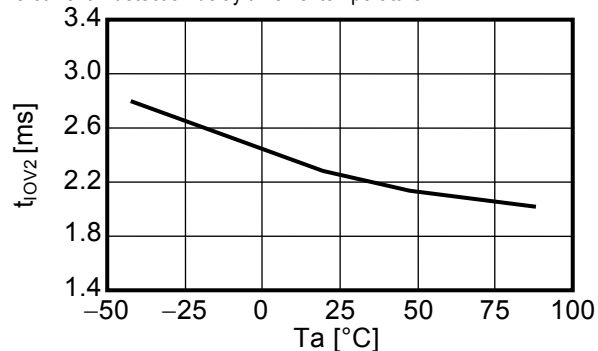
Overdischarge detection delay time vs. temperature



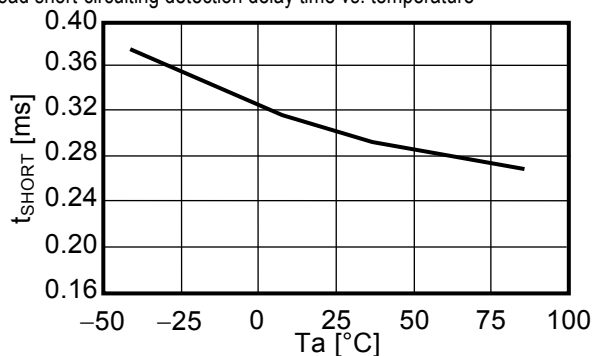
Overcurrent 1 detection delay time vs. temperature



Overcurrent 2 detection delay time vs. temperature

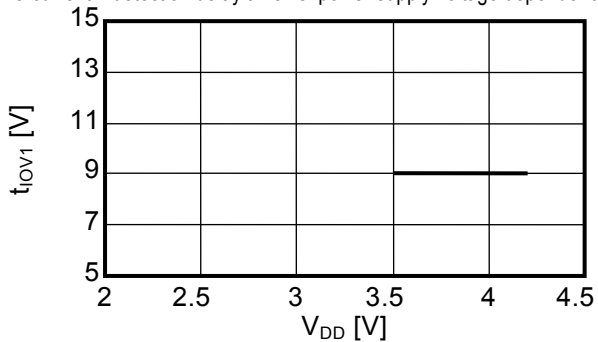


Load short-circuiting detection delay time vs. temperature

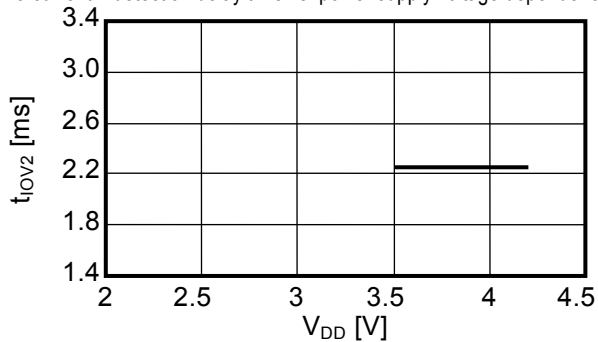


5. Delay Time Power-Voltage Characteristics ($T_a = 25^\circ\text{C}$)

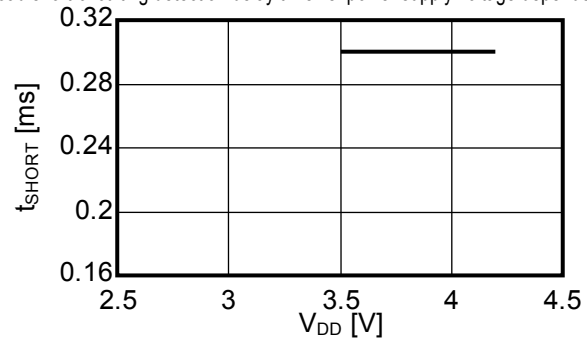
Overcurrent 1 detection delay time vs. power supply voltage dependency

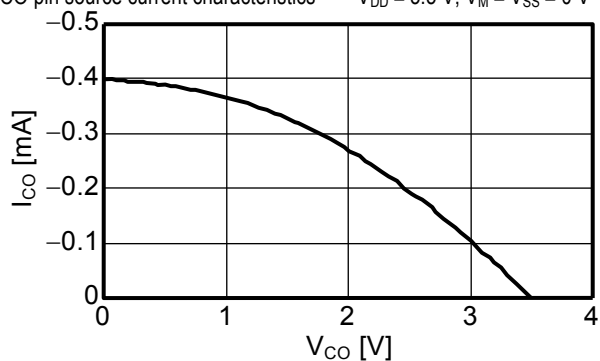
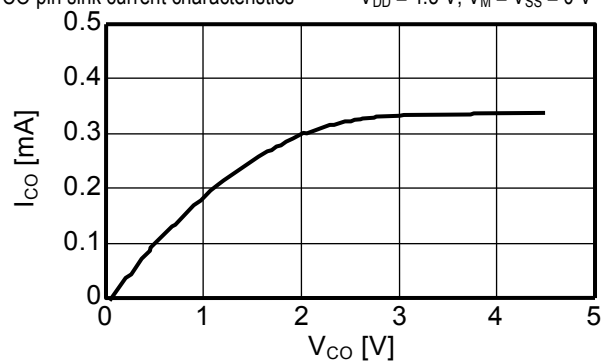
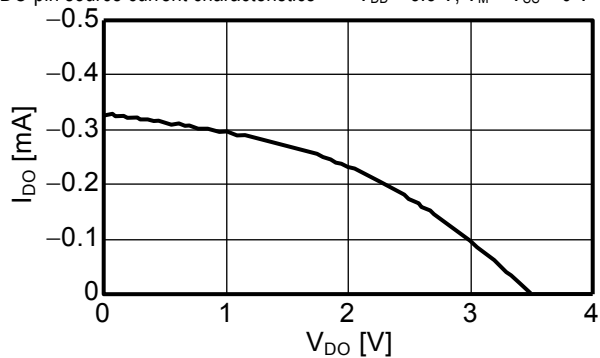
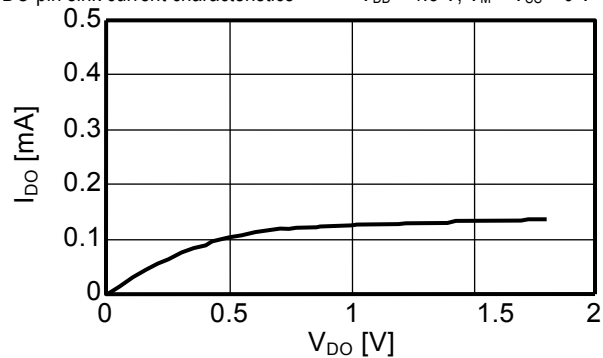


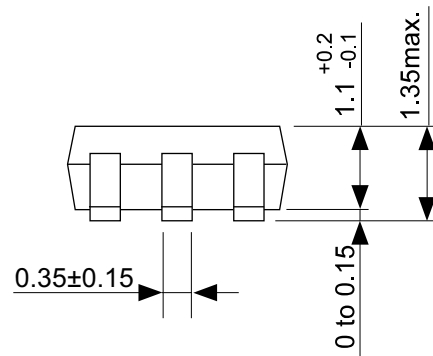
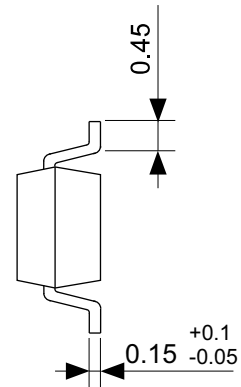
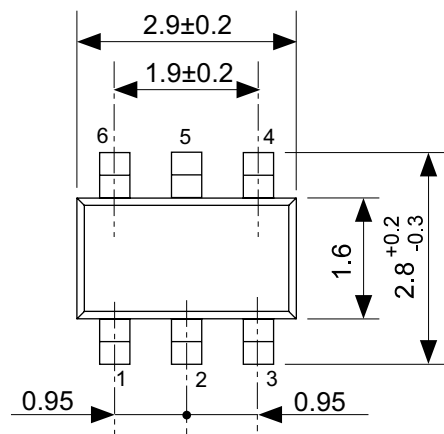
Overcurrent 2 detection delay time vs. power supply voltage dependency



Load short-circuiting detection delay time vs. power supply voltage dependency

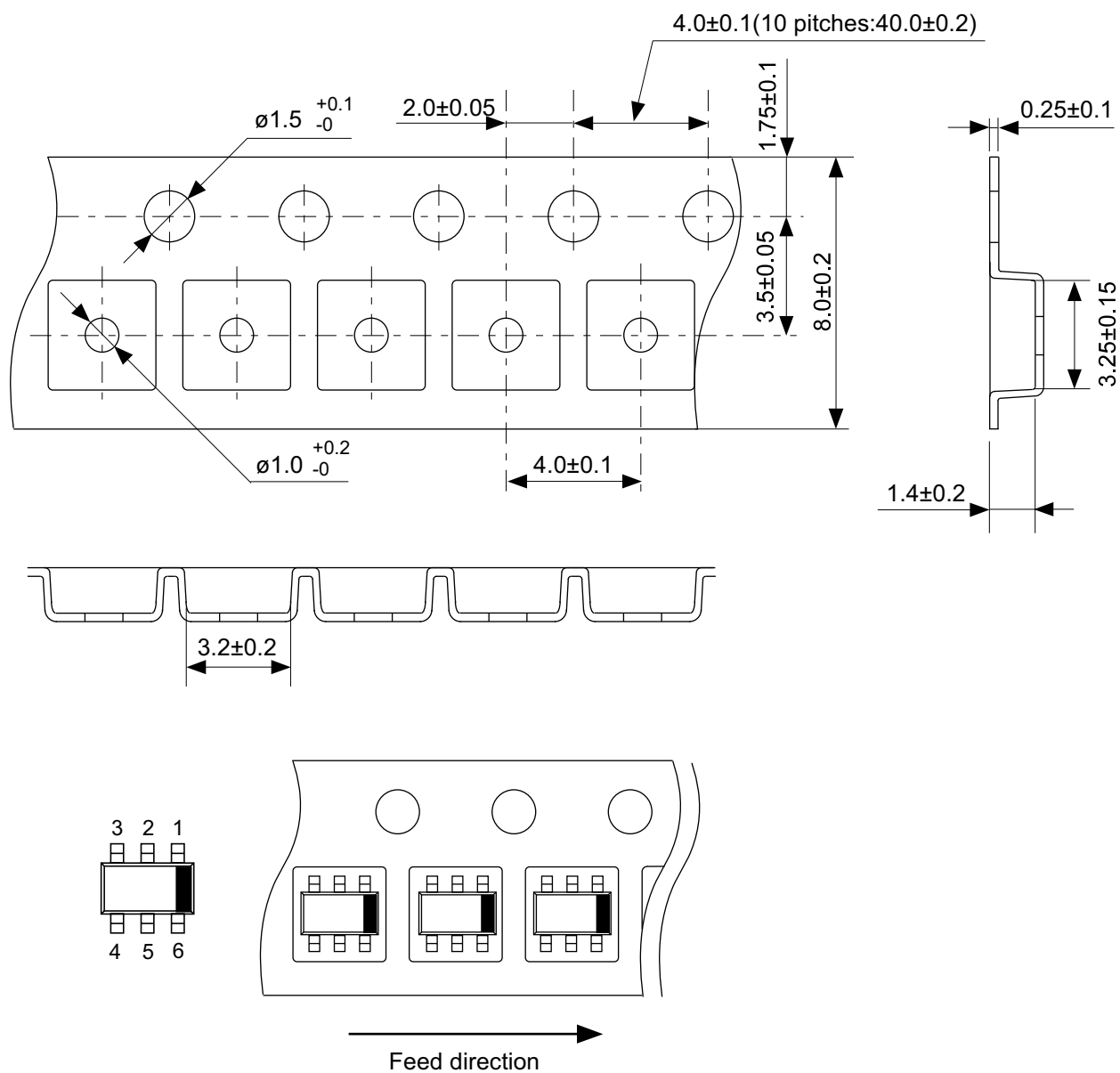


6. CO Pin / DO Pin Output Current Characteristics ($T_a = 25^\circ\text{C}$)CO pin source current characteristics $V_{DD} = 3.5\text{ V}$, $V_M = V_{SS} = 0\text{ V}$ CO pin sink current characteristics $V_{DD} = 4.5\text{ V}$, $V_M = V_{SS} = 0\text{ V}$ DO pin source current characteristics $V_{DD} = 3.5\text{ V}$, $V_M = V_{SS} = 0\text{ V}$ DO pin sink current characteristics $V_{DD} = 1.8\text{ V}$, $V_M = V_{SS} = 0\text{ V}$ 



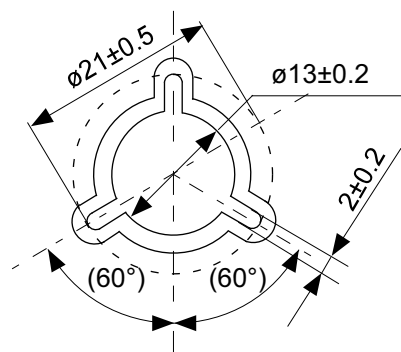
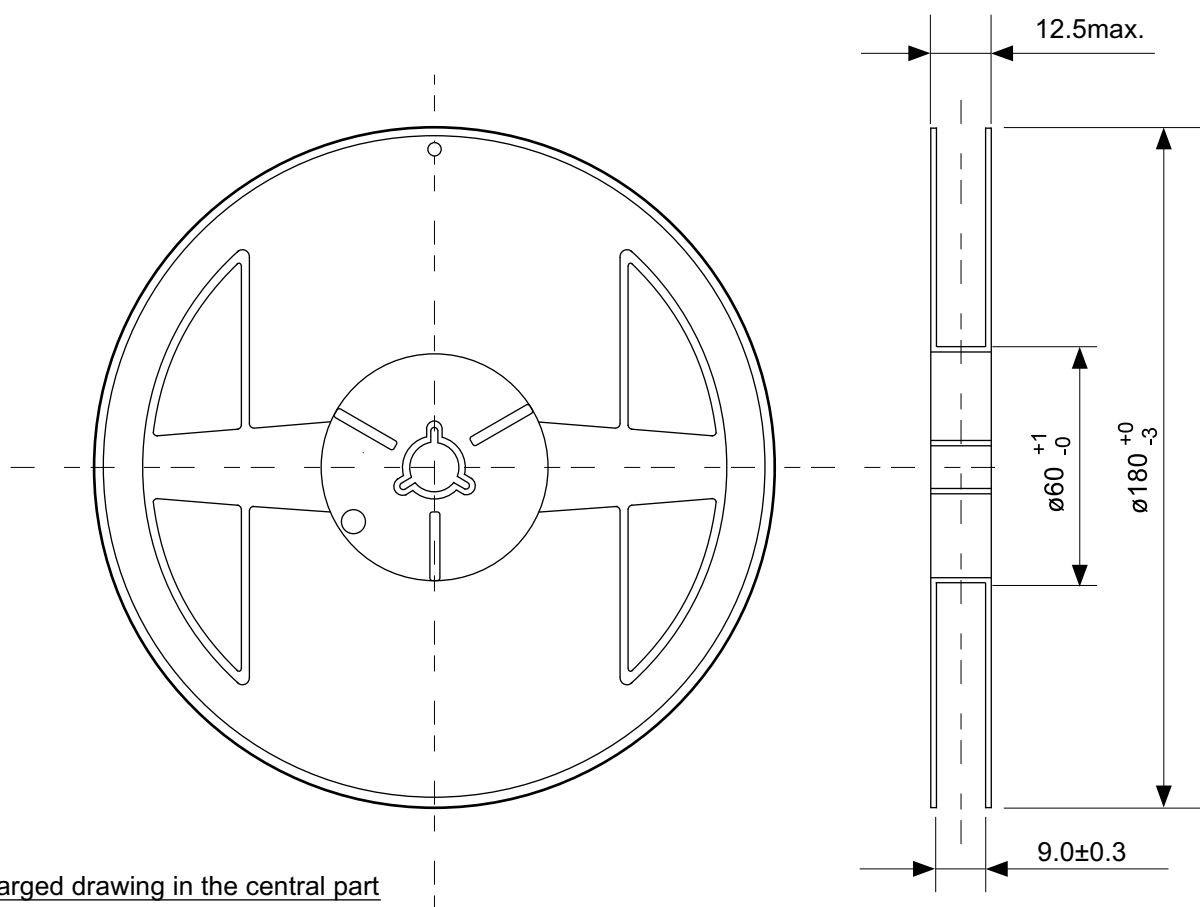
No. MP006-A-P-SD-2.1

TITLE	SOT236-A-PKG Dimensions
No.	MP006-A-P-SD-2.1
ANGLE	
UNIT	mm
ABLIC Inc.	



No. MP006-A-C-SD-3.1

TITLE	SOT236-A-Carrier Tape
No.	MP006-A-C-SD-3.1
ANGLE	
UNIT	mm
ABLIC Inc.	



No. MP006-A-R-SD-2.1

TITLE	SOT236-A-Reel		
No.	MP006-A-R-SD-2.1		
ANGLE		QTY	3,000
UNIT	mm		
ABLIC Inc.			

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2.4-2019.07