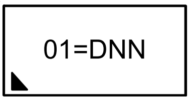
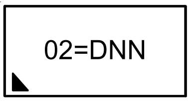
Marking Information

RT9728AHGE



01= : Product Code
DNN : Date Code

RT9728ALGE



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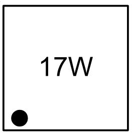

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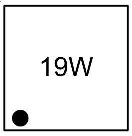

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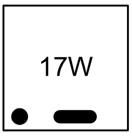

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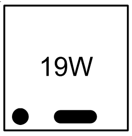
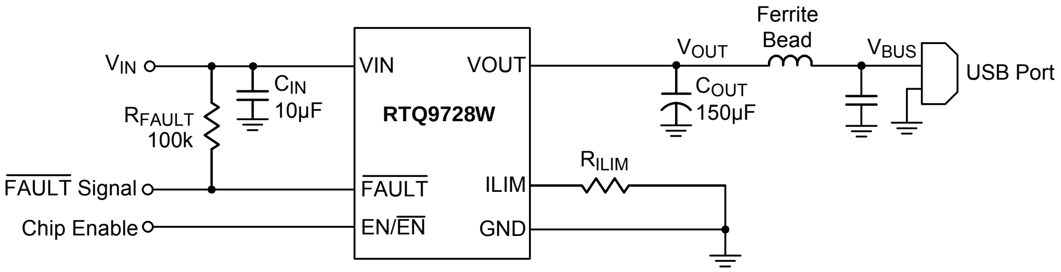


19 : Product Code
W : Date Code

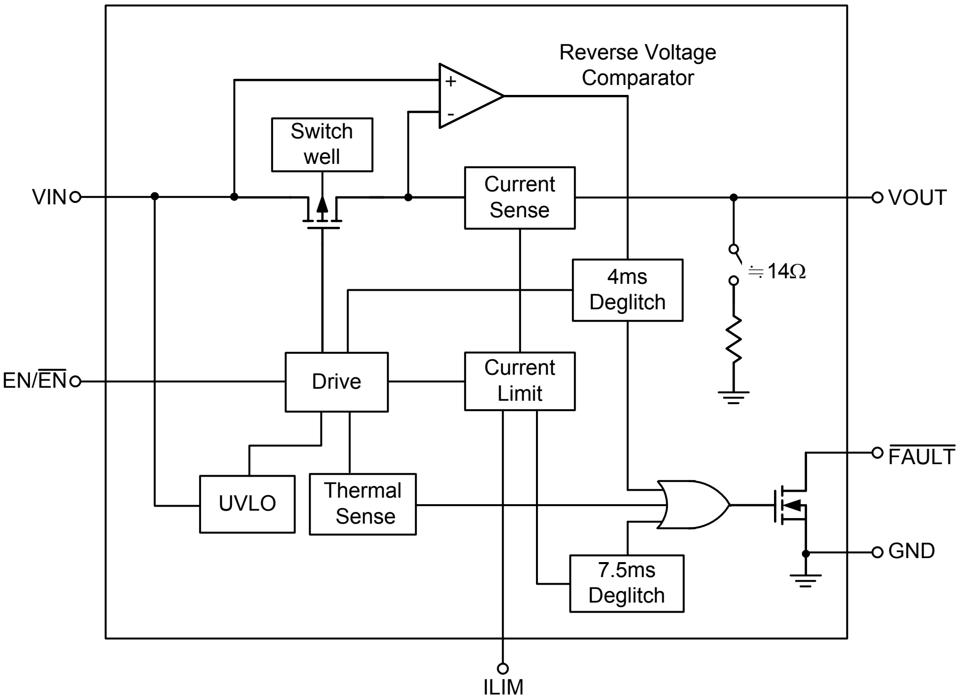
Typical Application Circuit



Functional Pin Description

Pin No.		Pin Name	Pin Function
SOT-23-6	WDFN-6L 2x2		
1	6	VIN	Input voltage.
2	5, 7 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
3	4	$EN/\overline{EN}$	Chip enable.
4	3	$\overline{FAULT}$	Active-low open-drain output. Asserted during over-current, over-temperature, or reverse-voltage conditions.
5	2	ILIM	Current limit set pin. External resistor is used to set current limit threshold, and 19.1kΩ ≤ R_{ILIM} ≤ 232kΩ is recommended.
6	1	VOUT	Power switch output.

Functional Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage -- –0.3V to 6V
- Other Pin Voltage -- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  - SOT-23-6 -- 0.4W
  - WDFN-6L 2x2 -- 0.606W
- Package Thermal Resistance (Note 2)
  - SOT-23-6, θ_{JA} -- 250°C/W
  - WDFN-6L 2x2, θ_{JA} -- 165°C/W
  - WDFN-6L 2x2, θ_{JC} -- 7°C/W
- Lead Temperature (Soldering, 10 sec.) -- 260°C
- Junction Temperature -- 150°C
- Storage Temperature Range -- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) -- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VIN -- 2.5V to 5.5V
- Junction Temperature Range -- –40°C to 125°C
- Ambient Temperature Range -- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 3.6V, 19.1kΩ ≤ R_{ILIM} ≤ 232kΩ, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions		Min	Typ	Max	Unit
EN Input Voltage	Logic-High	V_{IH}			1.1	--	--	V
	Logic- Low	V_{IL}			--	--	0.66	
Current Limit Threshold Resistor Range		R_{ILIM}	(nominal 1%) from ILIM to GND		19.1	--	232	kΩ
Under Voltage Lockout Threshold		V_{UVLO}	V_{IN} rising		--	2.3	--	V
			V_{IN} falling		--	2.1	--	
Shutdown Current		I_{SHDN}	V_{IN} = 5.5V, no load on V_{OUT}, V_{EN} = 0V		--	1	3	μA
Quiescent Current		I_Q	V_{IN} = 5.5V, no load on V_{OUT}	R_{ILIM} = 20kΩ	--	120	170	μA
				R_{ILIM} = 210kΩ	--	120	170	
Reverse Leakage Current		I_{REV}	V_{OUT} = 5.5V, V_{IN} = 0V		--	1	3	μA
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	I_{SW} = 0.2A		--	120	--	mΩ
Current Limit		I_{LIM}	R_{ILIM} = 20kΩ		1190	1295	1400	mA
			R_{ILIM} = 49.9kΩ		468	520	572	
			R_{ILIM} = 210kΩ		110	130	150	
			ILIM shorted to VIN		50	75	100	
Reverse Voltage Comparator Trip Point (V_{OUT} – V_{IN})					--	135	--	mV

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
$\overline{\text{FAULT}}$ Output Low Voltage	V_{OL}	$I_{\overline{\text{FAULT}}}$ = 1mA	--	180	--	mV
$\overline{\text{FAULT}}$ Off State Leakage		$V_{\overline{\text{FAULT}}}$ = 5.5V	--	1	--	μA
$\overline{\text{FAULT}}$ Deglitch		$\overline{\text{FAULT}}$ assertion or de-assertion due to over current condition	5	7.5	10	ms
		$\overline{\text{FAULT}}$ assertion or de-assertion due to reverse voltage condition	2	4	6	
$\overline{\text{FAULT}}$ Flag Assertion Offset	$V_{\overline{\text{FAULT}}\_OFS}$	Offset between fault flag assertion level versus ILIM trigger level (Note 5)	−100	--	0	mA
Thermal Shutdown Temperature	T_{SD}	(Note 5)	--	160	--	°C

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

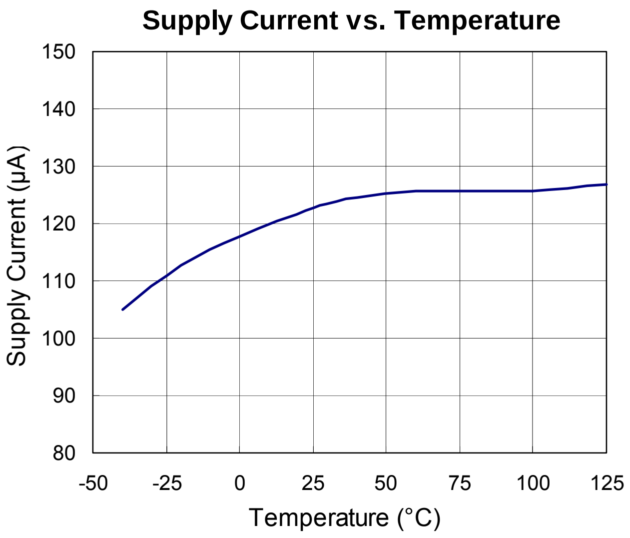
Note 2. θ_{JA} is measured at T_A = 25°C on a low effective thermal conductivity single-layer test board per JEDEC 51-3. θ_{JC} is measured at the exposed pad of the package.

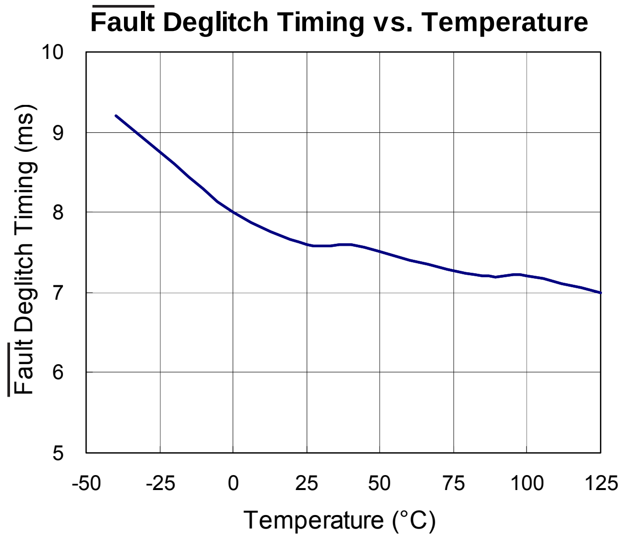
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

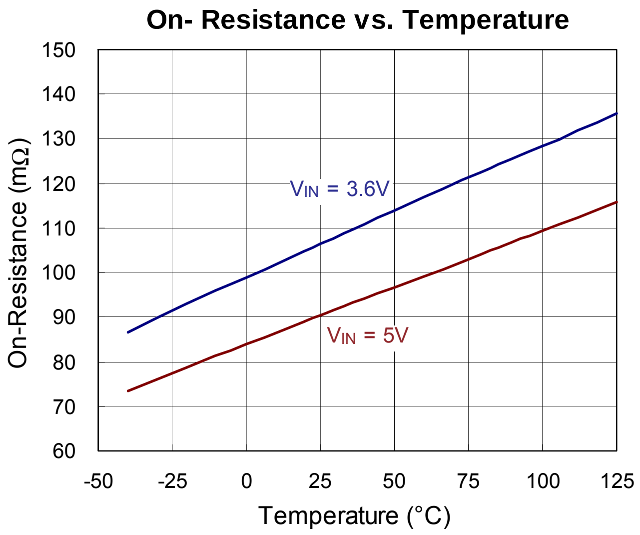
Note 4. The device is not guaranteed to function outside its operating conditions.

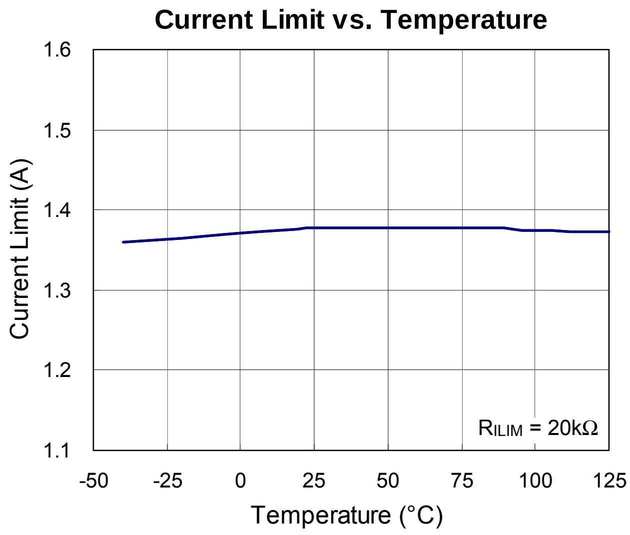
Note 5. Guarantee by design.

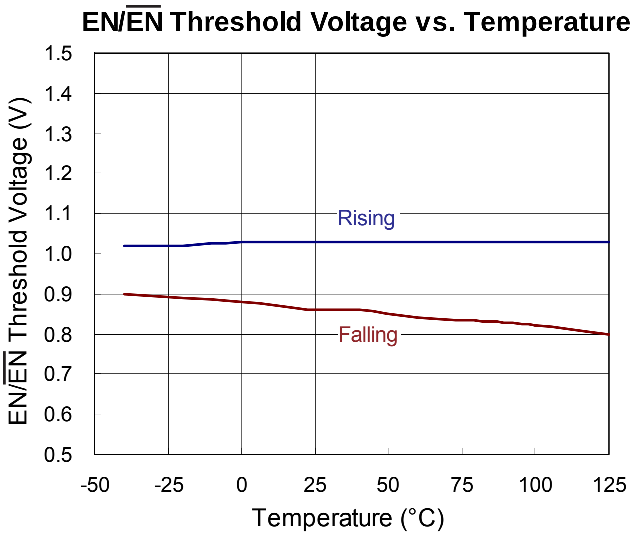
Typical Operating Characteristics

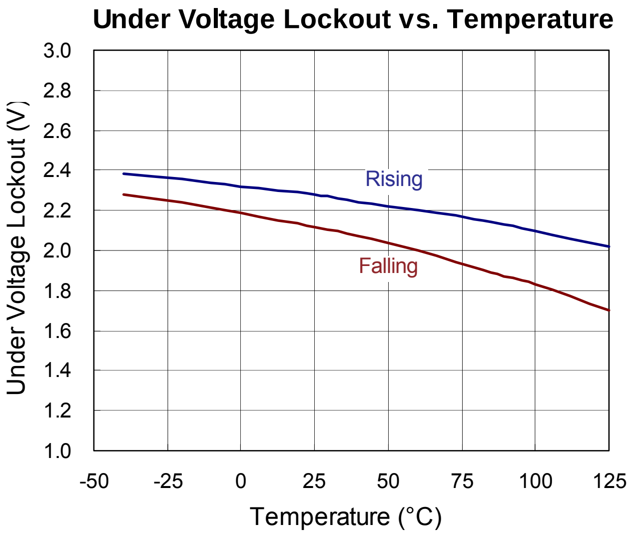

Supply Current vs. Temperature


$\overline{\text{Fault}}$ Deglitch Timing vs. Temperature

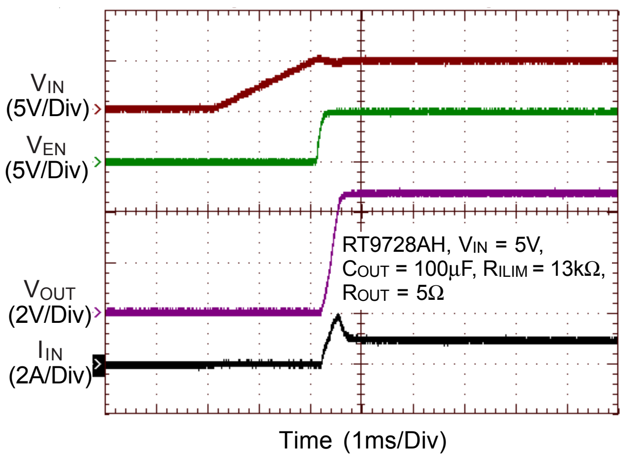

On- Resistance vs. Temperature


Current Limit vs. Temperature

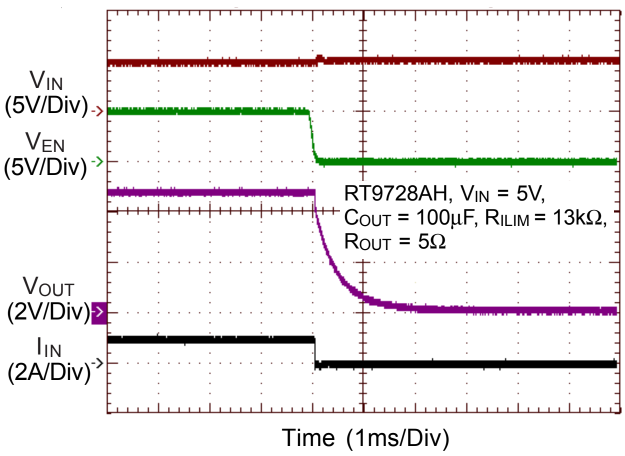

EN/$\overline{\text{EN}}$ Threshold Voltage vs. Temperature


Under Voltage Lockout vs. Temperature

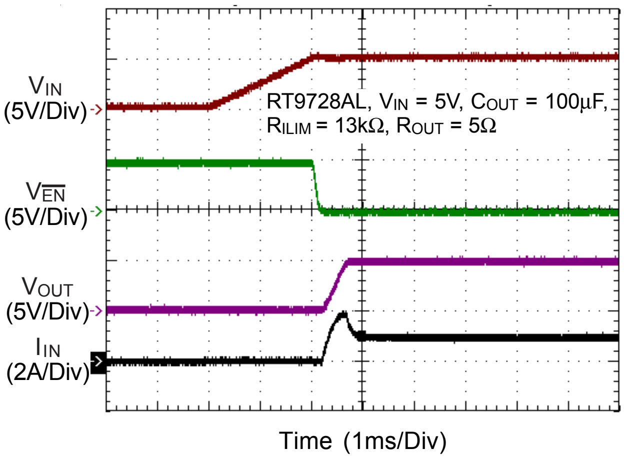
Power On from EN



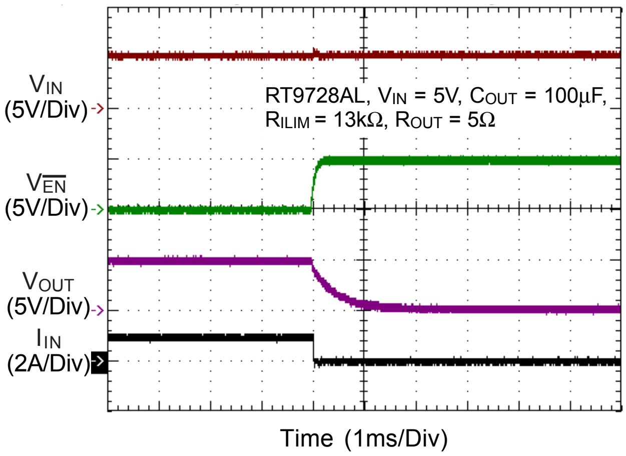
Power Off from EN



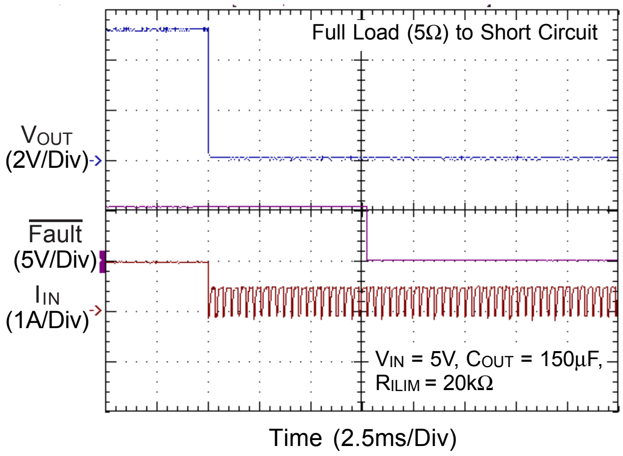
Power On from $\overline{\text{EN}}$



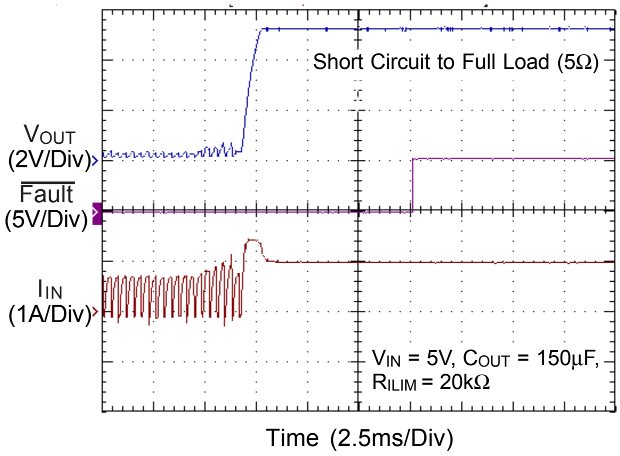
Power Off from $\overline{\text{EN}}$

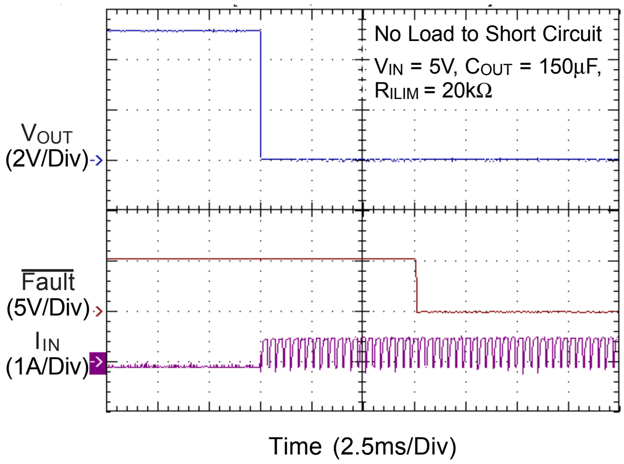


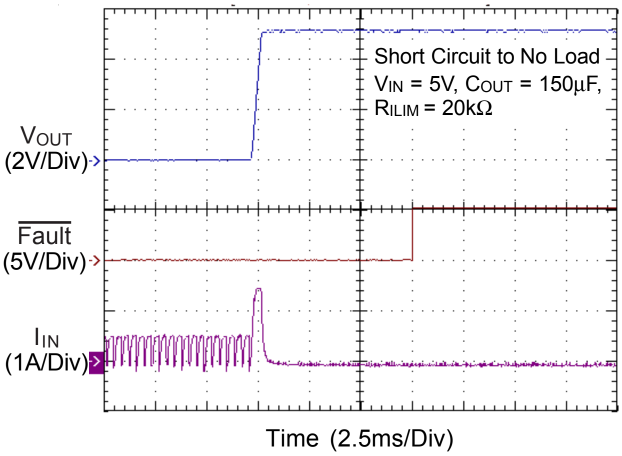
Current Limit

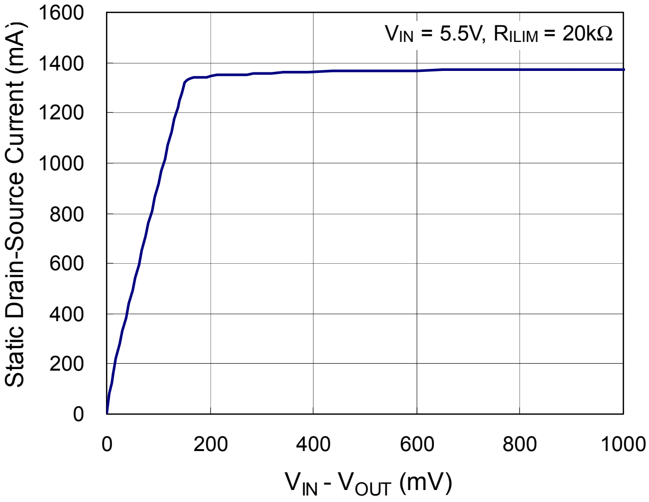


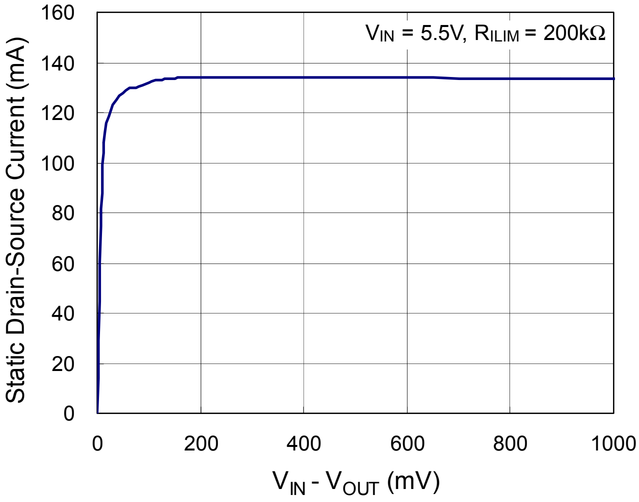
Current Limit




Current Limit


Current Limit


Static Drain-Source Current vs. V_{IN} - V_{OUT}


Static Drain-Source Current vs. V_{IN} - V_{OUT}

Applications Information

The RT9728A is a single P-MOSFET high-side power switch with active-high/low enable input, optimized for self-powered and bus-powered Universal Serial Bus (USB) applications. The switch's low $R_{DS(ON)}$ meets USB voltage drop requirements and a flag output is available to indicate fault conditions to the local USB controller.

Current Limiting and Short-Circuit Protection

When a heavy load or short circuit situation occurs while the switch is enabled, large transient current may flow through the device. The RT9728A includes a current-limit circuitry to prevent these large currents from damaging the MOSFET switch and the hub downstream ports. The RT9728A provides an adjustable current limit threshold between 120mA and 1.3A (typ) via an external resistor, R_{ILIM}, between 19.1kΩ and 232kΩ. However, if the ILIM pin is connected to V_{IN}, the current limit threshold will be 75mA (typ). The maximum –100mA fault flag assertion offset needs cautions, especially for very low ILIM applications. Taking the application of ILIM = 250mA as an example, the minimum fault flag assertion level might be 150mA (40% error versus its target). For short ILIM to VIN condition (75mA), the fault flag may go low. Once the current limit threshold is exceeded, the device enters constant-current mode until either thermal shutdown occurs or the fault is removed. The table1 shows a recommended current limit value vs. R_{ILIM} resistor.

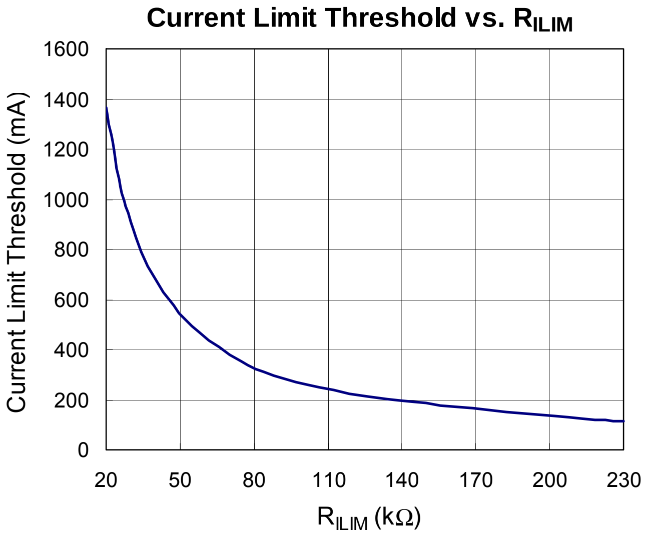


Figure 1. Current Limit Threshold vs R_{ILIM}

Table 1. Recommended R_{ILIM} Resistor Selections

Desired Nominal Current Limit (mA)	Ideal Resistor (kΩ)	Closet 1% Resistor (kΩ)	Actual Limits (Include R Tolerance)		
			IOS Min (mA)	IOS Nom (mA)	IOS Max (mA)
75	Short ILIM to VIN		50.0	75.0	100.0
120	226.1	226.0	101.3	120.0	142.1
200	134.0	133.0	173.7	201.5	233.9
300	88.5	88.7	262.1	299.4	342.3
400	65.9	66.5	351.1	396.7	448.7
500	52.5	52.3	443.9	501.6	562.4
600	43.5	43.2	535.1	604.6	674.1
700	37.2	37.4	616.0	696.0	776.0
800	32.4	32.4	708.7	800.8	892.9
900	28.7	28.7	797.8	901.5	1005.2
1000	25.8	26.1	875.4	989.1	1102.8
1100	23.4	23.2	982.1	1109.7	1237.3
1200	21.4	21.5	1057.9	1195.4	1332.9
1300	19.7	19.6	1178.0	1308.5	1439.0

Fault Flag

The RT9728A provides a $\overline{\text{FAULT}}$ signal pin which is an N-channel open drain MOSFET output. This open drain output goes low when current exceeds current limit threshold, $V_{OUT} - V_{IN}$ exceeds reverse voltage trip level, or the die temperature exceeds 160°C approximately. The $\overline{\text{FAULT}}$ output is capable of sinking a 1mA load to typically 180mV above ground. The $\overline{\text{FAULT}}$ pin requires a pull-up resistor; this resistor should be large in value to reduce energy drain. A 100kΩ pull-up resistor works well for most applications. In case of an over-current condition, $\overline{\text{FAULT}}$ will be asserted only after the flag response delay time, tD, has elapsed. This ensures that $\overline{\text{FAULT}}$ is asserted upon valid over-current conditions and that erroneous error reporting is eliminated. For example, false over-current conditions may occur during hot-plug events when extremely large capacitive loads are connected, which induces a high transient inrush current that exceeds the current limit threshold. The $\overline{\text{FAULT}}$ response delay time, t_D, is typically 7.5ms.

Supply Filter/Bypass Capacitor

A 10μF low ESR ceramic capacitor connected from V_{IN} to GND and located close to the device is strongly recommended to prevent input voltage drooping during hot-plug events. However, higher capacitor values may be used to further reduce the voltage droop on the input. Without this bypass capacitor, an output short may cause sufficient ringing on the input (from source lead inductance) to destroy the internal control circuitry. Note that the input transient voltage must never exceed 6V as stated in the Absolute Maximum Ratings.

Output Filter Capacitor

Standard bypass methods should be used to minimize inductance and resistance between the bypass capacitor and the downstream connector to reduce EMI and decouple voltage droop caused by hot-insertion transients in downstream cables. Ferrite beads in series with VBUS, the ground line and the bypass capacitors at the power connector pins are recommended for EMI and ESD protection. The bypass capacitor itself should have a low dissipation factor to allow decoupling at higher frequencies. For commercial applications where the ambient temperature is 0°C to 70°C (such as a PC or USB hub), the RT9728A supports an output capacitor range of up to 120μF. For industrial applications with an ambient temperature of −40°C to 125°C, please limit the output capacitance to less than 50μF to ensure normal startup.

Chip Enable Input

The RT9728AH/L will be disabled when the EN/$\overline{\text{EN}}$ pin is in a logic-low/high condition. During this condition, the internal circuitry and MOSFET are turned off, reducing the supply current to 1μA typical. Floating the input may cause unpredictable operation and the EN/$\overline{\text{EN}}$ should not be allowed to go negative with respect to GND. The EN/$\overline{\text{EN}}$ signal must be asserted after input voltage ready or higher than UVLO threshold to satisfy the power sequence.

Under-Voltage Lockout

Under-voltage lockout (UVLO) prevents the MOSFET switch from turning on until input voltage exceeds approximately 2.3V (typ.). If input voltage drops below approximately 2.1V (typ.), UVLO turns off the MOSFET switch.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For SOT-23-6 packages, the thermal resistance, θ_{JA}, is 250°C/W on a standard JEDEC 51-3 single-layer thermal test board. For WDFN-6L 2x2 packages, the thermal resistance, θ_{JA}, is 165°C/W on a standard JEDEC 51-3 single-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C − 25°C) / (250°C/W) = 0.400W for SOT-23-6 package

$P_{D(MAX)}$ = (125°C − 25°C) / (165°C/W) = 0.606W for WDFN-6L 2x2 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curves in Figure 2 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

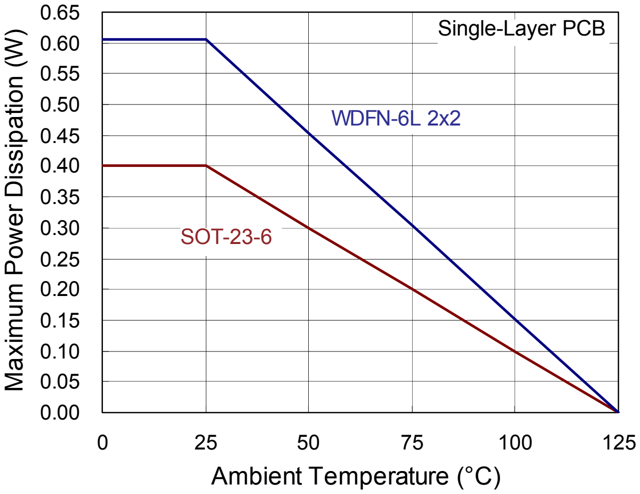
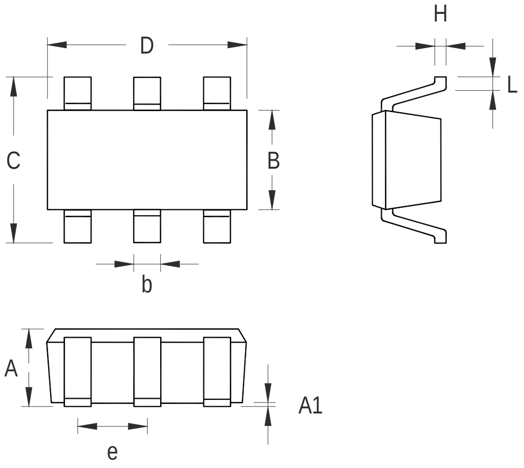


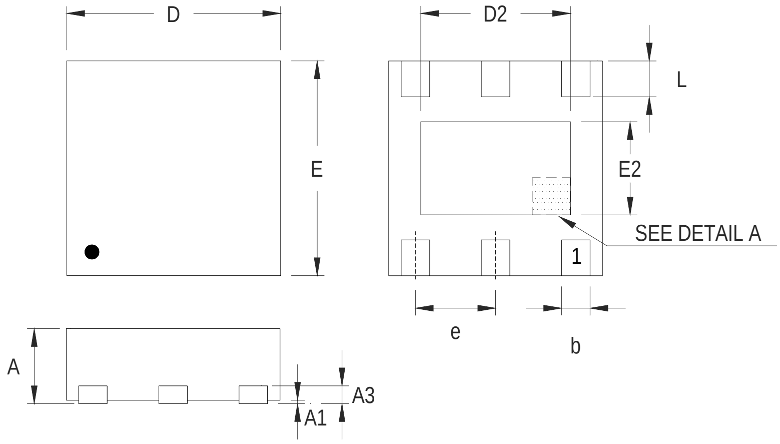
Figure 2. Derating Curve of Maximum Power Dissipation

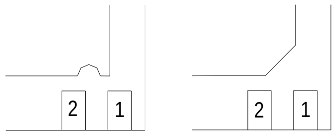
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.031	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.250	0.560	0.010	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

SOT-23-6 Surface Mount Package





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.350	0.008	0.014
D	1.950	2.050	0.077	0.081
D2	1.000	1.450	0.039	0.057
E	1.950	2.050	0.077	0.081
E2	0.500	0.850	0.020	0.033
e	0.650		0.026	
L	0.300	0.400	0.012	0.016

W-Type 6L DFN 2x2 Package

Richtek Technology Corporation

14F, No. 8, Tai Yuen 1st Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789