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REVISION HISTORY

Date	Revision #	Description
10/18/2008	1.0	Released Version 1.0 Datasheets
04/14/2009	1.1	Revised General Feature to reflect I-temp
10/10/2009	1.2	Updated Pin Description of PCI Express Signals
12/14/2009	1.3	Updated Pin Description of Power and Ground Pins
02/08/2009	1.4	Updated Section 10.2 System Management Bus
02/22/2010	1.5	Updated ESD Capability
05/20/2010	1.6	Updated Section 7 GPIO Pins and SM Bus Address
04/27/2011	1.7	Updated Section 2.2 PCI Express Signals
06/29/2011	1.8	Updated Section 2.3 PCI Signals (REQ_L [3:0], GNT_L [3:0])
05/19/2015	1.9	Added Section 15.4 PCIe Reference clock timing parameter
04/21/2016	2.0	Updated the Section 2.5 JTAG Boundary Scan Signals
01/23/2017	2.1	Updated Logo Added 6.3.93 Extended Configuration Access Address Register – Offset E0h Added 6.3.94 Extended Configuration Access Data Register – Offset E4h Added Table 15-5 PCI Express Interface - Differential Transmitter (TX) Output Characteristics AddedTable 15-6 PCI Express Interface - Differential Receiver (RX) Input Characteristics Added Section 15.4 Operating Ambient Temperature Updated Section 2.8 Pin Assignments Updated 6.3.95 Reserved Registers – Offset E8h – ECh Updated Section 15.1 AbsolutE Maximum Ratings Updated Section 15.2 DC Specifications
09/27/2017	3	Added Section 15 Power Sequencing Updated Section 18 Ordering Information Revision numbering system changed to whole number
07/30/2018	4	Updated Section 1.3 General Features Updated Section 6.3 PCI Configuration Registers Added 17-2 Part Marking
10/31/2018	5	Updated 6.3.76 Device Capability Register – OFFSET B4h Updated Section 18 Ordering Information
04/09/2020	6	Updated Section 15 Power Sequencing Added Section 15.2 Power-Off Sequence
07/03/2020	7	Updated 6.3.87 XPIP Configuration Register 2 – OFFSET D4h
01/18/2021	8	Updated Section 15 Power Sequencing

PREFACE

The datasheet of PI7C9X111SL will be enhanced periodically when updated information is available. Thetechnical information in this datasheet is subject to change without notice. This document describes the functionalities of PI7C9X111SL (PCI Express Bridge) and provides technical information for designers to design their hardware using PI7C9X111SL.

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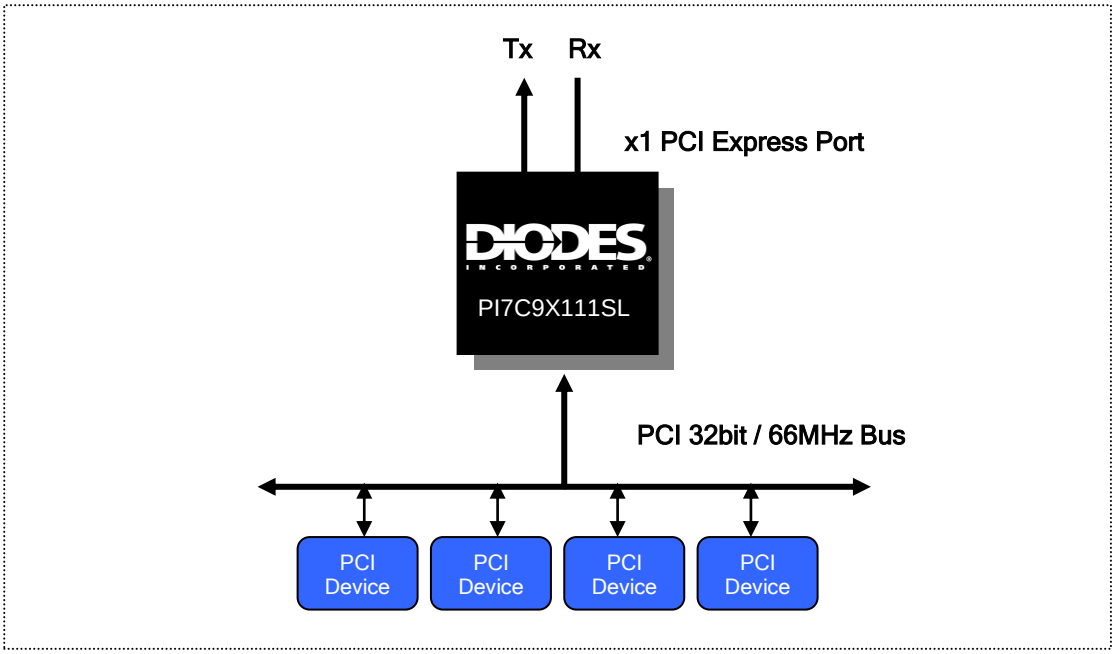
1 INTRODUCTION

PI7C9X111SL is a PCIe-to-PCI/PCI-X bridge. PI7C9X111SL is compliant with the *PCI Express Base Specification*, Revision 1.1, the *PCI Express Card Electromechanical Specification*, Revision 1.1, the *PCI Local Bus Specification*, Revision 3.0 and *PCI Express to PCI/PCI-X Bridge Specification*, Revision 1.0. PI7C9X111SL supports transparent mode operation. Also, PI7C9X111SL supports forward and reverse bridging. In forward bridge mode, PI7C9X111SL has an x1 PCI Express upstream port and a 32-bit PCI downstream port. The 32-bit PCI downstream port is 66MHz capable (see figure 1-1). In reverse bridge mode, PI7C9X111SL has a 32-bit PCI upstream port and an x1 PCI Express downstream port. PI7C9X111SL configuration registers are backward compatible with existing PCI bridge software and firmware. No modification of PCI bridge software and firmware is needed for the original operation.

Figure 1-1 PI7C9X111SL Topology



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1.1 PCI EXPRESS FEATURES

- Compliant with PCI Express Base Specification, Revision 1.1
- Compliant with PCI Express Card Electromechanical Specification, Revision 1.1
- Compliant with PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0
- Physical Layer interface (x1 link with 2.5Gb/s data rate)
- Lane polarity toggle
- Virtual Isochronous support (upstream TC1-7 generation, downstream TC1-7 mapping)
- ASPM support
- Beacon support
- CRC (16-bit), LCRC (32-bit)
- ECRC and advanced error reporting
- PRBS (Pseudo Random Bit Sequencing) generator/checker for chip testing
- Maximum payload size to 512 bytes

1.2 PCI FEATURES

- Compliant with PCI Local Bus Specification, Revision 3.0
- Compliant with PCI-to-PCI Bridge Architecture Specification, Revision 1.2
- Compliant with PCI Bus PM Interface Specification, Revision 1.1
- Compliant with PCI Hot-Plug Specification, Revision 1.1
- Compliant with PCI Mobile Design Guide, Version 1.1
- 3.3V PCI signaling with 5V I/O tolerance
- Provides two level arbitration support for four PCI Bus masters
- 16-bit address decode for VGA
- Subsystem Vendor and Subsystem Device IDs support
- PCI INT interrupt or MSI Function support

1.3 GENERAL FEATURES

- Compliant with Advanced Configuration and Power Interface Specification (ACPI), Revision 2.0b
- Compliant with System Management (SM) Bus, Version 2.0
- Forward bridging (PCI Express as primary bus, PCI as secondary bus)
- Reverse bridging (PCI as primary bus, PCI Express as secondary bus)
- Transparent mode support
- GPIO support (4 bi-directional pins)
- Power Management (including ACPI, CLKRUN_L,CLKREQ_L, PCI_PM)
- EEPROM (I2C) Interface
- SM Bus Interface
- Auxiliary powers (VAUX, VDDAUX, VDDCAUX) support
- Power consumption less than 0.45 Watt in typical condition
- Industrial temperature range (-40C ~ +85C)
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. “Green” Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.
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2 PIN DEFINITIONS

2.1 SIGNAL TYPES

TYPE OF SIGNAL	- DESCRIPTIONS
B	**Bi-directional**
I	**Input**
IU	**Input with pull-up**
ID	**Input with pull-down**
IOD	**Bi-directional with open drain output**
OD	**Open drain output**
O	**Output**
P	**Power**
G	**Ground**

2.2 PCI EXPRESS SIGNALS

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
REFCLKP REFCLKN	7 9	I	**Reference Clock Inputs:** Connect to external 100MHz differential clock. These signals require AC coupled with 0.1uF capacitors.
RP RN	17 18	I	**PCI Express data inputs:** Differential data receiver input signals
TP TN	14 13	O	**PCI Express data outputs:** Differential data transmitter output signals
PERST_L	36	B	**PCI Express Fundamental Reset:** PI7C9X111SL uses this reset to initialize the internal state machines.

2.3 PCI SIGNALS

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
AD [31:0]	125, 123, 124, 121, 120, 119, 118, 116, 114, 113, 110, 109, 108, 107, 105, 104, 89, 87, 86, 85, 84, 83, 82, 80, 77, 76, 74, 73, 72, 71, 69, 68	B	**Address / Data:** Multiplexed address and data bus. Address phase is aligned with first clock of FRAME_L assertion. Data phase is aligned with IRDY_L or TRDY_L assertion. Data is transferred on rising edges of CLKOUT[0] when both IRDY_L and TRDY_L are asserted. During bus idle (both FRAME_L and IRDY_L are de-asserted), PI7C9X111SL drives AD to a valid logic level when arbiter is parking to PI7C9X111SL on PCI bus.
CBE_L[3:0]	115, 102, 90, 79	B	**Command / Byte Enables (Active LOW):** Multiplexed command at address phase and byte enable at data phase. During address phase, the initiator drives commands on CBE [3:0] signals to start the transaction. If the command is a write transaction, the initiator will drive the byte enables during data phase. Otherwise, the target will drive the byte enables during data phase. During bus idle, PI7C9X111SL drives CBE [3:0] signals to a valid logic level when arbiter is parking to PI7C9X111SL on PCI bus.
PAR	93	B	**Parity Bit:** Parity bit is an even parity (i.e. even number of 1's), which generates based on the values of AD [31:0], CBE [3:0]. If PI7C9X111SL is an initiator with a write transaction, PI7C9X111SL will tri-state PAR. If PI7C9X111SL is a target and a write transaction, PI7C9X111SL will drive PAR one clock after the address or data phase. If PI7C9X111SL is a target and a read transaction, PI7C9X111SL will drive PAR one clock after the address phase and tri-state PAR during data phases. PAR is tri-stated one cycle after the AD lines are tri-stated. During bus idle, PI7C9X111SL drives PAR to a valid logic level when arbiter is parking to PI7C9X111SL on PCI bus.
FRAME_L	66	B	**FRAME (Active LOW):** Driven by the initiator of a transaction to indicate the beginning and duration an access. The de-assertion of FRAME_L indicates the final data phase signaled by the initiator in burst transfers. Before being tri-stated, it is driven to a de-asserted state for one cycle.

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NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
IRDY_L	99	B	**IRDY (Active LOW):** Driven by the initiator of a transaction to indicate its ability to complete current data phase on the primary side. Once asserted in a data phase, it is not de-asserted until the end of the data phase. Before tri-stated, it is driven to a de-asserted state for one cycle.
TRDY_L	100	B	**TRDY (Active LOW):** Driven by the target of a transaction to indicate its ability to complete current data phase on the primary side. Once asserted in a data phase, it is not de-asserted until the end of the data phase. Before tri-stated, it is driven to a de-asserted state for one cycle.
DEVSEL_L	98	B	**Device Select (Active LOW):** Asserted by the target indicating that the device is accepting the transaction. As a master, PI7C9X111SL waits for the assertion of this signal within 5 cycles of FRAME_L assertion; otherwise, terminate with master abort. Before tri-stated, it is driven to a de-asserted state for one cycle.
STOP_L	95	B	**STOP (Active LOW):** Asserted by the target indicating that the target is requesting the initiator to stop the current transaction. Before tri-stated, it is driven to a de-asserted state for one cycle.
LOCK_L	96	B	**LOCK (Active LOW):** Asserted by the initiator for multiple transactions to complete. PI7C9X111SL does not support any upstream LOCK transaction.
IDSEL	64	I	**Initialization Device Select:** Used as a chip select line for Type 0 configuration access to bridge's configuration space.
PERR_L	92	B	**Parity Error (Active LOW):** Asserted when a data parity error is detected for data received on the PCI bus interface. Before being tri-stated, it is driven to a de-asserted state for one cycle.
SERR_L	63	IOD	**System Error (Active LOW):** Can be driven LOW by any device to indicate a system error condition. If SERR control is enabled, PI7C9X111SL will drive this pin on: ▪ Address parity error ▪ Posted write data parity error on target bus ▪ Master abort during posted write transaction ▪ Target abort during posted write transaction ▪ Posted write transaction discarded ▪ Delayed write request discarded ▪ Delayed read request discarded ▪ Delayed transaction master timeout ▪ Errors reported from PCI Express port (advanced error reporting) in transparent mode. This signal is an open drain buffer that requires an external pull-up resistor for proper operation.
REQ_L [3:0]	40, 38, 37, 35	I	**Request (Active LOW):** REQ_L's are asserted by bus master devices to request for transactions on the PCI bus. The master devices de-assert REQ_Ls for at least 2 PCI clock cycles before asserting them again. If the device is in reverse mode or if external arbiter is selected, REQ_L [0] will be the bus grant input to PI7C9X111SL. Also, REQ_L [3:1] will become the GPI [2:0]. When powered up, if both REQ_L2 and REQ_L3 and pulled low (Active LOW) and stay low in normal operation, the PI7C9X111SL will change the function of CLKOUT[3] to CLKRUN and CLKOUT[2] to CLKREQ, respectively.
GNT_L [3:0]	44, 43, 42, 41	O	**Grant (Active LOW):** PI7C9X111SL asserts GNT_Ls to release PCI bus control to bus master devices. During idle and all GNT_Ls are de-asserted and arbiter is parking to PI7C9X111SL, PI7C9X111SL will drive AD, CBE, and PAR to valid logic levels. If the device is in reverse mode or if external arbiter is selected, GNT_L [0] will be the bus request from PI7C9X111SL to external arbiter. Also, GNT_L [3:1] will become the GPO [2:0].
CLKOUT [3:0]	52,56,59,58	I/O	**PCI Clock Outputs:** PCI clock outputs are derived from the CLKIN and provide clocking signals to external PCI Devices. In external feedback mode, CLKOUT[0] becomes an input for feedback clock and CLKOUT[1:3] remain as clock outputs to provide clock signals to external PCI Devices. Further detail on page 66.
M66EN	103	I	**66MHz Enable:** This input is used to specify if Bridge is capable of running at 66MHz. For 66MHz operation on the PCI bus, this signal should be pulled "HIGH". For 33MHz operation on the PCI bus, this signal should be pulled LOW.
RESET_L	49	B	**RESET_L (Active LOW):** When RESET_L active, all PCI signals should be asynchronously tri-stated.
INTA_L INTB_L INTC_L INTD_L	39 47 62 61	IOD	**Interrupt:** Signals are asserted to request an interrupt. After asserted, it can be cleared by the device driver. INTA_L, INTB_L, INTC_L, INTD_L signals are inputs and asynchronous to the clock in the forward mode. In reverse mode, INTA_L, INTB_L, INTC_L, and INTD_L are open drain buffers for sending interrupts to the

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NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
			host interrupt controller.
CLKIN	48	I	**PCI Clock Input:** PCI Clock Input Signal connects to an external clock source. The PCI Clock Outputs CLKOUT [3:0] pins are derived from CLKIN Input.

2.4 MODE SELECT AND STRAPPING SIGNALS

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
TM0	127	I	**Mode Select 0:** Mode Selection Pin to select EEPROM or SM Bus. TM0=0 for EEPROM (I2C) support and TM0=1 for SM Bus support. TM0 is also a strapping pin. See table 3-1 mode selection and 3-2 for strapping control.
TM1	26	I	**Mode Select 1:** Mode Selection Pin for normal operation. Set TM1=0 for normal operation. TM1=1 is reserved.
MSK_IN	126	I	Hot Plug Enable input.
REVRSB	31	I	**Forward or Reverse Bridging Pin:** REVRSB pin controls the Forward (REVRSB=0) or Reverse (REVRSB=1) Bridge Mode of PI7C9X111SL. This pin is also a strapping pin.

2.5 JTAG BOUNDARY SCAN SIGNALS

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
TCK	28	IU	**Test Clock:** TCK is the test clock to synchronize the state information and data on the PCI bus side of PI7C9X111SL during boundary scan operation. At normal operation mode, this pin should be left open(NC).
TMS	27	IU	**Test Mode Select:** TMS controls the state of the Test Access Port (TAP) controller. At normal operation mode, this pin should be pulled low through a 1K-Ohm pull-down resistor.
TDO	32	O	**Test Data Output:** TDO is the test data output and connects to the end of the JTAG scan chain. At normal operation mode, this pin should be left open(NC).
TDI	29	IU	**Test Data Input:** TDI is the test data input and connects to the beginning of the JTAG scan chain. It allows the test instructions and data to be serially shifted into the PCI side of PI7C9X111SL. At normal operation mode, this pin should be left open(NC).
TRST_L	30	IU	**Test Reset (Active LOW):** TRST_L is the test reset to initialize the Test Access Port (TAP) controller. At normal operation mode, this pin should be pulled low through a 1K-Ohm pull-down resistor.

2.6 MISCELLANEOUS SIGNALS

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
GPIO [3:0]	50, 51, 54, 55	B	**General Purpose I/O Data Pins:** The 4 general-purpose signals are programmable as either input-only or bi-directional signals by writing the GPIO output enable control register in the configuration space.
SMBCLK / SCL	3	B	**SMBUS / EEPROM Clock Pin:** When EEPROM (I2C) interface is selected (TM0=0), this pin is an output of SCL clock and connected to EEPROM clock input. When SMBUS interface is selected (TM0=1), this pin is an input for the clock of SMBUS.
SMBDATA / SDA	4	B/IOD	**SMBUS / EEPROM Data Pin:** Data Interface Pin to EERPOM or SMBUS. When EEPROM (I2C) interface is selected (TM0=0), this pin is a bi-directional signal. When SMBUS interface is selected (TM0=1), this pin is an open drain signal.
PME_L	1	B	**Power Management Event Pin:** Power Management Event Signal is asserted to request a change in the device or link power state.

2.7 POWER AND GROUND PINS

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
VDDA	8, 20, 21	P	**Analog Voltage Supply for PCI Express Interface:** Connect to the 1.0V Power Supply.
VDDP	11, 23, 24	P	**Digital Voltage Supply for PCI Express Interface:** Connect to the 1.0V Power

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NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
			Supply.
VDDAUX	15	P	**Auxiliary Voltage Supply for PCI Express Interface:** Connect to the 1.0V Power Supply.
VTT	12	P	**Termination Supply Voltage for PCI Express Interface:** Connect to the 1.5V Power Supply.
VDDC	45, 65, 75, 94, 112	P	**Core Supply Voltage:** Connect to the 1.0V Power Supply.
VDDCAUX	5	P	**Auxiliary Core Supply Voltage:** Connect to the 1.0V Power Supply.
VD33	33, 53, 60, 70, 81, 91, 101, 111, 122	P	**I/O Supply Voltage for PCI Interface:** Connect to the 3.3V Power Supply for PCI I/O Buffers.
VAUX	2	P	**Auxiliary I/O Supply Voltage for PCI interface:** Connect to the 3.3V Power Supply.
VSS	6, 10, 16, 19, 22, 25, 34, 46, 57, 67, 78, 88, 97, 106, 117, 128, 129	P	**Ground:** Connect to Ground.

2.8 PIN ASSIGNMENTS

Table 2-1 Pin Assignments

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	PME_L	34	VSS	67	VSS	100	TRDY_L
2	VAUX	35	REQ_L[0]	68	AD[0]	101	VD33
3	SMBCLK / SCL	36	PERST_L	69	AD[1]	102	CBE_L[2]
4	SMDAT / SDA	37	REQ_L[1]	70	VD33	103	M66EN
5	VDDCAUX	38	REQ_L[2]	71	AD[2]	104	AD[16]
6	VSS	39	INTA_L	72	AD[3]	105	AD[17]
7	REFCLKP	40	REQ_L[3]	73	AD[4]	106	VSS
8	VDDA	41	GNT_L[0]	74	AD[5]	107	AD[18]
9	REFCLKN	42	GNT_L[1]	75	VDDC	108	AD[19]
10	VSS	43	GNT_L[2]	76	AD[6]	109	AD[20]
11	VDDP	44	GNT_L[3]	77	AD[7]	110	AD[21]
12	VTT	45	VDDC	78	VSS	111	VD33
13	TXN	46	VSS	79	CBE[0]	112	VDDC
14	TXP	47	INTB_L	80	AD[8]	113	AD[22]
15	VDDAUX	48	CLKIN	81	VD33	114	AD[23]
16	VSS	49	RESET_L	82	AD[9]	115	CBE_L[3]
17	RXP	50	GPIO[3]	83	AD[10]	116	AD[24]
18	RXN	51	GPIO[2]	84	AD[11]	117	VSS
19	VSS	52	CLKOUT[3]	85	AD[12]	118	AD[25]
20	VDDA	53	VD33	86	AD[13]	119	AD[26]
21	VDDA	54	GPIO[1]	87	AD[14]	120	AD[27]
22	VSS	55	GPIO[0]	88	VSS	121	AD[28]
23	VDDP	56	CLKOUT[2]	89	AD[15]	122	VD33
24	VDDP	57	VSS	90	CBE_L[1]	123	AD[30]
25	VSS	58	CLKOUT[0]	91	VD33	124	AD[29]
26	TM1	59	CLKOUT[1]	92	PERR_L	125	AD[31]
27	TMS	60	VD33	93	PAR	126	MSK_IN
28	TCK	61	INTD_L	94	VDDC	127	TM0
29	TDI	62	INTC_L	95	STOP_L	128	VSS
30	TRST_L	63	SERR_L	96	LOCK_L	129	E-Pad
31	REVRSB	64	IDSEL	97	VSS		
32	TDO	65	VDDC	98	DEVSEL_L		
33	VD33	66	FRAME_L	99	IRDY_L		

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3 MODE SELECTION AND PIN STRAPPING

3.1 FUNCTIONAL MODE SELECTION

PI7C9X111SL uses TM1, TM0, and REVRSB pins to select different modes of operations. These three input signals are required to be stable during normal operation. One of the eight combinations of normal operation can be selected by setting the logic values for the three mode select pins. For example, if the logic values are low for all three (TM1, TM0, and REVRSB) pins, the normal operation will have EEPROM (I2C) support with internal arbiter in forward bridge mode. The designated operation with respect to the values of the TM1, TM0, and REVRSB pins are defined on Table 3-1:

Table 3-1 Mode Selection

TM1	TM0	REVRSB	Functional Mode
0	0	X	EEPROM (I2C) support
0	1	X	SM Bus support
0	X	0	Forward bridge mode
0	X	1	Reverse bridge mode

3.2 PIN STRAPPING

If TM1 is strapped to low, PI7C9X111SL uses REQ_L[3:2], REVRSB as the strapping pins at the PCIe PERST# de-assertion to enable Clock Power Management feature.

Table 3-2 Pin Strapping

TM1 Strapped	REQ_L[3:2]	REVRSB Strapped	Test Functions
0	2'b0	0	Clock Power Management is enabled, only two PCI devices supported. CLKOUT[2] is used as CLKREQ# CLKOUT[3] is used as CLKRUN#

If TM1 is strapped to high, PI7C9X111SL uses TM0, REVRSB as the strapping pins at the PCIe PERST# de-assertion transition in forward bridge mode or PCI RESET# de-assertion transition in reverse bridge mode.

TM1 Strapped	TM0 Strapped	REVRSB Strapped	Test Functions
1	1	X	Short initialization
1	0	1	Functional Loopback Test
1	0	0	Bridge test (PRBS, IDDQ, etc..)

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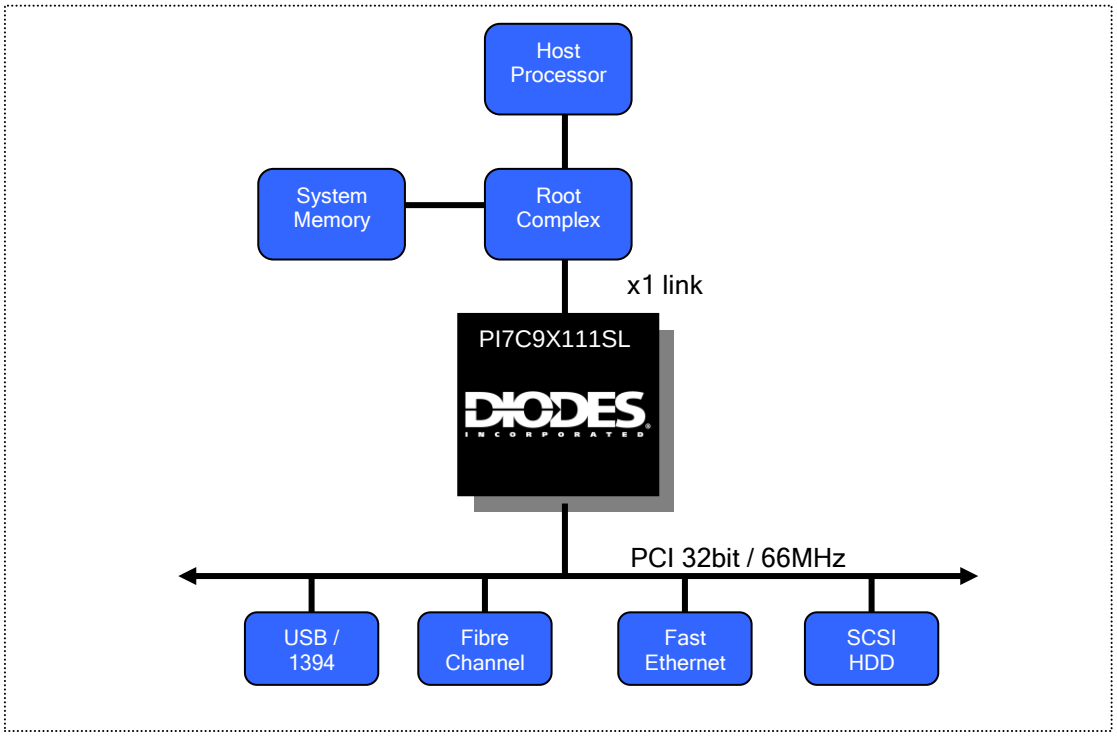
4 FORWARD AND REVERSE BRIDGING

PI7C9X111SL supports forward or reverse combination modes of operation. For example, when PI7C9X111SL is operating in forward PCIe Bridge (REVRSB=0), its PCI Express interface is connected to a root complex and its PCI bus interface is connected to PCI devices. Another example, PI7C9X111SL can be configured as a reverse PCIe Bridge (REVRSB=1).

PCI based systems and peripherals are ubiquitous in the I/O interconnect technology market today. It will be a tremendous effort to convert existing PCI based products to be used in PCI Express systems. PI7C9X111SL provides a solution to bridge existing PCI based products to the latest PCI Express technology.

Figure 4-1 Forward Bridge Mode



In reverse mode (REVRSB=1), PI7C9X111SL becomes a PCI-to-PCI Express bridge that its PCI bus interface is connected to the PCI Host Chipset between and the PCI Express x1 link. It enables the legacy PCI Host Systems to provide PCI Express Interface capability.

PI7C9X111SL provides a solution to convert existing PCI based designs to adapt quickly into PCI Express base platforms. Existing PCI based applications will not have to undergo a complete re-architecture in order to interface to PCI Express technology.

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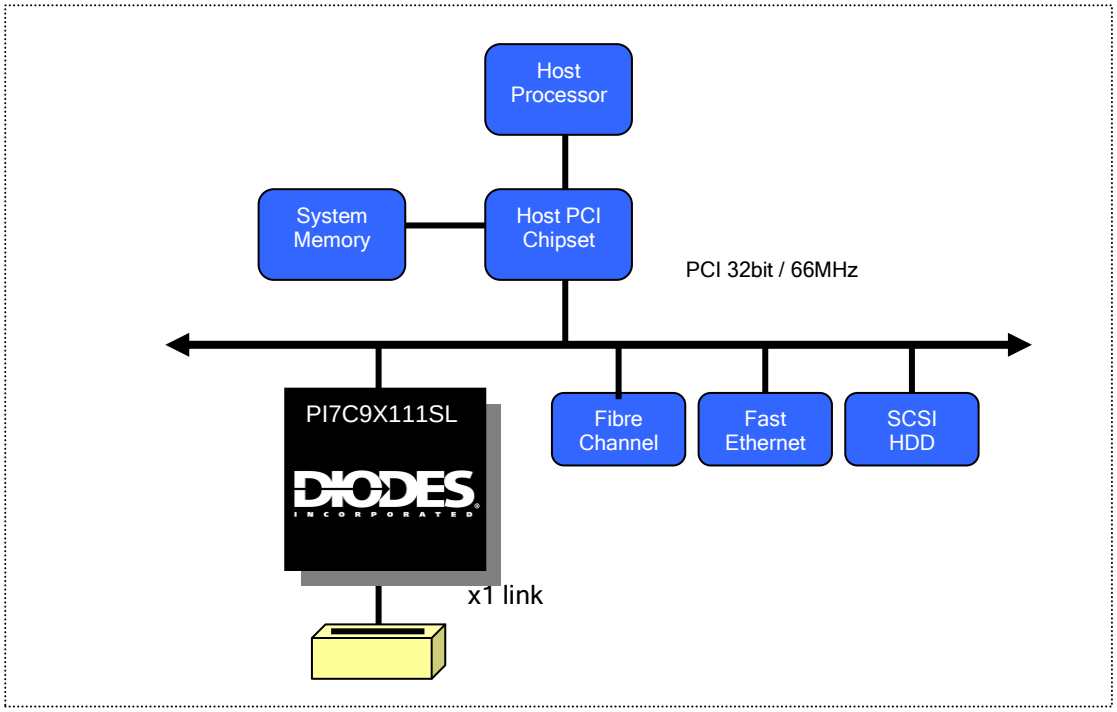
Figure 4-2 Reverse Bridge Mode



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5 PCI EXPRESS FUNCTIONAL OVERVIEW

5.1 TLP STRUCTURE

PCI Express TLP (Transaction Layer Packet) Structure is comprised of format, type, traffic class, attributes, TLP digest, TLP poison, and length of data payload.

There are four TLP formats defined in PI7C9X111SL based on the states of FMT [1] and FMT [0] as shown on Table 5-1.

Table 5-1 TLP Format

FMT [1]	FMT [0]	TLP Format
0	0	3 double word, without data
0	1	4 double word, without data
1	0	3 double word, with data
1	1	4 double word, with data

Data payload of PI7C9X111SL can range from 4 (1DW) to 256 (64DW) bytes. PI7C9X111SL supports three TLP routing mechanisms. They are comprised of Address, ID, and Implicit routings. Address routing is being used for Memory and IO requests. ID based (bus, device, function numbers) routing is being used for configuration requests. Implicit routing is being used for message routing. There are two message groups (baseline and advanced switching). The baseline message group contains INTx interrupt signaling, power management, error signaling, locked transaction support, slot power limit support, vendor defined messages, hot-plug signaling. The other is advanced switching support message group. The advanced switching support message contains data packet and signal packet messages. Advanced switching is beyond the scope of PI7C9X111SL implementation.

The r [2:0] values of the "type" field will determine the destination of the message to be routed. All baseline messages must use the default traffic class zero (TC0).

5.2 VIRTUAL ISOCHRONOUS OPERATION

This section provides a summary of Virtual Isochronous Operation supported by PI7C9X111SL. Virtual Isochronous support is disabled by default. Virtual Isochronous feature can be turned on with setting bit [26] of offset 40h to one. Control bits are designated for selecting which traffic class (TC1-7) to be used for upstream (PCI Express-to-PCI). PI7C9X111SL accepts only TC0 packets of configuration, IO, and message packets for downstream (PCI Express-to-PCI). If configuration, IO and message packets have traffic class other than TC0, PI7C9X111SL will treat them as malformed packets. PI7C9X111SL maps all downstream memory packets from PCI Express to PCI transactions regardless the virtual Isochronous operation is enabled or not.

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6 CONFIGURATION REGISTER ACCESS

PI7C9X111SL supports Type-0 and Type-1 configuration space headers and Capability ID of 01h (PCI power management) to 10h (PCI Express capability structure).

With pin REVRSB = 0, device-port type (bit [7:4]) of capability register will be set to 7h (PCI Express-to-PCI). When pin REVRSB = 1, device-port type (bit [7:4]) of capability register will be set to 8h (PCI-to-PCI Express bridge).

PI7C9X111SL supports PCI Express capabilities register structure with capability version set to 1h (bit [3:0] of offset 02h).

6.1 CONFIGURATION REGISTER MAP

PI7C9X111SL supports capability pointer with PCI power management (ID=01h), PCI bridge sub-system vendor ID (ID=0Dh), PCI Express (ID=10h), vital product data (ID=03h), and message signaled interrupt (ID=05h). Slot identification (ID=04h) is off by default and can be turned on through configuration programming.

Table 6-1 Configuration Register Map (00h – FFh)

Primary Bus Configuration Access or Secondary Bus Configuration Access	PCI Configuration Register Name (type1)	EEPROM (I2C) Access	SM Bus Access
01h - 00h	Vendor ID	Yes1	Yes2
03h – 02h	Device ID	Yes1	Yes2
05h – 04h	Command Register	Yes	Yes
07h – 06h	Primary Status Register	Yes	Yes
0Bh – 08h	Class Code and Revision ID	Yes1	Yes2
0Ch	Cacheline Size Register	Yes	Yes
0Dh	Primary Latency Timer	Yes	Yes
0Eh	Header Type Register	Yes	Yes
0Fh	Reserved	-	-
17h – 10h	Reserved	-	-
18h	Primary Bus Number Register	Yes	Yes
19h	Secondary Bus Number Register	Yes	Yes
1Ah	Subordinate Bus Number Register	Yes	Yes
1Bh	Secondary Latency Timer	Yes	Yes
1Ch	I/O Base Register	Yes	Yes
1Dh	I/O Limit Register	Yes	Yes
1Fh – 1Eh	Secondary Status Register	Yes	Yes
21h – 20h	Memory Base Register	Yes	Yes
23h – 22h	Memory Limit Register	Yes	Yes
25h – 24h	Prefetchable Memory Base Register	Yes	Yes
27h – 26h	Prefetchable Memory Limit Register	Yes	Yes
2Bh – 28h	Prefetchable Memory Base Upper 32-bit Register	Yes	Yes

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Primary Bus Configuration Access or Secondary Bus Configuration Access	PCI Configuration Register Name (type1)	EEPROM (I2C) Access	SM Bus Access
2Dh – 2Ch	Prefetchable Memory Limit Upper 32-bit Register	Yes	Yes
2Fh – 2Eh	Prefetchable Memory Limit Upper 32-bit Register	Yes	Yes
31h – 30h	I/O Base Upper 16-bit Register	Yes	Yes
33h – 32h	I/O Limit Upper 16-bit Register	Yes	Yes
34h	Capability Pointer	Yes	Yes
37h – 35h	Reserved	No	Yes
3Bh – 38h	Reserved	No	Yes
3Ch	Interrupt Line	Yes	Yes
3Dh	Interrupt Pin	Yes	Yes
3Eh	Bridge Control	Yes	Yes
3Fh	Bridge Control	Yes	Yes
41h – 40h	PCI Data Prefetching Control	Yes	Yes
43h – 42h	Chip Control 0	Yes	Yes
45h – 44h	Reserved	-	-
47h – 46h	Reserved	-	-
4Bh – 48h	Arbiter Mode, Enable, Priority	-	-
4Ch	Reserved	-	-
4Dh	Reserved	-	-
4Eh	Reserved	-	-
4Fh	Reserved	-	-
53h – 50h	Reserved	-	-
57h – 54h	Reserved	-	-
5Bh – 58h	Reserved	-	-
5Fh – 5Ch	Reserved	-	-
63h – 60h	Reserved	-	-
67h – 64h	Reserved	-	-
69h – 68h	PCI Express Tx and Rx Control	Yes	Yes
6Ah	Reserved	-	-
6Bh	Upstream memory write/read control	Yes	Yes
6Dh – 6Ch	Reserved	-	-
6Fh – 6Eh	Reserved	-	-
73h – 70h	EEPROM (I2C) Control and Status Register	No	Yes
77h – 74h	Reserved	-	-
7Bh – 78h	GPIO Data and Control	Yes	Yes
7Ch	Reserved	-	-
7Dh	Reserved	-	-
7Eh	Reserved	-	-
7Fh	Reserved	-	-
83h – 80h	PCI-X Capability	Yes	Yes
87h – 84h	PCI-X Bridge Status	Yes	Yes
8Bh – 88h	Upstream Split Transaction	Yes	Yes
8Fh – 8Ch	Downstream Split Transaction	Yes	Yes
93h – 90h	Power Management	Yes	Yes

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Primary Bus Configuration Access or Secondary Bus Configuration Access	PCI Configuration Register Name (type1)	EEPROM (I2C) Access	SM Bus Access
	Capability		
97h – 94h	Power Management Control and Status	Yes	Yes
9Bh – 98h	Reserved	-	-
9Fh – 9Ch	Reserved	-	-
A3h – A0h	Slot ID Capability	Yes	Yes
A7h – A4h	Secondary Clock and CLKRUN Control	Yes	Yes
ABh – A8h	SSID and SSVID Capability	Yes	Yes
AFh – ACh	Subsystem ID and Subsystem Vendor ID	Yes	Yes
B3h – B0h	PCI Express Capability	Yes	Yes
B7h – B4h	Device Capability	Yes	Yes
BBh – B8h	Device Control and Status	Yes	Yes
BFh – BCh	Link Capability	Yes	Yes
C3h – C0h	Link Control and Status	Yes	Yes
C7h – C4h	Slot Capability	Yes	Yes
CBh – C8h	Slot Control and Status	Yes	Yes
CFh – CCh	XPIP Configuration Register 0	Yes	Yes
D3h – D0h	XPIP Configuration Register 1	Yes	Yes
D6h – D4h	XPIP Configuration Register 2	Yes	Yes
D7h	Hot Swap Switch debounce count	Yes	Yes
DBh – D8h	VPD Capability Register	Yes	Yes
DFh – DCh	VPD Data Register	Yes3	Yes
E3h – E0h	Extended Config Access Address	Yes	Yes
E7h – E4h	Extended Config Access Data	Yes	Yes
EBh – E8h	Reserved	-	-
EFh – ECh	Reserved	-	-
F3h – F0h	MSI Capability Register	Yes	Yes
F7h – F4h	Message Address	Yes	Yes
FBh – F8h	Message Upper Address	Yes	Yes
FFh – FCh	Message Date	Yes	Yes

Note 1: When masquerade is enabled, it is pre-loadable.
Note 2: The VPD data is read/write through I2C during VPD operation.
Note 3: Read access only.

6.2 PCI EXPRESS EXTENDED CAPABILITY REGISTER MAP

PI7C9X111SL also supports PCI Express Extended Capabilities with from 257-byte to 4096-byte space. The offset range is from 100h to FFFh. The offset 100h is defined for Advance Error Reporting (ID=0001h). The offset 150h is defined for Virtual Channel (ID=0002h).

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Table 6-2 PCI Express Extended Capability Register Map (100h – FFFh)

Primary Bus Configuration Access or Secondary Bus Configuration Access	Transparent Mode (type1)	EEPROM (I2C) Access	SM Bus Access
103h – 100h	Advanced Error Reporting (AER) Capability	Yes	Yes2
107h – 104h	Uncorrectable Error Status	No	Yes
10Bh – 108h	Uncorrectable Error Mask	Yes	Yes
10Fh – 10Ch	Uncorrectable Severity	No	Yes
113h – 110h	Correctable Error Status	No	Yes
117h – 114h	Correctable Error Mask	No	Yes
11Bh – 118h	AER Control	No	Yes
12Bh – 11Ch	Header Log Register	No	Yes
12Fh – 12Ch	Secondary Uncorrectable Error Status	No	Yes
133h – 130h	Secondary Uncorrectable Error Mask	No	Yes
137h – 134h	Secondary Uncorrectable Severity	No	Yes
13Bh – 138h	Secondary AER Control	No	Yes
14Bh – 13Ch	Secondary Header Log Register	No	Yes
14Fh – 14Ch	Reserved	No	Yes
153h – 150h	VC Capability	No	Yes
157h – 154h	Port VC Capability 1	No	Yes
15Bh – 158h	Port VC Capability 2	No	Yes
15Fh – 15Ch	Port VC Status and Control	No	Yes
163h – 160h	VC0 Resource Capability	No	Yes
167h – 164h	VC0 Resource Control	No	Yes
16Bh – 168h	VC0 Resource Status	No	Yes
2FFh – 170h	Reserved	No	No
303h – 300h	Extended GPIO Data and Control	No	Yes
307h – 304h	Extended GPI/GPO Data and Control	No	Yes
30Fh – 308h	Reserved	No	No
310h	Replay and Acknowledge Latency Timer	Yes	Yes
4FFh – 314h	Reserved	No	No
503h – 500h	Reserved	No	No
504h	Reserved	No	No
50Fh – 505h	Reserved	No	No
510h	Reserved	No	No
FFFh – 514h	Reserved	No	No

Note 5: Read access only.

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6.3 PCI CONFIGURATION REGISTERS

The following section describes the configuration space when the device is in transparent mode. The descriptions for different register type are listed as follow:

Register Type	Descriptions
RO	Read Only
ROS	Read Only and Sticky
RW	Read/Write
RWC	Read/Write "1" to clear
RWS	Read/Write and Sticky
RWCS	Read/Write "1" to clear and Sticky

6.3.1 VENDOR ID – OFFSET 00h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Vendor ID	RO	Identifies Pericom as the vendor of this device. Returns 12D8h when read.

6.3.2 DEVICE ID – OFFSET 00h

BIT	FUNCTION	TYPE	DESCRIPTION
31:16	Device ID	RO	Identifies this device as the PI7C9X111SL. Returns E111 when read.

6.3.3 COMMAND REGISTER – OFFSET 04h

BIT	FUNCTION	TYPE	DESCRIPTION
0	I/O Space Enable	RW	0: Ignore I/O transactions on the primary interface 1: Enable response to memory transactions on the primary interface Reset to 0
1	Memory Space Enable	RW	0: Ignore memory read transactions on the primary interface 1: Enable memory read transactions on the primary interface Reset to 0
2	Bus Master Enable	RW	0: Do not initiate memory or I/O transactions on the primary interface and disable response to memory and I/O transactions on the secondary interface 1: Enable the bridge to operate as a master on the primary interfaces for memory and I/O transactions forwarded from the secondary interface. Reset to 0
3	Special Cycle Enable	RO	0: PI7C9X111SL does not respond as a target to Special Cycle transactions, so this bit is defined as Read-Only and must return 0 when read Reset to 0
4	Memory Write and Invalidate Enable	RO	0: PI7C9X111SL does not originate a Memory Write and Invalidate transaction. Implements this bit as Read-Only and returns 0 when read (unless forwarding a transaction for another master). Reset to 0
5	VGA Palette Snoop Enable	RO / RW	**This bit applies to reverse bridge only.** 0: Ignore VGA palette access on the primary 1: Enable positive decoding response to VGA palette writes on the primary interface with I/O address bits AD [9:0] equal to 3C6h, 3C8h, and 3C9h (inclusive of ISA alias; AD [15:0] are not decoded and may be any value) Reset to 0

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BIT	FUNCTION	TYPE	DESCRIPTION
6	Parity Error Response Enable	RW	0: May ignore any parity error that is detected and take its normal action 1: This bit if set, enables the setting of Master Data Parity Error bit in the Status Register when poisoned TLP received or parity error is detected and takes its normal action Reset to 0
7	Wait Cycle Control	RO	Wait cycle control not supported Reset to 0
8	SERR_L Enable Bit	RW	0: Disable 1: Enable PI7C9X111SL in forward bridge mode to report non-fatal or fatal error message to the Root Complex. Also, in reverse bridge mode to assert SERR_L on the primary interface Reset to 0
9	Fast Back-to-Back Enable	RO	Fast back-to-back enable not supported Reset to 0
10	Interrupt Disable	RW	**This bit applies to reverse bridge only.** 0: INTA_L can be asserted on PCI interface 1: Prevent INTA_L from being asserted on PCI interface Reset to 0
15:11	Reserved	RO	Reset to 00000

6.3.4 PRIMARY STATUS REGISTER – OFFSET 04h

BIT	FUNCTION	TYPE	DESCRIPTION
18:16	Reserved	RO	Reset to 000
19	Reserved	RO	Reset to 0
20	Capability List Capable	RO	1: PI7C9X111SL supports the capability list (offset 34h in the pointer to the data structure) Reset to 1
21	66MHz Capable	RO	**This bit applies to reverse bridge only.** 1: 66MHz capable Reset to 0 when forward bridge or 1 when reverse bridge.
22	Reserved	RO	Reset to 0
23	Fast Back-to-Back Capable	RO	**This bit applies to reverse bridge only.** 1: Enable fast back-to-back transactions Reset to 0 when forward bridge or 1 when reverse bridge in PCI mode.
24	Master Data Parity Error Detected	RWC	Bit set if its Parity Error Enable bit is set and either of the conditions occurs on the primary: FORWARD BRIDGE – Receives a completion marked poisoned Poisons a write request REVERSE BRIDGE – Detected parity error when receiving data or Split Response for read Observes P_PERR_L asserted when sending data or receiving Split Response for write Receives a Split Completion Message indicating data parity error occurred for non-posted write Reset to 0

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BIT	FUNCTION	TYPE	DESCRIPTION
26:25	DEVSEL_L Timing (medium decode)	RO	**These bits apply to reverse bridge only.** 00: fast DEVSEL_L decoding 01: medium DEVSEL_L decoding 10: slow DEVSEL_L decoding 11: reserved Reset to 00 when forward bridge or 01 when reverse bridge.
27	Signaled Target Abort	RWC	FORWARD BRIDGE – This bit is set when PI7C9X111SL completes a request using completer abort status on the primary REVERSE BRIDGE – This bit is set to indicate a target abort on the primary Reset to 0
28	Received Target Abort	RWC	FORWARD BRIDGE – This bit is set when PI7C9X111SL receives a completion with completer abort completion status on the primary REVERSE BRIDGE – This bit is set when PI7C9X111SL detects a target abort on the primary Reset to 0
29	Received Master Abort	RWC	FORWARD BRIDGE – This bit is set when PI7C9X111SL receives a completion with unsupported request completion status on the primary REVERSE BRIDGE – This bit is set when PI7C9X111SL detects a master abort on the primary
30	Signaled System Error	RWC	FORWARD BRIDGE – This bit is set when PI7C9X111SL sends an ERR_FATAL or ERR_NON_FATAL message on the primary REVERSE BRIDGE – This bit is set when PI7C9X111SL asserts SERR_L on the primary Reset to 0
31	Detected Parity Error	RWC	FORWARD BRIDGE – This bit is set when poisoned TLP is detected on the primary REVERSE BRIDGE – This bit is set when address or data parity error is detected on the primary Reset to 0

6.3.5 REVISION ID REGISTER – OFFSET 08h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Revision	RO	Reset to 00000002h

6.3.6 CLASS CODE REGISTER – OFFSET 08h

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Programming Interface	RO	Subtractive decoding of PCI-PCI bridge not supported Reset to 00000000
23:16	Sub-Class Code	RO	Sub-Class Code 00000100: PCI-to-PCI bridge Reset to 00000100
31:24	Base Class Code	RO	Base class code 00000110: Bridge Device Reset to 00000110

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6.3.7 CACHE LINE SIZE REGISTER – OFFSET 0Ch

BIT	FUNCTION	TYPE	DESCRIPTION
1:0	Reserved	RO	Bit [1:0] not supported Reset to 00
2	Cache Line Size	RW	1: Cache line size = 4 double words Reset to 0
3	Cache Line Size	RW	1: Cache line size = 8 double words Reset to 0
4	Cache Line Size	RW	1: Cache line size = 16 double words Reset to 0
5	Cache Line Size	RW	1: Cache line size = 32 double words Reset to 0
7:6	Reserved	RO	Bit [7:6] not supported Reset to 00

6.3.8 PRIMARY LATENCY TIMER REGISTER – OFFSET 0Ch

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Primary Latency Timer	RO / RW	8 bits of primary latency timer in PCI bus FORWARD BRIDGE – RO with reset to 00h REVERSE BRIDGE – RW with reset to 00h in PCI mode

6.3.9 PRIMARY HEADER TYPE REGISTER – OFFSET 0Ch

BIT	FUNCTION	TYPE	DESCRIPTION
22:16	PCI-to-PCI bridge configuration	RO RO	PCI-to-PCI bridge configuration (10 – 3Fh) Reset to 0000001
23	Single Function Device	RO	0: Indicates single function device Reset to 0
31:24	Reserved	RO	Reset to 00h

6.3.10 RESERVED REGISTERS – OFFSET 10h TO 17h

6.3.11 PRIMARY BUS NUMBER REGISTER – OFFSET 18h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Primary Bus Number	RW	Reset to 00h

6.3.12 SECONDARY BUS NUMBER REGISTER – OFFSET 18h

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Secondary Bus Number	RW	Reset to 00h

6.3.13 SUBORDINATE BUS NUMBER REGISTER – OFFSET 18h

BIT	FUNCTION	TYPE	DESCRIPTION
23:16	Subordinate Bus Number	RW	Reset to 00h

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6.3.14 SECONDARY LATENCY TIME REGISTER – OFFSET 18h

BIT	FUNCTION	TYPE	DESCRIPTION
31:24	Secondary Latency Timer	RW / RO	Secondary latency timer in PCI bus FORWARD BRIDGE – RW with reset to 00h in PCI mode REVERSE BRIDGE – RO with reset to 00h

6.3.15 I/O BASE REGISTER – OFFSET 1Ch

BIT	FUNCTION	TYPE	DESCRIPTION
1:0	32-bit I/O Addressing Support	RO	01: Indicates PI7C9X111SL supports 32-bit I/O addressing Reset to 01
3:2	Reserved	RO	Reset to 00
7:4	I/O Base	RW	Indicates the I/O base (0000_0000h) Reset to 0000

6.3.16 I/O LIMIT REGISTER – OFFSET 1Ch

BIT	FUNCTION	TYPE	DESCRIPTION
9:8	32-bit I/O Addressing Support	RO	01: Indicates PI7C9X111SL supports 32-bit I/O addressing Reset to 01
11:10	Reserved	RO	Reset to 00
15:12	I/O Base	RW	Indicates the I/O Limit (0000_0FFFh) Reset to 0000

6.3.17 SECONDARY STATUS REGISTER – OFFSET 1Ch

BIT	FUNCTION	TYPE	DESCRIPTION
20:16	Reserved	RO	Reset to 00000
21	66MHz Capable	RO	Indicates PI7C9X111SL is 66MHz capable Reset to 1
22	Reserved	RO	Reset to 0
23	Fast Back-to-Back Capable	RO	FORWARD BRIDGE: reset to 1 when secondary bus is in PCI mode (supports fast back-to-back transactions) REVERSE BRIDGE: reset to 0 (does not support fast back-to-back transactions)
24	Master Data Parity Error Detected	RWC	This bit is set if its parity error enable bit is set and either of the conditions occur on the primary: FORWARD BRIDGE – • Detected parity error when receiving data or split response for read • Observes S_PERR_L asserted when sending data or receiving split response for write • Receives a split completion message indicating data parity error occurred for non-posted write REVERSE BRIDGE – • Receives a completion marked poisoned • Poisons a write request Reset to 0

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BIT	FUNCTION	TYPE	DESCRIPTION
26:25	DEVSEL_L Timing (medium decoding)	RO	**These bits apply to forward bridge only.** 01: medium DEVSEL_L decoding Reset to 01 when forward mode or 00 when reverse mode.
27	Signaled Target Abort	RWC	FORWARD BRIDGE – Bit is set when PI7C9X111SL signals target abort REVERSE BRIDGE – Bit is set when PI7C9X111SL completes a request using completer abort completion status Reset to 0
28	Received Target Abort	RWC	FORWARD BRIDGE – Bit is set when PI7C9X111SL detects target abort on the secondary interface REVERSE BRIDGE – Bit is set when PI7C9X111SL receives a completion with completer abort completion status on the secondary interface Reset to 0
29	Received Master Abort	RWC	FORWARD BRIDGE – Bit is set when PI7C9X111SL detects master abort on the secondary interface REVERSE BRIDGE – Bit is set when PI7C9X111SL receives a completion with unsupported request completion status on the primary interface Reset to 0
30	Received System Error	RWC	FORWARD BRIDGE – Bit is set when PI7C9X111SL detects SERR_L assertion on the secondary interface REVERSE BRIDGE – Bit is set when PI7C9X111SL receives an ERR_FATAL or ERR_NON_FATAL message on the secondary interface Reset to 0
31	Detected Parity Error	RWC	FORWARD BRIDGE – Bit is set when PI7C9X111SL detects address or data parity error REVERSE BRIDGE – Bit is set when PI7C9X111SL detects poisoned TLP on secondary interface Reset to 0

6.3.18 MEMORY BASE REGISTER – OFFSET 20h

BIT	FUNCTION	TYPE	DESCRIPTION
3:0	Reserved	RO	Reset to 0000
15:4	Memory Base	RW	Memory Base (80000000h) Reset to 800h

6.3.19 MEMORY LIMIT REGISTER – OFFSET 20h

BIT	FUNCTION	TYPE	DESCRIPTION
19:16	Reserved	RO	Reset to 0000
31:20	Memory Limit	RW	Memory Limit (000FFFFFh) Reset to 000h

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6.3.20 PREFETCHABLE MEMORY BASE REGISTER – OFFSET 24h

BIT	FUNCTION	TYPE	DESCRIPTION
3:0	64-bit Addressing Support	RO	0001: Indicates PI7C9X111SL supports 64-bit addressing Reset to 0001
15:4	Prefetchable Memory Base	RW	Prefetchable Memory Base (00000000_80000000h) Reset to 800h

6.3.21 PREFETCHABLE MEMORY LIMIT REGISTER – OFFSET 24h

BIT	FUNCTION	TYPE	DESCRIPTION
19:16	64-bit Addressing Support	RO	0001: Indicates PI7C9X111SL supports 64-bit addressing Reset to 0001
31:20	Prefetchable Memory Limit	RW	Prefetchable Memory Limit (00000000_000FFFFFh) Reset to 000h

6.3.22 PREFETCHABLE BASE UPPER 32-BIT REGISTER – OFFSET 28h

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Prefetchable Base Upper 32-bit	RW	Bit [63:32] of prefetchable base Reset to 00000000h

6.3.23 PREFETCHABLE LIMIT UPPER 32-BIT REGISTER – OFFSET 2Ch

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Prefetchable Limit Upper 32-bit	RW	Bit [63:32] of prefetchable limit Reset to 00000000h

6.3.24 I/O BASE UPPER 16-BIT REGISTER – OFFSET 30h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	I/O Base Upper 16-bit	RW	Bit [31:16] of I/O Base Reset to 0000h

6.3.25 I/O LIMIT UPPER 16-BIT REGISTER – OFFSET 30h

BIT	FUNCTION	TYPE	DESCRIPTION
31:16	I/O Limit Upper 16-bit	RW	Bit [31:16] of I/O Limit Reset to 0000h

6.3.26 CAPABILITY POINTER – OFFSET 34h

BIT	FUNCTION	TYPE	DESCRIPTION
31:8	Reserved	RO	Reset to 0
7:0	Capability Pointer	RO	Capability pointer to 80h Reset to 80h

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6.3.27 EXPANSION ROM BASE ADDRESS REGISTER – OFFSET 38h

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Expansion ROM Base Address	RO	Expansion ROM not supported. Reset to 00000000h

6.3.28 INTERRUPT LINE REGISTER – OFFSET 3Ch

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Interrupt Line	RW	For initialization code to program to tell which input of the interrupt controller the PI7C9X111SL's INTA_L in connected to. Reset to 00000000

6.3.29 INTERRUPT PIN REGISTER – OFFSET 3Ch

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Interrupt Pin	RO	Designates interrupt pin INTA_L, is used Reset to 01h

6.3.30 BRIDGE CONTROL REGISTER – OFFSET 3Ch

BIT	FUNCTION	TYPE	DESCRIPTION
16	Parity Error Response Enable	RW	0: Ignore parity errors on the secondary 1: Enable parity error detection on secondary FORWARD BRIDGE – Controls the response to uncorrectable address attribute and data errors on the secondary REVERSE BRIDGE – Controls the setting of the master data parity error bit in response to a received poisoned TLP from the secondary (PCIe link) Reset to 0
17	SERR_L Enable	RW	0: Disable the forwarding of SERR_L to ERR_FATAL and ERR_NONFATAL 1: Enable the forwarding of SERR_L to ERR_FATAL and ERR_NONFATAL Reset to 0 (FORWARD BRIDGE) RO bit for REVERSE BRIDGE
18	ISA Enable	RW	0: Forward downstream all I/O addresses in the address range defined by the I/O Base and Limit registers 1: Forward upstream all I/O addresses in the address range defined by the I/O Base and Limit registers that are in the first 64KB of PCI I/O address space (top 768 bytes of each 1KB block) Reset to 0
19	VGA Enable	RW	0: Do not forward VGA compatible memory and I/O addresses from the primary to secondary, unless they are enabled for forwarding by the defined I/O and memory address ranges 1: Forward VGA compatible memory and I/O addresses from the primary and secondary (if the I/O enable and memory enable bits are set), independent of the ISA enable bit
20	VGA 16-bit Decode	RW	0: Execute 10-bit address decodes on VGA I/O accesses 1: Execute 16-bit address decode on VGA I/O accesses Reset to 0

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BIT	FUNCTION	TYPE	DESCRIPTION
21	Master Abort Mode	RW	0: Do not report master aborts (return FFFFFFFFh on reads and discards data on write) 1: Report master abort by signaling target abort if possible or by the assertion of SERR_L (if enabled). Reset to 0
22	Secondary Interface Reset	RW	0: Do not force the assertion of RESET_L on secondary PCI bus for forward bridge, or do not generate a hot reset on the PCIe link for reverse bridge 1: Force the assertion of RESET_L on secondary PCI bus for forward bridge, or generate a hot reset on the PCIe link for reverse bridge Reset to 0
23	Fast Back-to-Back Enable	RO	Fast back-to-back not supported Reset to 0
24	Primary Master Timeout	RW	0: Primary discard timer counts 2^{15} PCI clock cycles 1: Primary discard timer counts 2^{10} PCI clock cycles FORWARD BRIDGE – Bit is RO and ignored by the PI7C9X111SL Reset to 0
25	Secondary Master Timeout	RW	0: Secondary discard timer counts 2^{15} PCI clock cycles 1: Secondary discard timer counts 2^{10} PCI clock cycles REVERSE BRIDGE – Bit is RO and ignored by PI7C9X111SL Reset to 0
26	Master Timeout Status	RWC	Bit is set when the discard timer expires and a delayed completion is discarded at the PCI interface for the forward or reverse bridge Reset to 0
27	Discard Timer SERR_L Enable	RW	Bit is set to enable to generate ERR_NONFATAL or ERR_FATAL for forward bridge, or assert P_SERR_L for reverse bridge as a result of the expiration of the discard timer on the PCI interface. Reset to 0
31:28	Reserved	RO	Reset to 0000

6.3.31 PCI DATA BUFFERING CONTROL REGISTER – OFFSET 40h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Secondary Internal Arbiter's PARK Function	RW	0: Park to the last master 1: Park to PI7C9X111SL secondary port Reset to 0
1	Memory Read Prefetching Dynamic Control Disable	RW	0: Enable memory read prefetching dynamic control for PCI to PCIe read 1: Disable memory read prefetching dynamic control for PCI to PCIe read Reset to 0
2	Completion Data Prediction Control	RW	0: Enable completion data prediction for PCI to PCIe read. 1: Disable completion data prediction Reset to 0
3	CFG Type0-to-Type1 conversion Enable	RW	0: CFG Type0-to-Type1 conversion is disabled. 1: CFG Type0-to-Type1 conversion is enabled if the AD[31:28] is all 1s. bridge will ignore the AD[0] and always treats the cfg transaction as type 1, other AD bit (except AD[31:28], AD[0]) must meet the Type 1 format Reset to 0

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BIT	FUNCTION	TYPE	DESCRIPTION
5:4	PCI Read Multiple Prefetch Mode	RW	00: One cache line prefetch if memory read multiple address is in prefetchable range at the PCI interface 01: Full prefetch if address is in prefetchable range at PCI interface, and the PI7C9X111SL will keep remaining data after it disconnects the external master during burst read with read multiple command until the discard timer expires 10: Full prefetch if address is in prefetchable range at PCI interface 11: Full prefetch if address is in prefetchable range at PCI interface and the PI7C9X111SL will keep remaining data after the read multiple is terminated either by an external master or by the PI7C9X111SL, until the discard time expires Reset to 10
7:6	PCI Read Line Prefetch Mode	RW	00: Once cache line prefetch if memory read address is in prefetchable range at PCI interface 01: Full prefetch if address is in prefetchable range at PCI interface and the PI7C9X111SL will keep remaining data after it is disconnected by an external master during burst read with read line command, until discard timer expires 10: Full prefetch if memory read line address is in prefetchable range at PCI interface 11: Full prefetch if address is in prefetchable range at PCI interface and the PI7C9X111SL will keep remaining data after the read line is terminated either by an external master or by the PI7C9X111SL, until the discard timer expires Reset to 00
9:8	PCI Read Prefetch Mode	RW	00: One cache line prefetch if memory read address is in prefetchable range at PCI interface 01: Reserved 10: Full prefetch if memory read address is in prefetchable range at PCI interface 11: Disconnect on the first DWORD Reset to 00
10	PCI Special Delayed Read Mode Enable	RW	0: Retry any master at PCI bus that repeats its transaction with command code changes. 1: Allows any master at PCI bus to change memory command code (MR, MRL, MRM) after it has received a retry. The PI7C9X111SL will complete the memory read transaction and return data back to the master if the address and byte enables are the same. Reset to 0
11	Optional Malformed Packet checking Enable	RW	0: Optional Malformed Packet checking is disabled 1: Optional Malformed Packet checking is enabled Reset to 0

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BIT	FUNCTION	TYPE	DESCRIPTION
14:12	Maximum Memory Read Byte Count	RW	Maximum byte count is used by the PI7C9X111SL when generating memory read requests on the PCIe link in response to a memory read initiated on the PCI bus and bit [9:8], bit [7:6], and bit [5:4] are set to "full prefetch". 000: 512 bytes (default) 001: 128 bytes 010: 256 bytes 011: 512 bytes 100: 1024 bytes 101: 2048 bytes 110: 4096 bytes 111: 512 bytes Reset to 000

6.3.32 CHIP CONTROL 0 REGISTER – OFFSET 40h

BIT	FUNCTION	TYPE	DESCRIPTION
15	Flow Control Update Control	RW	0: Flow control is updated for every two credits available 1: Flow control is updated for every on credit available Reset to 0
16	PCI Retry Counter Status	RWC	0: The PCI retry counter has not expired since the last reset 1: The PCI retry counter has expired since the last reset Reset to 0
18:17	PCI Retry Counter Control	RW	00: No expiration limit 01: Allow 256 retries before expiration 10: Allow 64K retries before expiration 11: Allow 2G retries before expiration Reset to 00
19	PCI Discard Timer Disable	RW	0: Enable the PCI discard timer in conjunction with bit [27] offset 3Ch (bridge control register) 1: Disable the PCI discard timer in conjunction with bit [27] offset 3Ch (bridge control register) Reset to 0
20	PCI Discard Timer Short Duration	RW	0: Use bit [24] offset 3Ch for forward bridge or bit [25] offset 3Ch for reverse bridge to indicate how many PCI clocks should be allowed before the PCI discard timer expires 1: 64 PCI clocks allowed before the PCI discard timer expires Reset to 0
22:21	Configuration Request Retry Timer Counter Value Control	RW	00: Timer expires at 25us 01: Timer expires at 0.5ms 10: Timer expires at 5ms 11: Timer expires at 25ms Reset to 01
23	Delayed Transaction Order Control	RW	0: Enable out-of-order capability between delayed transactions 1: Disable out-of-order capability between delayed transactions Reset to 0
25:24	Completion Timer Counter Value Control	RW	00: Timer expires at 50us 01: Timer expires at 10ms 10: Timer expires at 50ms 11: Timer disabled Reset to 01

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BIT	FUNCTION	TYPE	DESCRIPTION
26	Isochronous Traffic Support Enable	RW	0: All memory transactions from PCI to PCIe will be mapped to TC0 1: All memory transactions from PCI to PCIe will be mapped to Traffic Class defined in bit [29:27] of offset 40h. Reset to 0
29:27	Traffic Class Used For Isochronous Traffic	RW	Reset to 001
30	Power Saving mode enable	RW	=0 : disable the power saving mode; =1 : enable the power saving mode, and the internal clock for mac/dll/tlp and pci logic is disabled at L1s and L1 state.
31	Primary Configuration Access Lockout	RW	=0 : 9X111 configuration space can be accessed from both interface. =1 : 9X111 configuration space can only be accessed from the secondary interface. primary bus accessed receives completion with CRS status for forward bridge, or target retry for reverse bridge.

6.3.33 RESERVED REGISTER – OFFSET 44h

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Reserved	RO	Reset to 00000000h

6.3.34 ARBITER ENABLE REGISTER – OFFSET 48h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Enable Arbiter 0	RW	0: Disable arbitration for internal PI7C9X111SL request 1: Enable arbitration for internal PI7C9X111SL request Reset to 1
1	Enable Arbiter 1	RW	0: Disable arbitration for master 1 1: Enable arbitration for master 1 Reset to 1
2	Enable Arbiter 2	RW	0: Disable arbitration for master 2 1: Enable arbitration for master 2 Reset to 1
3	Enable Arbiter 3	RW	0: Disable arbitration for master 3 1: Enable arbitration for master 3 Reset to 1
4	Reserved	RW	Reset to 1
5	Reserved	RO	Reset to 0
6	Reserved	RO	Reset to 0
7	Reserved	RO	Reset to 0
8	Reserved	RO	Reset to 0

6.3.35 ARBITER MODE REGISTER – OFFSET 48h

BIT	FUNCTION	TYPE	DESCRIPTION
9	External Arbiter Bit	RW	=0: Enable internal arbiter =1: When using an external arbiter Reset to 0

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BIT	FUNCTION	TYPE	DESCRIPTION
10	Broken Master Timeout Enable	RW	0: Broken master timeout disable 1: This bit enables the internal arbiter to count 16 PCI bus cycles while waiting for FRAME_L to become active when a device's PCI bus GNT is active and the PCI bus is idle. If the broken master timeout expires, the PCI bus GNT for the device is de-asserted. Reset to 0
11	Broken Master Refresh Enable	RW	0: A broken master will be ignored forever after de-asserting its REQ_L for at least 1 clock 1: Refresh broken master state after all the other masters have been served once Reset to 0
19:12	Arbiter Fairness Counter	RW	08h: These bits are the initialization value of a counter used by the internal arbiter. It controls the number of PCI bus cycles that the arbiter holds a device's PCI bus GNT active after detecting a PCI bus REQ_L from another device. The counter is reloaded whenever a new PCI bus GNT is asserted. For every new PCI bus GNT, the counter is armed to decrement when it detects the new fall of FRAME_L. If the arbiter fairness counter is set to 00h, the arbiter will not remove a device's PCI bus GNT until the device has de-asserted its PCI bus REQ. Reset to 08h
20	GNT_L Output Toggling Enable	RW	0: GNT_L not de-asserted after granted master assert FRAME_L 1: GNT_L de-asserts for 1 clock after 2 clocks of the granted master asserting FRAME_L Reset to 0
21	Reserved	RO	Reset to 0

6.3.36 ARBITER PRIORITY REGISTER – OFFSET 48h

BIT	FUNCTION	TYPE	DESCRIPTION
22	Arbiter Priority 0	RW	0: Low priority request to internal PI7C9X111SL 1: High priority request to internal PI7C9X111SL Reset to 1
23	Arbiter Priority 1	RW	0: Low priority request to master 1 1: High priority request to master 1 Reset to 0
24	Arbiter Priority 2	RW	0: Low priority request to master 2 1: High priority request to master 2 Reset to 0
25	Arbiter Priority 3	RW	0: Low priority request to master 3 1: High priority request to master 3 Reset to 0
26	Arbiter Priority 4	RW	0: Low priority request to master 4 1: High priority request to master 4 Reset to 0
27	Reserved	RO	Reset to 0
28	Reserved	RO	Reset to 0
29	Reserved	RO	Reset to 0
30	Reserved	RO	Reset to 0
31	Reserved	RO	Reset to 0

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6.3.37 RESERVED REGISTERS – OFFSET 4Ch

6.3.38 MEMORY READSMART BASE LOWER 32-Bit REGISTER 1 – OFFSET 50h

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Memory Readsmart Base Lower 32-bit Register 1	RW	Memory Readsmart Base Address 1 in conjunction with Memory Readsmart Base Lower 32-bit register 1 and Memory Readsmart Range Size register 1, defines address range 1 in which PCI memory read are allowed (or not allowed) to use the Readsmart mode which is controlled by bit [7:4] of 40h. Reset to 00000000h

6.3.39 MEMORY READSMART BASE UPPER 32-Bit REGISTER 1 – OFFSET 54h

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Memory Readsmart Base Upper 32-bit register 1	RW	Bit[63:32] of Memory Readsmart Base Address 1 Reset to 00000000h

6.3.40 MEMORY READSMART RANGE CONTROL REGISTER 1 – OFFSET 58h

BIT	FUNCTION	TYPE	DESCRIPTION
31:1	Memory Readsmart Range Address 1	RW	define the size of the range 1, maximum 4G byte with granuity of 2 bytes
0	Memory Readsmart Range control	RW	Memory Readsmart Range Control register 0: any PCI memory read with address falling in the range are not allowed to use Readsmart mode. 1: only PCI memory read with address falling in the range are allowed to use Readsmart mode. Reset to 0

6.3.41 MEMORY READSMART BASE LOWER 32-Bit REGISTER 2 – OFFSET 5Ch

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Readsmart Memory Base Lower 32-bit Register 2	RW	Memory Readsmart Base Address 1 in conjunction with Memory Readsmart Base Lower 32-bit register 2 and Memory Readsmart Range Size register 2, defines address range 1 in which PCI memory read are allowed (or not allowed) to use the Readsmart mode which is controlled by bit [7:4] of 40h. Reset to 00000000h

6.3.42 MEMORY READSMART BASE UPPER 32-Bit REGISTER 2 – OFFSET 60h

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Memory Readsmart Base Upper 32-bit register 2	RW	Bit[63:32] of Memory Readsmart Base Address 2 Reset to 00000000h

6.3.43 MEMORY READSMART RANGE SIZE REGISTER 2 – OFFSET 64h

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Memory Readsmart Range Size register 2	RW	Memory Readsmart Range Address 2 defines the size of the range 2, maximum 4G byte

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BIT	FUNCTION	TYPE	DESCRIPTION
			Reset to 00000000h

6.3.44 EXPRESS TRANSMITTER/RECEIVER REGISTER – OFFSET 68h

BIT	FUNCTION	TYPE	DESCRIPTION
1:0	Nominal Driver Current Control	RW	00: 20mA 01: 10mA 10: 28mA 11: Reserved Reset to 00
5:2	Driver Current Scale Multiple Control	RW	0000: 1.00 x nominal driver current 0001: 1.05 x nominal driver current 0010: 1.10 x nominal driver current 0011: 1.15 x nominal driver current 0100: 1.20 x nominal driver current 0101: 1.25 x nominal driver current 0110: 1.30 x nominal driver current 0111: 1.35 x nominal driver current 1000: 0.60 x nominal driver current 1001: 0.65 x nominal driver current 1010: 0.70 x nominal driver current 1011: 0.75 x nominal driver current 1100: 0.80 x nominal driver current 1101: 0.85 x nominal driver current 1110: 0.90 x nominal driver current 1111: 0.95 x nominal driver current Reset to 0000
7:6	Receiver equalization control for 0.13um PHY	RW	=00 : Max Rx Equalization, for input jitter > 0.25 UI =01 : Min Rx Equalization, for input jitter between 0.1 UI and 0.25 UI =1x : Rx Equalization off
11:8	Driver De-emphasis Level Control	RW	0000: 0.00 db 0001: -0.35 db 0010: -0.72 db 0011: -1.11 db 0100: -1.51 db 0101: -1.94 db 0110: -2.38 db 0111: -2.85 db 1000: -3.35 db 1001: -3.88 db 1010: -4.44 db 1011: -5.04 db 1100: -5.68 db 1101: -6.38 db 1110: -7.13 db 1111: -7.96 db Reset to 1000
13:12	Transmitter Termination Control	RW	00: 52 ohms 01: 57 ohms 10: 43 ohms 11: 46 ohms Reset to 00

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BIT	FUNCTION	TYPE	DESCRIPTION
15:14	Receiver Termination Control	RW	00: 52 ohms 01: 57 ohms 10: 43 ohms 11: 46 ohms Reset to 00
29:16	Reserved	RO	Reset to 00h

6.3.45 UPSTREAM MEMORY WRITE FRAGMENT CONTROL REGISTER – OFFSET 68h

BIT	FUNCTION	TYPE	DESCRIPTION
31:30	Memory Write Fragment Control	RW	Upstream Memory Write Fragment Control 00: Fragment at 32-byte boundary 01: Fragment at 64-byte boundary 1x: Fragement at 128-byte boundary Reset to 10h

6.3.46 RESERVED REGISTER – OFFSET 6Ch

6.3.47 EEPROM AUTOLOAD CONTROL/STATUS REGISTER – OFFSET 70h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Initiate EEPROM Read or Write Cycle	RW	This bit will be reset to 0 after the EEPROM operation is finished. 0: EEPROM AUTOLOAD disabled 0 -> 1: Starts the EEPROM Read or Write cycle Reset to 0
1	Control Command for EEPROM	RW	0: Read 1: Write Reset to 0
2	EEPROM Error	RO	0: EEPROM acknowledge is always received during the EEPROM cycle 1: EEPROM acknowledge is not received during EEPROM cycle Reset to 0
3	EPROM Autoload Complete Status	RO	0: EEPROM autoload is not successfully completed 1: EEPROM autoload is successfully completed Reset to 0
5:4	EEPROM Clock Frequency Control	RW	Where PCLK is 125MHz 00: PCLK / 4096 01: PCLK / 2048 10: PCLK / 1024 11: PCLK / 128 Reset to 00
6	EEPROM Autoload Control	RW	0: Enable EEPROM autoload 1: Disable EEPROM autoload Reset to 0
7	Fast EEPROM Autoload Control	RW	=0: normal speed of EEPROM autoload =1: speeds up EEPROM autoload by 8 times Reset to 1
8	EEPROM Autoload Status	RO	0: EEPROM autoload is not on going 1: EEPROM autoload is on going Reset to 0

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BIT	FUNCTION	TYPE	DESCRIPTION
15:9	EEPROM Word Address	RW	EEPROM word address for EEPROM cycle Reset to 0000000
31:16	EEPROM Data	RW	EEPROM data to be written into the EEPROM Reset to 0000h

6.3.48 RESERVED REGISTER – OFFSET 74h

6.3.49 GPIO DATA AND CONTROL REGISTER – OFFSET 78h

BIT	FUNCTION	TYPE	DESCRIPTION
11:0	Reserved	RO	Reset to 000h
15:12	GPIO Output Write-1-to-Clear	RW	Reset to 0h
19:16	GPIO Output Write-1-to-Set	RW	Reset to 0h
23:20	GPIO Output Enable Write-1-to-Clear	RW	Reset to 0h
27:24	GPIO Output Enable Write-1-to-Set	RW	Reset to 0h
31:28	GPIO Input Data Register	RO	Reset to 0h

6.3.50 RESERVED REGISTER – OFFSET 7Ch

6.3.51 PCI-X CAPABILITY ID REGISTER – OFFSET 80h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	PCI-X Capability ID	RO	PCI-X Capability ID Reset to 07h

6.3.52 NEXT CAPABILITY POINTER REGISTER – OFFSET 80h

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Next Capability Pointer	RO	Point to power management Reset to 90h

6.3.53 PCI-X SECONDARY STATUS REGISTER – OFFSET 80h

BIT	FUNCTION	TYPE	DESCRIPTION
16	64-bit Device on Secondary Bus Interface	RO	64-bit not supported Reset to 0
17	133MHz Capable	RO	133MHz capable on secondary interface. this bit is always RO.
18	Split Completion Discarded	RO	Split Completion Discarded this bit is always RO. Reset to 0
19	Unexpected Split Completion	RWC	=0: No unexpected split completion has been recevied. =1: An unexpected split completion has been recevied with the requeste ID equaled to the bridge's secondary port number, device number 00h, and function number 0 on the bridge secondary interface. this bit is RO for forward bridge. Reset to 0
20	Split Completion Overrun	RO	This bit is always RO. Reset to 0

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BIT	FUNCTION	TYPE	DESCRIPTION
21	Split Request Delayed	RWC/RO	=0: The bridge has not delayed a split request. =1: The bridge has delayed a split request because the bridge cannot forward a transaction to secondary port due to not enough room within the limit specified in the split transaction commitment limit field in the downstream split transaction control register. This bit is RO for forward bridge. Reset to 0
24:22	Secondary Clock Frequency	RO	These bits are only meaningful in forward bridge mode. In reverse bridge mode, all three bits are set to zero. 000: Conventional PCI mode (minimum clock period not applicable) 001: 66MHz (minimum clock period is 15ns) 010: 100 to 133MHz (minimum clock period is 7.5ns) 011: Reserved 1xx: Reserved Reset to 000
31:25	Reserved	RO	0000000

6.3.54 PCI-X BRIDGE STATUS REGISTER – OFFSET 84h

BIT	FUNCTION	TYPE	DESCRIPTION
2:0	Function Number	RO	Function Number; the function number (AD[10:8] of a type-0 configuration transaction) to which the bridge responds. Reset to 000
7:3	Device Number	RO	Device Number; the device number (AD[15:11] of a type-0 configuration transaction) is assigned to the bridge by the connection of system hardware. Each time the bridge is addressed by a configuration write transaction, the bridge updates this register with the contents of AD[15:11] of the address phase of the configuration transaction, regardless of which register in the bridge is addressed by the transaction. The bridge is addressed by a configuration write transaction if all of the following are true: • The transaction uses a configuration write command. • IDSEL is asserted during the address phase. • AD[1:0] are 00 (type-0 configuration transaction). • AD[10:8] of the configuration address contain the appropriate function number. Reset to 11111
15:8	Bus Number	RO	Bus Number; It is an additional address from which the contents of the primary bus number register on type-1 configuration space header is read. The bridge uses the bus number, device number, and function number fields to create the completer ID when responding with a split completion to a read of an internal bridge register. These fields are also used for cases when one interface is in conventional PCI mode and the other is in PCIX mode. Reset to 11111111
16	64-bit Device on Primary Bus Interface	RO	64-bit device. Reset to 0
17	133MHz Capable	RO	133MHz capable on primary interface. This bit is always RO. Reset to 0 in forward bridge mode or 1 in reverse bridge mode
18	Split Completion Discarded	RO	This bit is always RO. Reset to 0
19	Unexpected Split Completion	RWC	=0: No unexpected split completion has been recevied. =1: An unexpected split completion has been recevied with the request ID equaled to the bridge's primary port number, device number, and function number on the bridge primary interface. This bit is RO for reverse bridge. Reset to 0
20	Split Completion Overrun	RO	This bit is always RO. Reset to 0

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BIT	FUNCTION	TYPE	DESCRIPTION
21	Split Request Delayed	RWC	When this bit is set to 1, a split request is delayed because PI7C9X111SL is not able to forward the split request transaction to its primary bus due to insufficient room within the limit specified in the split transaction commitment limit field of the downstream split transaction control register Reset to 0
31:22	Reserved	RO	0000000000

6.3.55 UPSTREAM SPLIT TRANSACTION REGISTER – OFFSET 88h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Upstream Split Transaction Capability	RO	Upstream Split Transaction Capability specifies the size of the buffer (in the unit of ADQs) to store split completions for memory read. It applies to the requesters on the secondary bus in addressing the completers on the primary bus. The 0010h value shows that the buffer has 16 ADQs or 2K bytes storage Reset to 0010h
31:16	Upstream Split Transaction Commitment Limit	RW	Upstream Split Transaction Commitment Limit indicates the cumulative sequence size of the commitment limit in units of ADQs. This field can be programmed to any value or equal to the content of the split capability field. For example, if the limit is set to FFFFh, PI7C9X111SL is allowed to forward all split requests of any size regardless of the amount of buffer space available. The split transaction commitment limit is set to 0010h that is the same value as the split transaction capability. Reset to 0010h

6.3.56 DOWNSTREAM SPLIT TRANSACTION REGISTER – OFFSET 8Ch

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Downstream Split Transaction Capability	RO	Downstream Split Transaction Capability specifies the size of the buffer (in the unit of ADQs) to store split completions for memory read. It applies to the requesters on the primary bus in addressing the completers on the secondary bus. The 0010h value shows that the buffer has 16 ADQs or 2K bytes storage Reset to 0010h
31:16	Downstream Split Transaction Commitment Limit	RW	Downstream Split Transaction Commitment Limit indicates the cumulative sequence size of the commitment limit in units of ADQs. This field can be programmed to any value or equal to the content of the split capability field. For example, if the limit is set to FFFFh, PI7C9X111SL is allowed to forward all split requests of any size regardless of the amount of buffer space available. The split transaction commitment limit is set to 0010h that is the same value as the split transaction capability. Reset to 0010h

6.3.57 POWER MANAGEMENT ID REGISTER – OFFSET 90h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Power Management ID	RO	Power Management ID Register Reset to 01h

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6.3.58 NEXT CAPABILITY POINTER REGISTER – OFFSET 90h

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Next Pointer	RO	Next pointer (point to Subsystem ID and Subsystem Vendor ID) Reset to A8h

6.3.59 POWER MANAGEMENT CAPABILITY REGISTER – OFFSET 90h

BIT	FUNCTION	TYPE	DESCRIPTION
18:16	Version Number	RO	Version number that complies with revision 2.0 of the PCI Power Management Interface specification. Reset to 010
19	PME Clock	RO	PME clock is not required for PME_L generation Reset to 0
20	Reserved	RO	Reset to 0
21	Device Specific Initialization (DSI)	RO	DSI – no special initialization of this function beyond the standard PCI configuration header is required following transition to the D0 un-initialized state Reset to 0
24:22	AUX Current	RO	000: 0mA 001: 55mA 010: 100mA 011: 160mA 100: 220mA 101: 270mA 110: 320mA 111: 375mA Reset to 001
25	D1 Power Management	RO	D1 power management is not supported Reset to 0
26	D2 Power Management	RO	D2 power management is not supported Reset to 0
31:27	PME_L Support	RO	PME_L is supported in D3 cold, D3 hot, and D0 states. Reset to 11001

6.3.60 POWER MANAGEMENT CONTROL AND STATUS REGISTER – OFFSET 94h

BIT	FUNCTION	TYPE	DESCRIPTION
1:0	Power State	RW	Power State is used to determine the current power state of PI7C9X111SL. If a non-implemented state is written to this register, PI7C9X111SL will ignore the write data. When present state is D3 and changing to D0 state by programming this register, the power state change causes a device reset without activating the RESET_L of PCI bus interface 00: D0 state 01: D1 state not implemented 10: D2 state not implemented 11: D3 state Reset to 00
7:2	Reserved	RO	Reset to 000000
8	PME Enable	RWS	0: PME_L assertion is disabled 1: PME_L assertion is enabled Reset to 0

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BIT	FUNCTION	TYPE	DESCRIPTION
12:9	Data Select	RO	Data register is not implemented Reset to 0000
14:13	Data Scale	RO	Data register is not implemented Reset to 00
15	PME Status	RWCS	PME_L is supported Reset to 0

6.3.61 PCI-TO-PCI SUPPORT EXTENSION REGISTER – OFFSET 94h

BIT	FUNCTION	TYPE	DESCRIPTION
21:16	Reserved	RO	Reset to 000000
22	B2/B3 Support	RO	0: B2 / B3 not support for D3hot Reset to 0
23	PCI Bus Power/Clock Control Enable	RO	0: PCI Bus Power/Clock Disabled Reset to 0
31:24	Data Register	RO	Data register is not implemented Reset to 00h

6.3.62 RESERVED REGISTERS – OFFSET 98h – 9Ch

6.3.63 CAPABILITY ID REGISTER – OFFSET A0h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Capability ID	RO	Capability ID for Slot Identification. SI is off by default but can be turned on through EEPROM interface Reset to 04h

6.3.64 NEXT POINTER REGISTER – OFFSET A0h

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Next Pointer	RO	Next pointer – points to PCI Express capabilities register Reset to B0h

6.3.65 SLOT NUMBER REGISTER – OFFSET A0h

BIT	FUNCTION	TYPE	DESCRIPTION
20:16	Expansion Slot Number	RW	Expansion slot number Reset to 00000
21	First In Chassis	RW	First in chassis Reset to 0
23:22	Reserved	RO	Reset to 00

6.3.66 CHASSIS NUMBER REGISTER – OFFSET A0h

BIT	FUNCTION	TYPE	DESCRIPTION
31:24	Chassis Number	RW	Chassis number Reset to 00h

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6.3.67 SECONDARY CLOCK AND CLKRUN CONTROL REGISTER – OFFSET A4h

BIT	FUNCTION	TYPE	DESCRIPTION
1:0	S_CLKOUT0 Enable	RW	S_CLKOUT (Slot 0) Enable for forward bridge mode only 00: enable S_CLKOUT0 01: enable S_CLKOUT0 10: enable S_CLKOUT0 11: disable S_CLKOUT0 and driven LOW Reset to 00
3:2	S_CLKOUT1 Enable	RW	S_CLKOUT (Slot 1) Enable for forward bridge mode only 00: enable S_CLKOUT1 01: enable S_CLKOUT1 10: enable S_CLKOUT1 11: disable S_CLKOUT1 and driven LOW Reset to 00
5:4	S_CLKOUT2 Enable	RW	S_CLKOUT (Slot 2) Enable for forward bridge mode only 00: enable S_CLKOUT2 01: enable S_CLKOUT2 10: enable S_CLKOUT2 11: disable S_CLKOUT2 and driven LOW Reset to 00
7:6	S_CLKOUT3 Enable	RW	S_CLKOUT (Slot 3) Enable for forward bridge mode only 00: enable S_CLKOUT3 01: enable S_CLKOUT3 10: enable S_CLKOUT3 11: disable S_CLKOUT3 and driven LOW Reset to 00
8	Reserved	RO	Reset to 0h
9	Reserved	RO	Reset to 0h
10	Reserved	RO	Reset to 0h
11	Reserved	RO	Reset to 0h
12	Reserved	RO	Reset to 0h
13	Secondary Clock Stop Status	RO	Secondary clock stop status 0: secondary clock not stopped 1: secondary clock stopped Reset to 0
14	Secondary Clkrun Protocol Enable	RW	0: disable protocol 1: enable protocol Reset to 0
15	Clkrun Mode	RW	0: Stop the secondary clock only when bridge is at D3hot state 1: Stop the secondary clock whenever the secondary bus is idle and there are no requests from the primary bus Reset to 0
16	ASPM L0s enable control	RW	0: bridge may enter ASPM L0s regardless if Receiver is Electrical Idle 1: bridge may enter ASPM L0s only if Receiver is Electrical Idle Reset to 1
18:17	Scrambling control	RW	Reset to 0
31:19	Reserved	RO	Reset to 0

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6.3.68 CAPABILITY ID REGISTER – OFFSET A8h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Capability ID	RO	Capability ID for subsystem ID and subsystem vendor ID Reset to 0Dh

6.3.69 NEXT POINTER REGISTER – OFFSET A8h

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Next Item Pointer	RO	Next item pointer (point to PCI Express Capability by default but can be programmed to A0h if Slot Identification Capability is enabled) Reset to B0h

6.3.70 RESERVED REGISTER – OFFSET A8h

BIT	FUNCTION	TYPE	DESCRIPTION
31:16	Reserved	RO	Reset to 0000h

6.3.71 SUBSYSTEM VENDOR ID REGISTER – OFFSET ACh

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Subsystem Vendor ID	RO	Subsystem vendor ID identifies the particular add-in card or subsystem Reset to 00h

6.3.72 SUBSYSTEM ID REGISTER – OFFSET ACh

BIT	FUNCTION	TYPE	DESCRIPTION
31:16	Subsystem ID	RO	Subsystem ID identifies the particular add-in card or subsystem Reset to 00h

6.3.73 PCI EXPRESS CAPABILITY ID REGISTER – OFFSET B0h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	PCI Express Capability ID	RO	PCI Express capability ID Reset to 10h

6.3.74 NEXT CAPABILITY POINTER REGISTER – OFFSET B0h

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Next Item Pointer	RO	Next Capabilities Pointer Register Reset to F0h

6.3.75 PCI EXPRESS CAPABILITY REGISTER – OFFSET B0h

BIT	FUNCTION	TYPE	DESCRIPTION
19:16	Capability Version	RO	Reset to 1h

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BIT	FUNCTION	TYPE	DESCRIPTION
23:20	Device / Port Type	RO	0000: PCI Express endpoint device 0001: Legacy PCI Express endpoint device 0100: Root port of PCI Express root complex 0101: Upstream port of PCI Express switch 0110: Downstream port of PCI Express switch 0111: PCI Express to PCI bridge 1000: PCI to PCI Express bridge Others: Reserved Reset to 7h for Forward Bridge or 8h for Reverse Bridge
24	Slot Implemented	RO	Reset to 0 for Forward Bridge or 1 for Reverse Bridge
29:25	Interrupt Message Number	RO	Reset to 0h
31:30	Reserved	RO	Reset to 0

6.3.76 DEVICE CAPABILITY REGISTER – OFFSET B4h

BIT	FUNCTION	TYPE	DESCRIPTION
2:0	Maximum Payload Size	RO	000: 128 bytes 001: 256 bytes 010: 512 bytes 011: 1024 bytes 100: 2048 bytes 101: 4096 bytes 110: reserved 111: reserved Reset to 2h
4:3	Phantom Functions	RO	No phantom functions supported Reset to 00
5	8-bit Tag Field	RO	8-bit tag field supported Reset to 1
8:6	Endpoint L0's Latency	RO	Endpoint L0's acceptable latency 000: less than 64 ns 001: 64 – 128 ns 010: 128 – 256 ns 011: 256 – 512 ns 100: 512 ns – 1 us 101: 1 – 2 us 110: 2 – 4 us 111: more than 4 us Reset to 000
11:9	Endpoint L1's Latency	RO	Endpoint L1's acceptable latency 000: less than 1 us 001: 1 – 2 us 010: 2 – 4 us 011: 4 – 8 us 100: 8 – 16 us 101: 16 – 32 us 110: 32 – 64 us 111: more than 64 us Reset to 000
12	Attention Button Present	RO	0: If Hot Plug is disabled 1: If Hot Plug is enabled at Forward Bridge Reset to 0 when hot-plug is disabled or 1 when hot-plug is enabled through strapping.

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BIT	FUNCTION	TYPE	DESCRIPTION
13	Attention Indicator Present	RO	0: If Hot Plug is disabled 1: If Hot Plug is enable at Forward Bridge Reset to 0 when hot-plug is disabled or 1 when hot-plug is enabled through strapping.
14	Power Indicator Present	RO	0: If Hot Plug is disabled 1: If Hot Plug is enable at Forward Bridge Reset to 0 when hot-plug is disabled or 1 when hot-plug is enabled through strapping.
17:15	Reserved	RO	Reset to 001
25:18	Captured Slot Power Limit Value	RO	These bits are set by the Set_Slot_Power_Limit message Reset to 00h
27:26	Captured Slot Power Limit Scale	RO	This value is set by the Set_Slot_Power_Limit message Reset to 00
31:28	Reserved	RO	Reset to 0h

6.3.77 DEVICE CONTROL REGISTER – OFFSET B8h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Correctable Error Reporting Enable	RW	Reset to 0h
1	Non-Fatal Error Reporting Enable	RW	Reset to 0h
2	Fatal Error Reporting Enable	RW	Reset to 0h
3	Unsupported Request Reporting Enable	RW	Reset to 0h
4	Relaxed Ordering Enable	RO	Relaxed Ordering disabled Reset to 0h
7:5	Max Payload Size	RW	This field sets the maximum TLP payload size for the PI7C9X111SL 000: 128 bytes 001: 256 bytes 010: 512 bytes 011:1024 bytes 100: 2048 bytes 101: 4096 bytes 110: reserved 111: reserved Reset to 000
8	Extended Tag Field Enable	RW	Reset to 0
9	Phantom Functions Enable	RO	Phantom functions not supported Reset to 0
10	Auxiliary Power PM Enable	RO	Auxiliary power PM not supported Reset to 0
11	No Snoop Enable	RO	Bridge never sets the No Snoop attribute in the transaction it initiates Reset to 0

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BIT	FUNCTION	TYPE	DESCRIPTION
14:12	Maximum Read Request Size	RW	This field sets the maximum Read Request Size for the device as a requester 000: 128 bytes 001: 256 bytes 010: 512 bytes 011: 1024 bytes 100: 2048 bytes 101: 4096 bytes 110: reserved 111: reserved Reset to 2h
15	Configuration Retry Enable	RW	Reset to 0

6.3.78 DEVICE STATUS REGISTER – OFFSET B8h

BIT	FUNCTION	TYPE	DESCRIPTION
16	Correctable Error Detected	RWC	Reset to 0
17	Non-Fatal Error Detected	RWC	Reset to 0
18	Fatal Error Detected	RWC	Reset to 0
19	Unsupported Request Detected	RWC	Reset to 0
20	AUX Power Detected	RO	Reset to 1
21	Transaction Pending	RO	0: No transaction is pending on transaction layer interface 1: Transaction is pending on transaction layer interface Reset to 0
31:22	Reserved	RO	Reset to 0000000000

6.3.79 LINK CAPABILITY REGISTER – OFFSET BCh

BIT	FUNCTION	TYPE	DESCRIPTION
3:0	Maximum Link Speed	RO	Indicates the maximum speed of the Express link 0001: 2.5Gb/s link Reset to 1
9:4	Maximum Link Width	RO	Indicates the maximum width of the Express link (x1 at reset) 000000: reserved 000001: x1 000010: x2 000100: x4 001000: x8 001100: x12 010000: x16 100000: x32 Reset to 000001
11:10	ASPM Support	RO	This field indicates the level of Active State Power Management Support 00: reserved 01: L0's entry supported 10: reserved 11: L0's and L1's supported Reset to 11
14:12	L0's Exit Latency	RO	Reset to 3h
17:15	L1's Exit Latency	RO	Reset to 0/6h
23:18	Reserved	RO	Reset to 0/1h
31:24	Port Number	RO	Reset to 00h

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6.3.80 LINK CONTROL REGISTER – OFFSET C0h

BIT	FUNCTION	TYPE	DESCRIPTION
1:0	ASPM Control	RW	This field controls the level of ASPM supported on the Express link 00: disabled 01: L0's entry enabled 10: L1's entry enabled 11: L0's and L1's entry enabled Reset to 00
2	Reserved	RO	Reset to 0
3	Read Completion Boundary (RCB)	RO	Read completion boundary not supported Reset to 0
4	Link Disable	RO / RW	RO for Forward Bridge Reset to 0
5	Retrain Link	RO / RW	RO for Forward Bridge Reset to 0
6	Common Clock Configuration	RW	Reset to 0
7	Extended Sync	RW	Reset to 0
15:8	Reserved	RO	Reset to 00h

6.3.81 LINK STATUS REGISTER – OFFSET C0h

BIT	FUNCTION	TYPE	DESCRIPTION
19:16	Link Speed	RO	This field indicates the negotiated speed of the Express link 001: 2.5Gb/s link Reset to 1h
25:20	Negotiated Link Width	RO	000000: reserved 000001: x1 000010: x2 000100: x4 001000: x8 001100: x12 010000: x16 100000: x32 Reset to 000001
26	Link Train Error	RO	Reset to 0
27	Link Training	RO	Reset to 0
28	Slot Clock Configuration	RO	Reset to 1
31:29	Reserved	RO	Reset to 0

6.3.82 SLOT CAPABILITY REGISTER – OFFSET C4h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Attention Button Present	RO	0: If Hot Plug is disabled 1: If Hot Plug is enabled at reverse bridge Reset to 0 when hot-plug is disabled or 1 when hot-plug is enabled through strapping.
1	Power Controller Present	RO	Reset to 0

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BIT	FUNCTION	TYPE	DESCRIPTION
2	MRL Sensor Present	RO	0: If Hot Plug is disabled 1: If Hot Plug is enabled at reverse bridge Reset to 0 when hot-plug is disabled or 1 when hot-plug is enabled through strapping.
3	Attention Indicator Present	RO	0: If Hot Plug is disabled 1: If Hot Plug is enabled at reverse bridge Reset to 0 when hot-plug is disabled or 1 when hot-plug is enabled through strapping.
4	Power Indicator Present	RO	0: If Hot Plug is disabled 1: If Hot Plug is enabled at reverse bridge Reset to 0 when hot-plug is disabled or 1 when hot-plug is enabled through strapping.
5	Hot Plug Surprise	RO	Reset to 0
6	Hot Plug Capable	RO	0: If Hot Plug is disabled 1: If Hot Plug is enabled at reverse bridge Reset to 0 when hot-plug is disabled or 1 when hot-plug is enabled through strapping.
14:7	Slot Power Limit Value	RO	Reset to 00h
16:15	Slot Power Limit Scale	RO	Reset to 00
18:17	Reserved	RO	Reset to 00
31:19	Physical Slot Number	RO	Reset to 0

6.3.83 SLOT CONTROL REGISTER – OFFSET C8h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Attention Button Present Enable	RW	Reset to 0
1	Power Fault Detected Enable	RW	Reset to 0
2	MRL Sensor Changed Enable	RW	Reset to 0
3	Presence Detect Changed Enable	RW	Reset to 0
4	Command Completed Interrupt Enable	RW	Reset to 0
5	Hot Plug Interrupt Enable	RW	Reset to 0
7:6	Attention Indicator Control	RW	Reset to 0
9:8	Power Indicator Control	RW	Reset to 0
10	Power Controller Control	RW	Reset to 0
15:11	Reserved	RO	Reset to 0

6.3.84 SLOT STATUS REGISTER – OFFSET C8h

BIT	FUNCTION	TYPE	DESCRIPTION
16	Attention Button Pressed	RO	Reset to 0
17	Power Fault Detected	RO	Reset to 0
18	MRL Sensor Changed	RO	Reset to 0
19	Presence Detect Changed	RO	Reset to 0
20	Command Completed	RO	Reset to 0
21	MRL Sensor State	RO	Reset to 0
22	Presence Detect State	RO	Reset to 0
31:23	Reserved	RO	Reset to 0

6.3.85 XPIP CONFIGURATION REGISTER 0 – OFFSET CCh

BIT	FUNCTION	TYPE	DESCRIPTION
0	Hot Reset Enable	RW	Reset to 0

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BIT	FUNCTION	TYPE	DESCRIPTION
1	Loopback Function Enable	RW	Reset to 0
2	Cross Link Function Enable	RW	Reset to 0
3	Software Direct to Configuration State when in LTSSM state	RW	Reset to 0
4	Internal Selection for Debug Mode	RW	Reset to 0
7:5	Negotiate Lane Number of Times	RW	Reset to 3h
12:8	TS1 Number Counter	RW	Reset to 10h
15:13	Reserved	RO	Reset to 0
31:16	LTSSM Enter L1 Timer Default Value	RW	Reset to 0400h

6.3.86 XPIP CONFIGURATION REGISTER 1 – OFFSET D0h

BIT	FUNCTION	TYPE	DESCRIPTION
9:0	L0's Lifetime Timer	RW	Reset to 0
15:10	Reserved	RO	Reset to 0
31:16	L1 Lifetime Timer	RW	Reset to 0

6.3.87 XPIP CONFIGURATION REGISTER 2 – OFFSET D4h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	CDR Recovery Time (in the number of FTS order sets)	RW	Reset to 54h A Fast Training Sequence order set composes of one K28.5 (COM) Symbol and three K28.1 Symbols.
14:8	L0's Exit to L0 Latency	RW	Reset to 2h
15	RXP/RXN polarity inversion	RW	Reset to 0, when set to 1, enable RXP/RXN polarity inversion
22:16	L1 Exit to L0 Latency	RW	Reset to 19h
23	Reserved	RO	Reset to 0

6.3.88 L0 ENTER L1 WAITING PERIOD COUNTER – OFFSET D4h

BIT	FUNCTION	TYPE	DESCRIPTION
31:24	L0 enter L1 waiting period counter	RW	L0 enter L1 waiting period counter =d0: 128ms =d1: 129ms . . =d127: 256ms =d128: 0ms =d129: 1ms . . =d255: 127ms Reset to 00h

6.3.89 CAPABILITY ID REGISTER – OFFSET D8h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Capability ID for VPD Register	RO	Reset to 03h

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6.3.90 NEXT POINTER REGISTER – OFFSET D8h

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Next Pointer	RO	Next pointer (F0h, points to MSI capabilities) Reset to F0h

6.3.91 VPD REGISTER – OFFSET D8h

BIT	FUNCTION	TYPE	DESCRIPTION
17:16	Reserved	RO	Reset to 0
23:18	VPD Address for Read/Write Cycle	RW	Reset to 0
30:24	Reserved	RO	Reset to 0
31	VPD Operation	RW	0: Generate a read cycle from the EEPROM at the VPD address specified in bits [7:2] of offset D8h. This bit remains at '0' until EEPROM cycle is finished, after which the bit is then set to '1'. Data for reads is available at register ECh. 1: Generate a write cycle to the EEPROM at the VPD address specified in bits [7:2] of offset D8h. This bit remains at '1' until EEPROM cycle is finished, after which it is then cleared to '0'. Reset to 0

6.3.92 VPD DATA REGISTER – OFFSET DCh

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	VPD Data	RW	VPD Data (EEPROM data [address + 0x40]) The least significant byte of this register corresponds to the byte of VPD at the address specified by the VPD address register. The data read form or written to this register uses the normal PCI byte transfer capabilities. Reset to 0

6.3.93 EXTENDED CONFIGURATION ACCESS ADDRESS REGISTER – OFFSET E0h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Register Number	RW	Reset to 00h
11:8	Extended Register Number	RW	Reset to 0000
14:12	Function Number	RW	Reset to 000
19:15	Dervice Number	RW	Reset to 00000
27:20	BUS Number	RW	Reset to 00h
30:28	Reserved	RO	Reset to 000
31	Enable bit for extended cfg access from PCI bus	RW	When set to '1' Extended Configuration Access function is enabled Reset to 0

6.3.94 EXTENDED CONFIGURATION ACCESS DATA REGISTER – OFFSET E4h

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Extended Configuration Access Data	RW	Extended Cfg Aaccess Data Register Reset to 0

6.3.95 RESERVED REGISTERS – OFFSET E8h – ECh

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6.3.96 MESSAGE SIGNALED INTERRUPTS ID REGISTER – F0h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Capability ID for MSI Registers	RO	Reset to 05h

6.3.97 NEXT CAPABILITIES POINTER REGISTER – F0h

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Next Pointer	RO	Next pointer (00h indicates the end of capabilities) Reset to 00h

6.3.98 MESSAGE CONTROL REGISTER – OFFSET F0h

BIT	FUNCTION	TYPE	DESCRIPTION
16	MSI Enable	RW	0: Disable MSI and default to INTx for interrupt 1: Enable MSI for interrupt service and ignore INTx interrupt pins
19:17	Multiple Message Capable	RO	000: 1 message requested 001: 2 messages requested 010: 4 messages requested 011: 8 messages requested 100: 16 messages requested 101: 32 messages requested 110: reserved 111: reserved Reset to 000
22:20	Multiple Message Enable	RW	000: 1 message requested 001: 2 messages requested 010: 4 messages requested 011: 8 messages requested 100: 16 messages requested 101: 32 messages requested 110: reserved 111: reserved Reset to 000
23	64-bit Address Capable	RW	Reset to 1
31:24	Reserved	RO	Reset to 00h

6.3.99 MESSAGE ADDRESS REGISTER – OFFSET F4h

BIT	FUNCTION	TYPE	DESCRIPTION
1:0	Reserved	RO	Reset to 00
31:2	System Specified Message Address	RW	Reset to 0

6.3.100 MESSAGE UPPER ADDRESS REGISTER – OFFSET F8h

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	System Specified Message Upper Address	RW	Reset to 0

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6.3.101 MESSAGE DATA REGISTER – OFFSET FCh

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	System Specified Message Data	RW	Reset to 0
31:16	Reserved	RO	Reset to 0

6.3.102 ADVANCE ERROR REPORTING CAPABILITY ID REGISTER – OFFSET 100h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Advance Error Reporting Capability ID	RO	Reset to 0001h

6.3.103 ADVANCE ERROR REPORTING CAPABILITY VERSION REGISTER – OFFSET 100h

BIT	FUNCTION	TYPE	DESCRIPTION
19:16	Advance Error Reporting Capability Version	RO	Reset to 1h

6.3.104 NEXT CAPABILITY OFFSET REGISTER – OFFSET 100h

BIT	FUNCTION	TYPE	DESCRIPTION
31:20	Next Capability Offset	RO	Next capability offset (150h points to VC capability) Reset to 150h

6.3.105 UNCORRECTABLE ERROR STATUS REGISTER – OFFSET 104h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Training Error Status	RWCS	Reset to 0
3:1	Reserved	RO	Reset to 0
4	Data Link Protocol Error Status	RWCS	Reset to 0
11:5	Reserved	RO	Reset to 0
12	Poisoned TLP Status	RWCS	Reset to 0
13	Flow Control Protocol Error Status	RWCS	Reset to 0
14	Completion Timeout Status	RWCS	Reset to 0
15	Completer Abort Status	RWCS	Reset to 0
16	Unexpected Completion Status	RWCS	Reset to 0
17	Receiver Overflow Status	RWCS	Reset to 0
18	Malformed TLP Status	RWCS	Reset to 0
19	ECRC Error Status	RWCS	Reset to 0
20	Unsupported Request Error Status	RWCS	Reset to 0
31:21	Reserved	RO	Reset to 0

6.3.106 UNCORRECTABLE ERROR MASK REGISTER – OFFSET 108h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Training Error Mast	RWS	Reset to 0
3:1	Reserved	RO	Reset to 0
4	Data Link Protocol Error Mask	RWS	Reset to 0
11:5	Reserved	RO	Reset to 0
12	Poisoned TLP Mask	RWS	Reset to 0
13	Flow Control Protocol Error Mask	RWS	Reset to 0

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BIT	FUNCTION	TYPE	DESCRIPTION
14	Completion Timeout Mask	RWS	Reset to 0
15	Completion Abort Mask	RWS	Reset to 0
16	Unexpected Completion Mask	RWS	Reset to 0
17	Receiver Overflow Mask	RWS	Reset to 0
18	Malformed TLP Mask	RWS	Reset to 0
19	ECRC Error Mask	RWS	Reset to 0
20	Unsupported Request Error Mask	RWS	Reset to 0
31:21	Reserved	RO	Reset to 0

6.3.107 UNCORRECTABLE ERROR SEVERITY REGISTER – OFFSET 10Ch

BIT	FUNCTION	TYPE	DESCRIPTION
0	Training Error Severity	RWS	Reset to 1
3:1	Reserved	RO	Reset to 0
4	Data Link Protocol Error Severity	RWS	Reset to 1
11:5	Reserved	RO	Reset to 0
12	Poisoned TLP Severity	RWS	Reset to 0
13	Flow Control Protocol Error Severity	RWS	Reset to 1
14	Completion Timeout Severity	RWS	Reset to 0
15	Completer Abort Severity	RWS	Reset to 0
16	Unexpected Completion Severity	RWS	Reset to 0
17	Receiver Overflow Severity	RWS	Reset to 1
18	Malformed TLP Severity	RWS	Reset to 1
19	ECRC Error Severity	RWS	Reset to 0
20	Unsupported Request Error Severity	RWS	Reset to 0
31:21	Reserved	RO	Reset to 0

6.3.108 CORRECTABLE ERROR STATUS REGISTER – OFFSET 110h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Receiver Error Status	RWCS	Reset to 0
5:1	Reserved	RO	Reset to 0
6	Bad TLP Status	RWCS	Reset to 0
7	Bad DLLP Status	RWCS	Reset to 0
8	REPLAY_NUM Rollover Status	RWCS	Reset to 0
11:9	Reserved	RO	Reset to 0
12	Replay Timer Timeout Status	RWCS	Reset to 0
31:13	Reserved	RO	Reset to 0

6.3.109 CORRECTABLE ERROR MASK REGISTER – OFFSET 114h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Receiver Error Mask	RWS	Reset to 0
5:1	Reserved	RO	Reset to 0
6	Bad TLP Mask	RWS	Reset to 0
7	Bad DLLP Mask	RWS	Reset to 0
8	REPLAY_NUM Rollover Mask	RWS	Reset to 0
11:9	Reserved	RO	Reset to 0
12	Replay Timer Timeout Mask	RWS	Reset to 0
31:13	Reserved	RO	Reset to 0

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6.3.110 ADVANCED ERROR CAPABILITIES AND CONTROL REGISTER – OFFSET 118h

BIT	FUNCTION	TYPE	DESCRIPTION
4:0	First Error Pointer	ROS	Reset to 0h
5	ECRC Generation Capable	RO	Reset to 1
6	ECRC Generation Enable	RWS	Reset to 0
7	ECRC Check Capable	RO	Reset to 1
8	ECRC Check Enable	RWS	Reset to 0
31:9	Reserved	RO	Reset to 0

6.3.111 HEADER LOG REGISTER 1 – OFFSET 11Ch

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Header Byte 3	ROS	Reset to 0
15:8	Header Byte 2	ROS	Reset to 0
23:16	Header Byte 1	ROS	Reset to 0
31:24	Header Byte 0	ROS	Reset to 0

6.3.112 HEADER LOG REGISTER 2 – OFFSET 120h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Header Byte 7	ROS	Reset to 0
15:8	Header Byte 6	ROS	Reset to 0
23:16	Header Byte 5	ROS	Reset to 0
31:24	Header Byte 4	ROS	Reset to 0

6.3.113 HEADER LOG REGISTER 3 – OFFSET 124h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Header Byte 11	ROS	Reset to 0
15:8	Header Byte 10	ROS	Reset to 0
23:16	Header Byte 9	ROS	Reset to 0
31:24	Header Byte 8	ROS	Reset to 0

6.3.114 HEADER LOG REGISTER 4 – OFFSET 128h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Header Byte 15	ROS	Reset to 0
15:8	Header Byte 14	ROS	Reset to 0
23:16	Header Byte 13	ROS	Reset to 0
31:24	Header Byte 12	ROS	Reset to 0

6.3.115 SECONDARY UNCORRECTABLE ERROR STATUS REGISTER – OFFSET 12Ch

BIT	FUNCTION	TYPE	DESCRIPTION
0	Target Abort on Split Completion Status	RWCS	Reset to 0
1	Master Abort on Split Completion Status	RWCS	Reset to 0
2	Received Target Abort Status	RWCS	Reset to 0
3	Received Master Abort Status	RWCS	Reset to 0
4	Reserved	RO	Reset to 0
5	Unexpected Split Completion Error Status	RWCS	Reset to 0
6	Uncorrectable Split Completion Message Data Error Status	RWCS	Reset to 0

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BIT	FUNCTION	TYPE	DESCRIPTION
7	Uncorrectable Data Error Status	RWCS	Reset to 0
8	Uncorrectable Attribute Error Status	RWCS	Reset to 0
9	Uncorrectable Address Error Status	RWCS	Reset to 0
10	Delayed Transaction Discard Timer Expired Status	RWCS	Reset to 0
11	PERR_L Assertion Detected Status	RWCS	Reset to 0
12	SERR_L Assertion Detected Status	RWCS	Reset to 0
13	Internal Bridge Error Status	RWCS	Reset to 0
31:14	Reserved	RO	Reset to 0

6.3.116 SECONDARY UNCORRECTABLE ERROR MASK REGISTER – OFFSET 130h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Target Abort on Split Completion Mask	RWS	Reset to 0
1	Master Abort on Split Completion Mask	RWS	Reset to 0
2	Received Target Abort Mask	RWS	Reset to 0
3	Received Master Abort Mask	RWS	Reset to 1
4	Reserved	RO	Reset to 0
5	Unexpected Split Completion Error Mask	RWS	Reset to 1
6	Uncorrectable Split Completion Message Data Error Mask	RWS	Reset to 0
7	Uncorrectable Data Error Mask	RWS	Reset to 1
8	Uncorrectable Attribute Error Mask	RWS	Reset to 1
9	Uncorrectable Address Error Mask	RWS	Reset to 1
10	Delayed Transaction Discard Timer Expired Mask	RWS	Reset to 1
11	PERR_L Assertion Detected Mask	RWS	Reset to 0
12	SERR_L Assertion Detected Mask	RWS	Reset to 1
13	Internal Bridge Error Mask	RWS	Reset to 0
31:14	Reserved	RO	Reset to 0

6.3.117 SECONDARY UNCORRECTABLE ERROR SEVERITY REGISTER – OFFSET 134h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Target Abort on Split Completion Severity	RWS	Reset to 0
1	Master Abort on Split Completion Severity	RWS	Reset to 0
2	Received Target Abort Severity	RWS	Reset to 0
3	Received Master Abort Severity	RWS	Reset to 0
4	Reserved	RO	Reset to 0
5	Unexpected Split Completion Error Severity	RWS	Reset to 0

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BIT	FUNCTION	TYPE	DESCRIPTION
6	Uncorrectable Split Completion Message Data Error Severity	RWS	Reset to 1
7	Uncorrectable Data Error Severity	RWS	Reset to 0
8	Uncorrectable Attribute Error Severity	RWS	Reset to 1
9	Uncorrectable Address Error Severity	RWS	Reset to 1
10	Delayed Transaction Discard Timer Expired Severity	RWS	Reset to 0
11	PERR_L Assertion Detected Severity	RWS	Reset to 0
12	SERR_L Assertion Detected Severity	RWS	Reset to 1
13	Internal Bridge Error Severity	RWS	Reset to 0
31:14	Reserved	RO	Reset to 0

6.3.118 SECONDARY ERROR CAPABILITY AND CONTROL REGISTER – OFFSET 138h

BIT	FUNCTION	TYPE	DESCRIPTION
4:0	Secondary First Error Pointer	ROW	Reset to 0
31:5	Reserved	RO	Reset to 0

6.3.119 SECONDARY HEADER LOG REGISTER – OFFSET 13Ch – 148h

BIT	FUNCTION	TYPE	DESCRIPTION
35:0	Transaction Attribute	ROS	Transaction attribute, CBE [3:0] and AD [31:0] during attribute phase Reset to 0
39:36	Transaction Command Lower	ROS	Transaction command lower, CBE [3:0] during first address phase Reset to 0
43:40	Transaction Command Upper	ROS	Transaction command upper, CBE [3:0] during second address phase of DAC transaction Reset to 0
63:44	Reserved	ROS	Reset to 0
95:64	Transaction Address	ROS	Transaction address, AD [31:0] during first address phase Reset to 0
127:96	Transaction Address	ROS	Transaction address, AD [31:0] during second address phase of DAC transaction Reset to 0

6.3.120 RESERVED REGISTER – OFFSET 14Ch

6.3.121 VC CAPABILITY ID REGISTER – OFFSET 150h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	VC Capability ID	RO	Reset to 0002h

6.3.122 VC CAPABILITY VERSION REGISTER – OFFSET 150h

BIT	FUNCTION	TYPE	DESCRIPTION
19:16	VC Capability Version	RO	Reset to 1h

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6.3.123 NEXT CAPABILITY OFFSET REGISTER – OFFSET 150h

BIT	FUNCTION	TYPE	DESCRIPTION
31:20	Next Capability Offset	RO	Next capability offset – the end of capabilities Reset to 0

6.3.124 PORT VC CAPABILITY REGISTER 1 – OFFSET 154h

BIT	FUNCTION	TYPE	DESCRIPTION
2:0	Extended VC Count	RO	Reset to 0
3	Reserved	RO	Reset to 0
6:4	Low Priority Extended VC Count	RO	Reset to 0
7	Reserved	RO	Reset to 0
9:8	Reference Clock	RO	Reset to 0
11:10	Port Arbitration Table Entry Size	RO	Reset to 0
31:12	Reserved	RO	Reset to 0

6.3.125 PORT VC CAPABILITY REGISTER 2 – OFFSET 158h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	VC Arbitration Capability	RO	Reset to 0
23:8	Reserved	RO	Reset to 0
31:24	VC Arbitration Table Offset	RO	Reset to 0

6.3.126 PORT VC CONTROL REGISTER – OFFSET 15Ch

BIT	FUNCTION	TYPE	DESCRIPTION
0	Load VC Arbitration Table	RO	Reset to 0
3:1	VC Arbitration Select	RO	Reset to 0
15:4	Reserved	RO	Reset to 0

6.3.127 PORT VC STATUS REGISTER – OFFSET 15Ch

BIT	FUNCTION	TYPE	DESCRIPTION
16	VC Arbitration Table Status	RO	Reset to 0
31:17	Reserved	RO	Reset to 0

6.3.128 VC0 RESOURCE CAPABILITY REGISTER – OFFSET 160h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Port Arbitration Capability	RO	Reset to 0
13:8	Reserved	RO	Reset to 0
14	Advanced Packet Switching	RO	Reset to 0
15	Reject Snoop Transactions	RO	Reset to0
22:16	Maximum Time Slots	RO	Reset to 0
23	Reserved	RO	Reset to 0
31:24	Port Arbitration Table Offset	RO	Reset to 0

6.3.129 VC0 RESOURCE CONTROL REGISTER – OFFSET 164h

BIT	FUNCTION	TYPE	DESCRIPTION
0	TC / VC Map	RO	For TC0 Reset to 1
7:1	TC / VC Map	RW	For TC7 to TC1 Reset to 7Fh

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BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Reserved	RO	Reset to 0
16	Load Port Arbitration Table	RO	Reset to 0
19:17	Port Arbitration Select	RO	Reset to 0
23:20	Reserved	RO	Reset to 0
26:24	VC ID	RO	Reset to 0
30:27	Reserved	RO	Reset to 0
31	VC Enable	RO	Reset to 1

6.3.130 VC0 RESOURCE STATUS REGISTER – OFFSET 168h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Port Arbitration Table 1	RO	Reset to 0
1	VC0 Negotiation Pending	RO	Reset to 0
31:2	Reserved	RO	Reset to 0

6.3.131 RESERVED REGISTERS – OFFSET 16Ch – 300h

6.3.132 EXTRA GPI/GPO DATA AND CONTROL REGISTER – OFFSET 304h

BIT	FUNCTION	TYPE	DESCRIPTION
3:0	Extra GPO	RWC	GPO [3:0], write 1 to clear Reset to 0
7:4	Extra GPO	RWS	GPO [3:0], write 1 to set Reset to 0
11:8	Extra GPO enable	RWC	GPO [3:0] enable, write 1 to clear Reset to 0
15:12	Extra GPO enable	RWS	GPO [3:0] enable, write 1 to set Reset to 0
19:16	Extra GPI	RO	Extra GPI [3:0] Data Register Reset to 0
31:20	Reserved	RO	Reset to 0

6.3.133 RESERVED REGISTERS – OFFSET 308h – 30Ch

6.3.134 REPLAY AND ACKNOWLEDGE LATENCY TIMERS – OFFSET 310h

BIT	FUNCTION	TYPE	DESCRIPTION
11:0	Replay Timer	RW	Replay Timer Reset to 115h
12	Replay Timer Enable	RW	Replay Timer Enable Reset to 0
15:13	Reserved	RO	Reset to 0
29:16	Acknowledge Latency Timer	RW	Acknowledge Latency Timer Reset to 00CDh
30	Acknowledge Latency Timer Enable	RO	Acknowledge Latency Timer Enable Reset to 0
31	Reserved	RO	Reset to 0

6.3.135 RESERVED REGISTERS – OFFSET 314h – FFCh

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7 GPIO PINS AND SM BUS ADDRESS

GPIO[3:0] have been defined for hot-plug usage if MSK_IN=1.

For forward bridge:
GPIO[0] : PCI slot Card Presence Detection Input. "1" indicates that a card is present. "0" indicates that the slot is empty.
GPIO[1] : Attention Button Pressed Input. "1" indicates that the button has been pressed.
GPIO[2] : MRL Sensor Input. "1" indicates that the sensor input is closed. "0" indicates that the sensor input is open.
GPIO[3] : Attention / Power Indication Output. "High" indicates that Attention Indicator LED is on. "Low" indicates that Power Indicator LED is off. "High-Z" indicates that both Attention and Power Indicator LEDs are off.

The bridge receives Attention_Button_Pressed input and the debounced output generates an Attention_Button_Pressed message to PCIe link.

When receiving Attention_Indicator_On/Off/Blinking or Power_Indicator_On/Off/Blinking messges at PCIe link, the bridge drives Attention_Indicator output and Power_Indicator output to High/Low/Blinking (at 2Hz pulse) at GPIO[3].

For reverse bridge:
When the bridge receives an Attention_Button_Pressed message or Attention Button Pressed input, it updates the slot status register, and notifies a hot plug event if hot plug is enabled.

When the root complex writes to the Attention/Power Control register, the bridge transmits Attention/Power Indicator message to PCIe link, and changes Attention/Power Indicator output.

MRL Detect input: The bridge updates MRL status and notifies hot plug event if hot plug is enabled.
Presence Detect input: The bridge updates Presence Detect status and notifies hot plug event if hot plug is enabled.
Completed Hot Plug command: The bridge updates Command Completed bit and notifies hot plug event if hot plug is enabled.
DLL Active field changed: The bridge updates slot status register, and notifies hot plug event if hot plug is enabled.

GPIO[3:0] are defined for SMBUS device ID if TM0=1.

The address-strapping table of SMBUS with GPIO [3:0] pins is defined in the following table:

Table 7-1 SM Bus Device ID Strapping

SM Bus Address Bit	SM Bus device ID
Address bit [7]	= 1
Address bit [6]	= 1
Address bit [5]	= 0
Address bit [4]	= GPIO [3]
Address bit [3]	= GPIO [2]
Address bit [2]	= GPIO [1]
Address bit [1]	= GPIO [0]

The SMBus Commands of PI7C9X111SL are provided below:

Write Word protocol (PEC Disabled):

```
S + Slave Address[7:1] + 0(Wr) + A + 0000_1000 + A + Bus Number[7:0] + A + Device/Function + A + P
S + Slave Address[7:1] + 0(Wr) + A + 0000_1000 + A + Reg Number[7:0] + A + Reg Number[15:8] + A + P
S + Slave Address[7:1] + 0(Wr) + A + 0000_1000 + A + Data[7:0] + A + Data[15:8] + A + P
```


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Read Word protocol (PEC Disabled):

```
S + Slave Address[7:1] + 0(Wr) + A + 0000_1000 + A + Bus Number[7:0] + A + Device/Function + A + P
S + Slave Address[7:1] + 0(Wr) + A + 0000_1000 + A + Reg Number[7:0] + A + Reg Number[15:8] + A + P
S + Slave Address[7:1] + 0(Wr) + A + 0000_1000 + A + Sr + Slave Address[7:1] + 1(Rd) + A + Data[7:0] +
A + Data[15:8] + N + P
```

Where Bus number and device/Function filed have to be 0x00

GPIO[3:0] can be further defined to serve other functions in the further generations.

With 128QFP package, additional three GPI and three GPO pins can be used when external arbiter is selected, and REQ_L[3:1] and GNT_L[3:1] will be mapped to GPI[2:0] and GPO[2:0] respectively.

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8 CLOCK SCHEME

PCI Express interface:
PI7C9X111SL requires 100MHz differential clock inputs through the pins of REFCLKP and REFCLKN.
When the clock applied to PI7C9X111SLB and other end of the PCIe link are from the same clock source,
The MSK_IN input should be kept unchanged before and after reset (PERST_L for forward bridge or RESET_L
For reverse bridge). Otherwise, the MSK_IN input should be different before and after the reset.

PCI interface:
PI7C9X111SL generates four clock outputs, from either external clock input (1MHz to 66MHz) at CLKIN or internal clock generator:

PI7C9X111SL can use configuration control to enable or disable the secondary clock output: CLKOUT[3:0].

PI7C9X111SL used either internally feedbacked clock from CLKOUT[0] or external clock input applied at CLKOUT[0], for internal secondary interface logic.

For using internal clock source, the internal clock generator needs to be enabled with CLKIN driven high or low. CLKIN and M66EN signals become the selection for PCI Frequency at 50MHz/25MHz or 66MHz/33MHz.

Frequency of PCI CLKOUT with internal clock source:

CLKIN	M66EN	PCI Clock
0	0	33MHz
0	1	66MHz
1	0	25MHz
1	1	50MHz

The PI7C9X111SL PCI Clock Outputs, CLKOUT [3:0], can be enabled or disabled through the configuration register.

PI7C9X111SL supports three different implementation of PCI clock.

- Internal clock generator, and internal clock buffering.
  - Internal feedback
  - External feedback
- External clock source, and internal clock buffering.
  - Internal feedback
  - External feedback
- External clock source, and external clock buffering.

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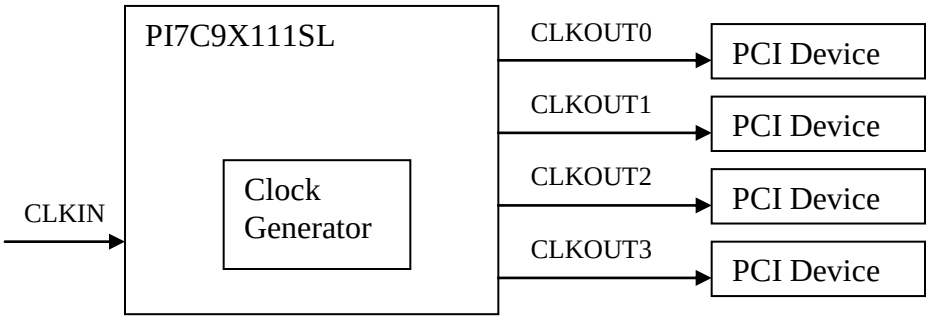
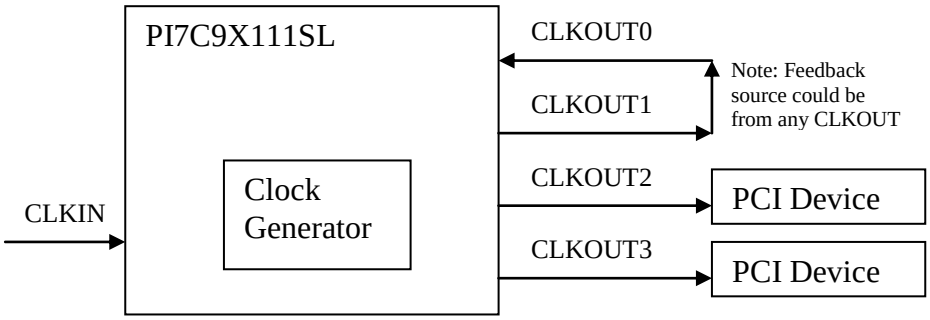
Topology of internal clock generator and internal clock buffering:

1. Internal Feedback:



2. External Feedback:



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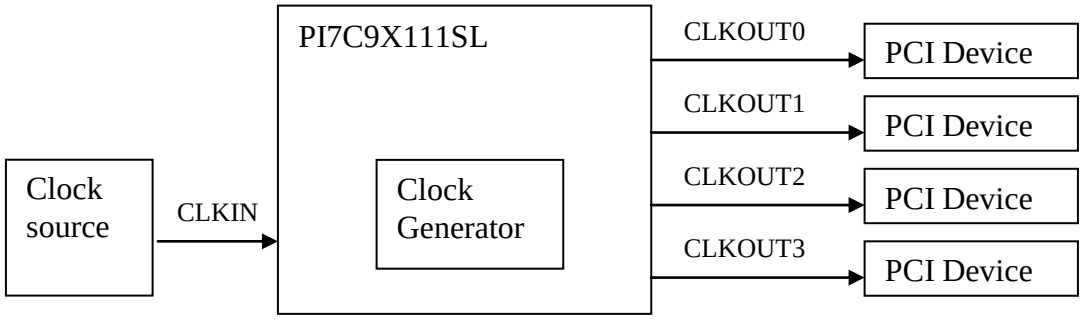
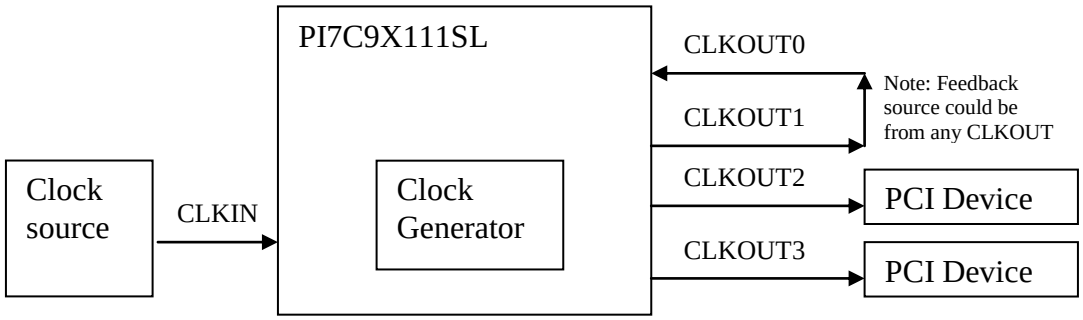
Topology of external clock source and internal clock buffering:

1. Internal Feedback:



2. External Feedback:



In this configuration, user simply connects the external clock source to CLKIN pin. And user needs to make sure the clock is preset (toggling) before the fundamental reset de-asserted (e.g. PERST_L when forward mode, and RESET_L when reverse mode). In this mode, the frequency is the same as the input clock source.

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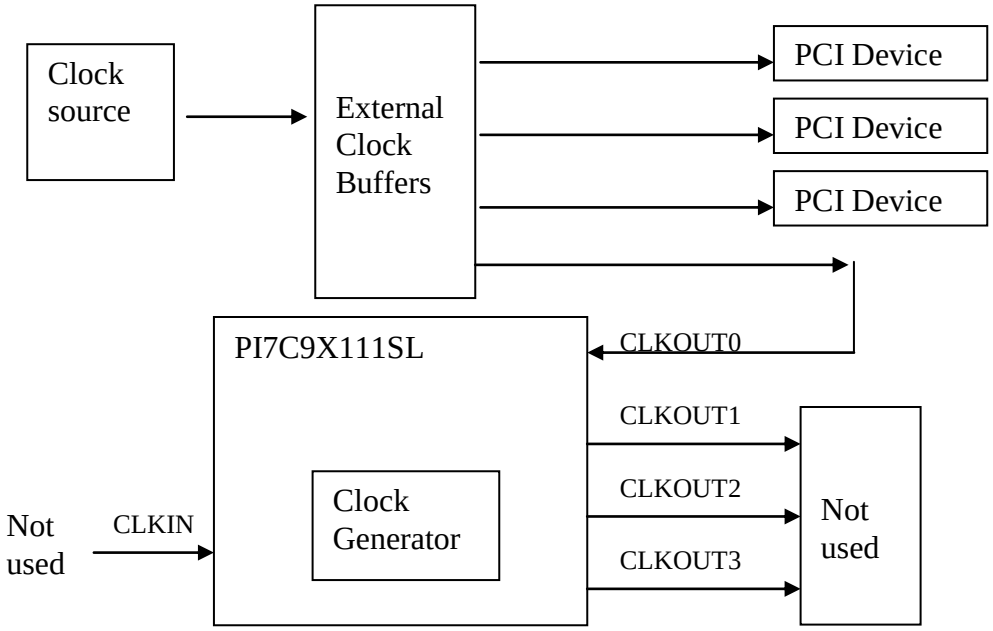
Topology of external clock source and external clock buffering:



In this configuration, user simply connects the external clock from the clock buffers to CLKOUT0. And user needs to make sure the clock is preset (toggling) before the fundamental reset de-asserted (e.g. PERST_L when forward mode, and RESET_L when reverse mode).

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9 INTERRUPTS

PI7C9X111SL supports interrupt message packets on PCIe side. PI7C9X111SL supports PCI interrupt (INTA, B, C, D) pins or MSI (Message Signaled Interrupts) on PCI side. PCI interrupts and MSI are mutually exclusive. In order words, if MSI is enabled, PCI interrupts will be disabled. PI7C9X111SL support 64-bit addressing MSI.

In reverse bridge mode, PI7C9X111SL maps the interrupt message packets to PCI interrupt pins or MSI if MSI is enable (see configuration register bit [16] of Offset F0h).

In forward bridge mode, PI7C9X111SL maps the PCI interrupts pins or MSI if enable on PCI side to interrupt message packets on PCIe side.

There are eight interrupt message packets. They are Assert_INTA, Assert_INTB, Assert_INTC, Assert_INTD, Deassert_INTA, Deassert_INTB, Deassert_INTC, and Deassert_INTD. These eight interrupt messages are mapped to the four PCI interrupts (INTA, INTB, INTC, and INTD). See Table 9-1 for interrupt mapping information in reverse bridge mode. PI7C9X111SL tracks the PCI interrupt (INTA, INTB, INTC, and INTD) pins and maps them to the eight interrupt messages. See Table 9-2 for interrupt mapping information in forward bridge mode.

Table 9-1 PCIe Interrupt Message to PCI interrupt Mapping in Reverse Bridge Mode

PCIe Interrupt messages (from sources of interrupt)	PCI Interrupts (to host controller)
INTA message	INTA
INTB message	INTB
INTC message	INTC
INTD message	INTD

Table 9-2 PCI Interrupt to PCIe Interrupt Message Mapping in Forward Bridge Mode

PCI Interrupts (from sources of interrupts)	PCIe Interrupt message packets (to host controller)
INTA	INTA message
INTB	INTB message
INTC	INTC message
INTD	INTD message

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10 EEPROM (I2C) INTERFACE AND SYSTEM MANAGEMENT BUS

10.1 EEPROM (I2C) INTERFACE

PI7C9X111SL supports EEPROM interface through I2C bus. In EEPROM interface, pin 3 is the EEPROM clock (SCL) and pin 4 is the EEPROM data (SDL). TM1 and TM0 are strapped accordingly to select EEPROM interface or System Management Bus. EEPROM (I2C) interface is enabled with TM1=0 and TM0=0. When EEPROM interface is selected, SCL is an output. SCL is the I2C bus clock to the I2C device. In addition, SDL is a bi-directional signal for sending and receiving data.

10.2 SYSTEM MANAGEMENT BUS

PI7C9X111SL supports SM bus protocol if TM1=0 and TM0=1. In addition, SMBCLK (pin 3) and SMBDAT (pin 4) are utilized as the clock and data pins respectively for the SM bus.

When SM bus interface is selected, SMBCLK pin is an input for the clock of SMbus and SMBDAT pin is an open drain buffer that requires external pull-up resistor for proper operation.

The SM Bus Commands of PI7C9X111SL are provided below:

Write Word protocol (PEC Disabled):

S + Slave Address[7:1] + 0(Wr) + A + 0000_1000 + A + Bus Number[7:0] + A + Device/Function + A + P
S + Slave Address[7:1] + 0(Wr) + A + 0000_1000 + A + Reg Number[7:0] + A + Reg Number[15:8] + A + P
S + Slave Address[7:1] + 0(Wr) + A + 0000_1000 + A + Data[7:0] + A + Data[15:8] + A + P

Read Word protocol (PEC Disabled):

S + Slave Address[7:1] + 0(Wr) + A + 0000_1000 + A + Bus Number[7:0] + A + Device/Function + A + P
S + Slave Address[7:1] + 0(Wr) + A + 0000_1000 + A + Reg Number[7:0] + A + Reg Number[15:8] + A + P
S + Slave Address[7:1] + 0(Wr) + A + 0000_1000 + A + Sr + Slave Address[7:1] + 1(Rd) + A + Data[7:0] + A + Data[15:8] + N + P

Where Bus number and device/Function filed have to be 0x00. For additional info on SMBus programming, please refer to section 7 of datasheets.

10.3 EEPROM AUTOLOAD CONFIGURATION

EEPROM Byte Addresses	Cfg Offset	Description
00-01h		EEPROM signature: Autoload will only proceed if it reads a value of 1516h on the first word loaded.
02h		Region Enable: Enables or disables certain regions of PCI configuration space from being loaded from the EEPROM. bit 0: reserved bit 4-1: 0000=stop autoload at offset 0Bh: Group 1 0001=stop autoload at offset 67h: Group 2 0011=stop autoload at offset AFh: Group 3 0111=stop autoload at offset D7h: Group 4 other combinations are undefined bit 7-5: reserved
03h		Enable Miscellaneous functions: (for transparent mode only) bit 0: ISA Enable control bit write protect: when this bit is set, 9x111 will change the bit 2 of 3Eh into RO, and ISA

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EEPROM Byte Addresses	Cfg Offset	Description
		enable feature will not be available.
04-05h	00-01h	Vendor ID
06-07h	02-03h	Device ID
08h	08h	Revision ID
09h	09h	Class Code: low bytes of Class Code register
0A-0Bh	0A-0Bh	Class Code higher bytes: upper bytes of Class Code register
0Ch	34h	Capability Pointer
0D-0Eh	40-41h	PCI data prefetching control
0F-10h	42-43h	Chip control 0
11-14h	48-4Bh	Arbiter Mode/Enable/Priority
15-18h	68-6Bh	PCIE Transmitter/Receiver control
19-1Ah	81-82h	PCIX Capability
1Bh	108h	Uncorrectable Error Mask register
1C-1Eh	91-93h	Power Management Capability
1F-21h	A1-A3h	SI Capability
22-25h	A4-A7h	Secondary Clock and Clkrun Control
26-29h	A8-ABh	SSID/SSVID Capability
2A-2Dh	AC-AFh	SSID/SSVID
2E-30h	B1-B3h	PCI Express Capabilities
31-34h	B4-B7h	Device Capabilities
35-38h	BC-BFh	Link Capabilities
39-3Ch	C4-C7h	Slot Capabilities
3D-40h	CC-CFh	XPIP Configuration Register 0
41-44h	D0-D3h	XPIP Configuration Register 1
45-48h	D4-D7h	XPIP Configuration Register 2
49-4Ah	D9-DAh	VPD Capability
4B-4Ch	F1-F2h	MSI Capability
4Dh	100h	Advance Error Reporting Capability
4E-4Fh	109-10Ah	Uncorrectable Error Mask register
50-51h	E0-E1h	Extended Cfg Access Address
52-55h	E4-E7h	Extended Cfg Access Data
56-57h	E0-E1h	Extended Cfg Access Address
58-5Bh	E4-E7h	Extended Cfg Access Data
5C-5Dh	E0_E1h	Extended Cfg Access Address
5E-61h	E4-E7h	Extended Cfg Access Data
62-63h	E0_E1h	Extended Cfg Access Address
64-67h	E4-E7h	Extended Cfg Access Data
68-77h		Reserved
79-7Bh	79-7Bh	GPIO Data and Control
7C-7Dh		Reserved
7Eh	86h	PCIX Bridge status
7F-82h	88-8Bh	Upstream Split Transaction
83-86h	8C-8Fh	Downstream Split Transaction
87-8Ah	94-97h	PM Control and Status
8B-8Eh	B4-B7h	Device Capabilities
8F-91h	B8-BAh	Device Control/Status
92h		Reserved
93h	C0h	Link Control/Status
94h		Reserved
95-96h	C2-C3h	Link Control/Status
97-98h	C8-C9h	Slot Control/Status
99-9Ah	3C-3Dh	Interrupt Control
9B-9Eh	DC-DFh	VPD data
9F-A2h	F4-F7h	Message Address
A3-A6h	F8-FBh	Message Upper Address
A7-A8h	FC-FDh	Message Data
A9h		Reserved
AA-ABh	7C-7Dh	Sec Interrupt Control
AC-ADh	310-311h	Replay Timer
AE-AFh	312-313h	Ack Latency Timer

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EEPROM Byte Addresses	Cfg Offset	Description
B0-B3h	04-07h	Command/Status
B4-B6h	0C-0Eh	Cacheline/Primary Latency Timer/Header Type
B7h		Reserved
B8-BBh	18-1Bh	Bus Number/Secondary Latency Timer
BC-BFh	1C-1Fh	I/O Base/Limit / Secondary Status
C0-C3h	20-23h	Memory Base/Limit
C4-C7h	24-27h	Prefetch Memory Base/Limit
C8-CBh	28-2Bh	Prefetch Upper 32 Base
CC-CFh	2C-2Fh	Prefetch Upper 32 Limit
D0-D3h	30-33h	I/O Upper 16 Base/Limit
D4-D5h		Reserved
D6-D7h	3E-3Fh	Bridge Control
D8-FFh		Reserved

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11 HOT PLUG OPERATION

PI7C9X111SL is not equipped with standard hot-plug controller (SHPC) integrated. However, PI7C9X111SL supports hot-plug signaling messages and registers to simplify the implementation of hot-plug system.

Using PI7C9X111SL on motherboard:

- PI7C9X111SL supports hot-plug on PCI bus if forward bridging is selected (REVRSB=0).
- PI7C9X111SL supports hot-plug function on PCI Express bus when reverse bridge mode is selected (REVRSB=1).

Using PI7C9X111SL on add-in card:

- PI7C9X111SL supports hot-plug on PCI Express bus in forward bridge mode. Hot-plug messages will be generated by PI7C9X111SL based on the add-in card conditions.
- PI7C9X111SL supports hot-plug function on PCI bus when reverse bridge mode is selected. PI7C9X111SL will tri-state the PCI bus when RESET is asserted. Also, PI7C9X111SL will de-assert INTA_L if RESET is asserted. The state machine of PI7C9X111SL PCI bus interface will remain idle if the RESET is asserted. After RESET is de-asserted, PI7C9X111SL will remain in idle state until an address phase containing a valid address for PI7C9X111SL or its downstream devices.
- PI7C9X111SL expects the REFCLK signal will be provided to its upstream PCI Express Port prior to the de-assertion of RESET. The Downstream PCI Port of PI7C9X111SL supports a range of frequency up to 66MHz.
- PI7C9X111SL also supports subsystem vendor and subsystem ID. PI7C9X111SL will ignore target response while the bus is idle.

PRSNT1# and PRSNT2# are not implemented on both PI7C9X111SL. The use of these two signals is mandatory on an add-in card in order to support hot-plug.

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12 RESET SCHEME

PI7C9X111SL requires the fundamental reset (PERST_L) input for internal logic when it is set as forward bridge mode. PI7C9X111SL requires the PCI reset (RESET_L) input when it is set as reverse bridge mode. Also, PI7C9X111SL has a power-on-reset (POR) circuit to detect VDDCAUX power supply for auxiliary logic control.

- Cold Reset:

A cold reset is a fundamental or power-on reset that occurs right after the power is applied to PI7C9X111SL (during initial power up). See section 7.1.1 of PCI Express to PCI Bridge Specification, Revision 1.0 for details.

- Warm Reset:

A warm reset is a reset that triggered by the hardware without removing and re-applying the power sources to PI7C9X111SL.

- Hot Reset:

A hot reset is a reset that used an in-band mechanism for propagating reset across a PCIe link to PI7C9X111SL. PI7C9X111SL will enter to training control reset when it receives two consecutive TS1 or TS2 order-sets with reset bit set.

- DL_DOWN Reset:

If the PCIe link goes down, the Transaction and Data Link Layer will enter DL_DOWN status. PI7C9X111SL discards all transactions and returns all logic and registers to initial state except the sticky registers.

Upon receiving reset (cold, warm, hot, or DL_DOWN) on PCIe interface, PI7C9X111SL will generate PCI reset (RESET_L) to the downstream devices on the PCI bus in forward bridge mode. The PCI reset de-assertion follows the de-assertion of the reset received from PCIe interface. The reset bit of Bridge Control Register may be set depending on the application. PI7C9X111SL will tolerant to receive and process SKIP order-sets at an average interval between 1180 to 1538 Symbol Times. PI7C9X111SL does not keep PCI reset active when VD33 power is off even though VAUX (3.3v) is supported. It is recommended to add a weak pull-down resistor on its application board to ensure PCI reset is low when VD33 power is off (see section 7.3.2 of PCI Bus Power management Specification Revision 1.1).

In reverse bridge mode, PI7C9X111SL generates fundamental reset (PERST_L) and then 1024 TS1 order-sets with reset bit set when PCI reset (RESET_L) is asserted to PI7C9X111SL. PI7C9X111SL has scheduling skip order-set for insertion at an interval between 1180 and 1538 Symbol Times.

PI7C9X111SL transmits one Electrical Idle order-set and enters to Electrical Idle.

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13 IEEE 1149.1 COMPATIBLE JTAG CONTROLLER

An IEEE 1149.1 compatible Test Access Port (TAP) controller and associated TAP pins are provided to support boundary scan in PI7C9X111SL for board-level continuity test and diagnostics. The TAP pins assigned are TCK, TDI, TDO, TMS and TRST_L. All digital input, output, input/output pins are tested except TAP pins.

The IEEE 1149.1 Test Logic consists of a TAP controller, an instruction register, and a group of test data registers including Bypass and Boundary Scan registers. The TAP controller is a synchronous 16-state machine driven by the Test Clock (TCK) and the Test Mode Select (TMS) pins. An independent power on reset circuit is provided to ensure the machine is in TEST_LOGIC_RESET state at power-up. The JTAG signal lines are not active when the PCI resource is operating PCI bus cycles.

13.1 INSTRUCTION REGISTER

PI7C9X111SL implements a 5-bit Instruction register to control the operation of the JTAG logic. The defined instruction codes are shown in Table 14-1. Those bit combinations that are not listed are equivalent to the BYPASS (11111) instruction:

Table 13-1 Instruction Register Codes

Instruction	Operation Code (binary)	Register Selected	Operation
EXTEST	00000	Boundary Scan	Drives / receives off-chip test data
SAMPLE	00001	Boundary Scan	Samples inputs / pre-loads outputs
HIGHZ	00101	Bypass	Tri-states output and I/O pins except TDO pin
CLAMP	00100	Bypass	Drives pins from boundary-scan register and selects Bypass register for shifts
IDCODE	01100	Device ID	Accesses the Device ID register, to read manufacturer ID, part number, and version number
BYPASS	11111	Bypass	Selected Bypass Register
INT_SCAN	00010	Internal Scan	Scan test
MEM_BIST	01010	Memory BIST	Memory BIST test

13.2 BYPASS REGISTER

The required bypass register (one-bit shift register) provides the shortest path between TDI and TDO when a bypass instruction is in effect. This allows rapid movement of test data to and from other components on the board. This path can be selected when no test operation is being performed on the PI7C9X111SL.

13.3 DEVICE ID REGISTER

This register identifies Pericom as the manufacturer of the device and details the part number and revision number for the device.

Table 13-2 JTAG Device ID Register

Bit	Type	Value	Description
31:28	RO	01h	Version number
27:12	RO	E110h	Last 4 digits (hex) of the die part number
11:1	RO	23Fh	Pericom identifier assigned by JEDEC
0	RO	1b	Fixed bit equal to 1'b1

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13.4 BOUNDARY SCAN REGISTER

The boundary scan register has a set of serial shift-register cells. A chain of boundary scan cells is formed by connected the internal signal of the PI7C9X111SL package pins. The VDD, VSS, and JTAG pins are not in the boundary scan chain. The input to the shift register is TDI and the output from the shift register is TDO. There are 4 different types of boundary scan cells, based on the function of each signal pin.

The boundary scan register cells are dedicated logic and do not have any system function. Data may be loaded into the boundary scan register master cells from the device input pins and output pin-drivers in parallel by the mandatory SAMPLE and EXTEST instructions. Parallel loading takes place on the rising edge of TCK.

13.5 JTAG BOUNDARY SCAN REGISTER ORDER

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14 POWER MANAGEMENT

PI7C9X111SL supports D0, D3-hot, D3-cold Power States. D1 and D2 states are not supported. The PCI Express Physical Link Layer of the PI7C9X111SL device supports the PCI Express Link Power Management with L0, L0s, L1, L2/L3 ready and L3 Power States. For the PCI Port of PI7C9X111SL, it supports the standard PCI Power Management States with B0, B1, B2 and B3.

During D3-hot state, the main power supplies of VDDP, VDDC, and VD33 can be turned off to save power while keeping the VDDAUX, VDDCAUX, and VAUX with the auxiliary power supplies to maintain all necessary information to be restored to the full power D0 state. PI7C9X111SL has been designed to have sticky registers that are powered by auxiliary power supplies. PME_L pin allows PCI devices to request power management state changes. Along with the operating system and application software, PCI devices can achieve optimum power saving by using PME_L in forward bridge mode. PI7C9X111SL converts PME_L signal information to power management messages to the upstream switches or root complex. In reverse bridge mode, PI7C9X111SL converts the power management event messages from PCIe devices to the PME_L signal and continues to request power management state change to the host bridge.

PI7C9X111SL also supports ASPM (Active State Power Management) to facilitate the link power saving.

PI7C9X111SL supports beacon generation but does not support WAKE# signal during power management.

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15 POWER SEQUENCING

The PI7C9X111SL requires two voltages: 3.3V I/O voltage and 1.0V core voltage. The 1.0V VDDCAUX is consider the same as core voltage, and can be combined as one. When designing the power supplies for PI7C9X111SL, the user can either apply all voltages at the same time, or turn on the higher voltage (3.3V) first, followed by the lower voltages (1.0V) within the suggested maximum delay (50ms). If all power rails are not applied at the same time, the PI7C9X111SL will not be damaged as long as 3.3V is applied either before or at the same time as 1.0V.

15.1 INITIAL POWER-UP (G3 TO L0)

As long as PERST# is active, all PCI Express functions are held in reset. The main supplies ramp up to their specified levels (3.3 V and 12 V). Sometime during this stabilization time, the REFCLK starts and stabilizes. After there has been time (T_{PVPERL}) for the power and clock to become stable, PERST# is deasserted high and the PCI Express functions can start up.

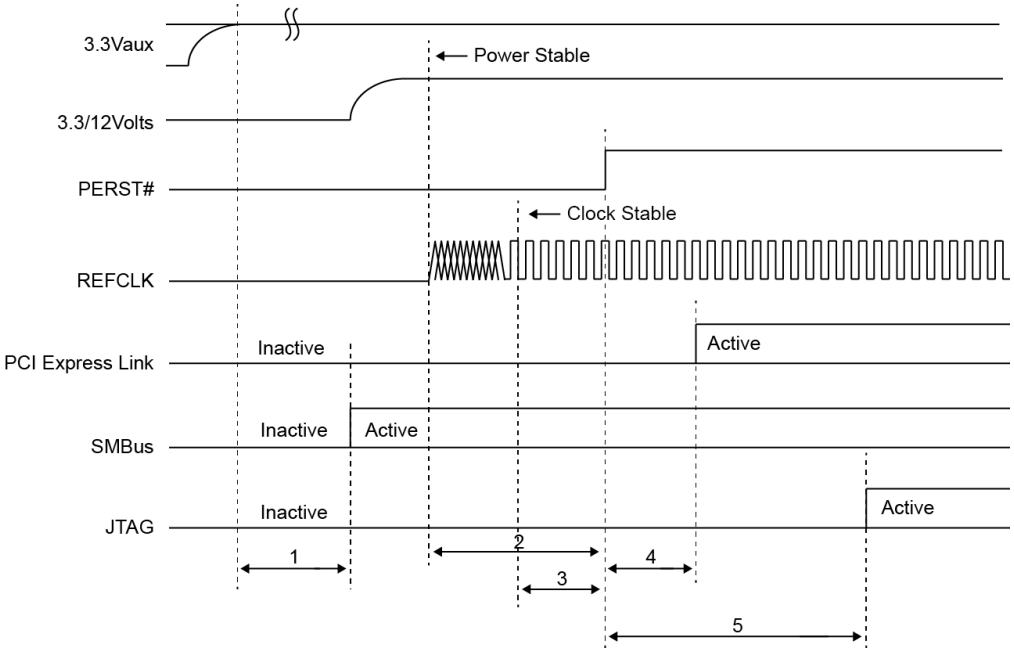

Figure 15-1 Initial Power-up

1. 3.3Vaux stable to SMBus driven (optional). If no 3.3Vaux on platform, the delay is from +3.3V stable
2. Minimum time from power rails within specified tolerance to PERST# inactive (T_{PVPERL})
3. Minimum clock valid to PERST# inactive ($T_{PERST-CLK}$)
4. Minimum PERST# inactive to PCI Express link out of electrical idle
5. Minimum PERST# inactive to JTAG driven (optional)

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Table 15-1 Power Sequencing and Reset Signal Timings

Symbol	Parameter	Min	Max	Units
T_{PVPERL} [1]	Power stable to PERST# inactive	100		ms
$T_{PERST-CLK}$ [2]	REF CLK stable before PERST# inactive	100		µs
T_{PERST}	PERST# active time	100		µs
T_{FAIL} [3]	Power level invalid to PERST# active		500	ns
T_{WKRF} [4]	WAKE# rise – fall time		100	ns

Note:

1. Any supplied power is stable when it meets the requirements specified for that power supply.
2. A supplied reference clock is stable when it meets the requirements specified for the reference clock. The PEREST# signal is asserted and de-asserted asynchronously with respect to the supplied reference clock.
3. The PEREST# signal must be asserted within T_{FAIL} of any supplied power going out specification.
4. Measured from WAKE# assertion/de-assertion to valid input level at the system PM controller. Since WAKE# is an open-drain signal, the rise time is dependent on the total capacitance on the platform and the system board pull-up resistor. It is the responsibility of the system designer to meet the rise time specification.

15.2 POWER-OFF SEQUENCE

The power off sequence is the reverse of the power on sequence, that is, asserts the PERST# first, then after T_{PERST_CLK} disable the REFCLK, and power off core power and I/O power, but I/O power off should be the same time or later than the core power off.

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16 ELECTRICAL AND TIMING SPECIFICATIONS

16.1 ABSOLUTE MAXIMUM RATINGS

Table 16-1 Absolute Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Item	Absolute Max. Rating
Storage Temperature	-65°C to 150°C
PCI Express supply voltage to ground potential (VDDA, VDDP, VDDC, VDDAUX, and VDDCAUX)	-0.3v to 1.2v
PCI Express Termination Supply Voltage to ground potential (VTT)	-0.3v to 2.0v
PCI supply voltage to ground potential (VD33 and VAUX)	-0.3v to 3.8v
DC input voltage for PCI Express signals	-0.3v to 1.2v
DC input voltage for PCI signals	-0.3v to 5.75v

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

16.2 DC SPECIFICATIONS

Table 16-2 DC Electrical Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
VDDA	Analog Power Supply for PCI Express Interface		0.9	1.0	1.1	V
VDDP	Digital Power Supply for PCI Express Interface		0.9	1.0	1.1	V
VDDC	Digital Power Supply for the Core		0.9	1.0	1.1	V
VDDAUX	Digital Auxiliary Power Supply for PCI Express Interface		0.9	1.0	1.1	V
VDDCAUX	Digital Auxiliary Power Supply for the Core		0.9	1.0	1.1	V
VTT	Termination Power Supply for PCI Express Interface		1.0	1.5	1.8	V
VD33	Digital Power Supply for PCI Interface		3.0	3.3	3.6	V
VAUX	Digital Auxiliary Power Supply for PCI Interface		3.0	3.3	3.6	V
V_{IH}	PCI Input High Voltage		1.55		5.5	V
V_{IL}	PCI Input Low Voltage		-0.3		1.08	V
I_{IL}	PCI Input Leakage Current	$0<V_{IN}<VD33$			±10	µA
V_{OH}	PCI Output High Voltage	I_{out} = -500µA	2.7			V
V_{OL}	PCI Output Low Voltage	I_{out} = 1500µA			0.36	V
C_{IN}	PCI Input Pin Capacitance				10	pF
C_{CLK}	PCI CLK Pin Capacitance		5		12	pF
C_{IDSEL}	PCI IDSEL Pin Capacitance				8	pF

In order to support auxiliary power management fully, it is recommended to have VDDP and VDDAUX separated. By the same token, VD33/VDDC and VAUX/VDDCAUX need to be separated for auxiliary power management support. However, if auxiliary power management is not required, VD33 and VDDC can be connected to VAUX and VDDCAUX respectively.

The typical power consumption of PI7C9X111SL is less than 0.45 watt.

PI7C9X111SL is capable of sustaining 2000V human body model for the ESD protection without any damages.

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16.3 AC SPECIFICATIONS

Table 16-3 PCI Bus Timing Parameters

Symbol	Parameter	66 MHz		33 MHz		Units
		Min	Max	Min	Max	
Tsu	Input setup time to CLK – bused signals [1,2,3]	3	-	7	-	ns
Tsu (ptp)	Input setup time to CLK – point-to-point [1,2,3]	5	-	10, 12[4]	-	
Th	Input signal hold time from CLK [1,2]	0	-	0	-	
Tval	CLK to signal valid delay – bused signals [1,2,3]	2	6	2	11	
Tval (ptp)	CLK to signal valid delay – point-to-point [1,2,3]	2	6	2	12	
Ton	Float to active delay [1,2]	2	-	2	-	
Toff	Active to float delay [1,2]	-	14	-	28	

1. See Figure 16 –1 PCI Signal Timing Measurement Conditions.
2. All PCI interface signals are synchronized to CLKOUT0.
3. Point-to-point signals are REQ_L [7:0], GNT_L [7:0], LOO, and ENUM_L. Bused signals are AD, CBE, PAR, PERR_L, SERR_L, FRAME_L, IRDY_L, TRDY_L, LOCK_L, STOP_L and IDSEL.
4. REQ_L signals have a setup of 10ns and GNT_L signals have a setup of 12ns.

Figure 16-1 PCI Signal Timing Conditions

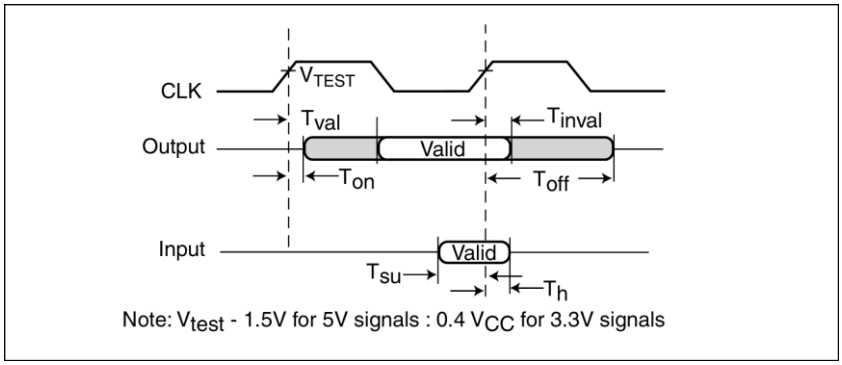

Table 16-4 specifies the voltage and timing requirements for the input clock signals.

Table 16-4 PCIe Reference Clock Timing Parameters

Symbol	Description	Min	Typical	Max	Unit
$ClkIn_{FREQ}$	Input clock frequency range		100		MHz
$ClkIn_{DC}$	Duty cycle of input clock	40	50	60	%
T_R, T_F	Rise/Fall time of input clocks			0.2	RCUI[a]
V_{SW}	Differential input voltage swing (peak-to-peak)	400	600	1200	mV
V_{CM}	Input common voltage	0.6	0.65	0.7	V

a. RCUI(Reference Clock Unit Interval) refers to the reference clock period.

Table 16-5 PCI Express Interface - Differential Transmitter (TX) Output Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Unit Interval	UI	399.88	400.0	400.12	ps
Differential p-p TX voltage swing	$V_{TX-DIFF-P-P}$	800	-	-	mV ppd
Lower power differential p-p TX voltage swing	$V_{TX-DIFF-P-P-LOW}$	400	-	-	mV ppd
TX de-emphasis level ratio	$V_{TX-DE-RATIO}$	-3.0	-	-4.0	dB

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Parameter	Symbol	Min	Typ	Max	Unit
Minimum TX eye width	T_{TX-EYE}	0.75	-	-	UI
Maximum time between the jitter median and max deviation from the median	$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	-	-	0.125	UI
Transmitter rise and fall time	$T_{TX-RISE-FALL}$	0.125	-	-	UI
Maximum TX PLL Bandwidth	BW_{TX-PLL}	-	-	22	MHz
Maximum TX PLL BW for 3dB peaking	$BW_{TX-PLL-LO-3DB}$	1.5	-	-	MHz
Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle	$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	0	-	100	mV
Absolute Delta of DC Common Mode Voltage between D+ and D–	$V_{TX-CM-DC-LINE-DELTA}$	0	-	25	mV
Electrical Idle Differential Peak Output Voltage	$V_{TX-IDLE-DIFF-AC-p}$	0	-	20	mV
The Amount of Voltage Change Allowed During Receiver Detection	$V_{TX-RCV-DETECT}$	-	-	600	mV
Transmitter DC Common Mode Voltage	$V_{TX-DC-CM}$	0	-	3.6	V
Transmitter Short-Circuit Current Limit	$I_{TX-SHORT}$	-	-	90	mA
DC Differential TX Impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω
Lane-to-Lane Output Skew	$L_{TX-SKEW}$	-	-	500 ps + 2 UI	ps

Table 16-6 PCI Express Interface - Differential Receiver (RX) Input Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Unit Interval	UI	399.88	400.0	400.12	ps
Differential RX Peak-to-Peak Voltage	$V_{RX-DIFF-PP-CC}$	175	-	1200	mV
Receiver eye time opening	T_{RX-EYE}	0.4	-	-	UI
Maximum time delta between median and deviation from median	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	-	-	0.3	UI
Receiver DC common mode impedance	Z_{RX-DC}	40	-	60	Ω
DC differential impedance	$Z_{RX-DIFF-DC}$	80	-	120	Ω
RX AC Common Mode Voltage	$V_{RX-CM-AC-P}$	-	-	150	mV
DC input CM input impedance during reset or power down	$Z_{RX-HIGH-IMP-DC}$	200	-	-	kΩ
Electrical Idle Detect Threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	-	175	mV
Lane to Lane skew	$L_{RX-SKEW}$	-	-	20	ns

16.4 OPERATING AMBIENT TEMPERATURE

Table 16-7 Operating Ambient Temperature

(Above witch the useful life may be impaired.)

Item	Low	High	Unit
Ambient Temperature with power applied	-40	85	°C

Note: Exposure to high temperature conditions for extended periods of time may affect reliability.

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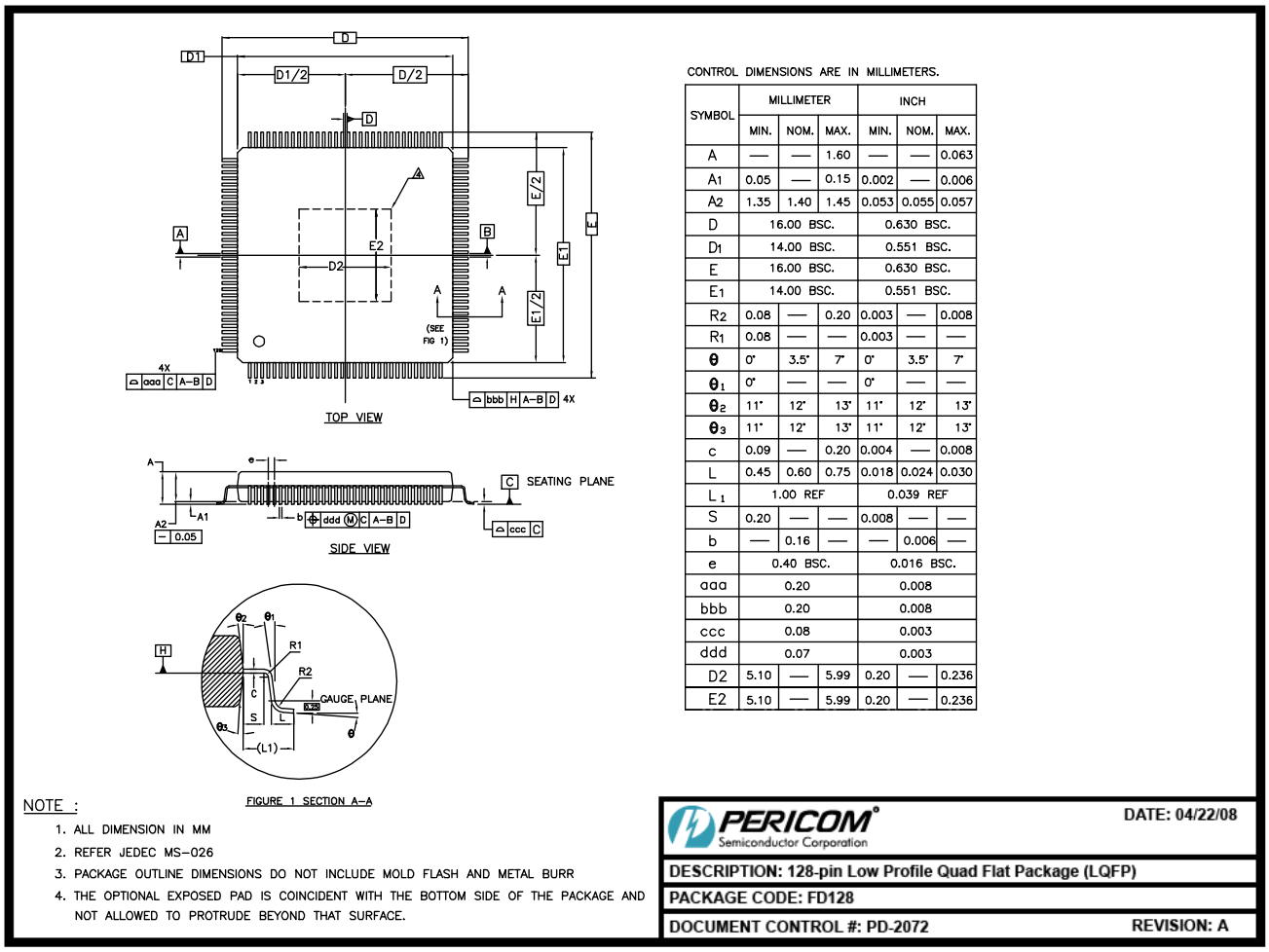
17 PACKAGE INFORMATION

The package of PI7C9X111SL comes in 14mm x 14mm LQFP (128 Pin) package. The pin pitch is 0.4mm. This package also includes an exposed ground on the bottom surface of the package. Pericom highly recommends implementing this exposed ground pad on any customer boards. The following are the package information and mechanical dimension:



CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	16.00 BSC.			0.630 BSC.		
D1	14.00 BSC.			0.551 BSC.		
E	16.00 BSC.			0.630 BSC.		
E1	14.00 BSC.			0.551 BSC.		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	—	0.16	—	—	0.006	—
e	0.40 BSC.			0.016 BSC.		
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		
D2	5.10	—	5.99	0.20	—	0.236
E2	5.10	—	5.99	0.20	—	0.236

NOTE :
1. ALL DIMENSION IN MM
2. REFER JEDEC MS–026
3. PACKAGE OUTLINE DIMENSIONS DO NOT INCLUDE MOLD FLASH AND METAL BURR
4. THE OPTIONAL EXPOSED PAD IS COINCIDENT WITH THE BOTTOM SIDE OF THE PACKAGE AND NOT ALLOWED TO PROTRUDE BEYOND THAT SURFACE.

PERICOM Semiconductor Corporation — DATE: 04/22/08

DESCRIPTION: 128-pin Low Profile Quad Flat Package (LQFP)

PACKAGE CODE: FD128

DOCUMENT CONTROL #: PD-2072 — REVISION: A

07-0353

Figure 17-1 Package Outline Drawing

YY: Year
WW: Workweek
1st X: Assembly Code
2nd X: Fab Code

Figure 17-2 Part Marking

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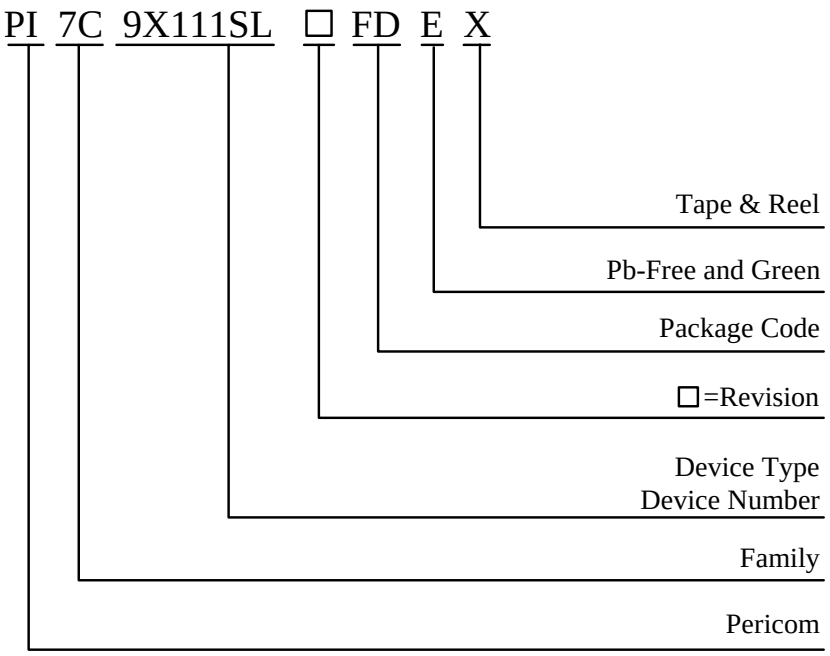
18 ORDERING INFORMATION

Part Number	Pin – Package	Pb-Free & Green	Temperature Range
PI7C9X111SL □FDEX	128-pin, Low Profile Quad Flat Package (LQFP) (Exposed ground pad)	YES	-40°C to 85°C

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.



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