Pin Description

Pin #	Pin Name	I/O	Description
B1, F1, D2, E2, B3, F3, H4, B8, F8, B10, F10	V_{DD}	PWR	Supply Voltage, 1.5V to 1.8V ± 0.1V
C3 D3	AI+ AI-	I	CML Input Channel A with internal 50Ω pull down
E1, J1, F2, E3, J3, H7, E8, J8, D9, E9, F9, E10, J10	GND	PWR	Supply Ground
C8 D8	BI+ BI-	I	CML Input Channel B with internal 50Ω pull down
G3 H3	CI+ CI-	I	CML Input Channel C with internal 50Ω pull down
G8 H8	DI+ DI-	I	CML Input Channel D with internal 50Ω pull down
A3, B4, B5	SEL[0:2]_A	I	Selection pins for equalizer (see Amplifier Configuration Table) w/ 50kΩ internal pull up
A4, C4, C5	SEL[0:2]_B	I	
G2, J2, J4	SEL[0:2]_C	I	
H2, K2, J5	SEL[0:2]_D	I	
B6, A5	SEL[3:4]_A	I	Selection pins for amplifier (see Amplifier Configuration Table) w/ 50kΩ internal pull up
C6, A6	SEL[3:4]_B	I	
K3, K4	SEL[3:4]_C	I	
J6, J9	SEL[3:4]_D	I	
B7, A7	SEL[5:6]_A	I	Selection pins for De-Emphasis (See De-Emphasis Configuration Table) w/ 50kΩ internal pull up
C7, A8	SEL[5:6]_B	I	
K9, G9	SEL[5:6]_C	I	
K10, H9	SEL[5:6]_D	I	
C10 D10	AO+ AO-	O	CML Output Channel A internal 50Ω pull up to V_{DD} during normal operation and 2kΩ when EN_A=0. Drives to output common mode voltage when input is $<V_{TH-}$.
C1 D1	BO+ BO-	O	CML Output Channel B with internal 50Ω pull up to V_{DD} during normal operation and 2kΩ when EN_B=0. Drives to output common mode voltage when input is $<V_{TH-}$.
G10 H10	CO+ CO-	O	CML Output Channel C with internal 50Ω pull up to V_{DD} during normal operation and 2kΩ when EN_C=0. Drives to output common mode voltage when input is $<V_{TH-}$.
G1 H1	DO+ DO-	O	CMLOutput Channel D with internal 50Ω pull up to V_{DD} during normal operation and 2kΩ when EN_D=0. Drives to output common mode voltage when input is $<V_{TH-}$.
A9, A10, B9, C9	EN_ [A,B,C,D]	I	Active HIGH LVCMOS signal input pins, when HIGH, it enables the CML output. When LOW, it disables the CML output (x0+, x0-) to HI-z state. Both x0+ & x0- outputs will be pulled up to V_{DD} by internal 2kΩ resistor.

(Continued)

Pin #	Pin Name	I/O	Description
H6 H5	CKIN- CKIN+	I	Differential Reference Clock Input
K5 K6	OUT0+, OUT0-	O	Differential Reference Clock Outputs
K7 K8	OUT1+, OUT1-	O	
J7	IREF	O	External 475Ω resistor connection to set the differential output current
K1	EN_CLK	I	Active HIGH LVCMOS signal input pin. When HIGH, it enables the OUTx+/OUTx- outputs. When LOW, it disables these outputs, with 50Ω to ground termination.
C2,B2,A1,A2	SD_A, SD_B, SD_C, SD_D	O	Signal detect output. Provides a LVCMOS high output when a valid input signal is detected. When low, SD_X indicates that the input signal level is below the signal detect threshold level.

Output Swing Control

SEL3_[A:D]	SEL4_[A:D]	Swing
0	0	1x
0	1	0.8x
1	0	1.2x
1	1	1.4x

Output De-emphasis Adjustment

SEL5_[A:D]	SEL6_[A:D]	De-emphasis
0	0	0dB
0	1	-2.5dB
1	0	-3.5dB
1	1	-4.5dB

Equalizer Selection

SEL0_[A:D]	SEL1_[A:D]	SEL2_[A:D]	Compliance Channel @ 1.6GHz
0	0	0	No Equalization
0	0	1	0.5dB ± 0.5dB
0	1	0	1.5dB ± 1.0dB
0	1	1	2.5dB ± 1.0dB
1	0	0	3.5dB ± 1.0dB
1	0	1	4.5dB ± 1.0dB
1	1	0	5.5dB ± 1.0dB
1	1	1	6.5dB ± 1.0dB

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5V to +2.5V
DC SIG Voltage	–0.5V to V_{DD} +0.5V
Current Output	-25mA to +25mA
Power Dissipation Continous	800mW
Operating Temperature	–40 to +85°C

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

AC/DC Electrical Characteristics (V_{DD} = 1.4V to 1.9V)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Ps	Supply Power	EN = LVCMOS Low			0.1	W
		EN = LVCMOS High			0.6	
t_{PD}	Latency	From input to output		2.0		ns
CML Receiver Input						
$V_{RX-DIFFP-P}$	Differential Input Peak-to-peak Voltage		0.200			V
$V_{RX-CM-ACP}$	AC Peak Common Mode Input Voltage				150	mV
V_{TH}-	Signal Detect Threshold	E_{N_X} = High	50		200	mVp-p
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance		80	100	120	Ω
Z_{RX-DC}	DC Input Impedance		40	50	60	
Equalization						
J_{RS}	Residual Jitter(1,2)	Total Jitter			0.3	Ulp-p
		Deterministic jitter			0.2	
J_{RM}	Random Jitter(1,2)			1.5		psrms

Notes

1. K28.7 pattern is applied differentially at point A as shown in Figure 1.
2. Total jitter does not include the signal source jitter. Total jitter (TJ) = (14.1 × RJ + DJ) where RJ is random RMS jitter and DJ is maximum deterministic jitter. Signal source is a K28.5 ± pattern (00 1111 1010 11 0000 0101) for the deterministic jitter test and K28.7 (0011111000) or equivalent for random jitter test. Residual jitter is that which remains after equalizing media-induced losses of the environment of Figure 1 or its equivalent. The deterministic jitter at point B must be from media-induced loss, and not from clock source modulation. Jitter is measured at 0V at point C of Figure 1.

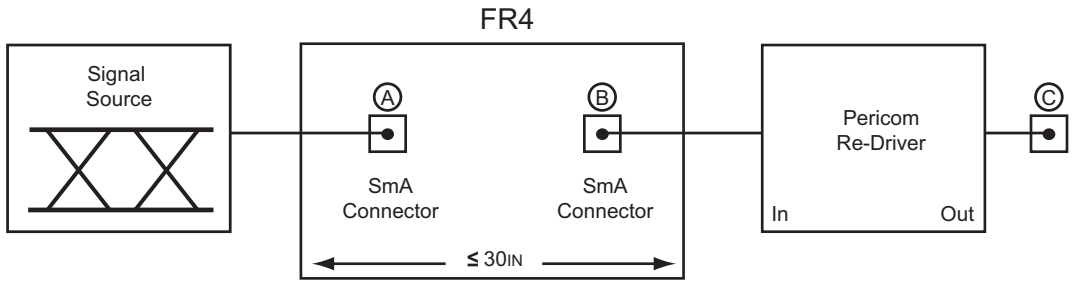


Figure 1. Test Condition Referenced in the Electrical Characteristic Table

AC/DC Electrical Characteristics (V_{DD} = 1.4V to 1.9V)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
CML Transmitter Output (100-Ohm differential)						
V_{DIFFP}	Output Voltage Swing | V_{TX-D+} - V_{TX-D-} |		200		600	mVp-p
$V_{TX-DIFFP-P}$	Output Voltage Swing | V_{TX-D+} - V_{TX-D-} |		400(2)		1200(3)	mVp-pd
V_{TX-C}(4)	Common-Mode Voltage	| V_{TX-D+} - V_{TX-D-} | / 2		V_{DD} - 0.3		
t_F, t_R	Transition Time	20% to 80%(1)			150	ps
Z_{OUT}	Output Resistance	Single-ended	40	50	60	Ω
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance		80	100	120	Ω
C_{TX}	AC Coupling Capacitor		75		200	nF
LVCMOS Control Pins						
V_{IH}	Input High Voltage		0.65 × V_{DD}		V_{DD}	V
V_{IL}	Input Low Voltage				0.35 × V_{DD}	
I_{IH}	Input High Current				250	µA
I_{IL}	Input Low Current				500	
LVCMOS Outputs						
V_{OH}	Output HIGH Voltage	I_{OH} = -10mA	V_{DD}-0.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 10mA			0.4	V

Note:
1. Using K28.7 (0011111000) pattern)
2. When 0.8x swing selected
3. When 1.4x swing selected
4. The parameter is determined by device characterization, and is not production tested

AC Switching Characteristics for Clock Buffer (V_{DD} = 1.4 to 1.9V) [3]

Symbol	Parameters	Min	Max.	Units	Notes
T_{rise} / T_{fall}	Rise and Fall Time (measured between 0.175V to 0.525V) [1]	125	525	ps	1
ΔT_{rise} / ΔT_{fall}	Rise and Fall Time Variation		75		1
V_{HIGH}	Voltage High including overshoot	660	900	mV	1
V_{LOW}	Voltage Low including undershoot	-150			1
V_{CROSS}	Absolute crossing point voltages	-200	550		1
ΔV_{CROSS}	Total Variation of Vcross over all edges	200	250		1
T_{DC}	Duty Cycle (input duty cycle = 50%) [2]	45	55	%	2

Notes:
1. Measurement taken from Single Ended waveform.
2. Measurement taken from Differential waveform.
3. Test configuration is R_S = 33.2Ω, Rp = 49.9Ω, and 2pF.

Configuration Test Load Board Termination

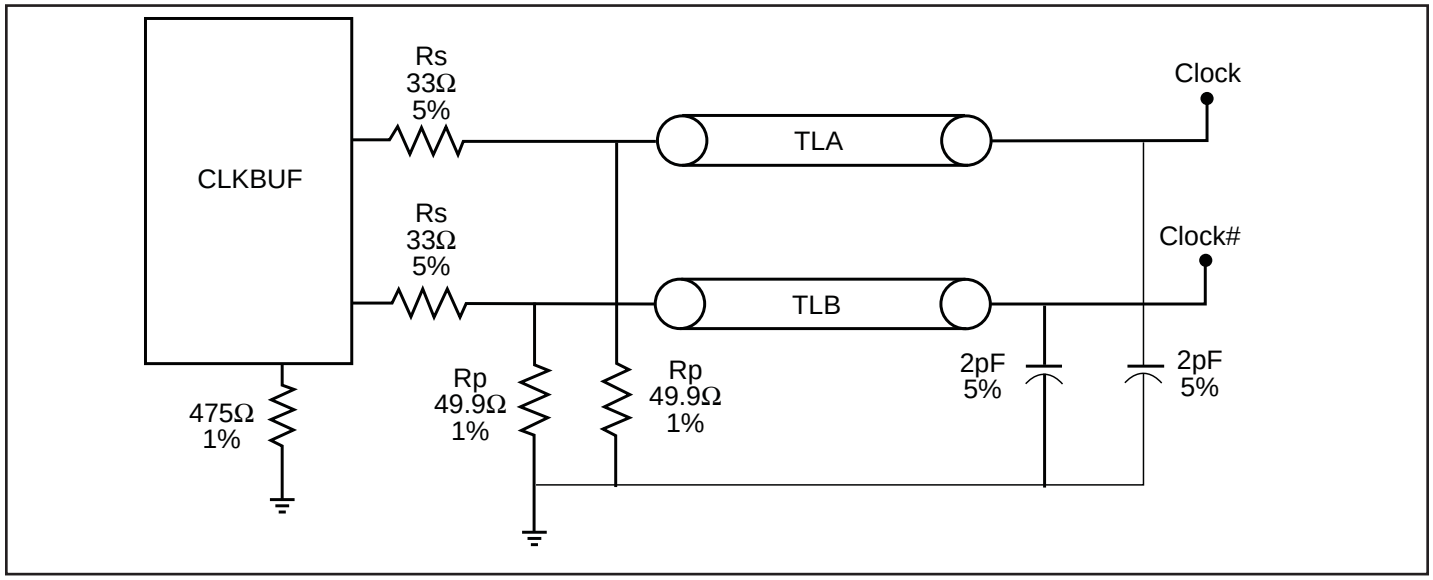
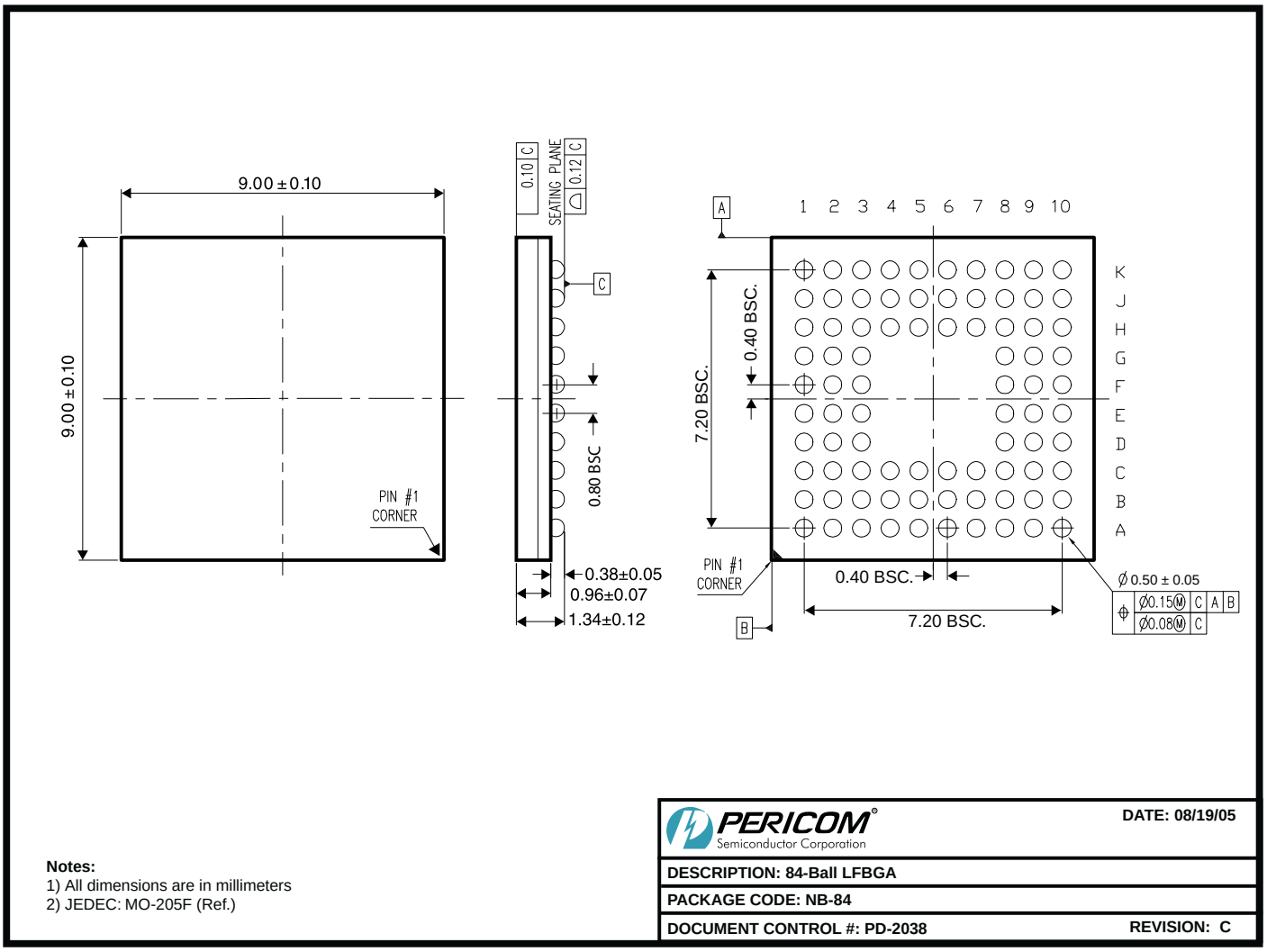


Figure 2. Configuration test load board termination

Note:
• TLA and TLB are 3” transmission lines.

Package Mechanical: 84-ball LFBGA (NB)



PERICOM Semiconductor Corporation

DATE: 08/19/05

DESCRIPTION: 84-Ball LFBGA

PACKAGE CODE: NB-84

DOCUMENT CONTROL #: PD-2038 REVISION: C

Notes:
1) All dimensions are in millimeters
2) JEDEC: MO-205F (Ref.)

05-5338

Ordering Information

Ordering Number	Package Code	Package Description
PI2EQX3202BNBE	NB	Pb-free & Green 84-Ball LFBGA

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- X suffix = Tape/Reel