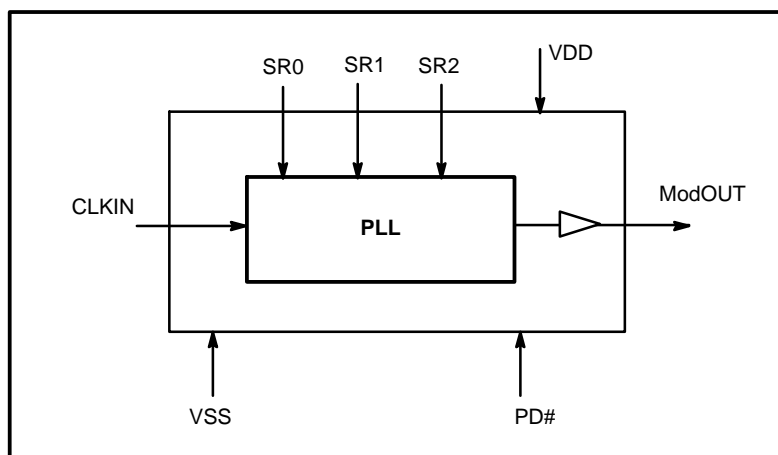# PCS3PS550A



**Figure 1. Block Diagram**

PCS3PS550A modulates the output of a single PLL in order to "spread" the bandwidth of a synthesized clock, and more importantly, decreases the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal's bandwidth is called 'spread spectrum clock generation'.

PCS3PS550A accepts an input from an external reference clock and locks to a 1x modulated clock output. SR0, SR1 and SR2 pins enable selecting one of the eight different frequency deviations (Refer *Frequency Deviation Selection table*). PCS3PS550A also features power down option for power save. PCS3PS550A operates over a supply voltage range of 2.3 V to 3.6 V. PCS3PS550A is available in an 8 Pin WDFN, (2 mm x 2 mm) Package.

**Table 1. PIN DESCRIPTION**

| Pin# | Pin Name | Type | Description |
|------|----------|------|-------------|
| 1 | CLKIN | I | External reference clock input. |
| 2 | SR2 | I | Digital logic input used to select Spreading Range. There is NO default state.<br>Refer Frequency Deviation Selection Table. |
| 3 | PD# | I | Power−down control pin. Powers down the entire chip. There is NO default state. Pull low to enable power−down mode. Connect to VDD to disable Power Down.<br>Output Clock will be LOW when power down is enabled |
| 4 | VSS | P | Ground connection. |
| 5 | ModOUT | O | Spread Spectrum Clock Output. |
| 6 | SR1 | I | Digital logic input used to select Spreading Range. This pin has an internal pull−up resistor.<br>*Refer Modulation Selection Table.* |
| 7 | SR0 | I | Digital logic input used to select Spreading Range. There is NO default state.<br>Refer Frequency Deviation Selection Table. |
| 8 | VDD | P | Power supply for the entire chip |

# PCS3PS550A

**Table 2. FREQUENCY DEVIATION SELECTION TABLE**

| SR2 | SR1 | SR0 | Spreading Range ( ± %) (@ 24 MHz) |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 2.5 |
| 0 | 1 | 0 | 1.25 |
| 0 | 1 | 1 | 1.5 |
| 1 | 0 | 0 | 0.4 |
| 1 | 0 | 1 | 0.75 |
| 1 | 1 | 0 | 1.75 |
| 1 | 1 | 1 | 2 |

**Table 3. OPERATING CONDITIONS**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage with respect to $V_{SS}$ | 2.3 | 3.6 | V |
| $T_A$ | Operating temperature | −20 | +85 | °C |
| $C_L$ | Load Capacitance | | 15 | pF |
| $C_{IN}$ | Input Capacitance | | 7 | pF |

**Table 4. ABSOLUTE MAXIMUM RATING**

| Symbol | Parameter | Rating | Unit |
|---|---|---|---|
| $V_{DD}$, $V_{IN}$ | Voltage on any input pin with respect to VSS | −0.5 to +4.6 | V |
| $T_{STG}$ | Storage temperature | −65 to +125 | °C |
| $T_A$ | Operating temperature | −40 to +85 | °C |
| $T_s$ | Max. Soldering Temperature (10 sec) | 260 | °C |
| $T_J$ | Junction Temperature | 150 | °C |
| $T_{DV}$ | Static Discharge Voltage (As per JEDEC STD22−A114−B) | 2 | kV |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**Table 5. DC ELECTRICAL CHARACTERISTICS**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage with respect to $V_{SS}$ | 2.3 | 2.8 | 3.6 | V |
| $V_{IH}$ | Input high voltage | 0.65 * $V_{DD}$ | | | V |
| $V_{IL}$ | Input low voltage | | | 0.3 * $V_{DD}$ | V |
| $I_{IH}$ | Input high current (SR1 control pin) | | | 50 | μA |
| $I_{IL}$ | Input low current (SR1 control pin) | | | 50 | μA |
| $V_{OH}$ | Output high voltage ($I_{OH}$ = −8 mA) | 0.75 * $V_{DD}$ | | | V |
| $V_{OL}$ | Output low voltage ($I_{OL}$ = 8 mA) | | | 0.2 * $V_{DD}$ | V |
| $I_{CC}$ | Static supply current (PD# pulled to $V_{SS}$) | | | 1 | μA |
| $I_{DD}$ | Dynamic supply current (Unloaded Output @ 24 MHz) | | 6 | 9 | mA |
| $Z_{OUT}$ | Output impedance | | 40 | | Ω |

**Table 6. AC ELECTRICAL CHARACTERISTICS**

| Symbol | Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| CLKIN | Input Clock frequency | | 18 | 24 | 40 | MHz |
| ModOUT | Output Clock frequency | | 18 | 24 | 40 | MHz |
| $t_{LH}$ (Note 1) | Output rise time (Measured between 20% to 80%) | Unloaded Output | | 0.8 | 1.2 | ns |
| | | CL = 15 pF | | 2.4 | 3 | |
| $t_{HL}$ (Note 1) | Output fall time (Measured between 80% to 20%) | Unloaded Output | | 0.6 | 1 | ns |
| | | CL = 15 pF | | 1.9 | 2.8 | |
| $t_{JC}$ (Note 1) | Jitter (cycle to cycle) Unloaded Output | | | ± 175 | ± 250 | ps |
| $t_D$ (Note 1) | Output duty cycle | | 45 | 50 | 55 | % |
| $t_{ON}$ (Note 1) | PLL lock Time (Stable power supply, valid clock presented on CLKIN pin, PD# toggled from Low to High) | | | | 3 | ms |
| $fd_{var}$ | Frequency Deviation Variation across PVT | | | ± 2.5 | ± 5 | % |

1. Parameter is guaranteed by design and characterization. Not 100% tested in production

# PCS3PS550A
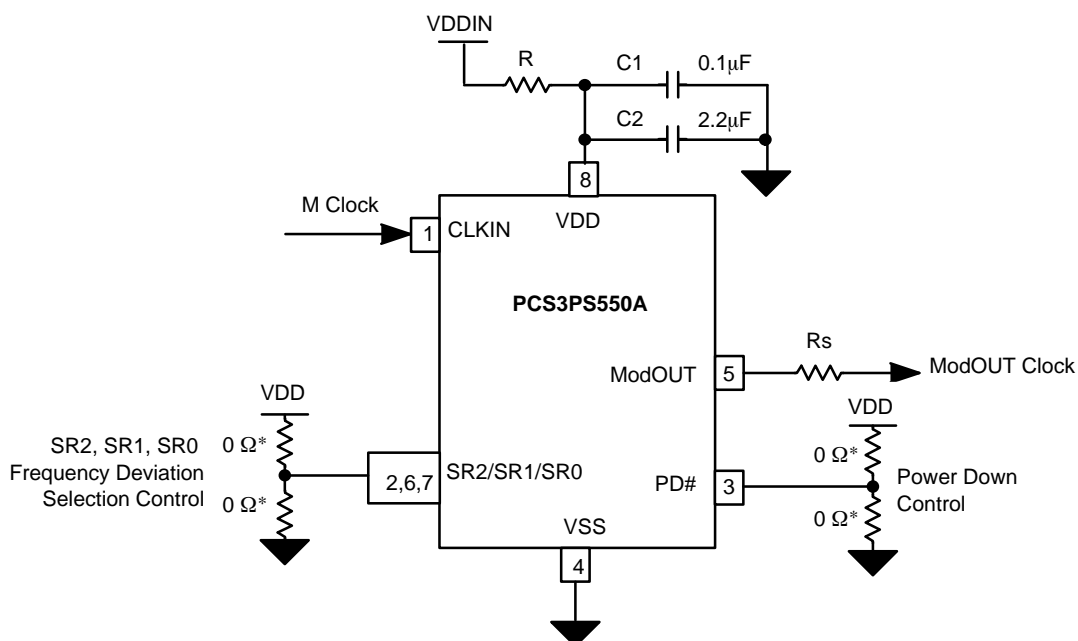


NOTE: Refer Pin Description table for Functionality details.

*Choose the 0 Ohms resistor either to VDD or to VSS based on the logic state to be set for the control signal

**Figure 2. Typical Application Schematic**

**PCB Layout Recommendation**

For optimum device performance, following guidelines are recommended.

- Dedicated $V_{DD}$ and $V_{SS}$ (GND) planes.
- The device must be isolated from system power supply noise. A 0.1μF and a 2.2 μF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between the decoupling capacitor and VDD pin. The PCB trace to VDD pin and the ground via should be kept as short as possible. All the VDD pins should have decoupling capacitors.
- In an optimum layout all components are on the same side of the board, minimizing vias through other signal layers.

A typical layout is shown in the figure
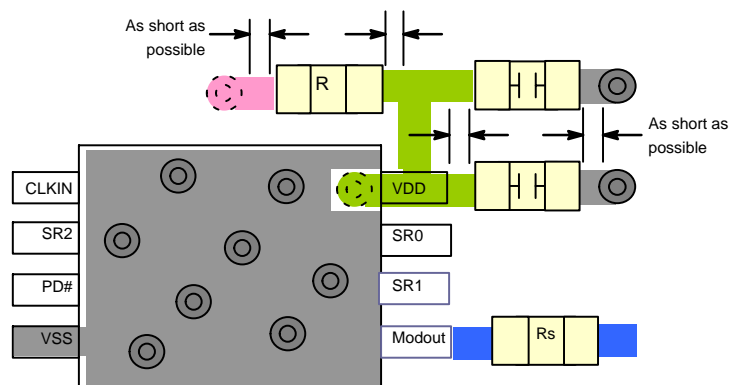


**Figure 3.**

**ORDERING INFORMATION**

| Part Number | Top Marking | Temperature | Package Type | Shipping† |
|---|---|---|---|---|
| PCS3PS550AG–08CR | CA | –20°C to +85°C | 8L– WDFN (TDFN) (Pb–Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*A "microdot" placed at the end of last row of marking or just below the last row toward the center of package indicates Pb–Free.

# PCS3PS550A

## PACKAGE DIMENSIONS

**WDFN8 2x2, 0.5P**
CASE 511AQ
ISSUE A
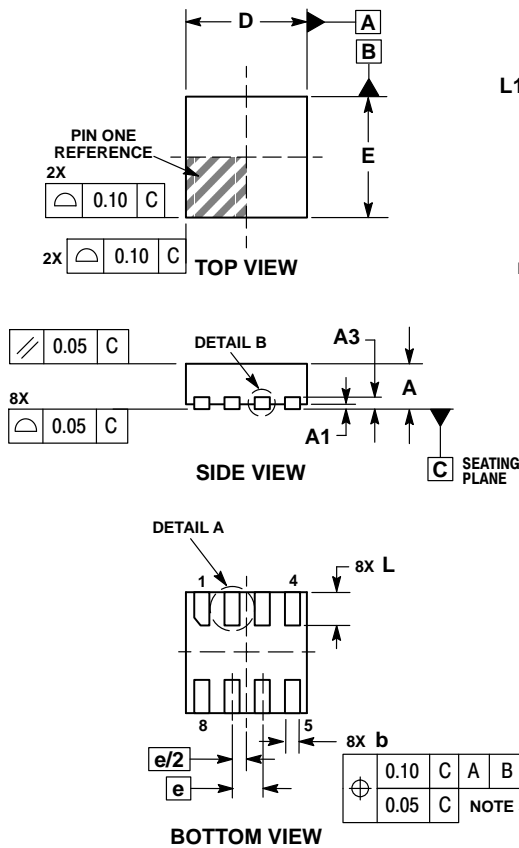
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL.

| DIM | MILLIMETERS | |
| | MIN | MAX |
| --- | --- | --- |
| A | 0.70 | 0.80 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.20 | 0.30 |
| D | 2.00 BSC | |
| E | 2.00 BSC | |
| e | 0.50 BSC | |
| L | 0.50 | 0.60 |
| L1 | --- | 0.15 |

**TOP VIEW**

PIN ONE REFERENCE
2X

2X

**DETAIL A**
OPTIONAL CONSTRUCTIONS

**SIDE VIEW**

DETAIL B

SEATING PLANE

EXPOSED Cu    MOLD CMPD

**DETAIL B**
OPTIONAL CONSTRUCTION

**BOTTOM VIEW**

DETAIL A

8X L

8X b

e/2

e

## RECOMMENDED SOLDERING FOOTPRINT*

PACKAGE OUTLINE

7X
0.78

2.30

0.88

8X
0.35

1

0.50
PITCH

DIMENSIONS: MILLIMETERS
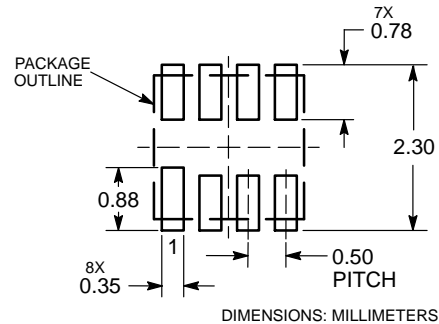
*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Timing–Safe is a trademark of Semiconductor Components Industries, LLC (SCILLC).

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