

P3MS650100H

Table 1. PIN DESCRIPTION

Pin #	Pin Name	Type	Description
1	VSS	Power	Ground connection.
2	CLKIN	Input	LVC MOS External reference clock input.
3	ModOUT	Output	Spread Spectrum Clock Output.
4	VDD	Power	Power supply for the entire chip

Table 2. OPERATING CONDITIONS

Symbol	Description	Min	Max	Unit
V _{DD} (1.8 V)	Supply Voltage with respect to V _{SS}	1.6	2.0	V
V _{DD} (2.5 V/3.3 V)		2.3	3.6	
T _A	Operating temperature	–20	+85	°C
C _L	Load Capacitance		15	pF
C _{IN}	Input Capacitance		5	pF

Table 3. ABSOLUTE MAXIMUM RATING

Symbol	Description	Rating	Unit
V _{DD} , V _{IN}	Voltage on any input pin with respect to V _{SS}	–0.5 to +4.6	V
T _{STG}	Storage temperature	–65 to +125	°C
T _s	Max. Soldering Temperature (10 sec)	260	°C
T _J	Junction Temperature	150	°C
T _{DV}	Static Discharge Voltage (As per JEDEC STD22– A114–B)	2	kV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

P3MS650100H

Table 4. DC Electrical Characteristics $V_{DD} = 1.6\text{ V} - 2.0\text{ V}$, $T_A = -20^\circ\text{C}$ to $+85^\circ\text{C}$

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply Voltage with respect to VSS	1.6	1.8	2.0	V
I_{DD}	Dynamic supply current (Unloaded Output)	15MHz	1.3	1.8	mA
		30MHz	2	2.8	
I_{CC}	Static supply current (No Clock @ CLKIN)			1	μA
V_{IH}	Input high voltage	$0.65 \cdot V_{DD}$			V
V_{IL}	Input low voltage			$0.3 \cdot V_{DD}$	V
I_{IH}	Input high current (CLKIN pin)			10	μA
I_{IL}	Input low current (CLKIN pin)			10	μA
V_{OH}	Output high voltage, $I_{OH} = -8\text{mA}$	$0.75 \cdot V_{DD}$			V
V_{OL}	Output low voltage, $I_{OL} = 8\text{mA}$			$0.2 \cdot V_{DD}$	V
Z_{OUT}	Output impedance		28		Ω

Table 5. AC ELECTRICAL CHARACTERISTICS $V_{DD} = 1.6\text{ V} - 2.0\text{ V}$, $T_A = -20^\circ\text{C}$ to $+85^\circ\text{C}$

Symbol	Parameter	Min	Typ	Max	Unit
CLKIN	Input Clock frequency	15		30	MHz
ModOUT	Output Clock frequency	15		30	MHz
t_{LH} (Notes 1 and 2)	Output rise time (Measured between 20% to 80%)		1.7	2.7	nS
t_{HL} (Notes 1 and 2)	Output fall time (Measured between 80% to 20%)		1.4	2.4	nS
t_{JC} (Notes 2)	Cycle-to-cycle Jitter, Peak (1000 cycles)	15 MHz	400		pS
		24 MHz	250		
		30 MHz			
t_D (Notes 1 and 2)	Output duty cycle (Measured @ 50%)	45	50	55	%
t_{ON} (Notes 1 and 2)	PLL lock Time (Stable power supply, valid clock presented on CLKIN)			3	mS
fd	Frequency Deviation @ 24 MHz		± 1.4	± 1.55	%

1. All parameters are specified with 15 pF loaded output.
2. Parameter is guaranteed by design and characterization. Not 100% tested in production

P3MS650100H

Table 6. DC ELECTRICAL CHARACTERISTICS $V_{DD} = 2.3\text{ V} - 3.6\text{ V}$, $T_A = -20^\circ\text{C}$ to $+85^\circ\text{C}$

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply Voltage with respect to VSS	2.3	2.8	3.6	V
I_{DD}	Dynamic supply current (Unloaded Output)	15MHz	1.7	3	mA
		30MHz	2.8	5	
		60MHz	5	9	
I_{CC}	Static supply current (No Clock @ CLKIN)			2	μA
V_{IH}	Input high voltage	$0.65 * V_{DD}$			V
V_{IL}	Input low voltage			$0.3 * V_{DD}$	V
I_{IH}	Input high current (CLKIN pin)			10	μA
I_{IL}	Input low current (CLKIN pin)			10	μA
V_{OH}	Output high voltage, $I_{OH} = -16\text{ mA}$	$0.75 * V_{DD}$			V
V_{OL}	Output low voltage, $I_{OL} = 16\text{ mA}$			$0.2 * V_{DD}$	V
Z_{OUT}	Output impedance		20		Ω

Table 7. AC ELECTRICAL CHARACTERISTICS $V_{DD} = 2.3\text{ V} - 3.6\text{ V}$, $T_A = -20^\circ\text{C}$ to $+85^\circ\text{C}$

Symbol	Parameter	Min	Typ	Max	Unit
CLKIN	Input Clock frequency	15		60	MHz
ModOUT	Output Clock frequency	15		60	MHz
t_{LH} (Notes 3 and 4)	Output rise time (Measured between 20% to 80%)		0.8	1.6	nS
t_{HL} (Notes 3 and 4)	Output fall time (Measured between 80% to 20%)		0.8	1.6	nS
t_{JC} (Notes 4)	Cycle-to-cycle Jitter, Peak (1000 cycles)	15 MHz	350		pS
		24 MHz	250		
		60 MHz	100		
t_D (Notes 3 and 4)	Output duty cycle	45	50	55	%
t_{ON} (Notes 3 and 4)	PLL lock Time (Stable power supply, valid clock presented on CLKIN)			3	mS
fd	Frequency Deviation @ 24 MHz		± 1.4	± 1.55	%

3. All parameters are specified with 15 pF loaded output.

4. Parameter is guaranteed by design and characterization. Not 100% tested in production

P3MS650100H

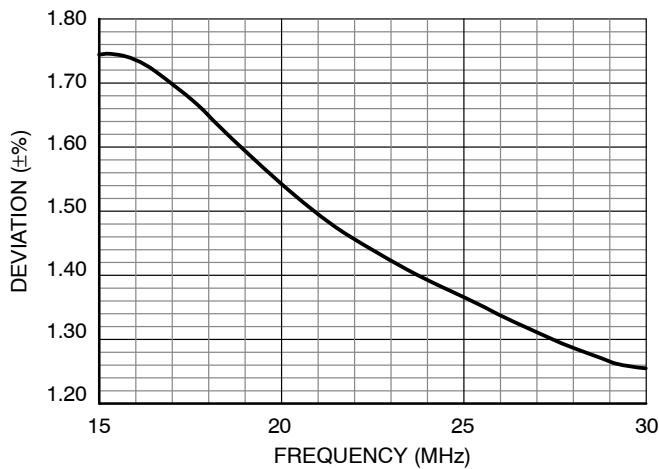


Figure 2. Deviation vs. Frequency
(V_{DD} = 1.6 V - 2.0 V)

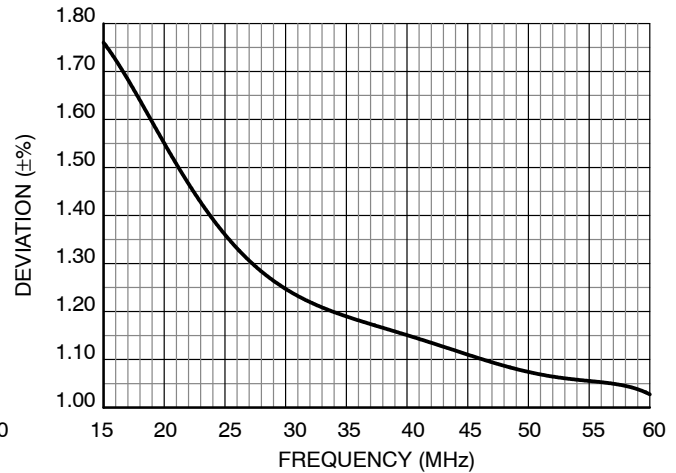
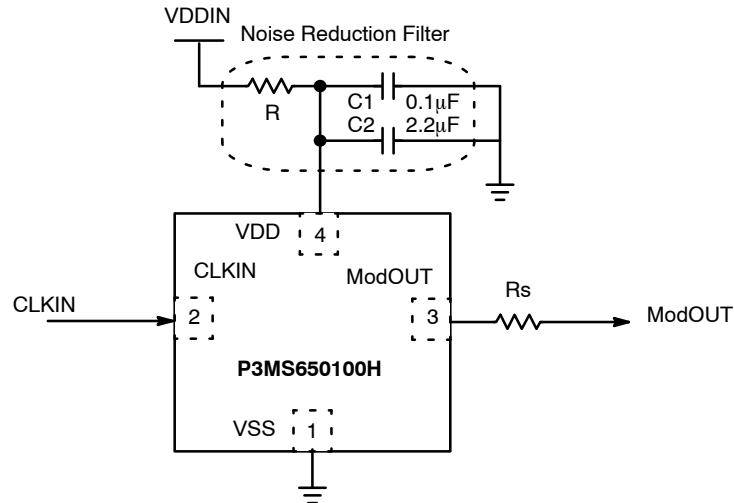


Figure 3. Deviation vs. Frequency
(V_{DD} = 2.3 V - 3.6 V)



Rs = Trace Impedance of PCB – Output Impedance of Device (Z₀)
Note: Refer Pin Description table for Functionality details

Figure 4. Typical Application Schematic

PCB Layout Recommendation

For optimum device performance, following guidelines are recommended.

- ◆ Dedicated V_{DD} and GND planes.
- ◆ The device must be isolated from system power supply noise. A 0.1µF and a 2.2 µF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between the decoupling capacitor and VDD pin. The PCB trace to VDD pin and the ground via should be kept as short as possible. All the VDD pins should have decoupling capacitors.
- ◆ In an optimum layout all components are on the same side of the board, minimizing vias through other signal layers.

P3MS650100H

A typical layout is shown in the figure below.

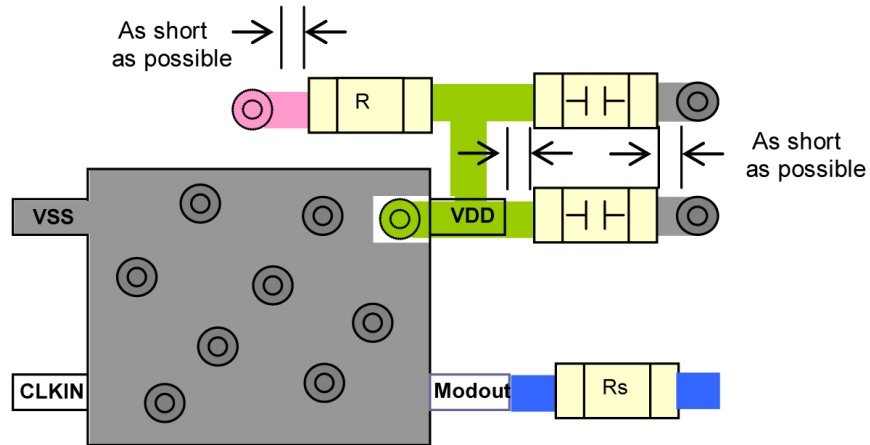


Figure 5. Recommended PCB Layout

ORDERING INFORMATION

Ordering Code	Marking	Temperature	Package Type	Shipping [†]
P3MS650100H-4CR	A	-20°C to +85°C	4-pin (1.2 mm x 1.0 mm) WDFN (Pb-Free)	3000 / Tape & Reel

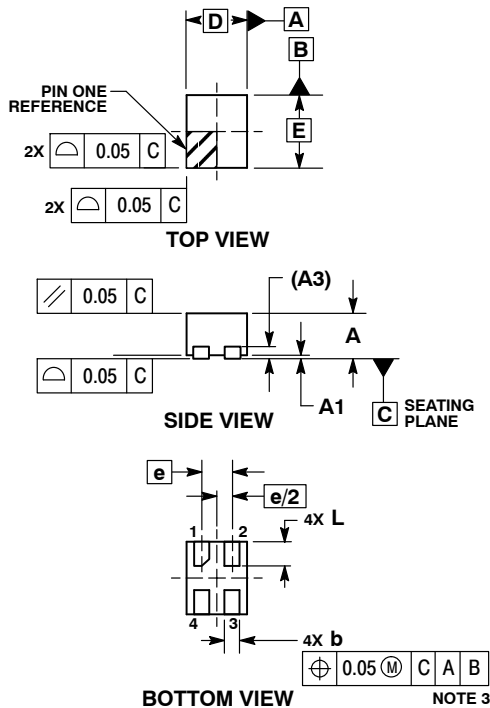
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*A "microdot" placed at the end of last row of marking or just below the last row toward the center of package indicates Pb-Free.

P3MS650100H

PACKAGE DIMENSIONS

WDFN4, 1.0x1.2, 0.5P
CASE 511BS-01
ISSUE O

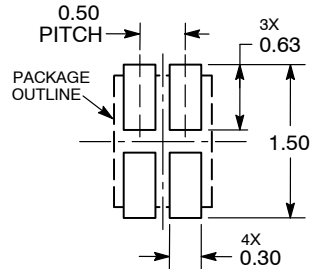


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 mm FROM THE TERMINAL TIPS.
4. PACKAGE DIMENSIONS EXCLUSIVE OF BURRS AND MOLD FLASH.

MILLIMETERS		
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	1.00 BSC	
E	1.20 BSC	
e	0.50 BSC	
L	0.35	0.45

RECOMMENDED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative

P3MS650100H/D