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# 1 Ordering parts

## 1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to [nxp.com](http://nxp.com) and perform a part number search for the following device numbers: KE06Z.

# 2 Part identification

## 2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

## 2.2 Format

Part numbers for this device have the following format:

Q KE## A FFF R T PP CC N

## 2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	<ul style="list-style-type: none"> <li>M = Fully qualified, general market flow</li> <li>P = Prequalification</li> </ul>
KE##	Kinetis family	<ul style="list-style-type: none"> <li>KE04</li> </ul>
A	Key attribute	<ul style="list-style-type: none"> <li>Z = M0+ core</li> </ul>
FFF	Program flash memory size	<ul style="list-style-type: none"> <li>128 = 128 KB</li> </ul>
R	Silicon revision	<ul style="list-style-type: none"> <li>(Blank) = Main</li> <li>A = Revision after main</li> </ul>
T	Temperature range (°C)	<ul style="list-style-type: none"> <li>V = -40 to 105</li> </ul>
PP	Package identifier	<ul style="list-style-type: none"> <li>LD = 44 LQFP (10 mm x 10 mm)</li> </ul>

*Table continues on the next page...*

Field	Description	Values
		<ul style="list-style-type: none"> <li>• QH = 64 QFP (14 mm x 14 mm)</li> <li>• LH = 64 LQFP (10 mm x 10 mm)</li> <li>• LK = 80 LQFP (14 mm x 14 mm)</li> </ul>
CC	Maximum CPU frequency (MHz)	<ul style="list-style-type: none"> <li>• 4 = 48 MHz</li> </ul>
N	Packaging type	<ul style="list-style-type: none"> <li>• R = Tape and reel</li> <li>• (Blank) = Trays</li> </ul>

## 2.4 Example

This is an example part number:

MKE06Z128VLK4

## 3 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

**Table 1. Parameter classifications**

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

### NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

## 4 Ratings

### 4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T <sub>STG</sub>	Storage temperature	–55	150	°C	1
T <sub>SDR</sub>	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

### 4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

### 4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V <sub>HBM</sub>	Electrostatic discharge voltage, human body model	–6000	+6000	V	1
V <sub>CDM</sub>	Electrostatic discharge voltage, charged-device model	–500	+500	V	2
I <sub>LAT</sub>	Latch-up current at ambient temperature of 125°C	–100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78D, *IC Latch-up Test*.
  - Test was performed at 125 °C case temperature (Class II).
  - I/O pins pass ±100 mA I-test with I<sub>DD</sub> current limit at 400 mA.
  - I/O pins pass +50/-100 mA I-test with I<sub>DD</sub> current limit at 1000 mA.
  - Supply groups pass 1.5 V<sub>ccmax</sub>.
  - RESET pin was only tested with negative I-test due to product conditioning requirement.

## 4.4 Voltage and current operating ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in the following table may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this document.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either  $V_{SS}$  or  $V_{DD}$ ) or the programmable pullup resistor associated with the pin is enabled.

**Table 2. Voltage and current operating ratings**

Symbol	Description	Min.	Max.	Unit
$V_{DD}$	Digital supply voltage	-0.3	6.0	V
$I_{DD}$	Maximum current into $V_{DD}$	—	120	mA
$V_{IN}$	Input voltage except true open drain pins	-0.3	$V_{DD} + 0.3$ <sup>1</sup>	V
	Input voltage of true open drain pins	-0.3	6	V
$I_D$	Instantaneous maximum current single pin limit (applies to all port pins)	-25	25	mA
$V_{DDA}$	Analog supply voltage	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V

1. Maximum rating of  $V_{DD}$  also applies to  $V_{IN}$ .

## 5 General

### 5.1 Nonswitching electrical specifications

#### 5.1.1 DC characteristics

This section includes information about power supply requirements and I/O pin characteristics.

**Table 3. DC characteristics**

Symbol	C	Descriptions		Min	Typical <sup>1</sup>	Max	Unit
—	—	Operating voltage <sup>2</sup>	—	2.7	—	5.5	V

*Table continues on the next page...*

**Table 3. DC characteristics (continued)**

Symbol	C	Descriptions			Min	Typical <sup>1</sup>	Max	Unit
$V_{OH}$	P	Output high voltage	All I/O pins, except PTA2 and PTA3, standard-drive strength	5 V, $I_{load} = -5$ mA	$V_{DD} - 0.8$	—	—	V
	C			3 V, $I_{load} = -2.5$ mA	$V_{DD} - 0.8$	—	—	V
	P		High current drive pins, high-drive strength <sup>3</sup>	5 V, $I_{load} = -20$ mA	$V_{DD} - 0.8$	—	—	V
	C			3 V, $I_{load} = -10$ mA	$V_{DD} - 0.8$	—	—	V
$I_{OHT}$	D	Output high current	Max total $I_{OH}$ for all ports	5 V	—	—	-100	mA
				3 V	—	—	-60	
$V_{OL}$	P	Output low voltage	All I/O pins, standard-drive strength	5 V, $I_{load} = 5$ mA	—	—	0.8	V
	C			3 V, $I_{load} = 2.5$ mA	—	—	0.8	V
	P		High current drive pins, high-drive strength <sup>3</sup>	5 V, $I_{load} = 20$ mA	—	—	0.8	V
	C			3 V, $I_{load} = 10$ mA	—	—	0.8	V
$I_{OLT}$	D	Output low current	Max total $I_{OL}$ for all ports	5 V	—	—	100	mA
				3 V	—	—	60	
$V_{IH}$	P	Input high voltage	All digital inputs	$4.5 \leq V_{DD} < 5.5$ V	$0.65 \times V_{DD}$	—	—	V
				$2.7 \leq V_{DD} < 4.5$ V	$0.70 \times V_{DD}$	—	—	
$V_{IL}$	P	Input low voltage	All digital inputs	$4.5 \leq V_{DD} < 5.5$ V	—	—	$0.35 \times V_{DD}$	V
				$2.7 \leq V_{DD} < 4.5$ V	—	—	$0.30 \times V_{DD}$	
$V_{hys}$	C	Input hysteresis	All digital inputs	—	$0.06 \times V_{DD}$	—	—	mV
$ I_{In} $	P	Input leakage current	Per pin (pins in high impedance input mode)	$V_{IN} = V_{DD}$ or $V_{SS}$	—	0.1	1	$\mu$ A
$ I_{INTOT} $	C	Total leakage combined for all port pins	Pins in high impedance input mode	$V_{IN} = V_{DD}$ or $V_{SS}$	—	—	2	$\mu$ A
$R_{PU}$	P	Pullup resistors	All digital inputs, when enabled (all I/O pins other than PTA2 and PTA3)	—	30.0	—	50.0	k $\Omega$
$R_{PU}^4$	P	Pullup resistors	PTA2 and PTA3 pins	—	30.0	—	60.0	k $\Omega$
$I_{IC}$	D	DC injection current <sup>5, 6, 7</sup>	Single pin limit	$V_{IN} < V_{SS}$ , $V_{IN} > V_{DD}$	-2	—	2	mA
			Total MCU limit, includes sum of all stressed pins		-5	—	25	
$C_{in}$	C	Input capacitance, all pins		—	—	—	7	pF
$V_{RAM}$	C	RAM retention voltage		—	2.0	—	—	V

1. Typical values are measured at 25 °C. Characterized, not tested.

2. Maximum power supply VDD ramp-up rate is 70V/ms, characterized on samples of different lots.

- Only PTB4, PTB5, PTD0, PTD1, PTE0, PTE1, PTH0 (64-pin and 80-pin packages only), and PTH1 (64-pin and 80-pin packages only) support high current output.
- The specified resistor value is the actual value internal to the device. The pullup value may appear higher when measured externally on the pin.
- All functional non-supply pins, except for PTA2 and PTA3, are internally clamped to  $V_{SS}$  and  $V_{DD}$ . PTA2 and PTA3 are true open drain I/O pins that are internally clamped to  $V_{SS}$ .
- Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger value.
- Power supply must maintain regulation within operating  $V_{DD}$  range during instantaneous and operating maximum current conditions. If the positive injection current ( $V_{in} > V_{DD}$ ) is higher than  $I_{DD}$ , the injection current may flow out of  $V_{DD}$  and could result in external power supply going out of regulation. Ensure that external  $V_{DD}$  load will shunt current higher than maximum injection current when the MCU is not consuming power, such as when no system clock is present, or clock rate is very low (which would reduce overall power consumption).

**Table 4. LVD and POR specification**

Symbol	C	Description		Min	Typ	Max	Unit
V <sub>POR</sub>	D	POR re-arm voltage <sup>1</sup>		1.5	1.75	2.0	V
V <sub>LVDH</sub>	C	Falling low-voltage detect threshold—high range (LVDV = 1) <sup>2</sup>		4.2	4.3	4.4	V
V <sub>LVW1H</sub>	C	Falling low-voltage warning threshold—high range	Level 1 falling (LVWV = 00)	4.3	4.4	4.5	V
V <sub>LVW2H</sub>	C		Level 2 falling (LVWV = 01)	4.5	4.5	4.6	V
V <sub>LVW3H</sub>	C		Level 3 falling (LVWV = 10)	4.6	4.6	4.7	V
V <sub>LVW4H</sub>	C		Level 4 falling (LVWV = 11)	4.7	4.7	4.8	V
V <sub>HYSH</sub>	C	High range low-voltage detect/warning hysteresis		—	100	—	mV
V <sub>LVDL</sub>	C	Falling low-voltage detect threshold—low range (LVDV = 0)		2.56	2.61	2.66	V
V <sub>LVW1L</sub>	C	Falling low-voltage warning threshold—low range	Level 1 falling (LVWV = 00)	2.62	2.7	2.78	V
V <sub>LVW2L</sub>	C		Level 2 falling (LVWV = 01)	2.72	2.8	2.88	V
V <sub>LVW3L</sub>	C		Level 3 falling (LVWV = 10)	2.82	2.9	2.98	V
V <sub>LVW4L</sub>	C		Level 4 falling (LVWV = 11)	2.92	3.0	3.08	V
V <sub>HYSDL</sub>	C	Low range low-voltage detect hysteresis		—	40	—	mV
V <sub>HYSWL</sub>	C	Low range low-voltage warning hysteresis		—	80	—	mV
V <sub>BG</sub>	P	Buffered bandgap output <sup>3</sup>		1.14	1.16	1.18	V

- Maximum is highest voltage that POR is guaranteed.
- Rising thresholds are falling threshold + hysteresis.
- voltage Factory trimmed at  $V_{DD} = 5.0$  V, Temp = 25 °C



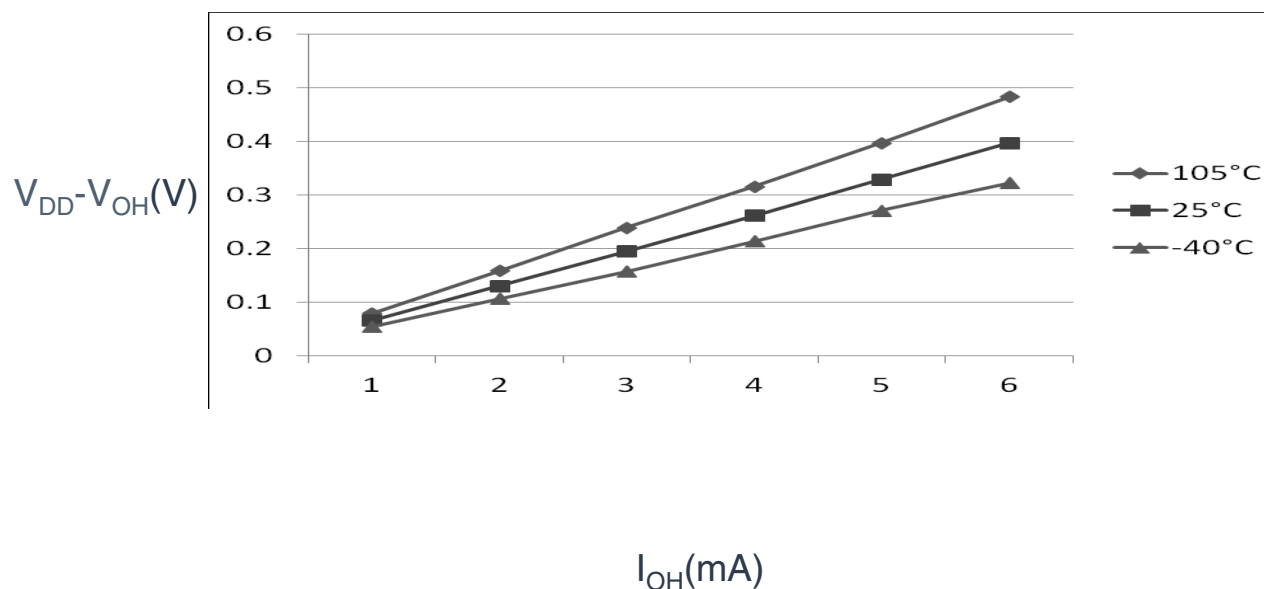


Figure 1. Typical  $V_{DD}-V_{OH}$  Vs.  $I_{OH}$  (standard drive strength) ( $V_{DD} = 5$  V)

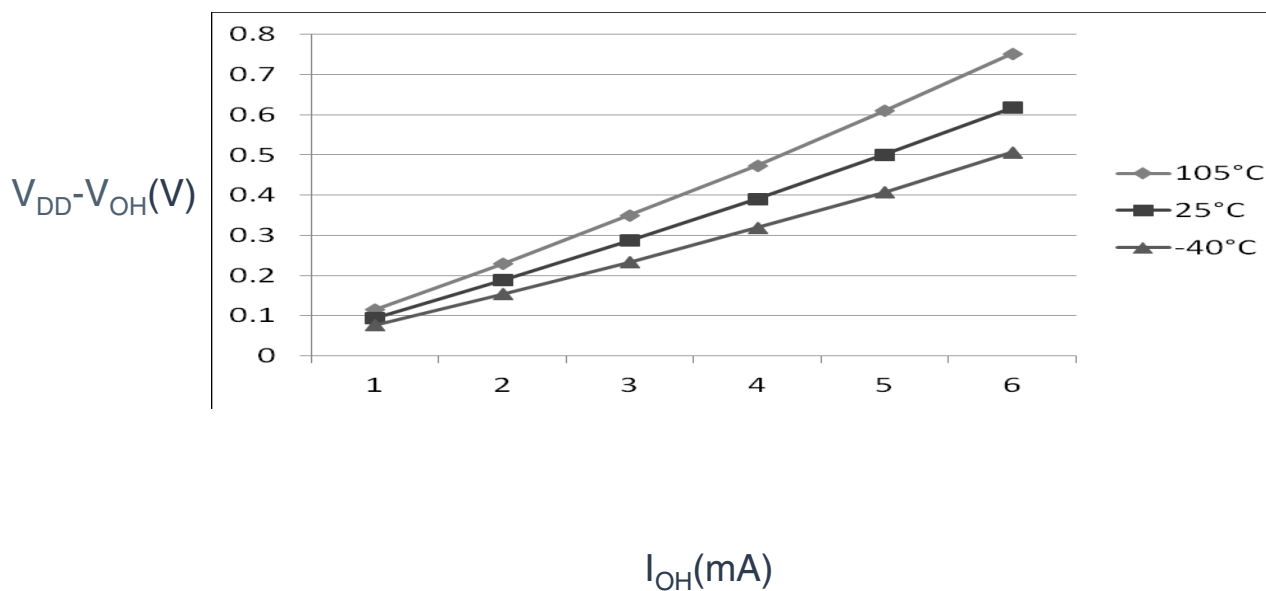


Figure 2. Typical  $V_{DD}-V_{OH}$  Vs.  $I_{OH}$  (standard drive strength) ( $V_{DD} = 3$  V)

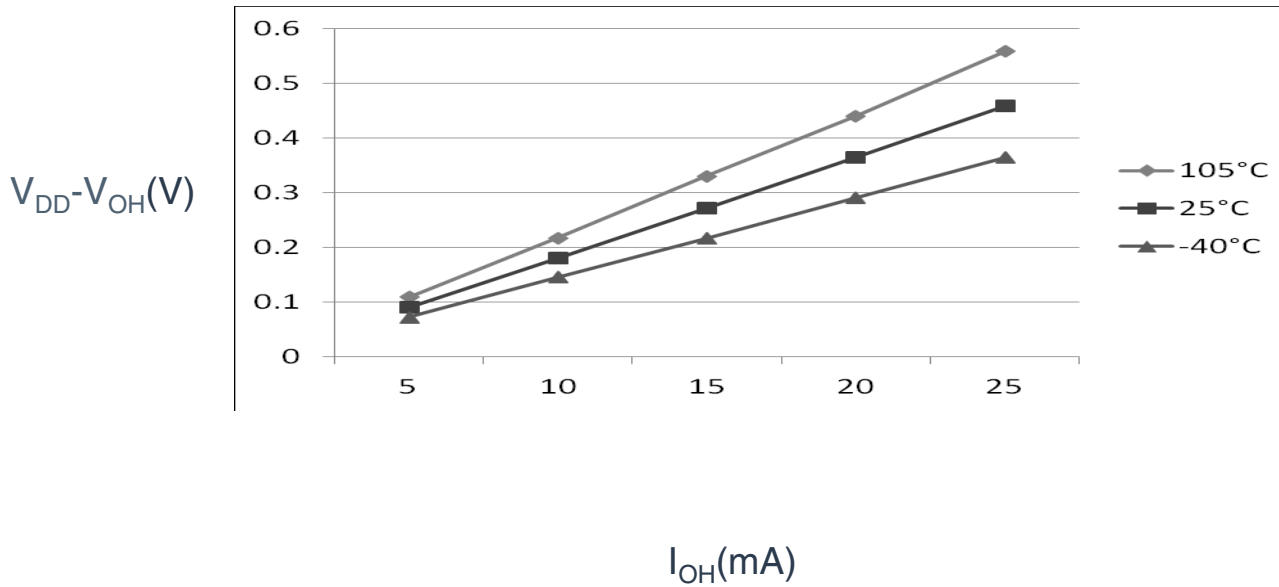


Figure 3. Typical  $V_{DD}-V_{OH}$  Vs.  $I_{OH}$  (high drive strength) ( $V_{DD} = 5$  V)

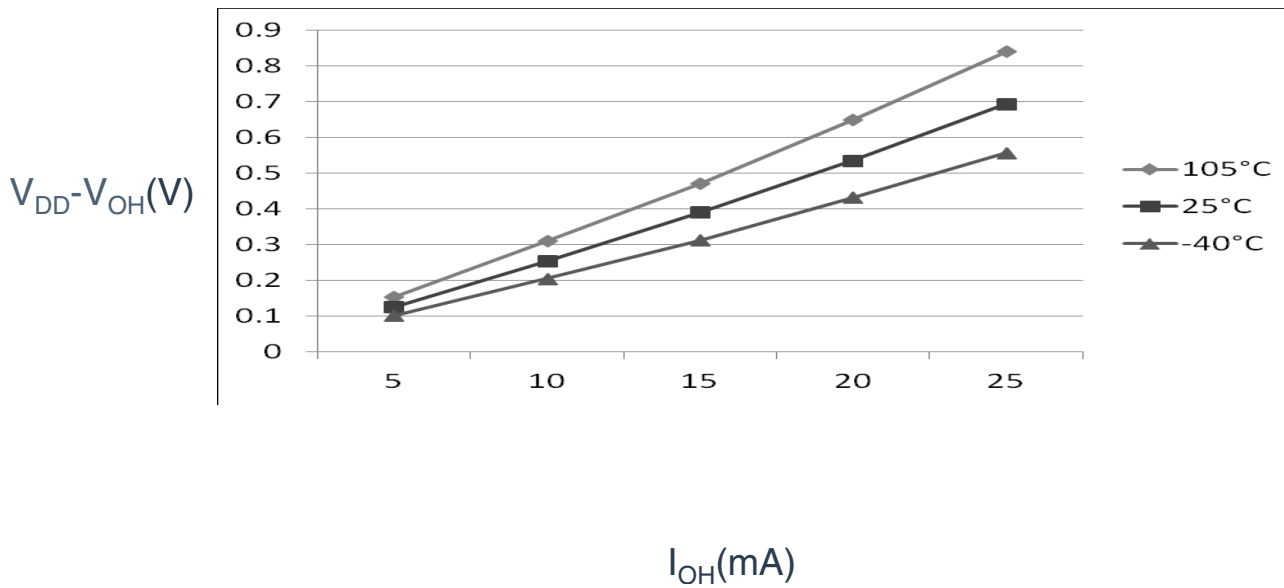


Figure 4. Typical  $V_{DD}-V_{OH}$  Vs.  $I_{OH}$  (high drive strength) ( $V_{DD} = 3$  V)

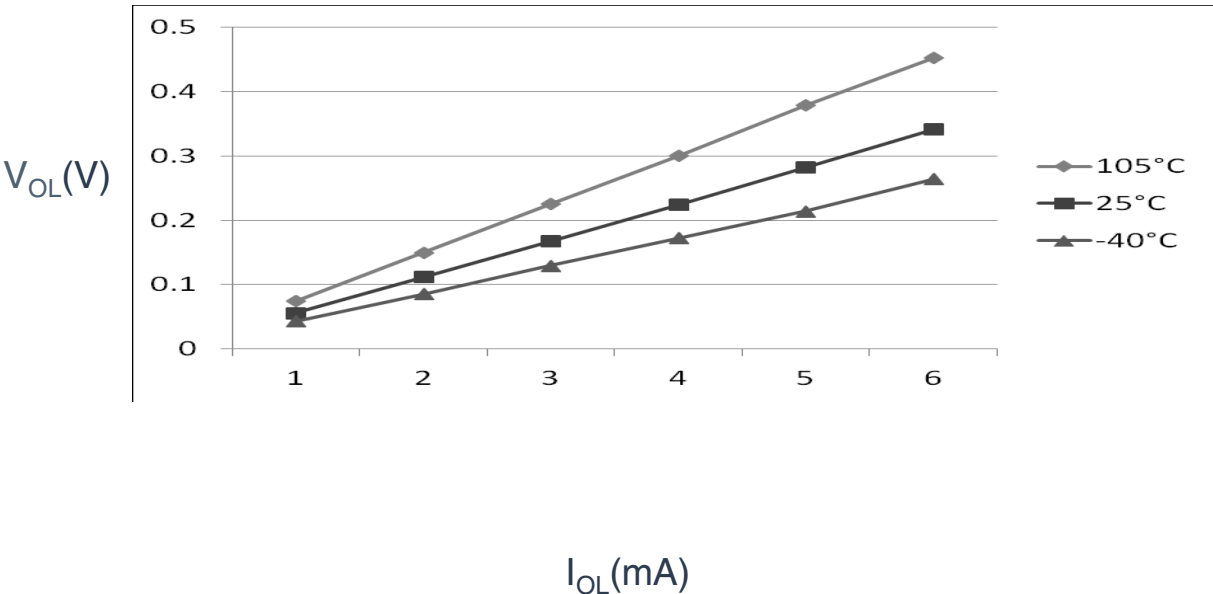


Figure 5. Typical  $V_{OL}$  Vs.  $I_{OL}$  (standard drive strength) ( $V_{DD} = 5\text{ V}$ )

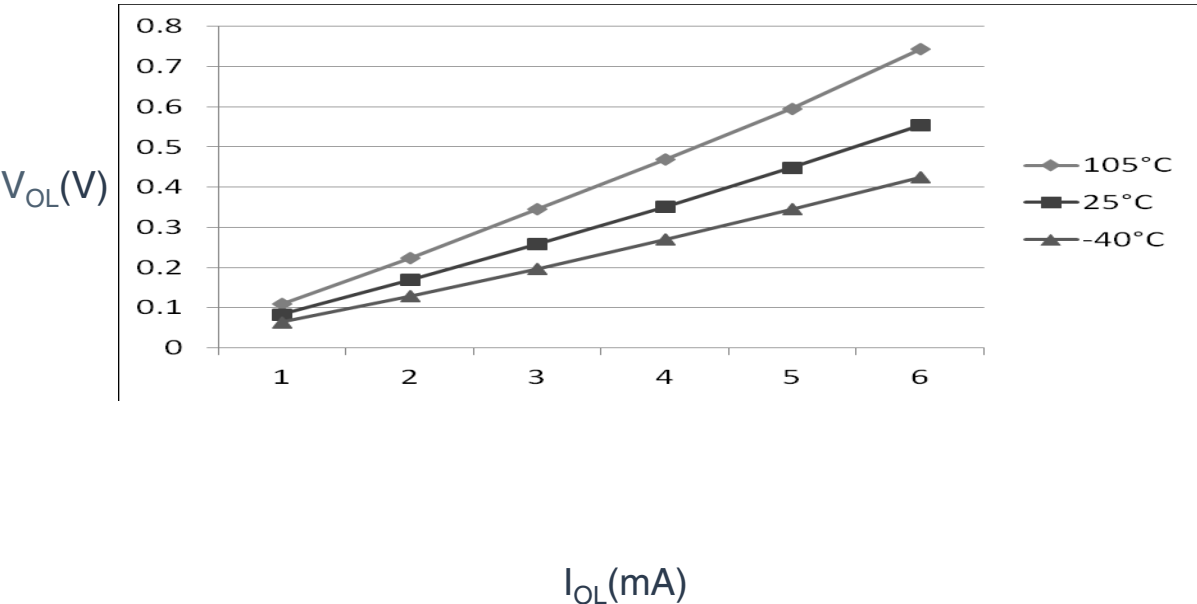


Figure 6. Typical  $V_{OL}$  Vs.  $I_{OL}$  (standard drive strength) ( $V_{DD} = 3\text{ V}$ )

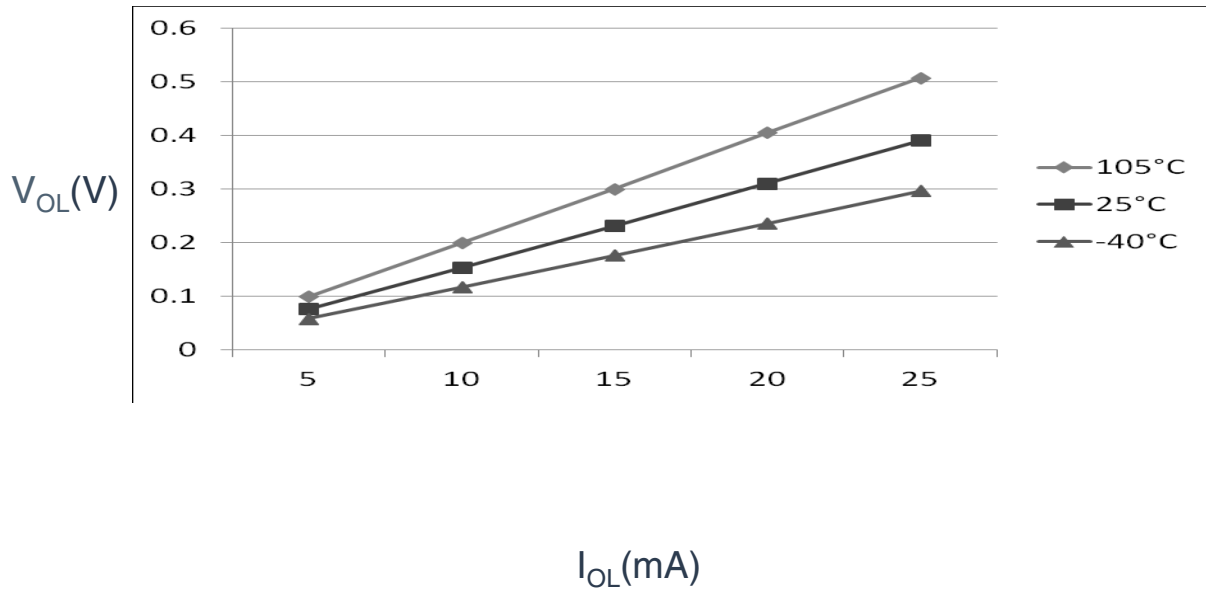


Figure 7. Typical  $V_{OL}$  Vs.  $I_{OL}$  (high drive strength) ( $V_{DD} = 5\text{ V}$ )

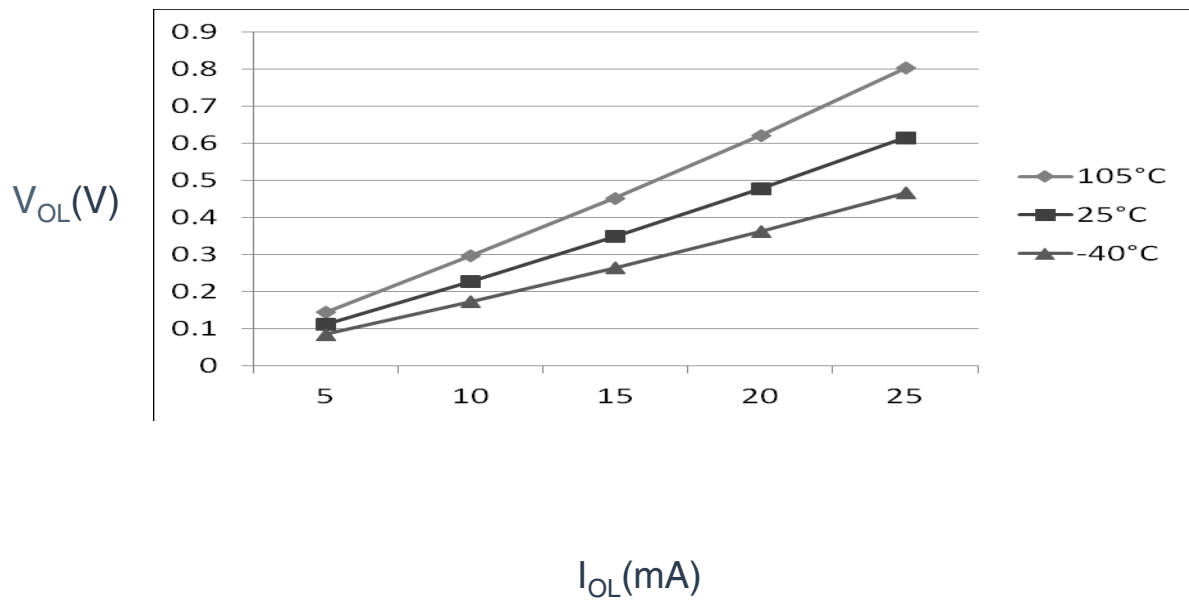


Figure 8. Typical  $V_{OL}$  Vs.  $I_{OL}$  (high drive strength) ( $V_{DD} = 3\text{ V}$ )

## 5.1.2 Supply current characteristics

This section includes information about power supply current in various operating modes.

**Table 5. Supply current characteristics**

C	Parameter	Symbol	Core/Bus Freq	V <sub>DD</sub> (V)	Typical <sup>1</sup>	Max <sup>2</sup>	Unit	Temp
C	Run supply current FEI mode, all modules clocks enabled; run from flash	R <sub>I</sub> DD	48/24 MHz	5	11.1	—	mA	-40 to 105 °C
C			24/24 MHz		8	—		
C			12/12 MHz		5	—		
C			1/1 MHz		2.4	—		
C			48/24 MHz	3	11	—		
C			24/24 MHz		7.9	—		
C			12/12 MHz		4.9	—		
C			1/1 MHz		2.3	—		
C	Run supply current FEI mode, all modules clocks disabled and gated; run from flash	R <sub>I</sub> DD	48/24 MHz	5	7.8	—	mA	-40 to 105 °C
C			24/24 MHz		5.5	—		
C			12/12 MHz		3.8	—		
C			1/1 MHz		2.3	—		
C			48/24 MHz	3	7.7	—		
C			24/24 MHz		5.4	—		
C			12/12 MHz		3.7	—		
C			1/1 MHz		2.2	—		
C	Run supply current FBE mode, all modules clocks enabled; run from RAM	R <sub>I</sub> DD	48/24 MHz	5	14.7	—	mA	-40 to 105 °C
P			24/24 MHz		9.8	14.9		
C			12/12 MHz		6	—		
C			1/1 MHz		2.4	—		
C			48/24 MHz	3	14.6	—		
P			24/24 MHz		9.6	12.8		
C			12/12 MHz		5.9	—		
C			1/1 MHz		2.3	—		
C	Run supply current FBE mode, all modules clocks disabled and gated; run from RAM	R <sub>I</sub> DD	48/24 MHz	5	11.4	—	mA	-40 to 105 °C
P			24/24 MHz		7.7	12.5		
C			12/12 MHz		4.7	—		
C			1/1 MHz		2.3	—		
C			48/24 MHz	3	11.3	—		
P			24/24 MHz		7.6	9.5		
C			12/12 MHz		4.6	—		
C			1/1 MHz		2.2	—		

Table continues on the next page...

**Table 5. Supply current characteristics (continued)**

C	Parameter	Symbol	Core/Bus Freq	V <sub>DD</sub> (V)	Typical <sup>1</sup>	Max <sup>2</sup>	Unit	Temp
C	Wait mode current FEI mode, all modules clocks enabled	W <sub>I</sub> DD	48/24 MHz	5	8.4	—	mA	-40 to 105 °C
P			24/24 MHz		6.5	7.2		
C			12/12 MHz		4.3	—		
C			1/1 MHz		2.4	—		
C			48/24 MHz	3	8.3	—		
P			24/24 MHz		6.4	7		
C			12/12 MHz		4.2	—		
C			1/1 MHz		2.3	—		
P	Stop mode supply current no clocks active (except 1 kHz LPO clock) <sup>3</sup>	S <sub>I</sub> DD	—	5	2	105	μA	-40 to 105 °C
P			—	3	1.9	95		-40 to 105 °C
C	ADC adder to Stop ADLPC = 1 ADLSMP = 1 ADCO = 1 MODE = 10B ADICLK = 11B	—	—	5	86	—	μA	-40 to 105 °C
C				3	82	—		
C	ACMP adder to Stop	—	—	5	12	—	μA	-40 to 105 °C
C				3	12	—		
C	LVD adder to Stop <sup>4</sup>	—	—	5	130	—	μA	-40 to 105 °C
C				3	125	—		

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. The Max current is observed at high temperature of 105 °C.
3. RTC adder cause <1 μA I<sub>DD</sub> increase typically, RTC clock source is 1 kHz LPO clock.
4. LVD is periodically woken up from Stop by 5% duty cycle. The period is equal to or less than 2 ms.

### 5.1.3 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation play a significant role in EMC performance. The system designer must consult the following applications notes, available on [nxp.com](http://nxp.com) for advice and guidance specifically targeted at optimizing EMC performance.

- AN2321: Designing for Board Level Electromagnetic Compatibility
- AN1050: Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers
- AN1263: Designing for Electromagnetic Compatibility with Single-Chip Microcontrollers

## Switching specifications

- AN2764: Improving the Transient Immunity Performance of Microcontroller-Based Applications
- AN1259: System Design and Layout Techniques for Noise Reduction in MCU-Based Systems

### 5.1.3.1 EMC radiated emissions operating behaviors

**Table 6. EMC radiated emissions operating behaviors for 80-pin LQFP package**

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V <sub>RE1</sub>	Radiated emissions voltage, band 1	0.15–50	6	dBμV	1, 2
V <sub>RE2</sub>	Radiated emissions voltage, band 2	50–150	6	dBμV	
V <sub>RE3</sub>	Radiated emissions voltage, band 3	150–500	11	dBμV	
V <sub>RE4</sub>	Radiated emissions voltage, band 4	500–1000	5	dBμV	
V <sub>RE_IEC</sub>	IEC level	0.15–1000	N <sup>3</sup>	—	2, 4

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
2. V<sub>DD</sub> = 5.0 V, T<sub>A</sub> = 25 °C, f<sub>OSC</sub> = 8 MHz (crystal), f<sub>SYS</sub> = 40 MHz, f<sub>BUS</sub> = 20 MHz
3. IEC/SAE Level Maximums: N≤12 dBμV, M≤18 dBμV, K≤30 dBμV, L≤36 dBμV, H≤42 dBμV.
4. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

## 5.2 Switching specifications

### 5.2.1 Control timing

**Table 7. Control timing**

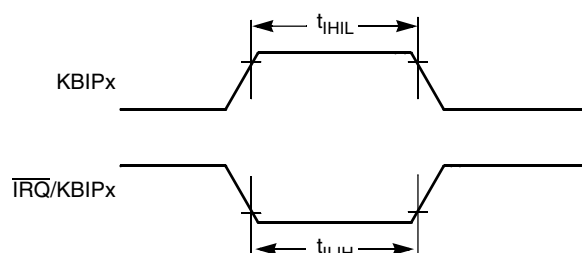
Num	C	Rating		Symbol	Min	Typical <sup>1</sup>	Max	Unit
1	D	System and core clock		f <sub>Sys</sub>	DC	—	48	MHz
2	P	Bus frequency (t <sub>cyc</sub> = 1/f <sub>Bus</sub> )		f <sub>Bus</sub>	DC	—	24	MHz
3	P	Internal low power oscillator frequency		f <sub>LPO</sub>	0.67	1.0	1.25	KHz
4	D	External reset pulse width <sup>2</sup>		t <sub>extrst</sub>	1.5 × t <sub>cyc</sub>	—	—	ns
5	D	Reset low drive		t <sub>rstdrv</sub>	34 × t <sub>cyc</sub>	—	—	ns
6	D	IRQ pulse width	Asynchronous path <sup>2</sup>	t <sub>ILIH</sub>	100	—	—	ns
	D		Synchronous path <sup>3</sup>	t <sub>IHIL</sub>	1.5 × t <sub>cyc</sub>	—	—	ns

Table continues on the next page...

**Table 7. Control timing (continued)**

Num	C	Rating	Symbol	Min	Typical <sup>1</sup>	Max	Unit
7	D	Keyboard interrupt pulse width	Asynchronous path <sup>2</sup>	$t_{\text{LIH}}$	100	—	ns
	D		Synchronous path	$t_{\text{IHIL}}$	$1.5 \times t_{\text{cyc}}$	—	ns
8	C	Port rise and fall time - Normal drive strength (load = 50 pF) <sup>4</sup>	—	$t_{\text{Rise}}$	—	10.2	ns
	C		—	$t_{\text{Fall}}$	—	9.5	ns
	C	Port rise and fall time - high drive strength (load = 50 pF) <sup>4</sup>	—	$t_{\text{Rise}}$	—	5.4	ns
	C		—	$t_{\text{Fall}}$	—	4.6	ns

1. Typical values are based on characterization data at  $V_{\text{DD}} = 5.0 \text{ V}$ ,  $25^\circ\text{C}$  unless otherwise stated.
2. This is the shortest pulse that is guaranteed to be recognized as a RESET pin request.
3. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized.
4. Timing is shown with respect to 20%  $V_{\text{DD}}$  and 80%  $V_{\text{DD}}$  levels. Temperature range  $-40^\circ\text{C}$  to  $105^\circ\text{C}$ .

**Figure 9. Reset timing****Figure 10. KBIPx timing**

## 5.2.2 FTM module timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

**Table 8. FTM input timing**

C	Function	Symbol	Min	Max	Unit
D	Timer clock frequency	$f_{\text{Timer}}$	$f_{\text{Bus}}$	$f_{\text{Sys}}$	Hz
D	External clock frequency	$f_{\text{TCLK}}$	0	$f_{\text{Timer}}/4$	Hz

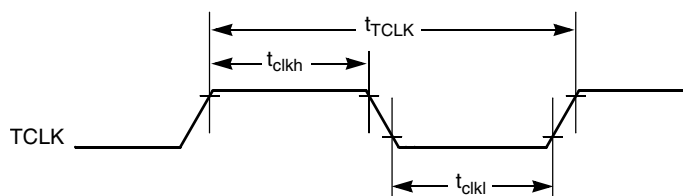
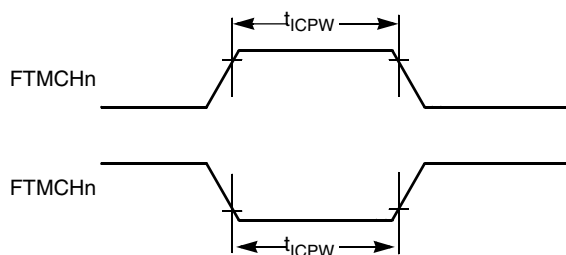
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**Table 8. FTM input timing (continued)**

C	Function	Symbol	Min	Max	Unit
D	External clock period	$t_{TCLK}$	4	—	$t_{Timer}^1$
D	External clock high time	$t_{clkh}$	1.5	—	$t_{Timer}^1$
D	External clock low time	$t_{ckl}$	1.5	—	$t_{Timer}^1$
D	Input capture pulse width	$t_{ICPW}$	1.5	—	$t_{Timer}^1$

1.  $t_{Timer} = 1/f_{Timer}$

**Figure 11. Timer external clock****Figure 12. Timer input capture pulse**

## 5.3 Thermal specifications

### 5.3.1 Thermal operating requirements

**Table 9. Thermal operating requirements**

Symbol	Description	Min.	Max.	Unit	Notes
$T_J$	Die junction temperature	-40	125	°C	
$T_A$	Ambient temperature	-40	105	°C	1

1. Maximum  $T_A$  can be exceeded only if the user ensures that  $T_J$  does not exceed maximum  $T_J$ . The simplest method to determine  $T_J$  is:  $T_J = T_A + \theta_{JA} \times \text{chip power dissipation}$

### 5.3.2 Thermal characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take  $P_{I/O}$  into account in power calculations, determine the difference between actual pin voltage and  $V_{SS}$  or  $V_{DD}$  and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and  $V_{SS}$  or  $V_{DD}$  will be very small.

**Table 10. Thermal attributes**

Board type	Symbol	Description	64 LQFP	64 QFP	44 LQFP	80 LQFP	Unit	Notes
Single-layer (1S)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	71	61	75	57	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	53	47	53	44	°C/W	1, 3
Single-layer (1S)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	59	50	62	47	°C/W	1, 3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	46	41	47	38	°C/W	1, 3
—	$R_{\theta JB}$	Thermal resistance, junction to board	35	32	34	28	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	20	23	20	15	°C/W	5
—	$\Psi_{JT}$	Thermal characterization parameter, junction to package top outside center (natural convection)	5	8	5	3	°C/W	6

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.
3. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the solder pad on the bottom of the package. Interface resistance is ignored.
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization.

The average chip-junction temperature ( $T_J$ ) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA})$$

Where:

$T_A$  = Ambient temperature, °C

$\theta_{JA}$  = Package thermal resistance, junction-to-ambient, °C/W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$ , Watts - chip internal power

$P_{I/O}$  = Power dissipation on input and output pins - user determined

For most applications,  $P_{I/O} \ll P_{int}$  and can be neglected. An approximate relationship between  $P_D$  and  $T_J$  (if  $P_{I/O}$  is neglected) is:

$P_D = K \div (T_J + 273 \text{ °C})$

Solving the equations above for K gives:

$K = P_D \times (T_A + 273 \text{ °C}) + \theta_{JA} \times (P_D)^2$

where K is a constant pertaining to the particular part. K can be determined by measuring  $P_D$  (at equilibrium) for an known  $T_A$ . Using this value of K, the values of  $P_D$  and  $T_J$  can be obtained by solving the above equations iteratively for any value of  $T_A$ .

## 6 Peripheral operating requirements and behaviors

### 6.1 Core modules

#### 6.1.1 SWD electricals

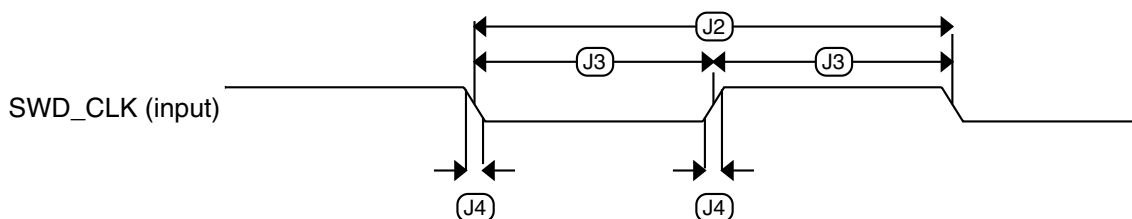
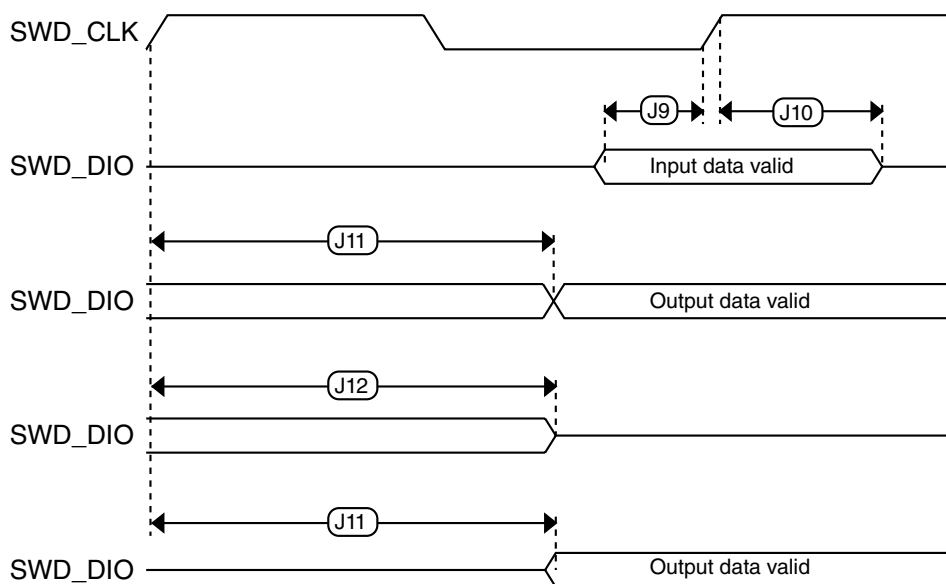
Table 11. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	5.5	V
J1	SWD_CLK frequency of operation <ul style="list-style-type: none"> <li>Serial wire debug</li> </ul>	0	24	MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width <ul style="list-style-type: none"> <li>Serial wire debug</li> </ul>	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	3	—	ns

Table continues on the next page...

**Table 11. SWD full voltage range electricals (continued)**

Symbol	Description	Min.	Max.	Unit
J11	SWD_CLK high to SWD_DIO data valid	—	35	ns
J12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

**Figure 13. Serial wire clock input timing****Figure 14. Serial wire data timing**

## 6.2 External oscillator (OSC) and ICS characteristics

**Table 12. OSC and ICS specifications (temperature range = -40 to 105 °C ambient)**

Num	C	Characteristic		Symbol	Min	Typical <sup>1</sup>	Max	Unit
1	C	Crystal or resonator frequency	Low range (RANGE = 0)	f <sub>lo</sub>	31.25	32.768	39.0625	kHz
	C		High range (RANGE = 1)	f <sub>hi</sub>	4	—	24	MHz

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**Table 12. OSC and ICS specifications (temperature range = -40 to 105 °C ambient)  
(continued)**

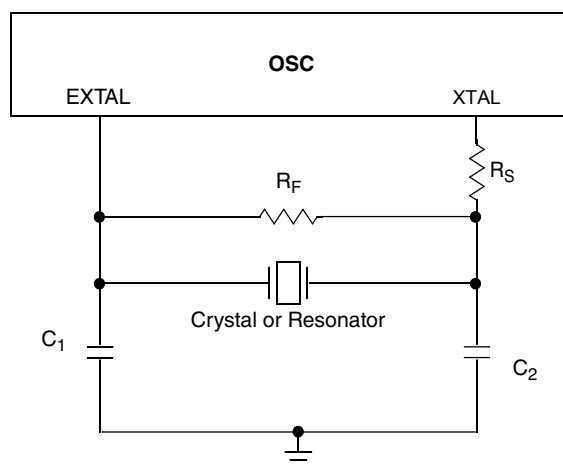
Num	C	Characteristic		Symbol	Min	Typical <sup>1</sup>	Max	Unit
2	D	Load capacitors		C1, C2	See Note <sup>2</sup>			
3	D	Feedback resistor	Low Frequency, Low-Power Mode <sup>3</sup>	$R_F$	—	—	—	MΩ
			Low Frequency, High-Gain Mode		—	10	—	MΩ
			High Frequency, Low-Power Mode		—	1	—	MΩ
			High Frequency, High-Gain Mode		—	1	—	MΩ
4	D	Series resistor - Low Frequency	Low-Power Mode <sup>3</sup>	$R_S$ <sup>2</sup>	—	0	—	kΩ
			High-Gain Mode		—	200	—	kΩ
5	D	Series resistor - High Frequency	Low-Power Mode <sup>3</sup>	$R_S$ <sup>2</sup>	—	0	—	kΩ
	D	Series resistor - High Frequency, High-Gain Mode	4 MHz		—	0	—	kΩ
	D		8 MHz		—	0	—	kΩ
	D		16 MHz		—	0	—	kΩ
6	C	Crystal start-up time low range = 32.768 kHz crystal; High range = 20 MHz crystal <sup>4,5</sup>	Low range, low power	$t_{CSTL}$	—	1000	—	ms
	C		Low range, high gain		—	800	—	ms
	C		High range, low power	$t_{CSTH}$	—	3	—	ms
	C		High range, high gain		—	1.5	—	ms
7	T	Internal reference start-up time		$t_{IRST}$	—	20	50	μs
8	P	Internal reference clock (IRC) frequency trim range		$f_{int\_t}$	31.25	—	39.0625	kHz
9	P	Internal reference clock frequency, factory trimmed	T = 25 °C, $V_{DD}$ = 5 V	$f_{int\_ft}$	—	37.5	—	kHz
10	P	DCO output frequency range	FLL reference = $f_{int\_t}$ , $f_{lo}$ , or $f_{hi}/RDIV$	$f_{dco}$	40	—	50	MHz
11	P	Factory trimmed internal oscillator accuracy <sup>6</sup>	T = 25 °C, $V_{DD}$ = 5 V	$\Delta f_{int\_ft}$	-0.5	—	0.5	%
12	C	Deviation of IRC over temperature when trimmed at T = 25 °C, $V_{DD}$ = 5 V	Over temperature range from -40 °C to 105 °C	$\Delta f_{int\_t}$	-1	—	0.5	%
			Over temperature range from 0 °C to 105 °C	$\Delta f_{int\_t}$	-0.5	—	0.5	
13	C	Frequency accuracy of DCO output using factory trim value	Over temperature range from -40 °C to 105 °C	$\Delta f_{dco\_ft}$	-1.5	—	1	%
			Over temperature range from 0 °C to 105 °C	$\Delta f_{dco\_ft}$	-1	—	1	

Table continues on the next page...

**Table 12. OSC and ICS specifications (temperature range = -40 to 105 °C ambient)  
(continued)**

Num	C	Characteristic	Symbol	Min	Typical <sup>1</sup>	Max	Unit
14	C	FLL acquisition time <sup>4,7</sup>	$t_{\text{Acquire}}$	—	—	2	ms
15	C	Long term jitter of DCO output clock (averaged over 2 ms interval) <sup>8</sup>	$C_{\text{Jitter}}$	—	0.02	0.2	% $f_{\text{dco}}$

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. See crystal or resonator manufacturer's recommendation.
3. Load capacitors ( $C_1, C_2$ ), feedback resistor ( $R_F$ ) and series resistor ( $R_S$ ) are incorporated internally when RANGE = HGO = 0.
4. This parameter is characterized and not tested on each device.
5. Proper PC board layout procedures must be followed to achieve specifications.
6. The accuracy is for factory trimmed deviation when performing trim process in NXP, however, the reflow process may cause an extra 0.5% drift at the room temperature.
7. This specification applies to any time the FLL reference source or reference divider is changed, trim value changed, or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
8. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum  $f_{\text{Bus}}$ . Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via  $V_{\text{DD}}$  and  $V_{\text{SS}}$  and variation in crystal oscillator frequency increase the  $C_{\text{Jitter}}$  percentage for a given interval.

**Figure 15. Typical crystal or resonator circuit**

## 6.3 NVM specifications

This section provides details about program/erase times and program/erase endurance for the flash memories.

**Table 13. Flash characteristics**

C	Characteristic	Symbol	Min <sup>1</sup>	Typical <sup>2</sup>	Max <sup>3</sup>	Unit <sup>4</sup>
D	Supply voltage for program/erase -40 °C to 105 °C	$V_{\text{prog/erase}}$	2.7	—	5.5	V

Table continues on the next page...

**Table 13. Flash characteristics (continued)**

C	Characteristic	Symbol	Min <sup>1</sup>	Typical <sup>2</sup>	Max <sup>3</sup>	Unit <sup>4</sup>
D	Supply voltage for read operation	V <sub>Read</sub>	2.7	—	5.5	V
D	NVM Bus frequency	f <sub>NVMBUS</sub>	1	—	24	MHz
D	NVM Operating frequency	f <sub>NVMOP</sub>	0.8	1	1.05	MHz
D	Erase Verify All Blocks	t <sub>VFYALL</sub>	—	—	2605	t <sub>cyc</sub>
D	Erase Verify Flash Block	t <sub>RD1BLK</sub>	—	—	2579	t <sub>cyc</sub>
D	Erase Verify Flash Section	t <sub>RD1SEC</sub>	—	—	485	t <sub>cyc</sub>
D	Read Once	t <sub>RDONCE</sub>	—	—	464	t <sub>cyc</sub>
D	Program Flash (2 word)	t <sub>PGM2</sub>	0.12	0.13	0.31	ms
D	Program Flash (4 word)	t <sub>PGM4</sub>	0.21	0.21	0.49	ms
D	Program Once	t <sub>PGMONCE</sub>	0.20	0.21	0.21	ms
D	Erase All Blocks	t <sub>ERSALL</sub>	95.42	100.18	100.30	ms
D	Erase Flash Block	t <sub>ERSBLK</sub>	95.42	100.18	100.30	ms
D	Erase Flash Sector	t <sub>ERSPG</sub>	19.10	20.05	20.09	ms
D	Unsecure Flash	t <sub>UNSECU</sub>	95.42	100.19	100.31	ms
D	Verify Backdoor Access Key	t <sub>VFYKEY</sub>	—	—	482	t <sub>cyc</sub>
D	Set User Margin Level	t <sub>MLOADU</sub>	—	—	415	t <sub>cyc</sub>
C	FLASH Program/erase endurance T <sub>L</sub> to T <sub>H</sub> = -40 °C to 105 °C	n <sub>FLPE</sub>	10 k	100 k	—	Cycles
C	Data retention at an average junction temperature of T <sub>Javg</sub> = 85°C after up to 10,000 program/erase cycles	t <sub>D_ret</sub>	15	100	—	years

1. Minimum times are based on maximum f<sub>NVMOP</sub> and maximum f<sub>NVMBUS</sub>
2. Typical times are based on typical f<sub>NVMOP</sub> and maximum f<sub>NVMBUS</sub>
3. Maximum times are based on typical f<sub>NVMOP</sub> and typical f<sub>NVMBUS</sub> plus aging
4. t<sub>cyc</sub> = 1 / f<sub>NVMBUS</sub>

Program and erase operations do not require any special power sources other than the normal V<sub>DD</sub> supply. For more detailed information about program/erase operations, see the Flash Memory Module section in the reference manual.

## 6.4 Analog

### 6.4.1 ADC characteristics

**Table 14. 5 V 12-bit ADC operating conditions**

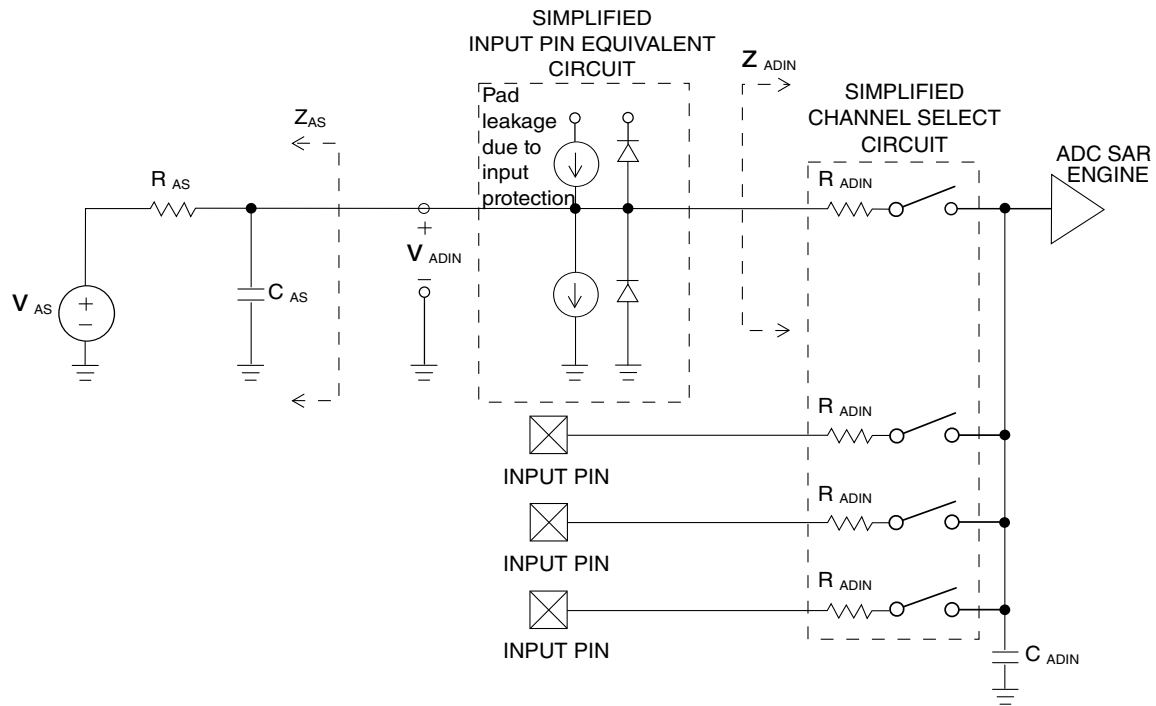
Characteristic	Conditions	Symbol	Min	Typ <sup>1</sup>	Max	Unit	Comment
Reference potential	<ul style="list-style-type: none"> <li>• Low</li> <li>• High</li> </ul>	V <sub>REFL</sub>	V <sub>SSA</sub>	—	V <sub>DDA</sub> /2	V	—
		V <sub>REFH</sub>	V <sub>DDA</sub> /2	—	V <sub>DDA</sub>		

Table continues on the next page...

**Table 14. 5 V 12-bit ADC operating conditions (continued)**

Characteristic	Conditions	Symbol	Min	Typ <sup>1</sup>	Max	Unit	Comment
Supply voltage	Absolute	$V_{DDA}$	2.7	—	5.5	V	—
	Delta to $V_{DD}$ ( $V_{DD}-V_{DDA}$ )	$\Delta V_{DDA}$	-100	0	+100	mV	—
Input voltage		$V_{ADIN}$	$V_{REFL}$	—	$V_{REFH}$	V	—
Input capacitance		$C_{ADIN}$	—	4.5	5.5	pF	—
Input resistance		$R_{ADIN}$	—	3	5	k $\Omega$	—
Analog source resistance	12-bit mode	$R_{AS}$	—	—	2	k $\Omega$	External to MCU
	• $f_{ADCK} > 4$ MHz		—	—	5		
	• $f_{ADCK} < 4$ MHz		—	—	5		
	10-bit mode		—	—	5		
	• $f_{ADCK} > 4$ MHz		—	—	10		
	• $f_{ADCK} < 4$ MHz		—	—	10		
	8-bit mode		—	—	10		
	(all valid $f_{ADCK}$ )		—	—	10		
ADC conversion clock frequency	High speed (ADLPC=0)	$f_{ADCK}$	0.4	—	8.0	MHz	—
	Low power (ADLPC=1)		0.4	—	4.0		

1. Typical values assume  $V_{DDA} = 5.0$  V, Temp = 25°C,  $f_{ADCK}=1.0$  MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

**Figure 16. ADC input impedance equivalency diagram**



**Table 15. 12-bit ADC characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ )**

Characteristic	Conditions	C	Symbol	Min	Typ <sup>1</sup>	Max	Unit
Supply current ADLPC = 1 ADLSMP = 1 ADCO = 1		T	$I_{DDA}$	—	133	—	$\mu A$
Supply current ADLPC = 1 ADLSMP = 0 ADCO = 1		T	$I_{DDA}$	—	218	—	$\mu A$
Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1		T	$I_{DDA}$	—	327	—	$\mu A$
Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1		T	$I_{DDA}$	—	582	990	$\mu A$
Supply current	Stop, reset, module off	T	$I_{DDA}$	—	0.011	1	$\mu A$
ADC asynchronous clock source	High speed (ADLPC = 0)	P	$f_{ADACK}$	2	3.3	5	MHz
	Low power (ADLPC = 1)			1.25	2	3.3	
Conversion time (including sample time)	Short sample (ADLSMP = 0)	T	$t_{ADC}$	—	20	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	40	—	
Sample time	Short sample (ADLSMP = 0)	T	$t_{ADS}$	—	3.5	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	23.5	—	
Total unadjusted Error <sup>2</sup>	12-bit mode	C	$E_{TUE}$	—	$\pm 5.0$	—	LSB <sup>3</sup>
	10-bit mode	C		—	$\pm 1.5$	—	
	8-bit mode	C		—	$\pm 0.8$	—	
Differential Non-Linearity	12-bit mode	C	DNL	—	$\pm 1.5$	—	LSB <sup>3</sup>
	10-bit mode	C		—	$\pm 0.4$	—	
	8-bit mode	C		—	$\pm 0.15$	—	
Integral Non-Linearity	12-bit mode	C	INL	—	$\pm 1.5$	—	LSB <sup>3</sup>
	10-bit mode	C		—	$\pm 0.4$	—	
	8-bit mode	C		—	$\pm 0.15$	—	
Zero-scale error <sup>4</sup>	12-bit mode	C	$E_{ZS}$	—	$\pm 1.0$	—	LSB <sup>3</sup>
	10-bit mode	C		—	$\pm 0.2$	—	

Table continues on the next page...

**Table 15. 12-bit ADC characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ ) (continued)**

Characteristic	Conditions	C	Symbol	Min	Typ <sup>1</sup>	Max	Unit
Full-scale error <sup>5</sup>	8-bit mode	C	$E_{FS}$	—	$\pm 0.35$	—	LSB <sup>3</sup>
	12-bit mode	C		—	$\pm 2.5$	—	
	10-bit mode	C		—	$\pm 0.3$	—	
	8-bit mode	C		—	$\pm 0.25$	—	
Quantization error	$\leq 12$ bit modes	D	$E_Q$	—	—	$\pm 0.5$	LSB <sup>3</sup>
Input leakage error <sup>6</sup>	all modes	D	$E_{IL}$	$I_{in} * R_{AS}$			mV
Temp sensor slope	-40 °C–25 °C	D	m	—	3.266	—	mV/°C
	25 °C–125 °C			—	3.638	—	
Temp sensor voltage	25 °C	D	$V_{TEMP25}$	—	1.396	—	V

1. Typical values assume  $V_{DDA} = 5.0$  V, Temp = 25 °C,  $f_{ADCK} = 1.0$  MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. Includes quantization
3.  $1 \text{ LSB} = (V_{REFH} - V_{REFL})/2^N$
4.  $V_{ADIN} = V_{SSA}$
5.  $V_{ADIN} = V_{DDA}$
6.  $I_{in}$  = leakage current (refer to DC characteristics)

## 6.4.2 Analog comparator (ACMP) electricals

**Table 16. Comparator electrical specifications**

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage	$V_{DDA}$	2.7	—	5.5	V
T	Supply current (Operation mode)	$I_{DDA}$	—	10	20	$\mu\text{A}$
D	Analog input voltage	$V_{AIN}$	$V_{SS} - 0.3$	—	$V_{DDA}$	V
P	Analog input offset voltage	$V_{AIO}$	—	—	40	mV
C	Analog comparator hysteresis (HYST=0)	$V_H$	—	15	20	mV
C	Analog comparator hysteresis (HYST=1)	$V_H$	—	20	30	mV
T	Supply current (Off mode)	$I_{DDAOFF}$	—	60	—	nA
C	Propagation Delay	$t_D$	—	0.4	1	$\mu\text{s}$

## 6.5 Communication interfaces

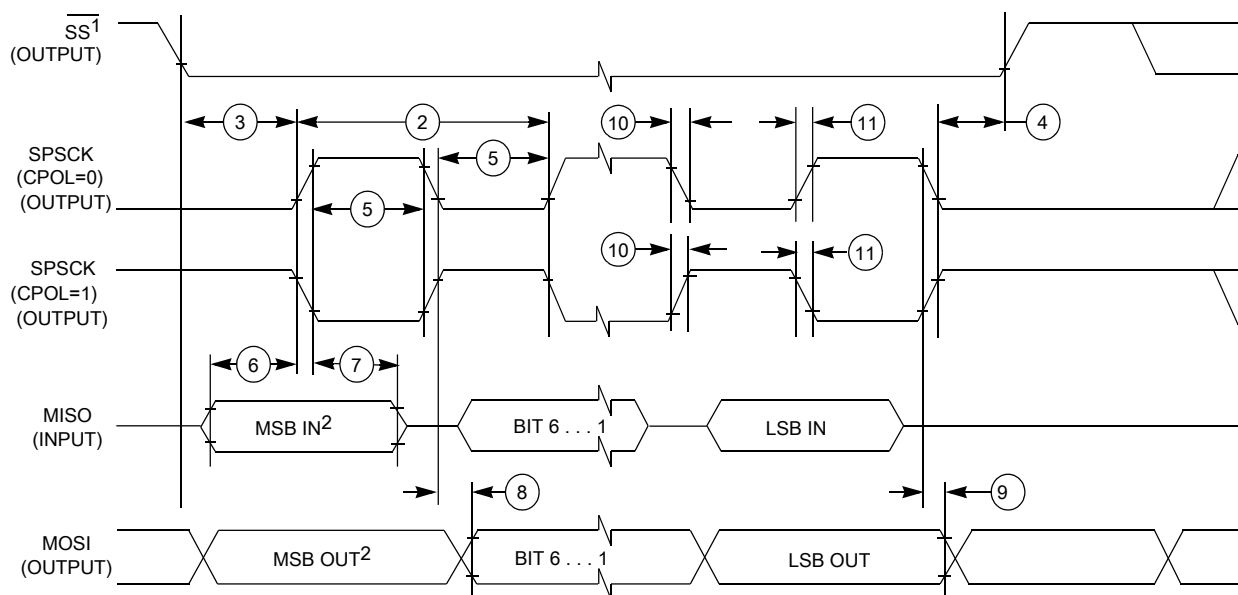
### 6.5.1 SPI switching specifications

The serial peripheral interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the

chip's reference manual for information about the modified transfer formats used for communicating with slower peripheral devices. All timing is shown with respect to 20%  $V_{DD}$  and 80%  $V_{DD}$ , unless noted, and 25 pF load on all SPI pins. All timing assumes high-drive strength is enabled for SPI output pins.

**Table 17. SPI master mode timing**

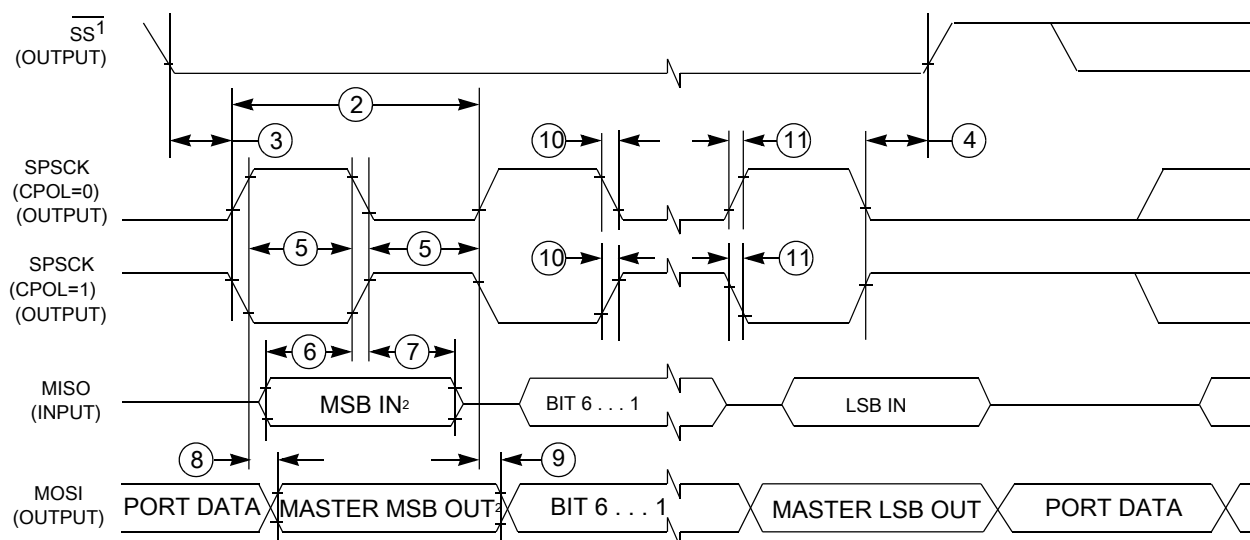
Nu m.	Symbol	Description	Min.	Max.	Unit	Comment
1	$f_{op}$	Frequency of operation	$f_{Bus}/2048$	$f_{Bus}/2$	Hz	$f_{Bus}$ is the bus clock
2	$t_{SPSCK}$	SPSCK period	$2 \times t_{Bus}$	$2048 \times t_{Bus}$	ns	$t_{Bus} = 1/f_{Bus}$
3	$t_{Lead}$	Enable lead time	1/2	—	$t_{SPSCK}$	—
4	$t_{Lag}$	Enable lag time	1/2	—	$t_{SPSCK}$	—
5	$t_{WSPSCK}$	Clock (SPSCK) high or low time	$t_{Bus} - 30$	$1024 \times t_{Bus}$	ns	—
6	$t_{SU}$	Data setup time (inputs)	8	—	ns	—
7	$t_{HI}$	Data hold time (inputs)	8	—	ns	—
8	$t_v$	Data valid (after SPSCK edge)	—	25	ns	—
9	$t_{HO}$	Data hold time (outputs)	20	—	ns	—
10	$t_{RI}$	Rise time input	—	$t_{Bus} - 25$	ns	—
	$t_{FI}$	Fall time input	—	—	—	—
11	$t_{RO}$	Rise time output	—	25	ns	—
	$t_{FO}$	Fall time output	—	—	—	—



1. If configured as an output.

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure 17. SPI master mode timing (CPHA=0)**



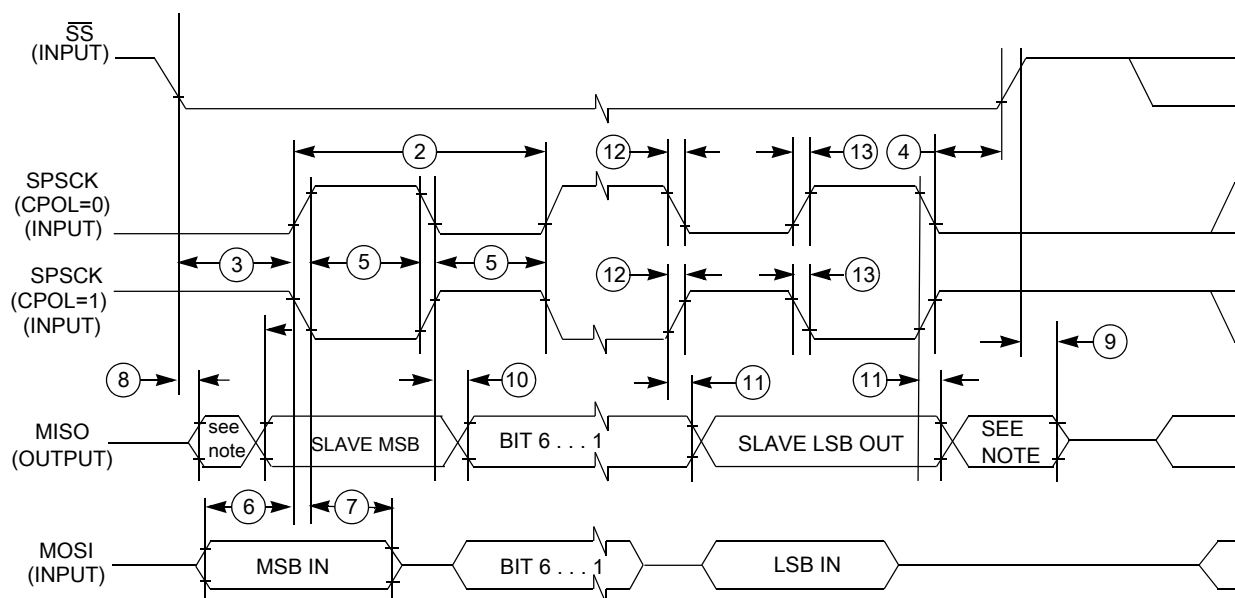
1. If configured as output

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure 18. SPI master mode timing (CPHA=1)**

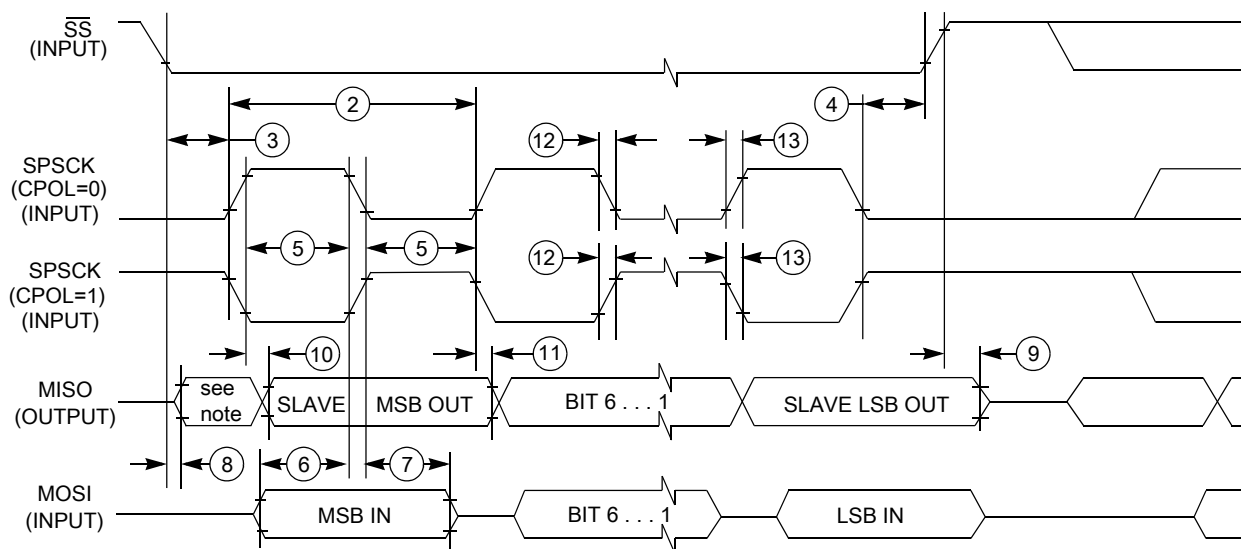
**Table 18. SPI slave mode timing**

Nu m.	Symbol	Description	Min.	Max.	Unit	Comment
1	$f_{op}$	Frequency of operation	0	$f_{Bus}/4$	Hz	$f_{Bus}$ is the bus clock as defined in <a href="#">Control timing</a> .
2	$t_{SPSCK}$	SPSCCK period	$4 \times t_{Bus}$	—	ns	$t_{Bus} = 1/f_{Bus}$
3	$t_{Lead}$	Enable lead time	1	—	$t_{Bus}$	—
4	$t_{Lag}$	Enable lag time	1	—	$t_{Bus}$	—
5	$t_{WSPSCK}$	Clock (SPSCCK) high or low time	$t_{Bus} - 30$	—	ns	—
6	$t_{SU}$	Data setup time (inputs)	15	—	ns	—
7	$t_{HI}$	Data hold time (inputs)	25	—	ns	—
8	$t_a$	Slave access time	—	$t_{Bus}$	ns	Time to data active from high-impedance state
9	$t_{dis}$	Slave MISO disable time	—	$t_{Bus}$	ns	Hold time to high-impedance state
10	$t_v$	Data valid (after SPSCCK edge)	—	25	ns	—
11	$t_{HO}$	Data hold time (outputs)	0	—	ns	—
12	$t_{RI}$	Rise time input	—	$t_{Bus} - 25$	ns	—
	$t_{FI}$	Fall time input				
13	$t_{RO}$	Rise time output	—	25	ns	—
	$t_{FO}$	Fall time output				



NOTE: Not defined

Figure 19. SPI slave mode timing (CPHA = 0)



NOTE: Not defined

Figure 20. SPI slave mode timing (CPHA=1)

## 7 Dimensions

### 7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to [nxp.com](http://nxp.com) and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
44-pin LQFP	98ASS23225W
64-pin QFP	98ASB42844B
64-pin LQFP	98ASS23234W
80-pin LQFP	98ASS23237W

## 8 Pinout

### 8.1 Signal multiplexing and pin assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

#### NOTE

VSS and VSSA are internally connected.

VREFH and VDDA are internally connected in 64-pin packages.

PTB4, PTB5, PTD0, PTD1, PTE0, PTE1, PTH0, and PTH1 are high-current drive pins when operated as output.

PTA2 and PTA3 are true open-drain pins when operated as output.

80 LQFP	64 LQFP /QFP	44 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
1	1	1	PTD1	DISABLED	PTD1	KB10_P25	FTM2_CH3	SPI1_MOSI				
2	2	2	PTD0	DISABLED	PTD0	KB10_P24	FTM2_CH2	SPI1_SCK				
3	3	—	PTH7	DISABLED	PTH7	KB11_P31	PWT_IN1					
4	4	—	PTH6	DISABLED	PTH6	KB11_P30						
5	—	—	PTH5	DISABLED	PTH5	KB11_P29						
6	5	3	PTE7	DISABLED	PTE7	KB11_P7	TCLK2		FTM1_CH1			
7	6	4	PTH2	DISABLED	PTH2	KB11_P26	BUSOUT		FTM1_CH0			
8	7	5	VDD	VDD							VDD	
9	8	6	VDDA	VDDA						VREFH	VDDA	

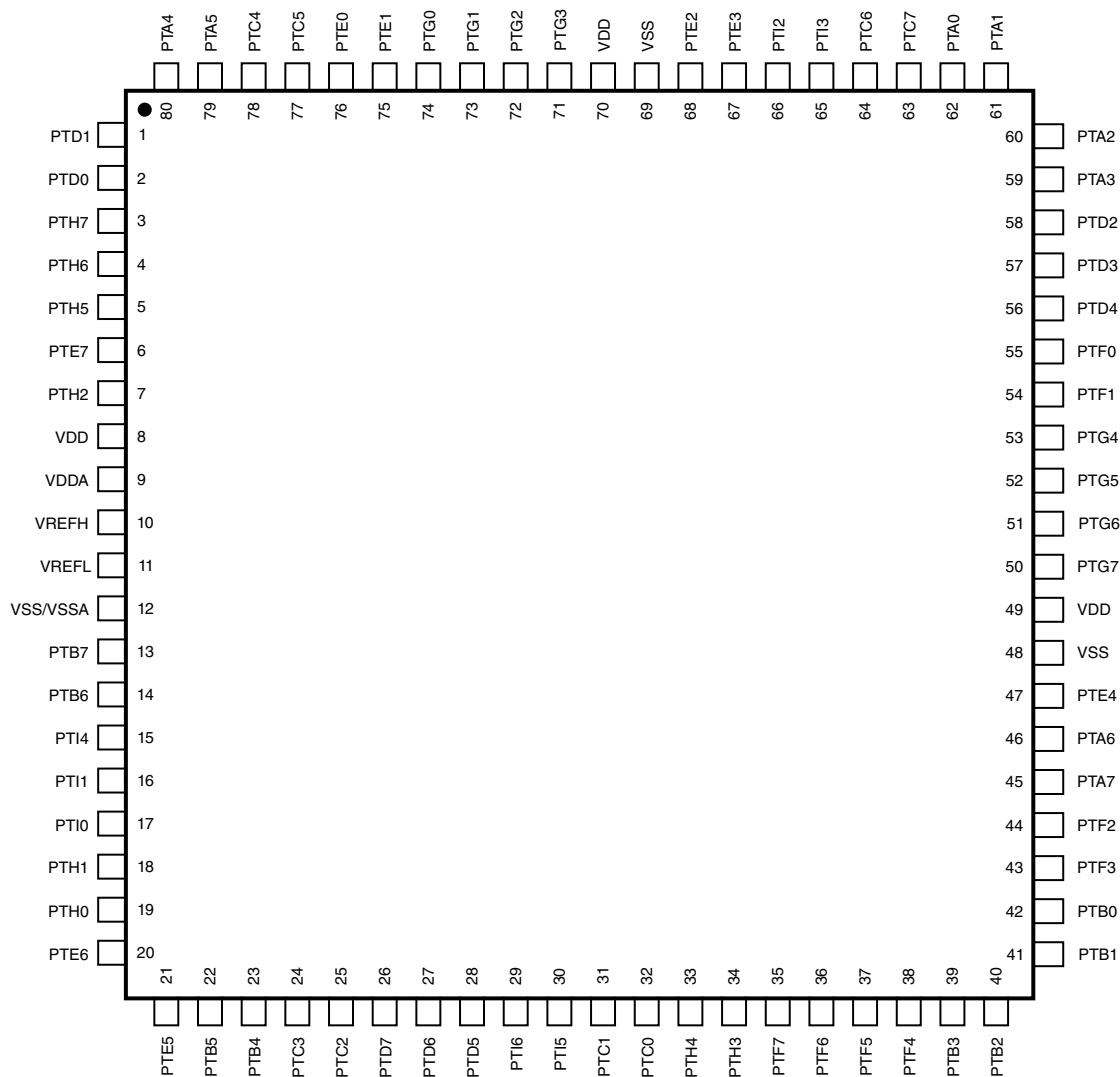
## Pinout

80 LQFP	64 LQFP /QFP	44 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
10	—	—	VREFH	VREFH							VREFH	
11	9	7	VREFL	VREFL							VREFL	
12	10	8	VSS/ VSSA	VSS/ VSSA						VSSA	VSS	
13	11	9	PTB7	EXTAL	PTB7	KB10_P15	I2C0_SCL				EXTAL	
14	12	10	PTB6	XTAL	PTB6	KB10_P14	I2C0_SDA				XTAL	
15	13	11	PTI4	DISABLED	PTI4		IRQ					
16	—	—	PTI1	DISABLED	PTI1		IRQ	UART2_TX				
17	—	—	PTI0	DISABLED	PTI0		IRQ	UART2_RX				
18	14	—	PTH1	DISABLED	PTH1	KB11_P25	FTM2_CH1					
19	15	—	PTH0	DISABLED	PTH0	KB11_P24	FTM2_CH0					
20	16	—	PTE6	DISABLED	PTE6	KB11_P6						
21	17	—	PTE5	DISABLED	PTE5	KB11_P5						
22	18	12	PTB5	DISABLED	PTB5	KB10_P13	FTM2_CH5	SPI0_PCS	ACMP1_OUT			
23	19	13	PTB4	NMI_b	PTB4	KB10_P12	FTM2_CH4	SPI0_MISO	ACMP1_IN2	NMI_b		
24	20	14	PTC3	ADC0_SE11	PTC3	KB10_P19	FTM2_CH3		ADC0_SE11			
25	21	15	PTC2	ADC0_SE10	PTC2	KB10_P18	FTM2_CH2		ADC0_SE10			
26	22	16	PTD7	DISABLED	PTD7	KB10_P31	UART2_TX					
27	23	17	PTD6	DISABLED	PTD6	KB10_P30	UART2_RX					
28	24	18	PTD5	DISABLED	PTD5	KB10_P29	PWT_IN0					
29	—	—	PTI6	DISABLED	PTI6	IRQ						
30	—	—	PTI5	DISABLED	PTI5	IRQ						
31	25	19	PTC1	ADC0_SE9	PTC1	KB10_P17	FTM2_CH1		ADC0_SE9			
32	26	20	PTC0	ADC0_SE8	PTC0	KB10_P16	FTM2_CH0		ADC0_SE8			
33	—	—	PTH4	DISABLED	PTH4	KB11_P28	I2C1_SCL					
34	—	—	PTH3	DISABLED	PTH3	KB11_P27	I2C1_SDA					
35	27	—	PTF7	ADC0_SE15	PTF7	KB11_P15			ADC0_SE15			
36	28	—	PTF6	ADC0_SE14	PTF6	KB11_P14			ADC0_SE14			
37	29	—	PTF5	ADC0_SE13	PTF5	KB11_P13			ADC0_SE13			
38	30	—	PTF4	ADC0_SE12	PTF4	KB11_P12			ADC0_SE12			
39	31	21	PTB3	ADC0_SE7	PTB3	KB10_P11	SPI0_MOSI	FTM0_CH1	ADC0_SE7			
40	32	22	PTB2	ADC0_SE6	PTB2	KB10_P10	SPI0_SCK	FTM0_CH0	ADC0_SE6			
41	33	23	PTB1	ADC0_SE5	PTB1	KB10_P9	UART0_TX		ADC0_SE5			
42	34	24	PTB0	ADC0_SE4	PTB0	KB10_P8	UART0_RX	PWT_IN1	ADC0_SE4			
43	35	—	PTF3	DISABLED	PTF3	KB11_P11	UART1_TX					
44	36	—	PTF2	DISABLED	PTF2	KB11_P10	UART1_RX					
45	37	25	PTA7	ADC0_SE3	PTA7	KB10_P7	FTM2_FLT2	ACMP1_IN1	ADC0_SE3			
46	38	26	PTA6	ADC0_SE2	PTA6	KB10_P6	FTM2_FLT1	ACMP1_IN0	ADC0_SE2			
47	39	—	PTE4	DISABLED	PTE4	KB11_P4						
48	40	27	VSS	VSS							VSS	
49	41	28	VDD	VDD							VDD	

80 LQFP	64 LQFP /QFP	44 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
50	—	—	PTG7	DISABLED	PTG7	KBI1_P23	FTM2_CH5	SPI1_PCS				
51	—	—	PTG6	DISABLED	PTG6	KBI1_P22	FTM2_CH4	SPI1_MISO				
52	—	—	PTG5	DISABLED	PTG5	KBI1_P21	FTM2_CH3	SPI1_MOSI				
53	—	—	PTG4	DISABLED	PTG4	KBI1_P20	FTM2_CH2	SPI1_SCK				
54	42	—	PTF1	DISABLED	PTF1	KBI1_P9	FTM2_CH1					
55	43	—	PTF0	DISABLED	PTF0	KBI1_P8	FTM2_CH0					
56	44	29	PTD4	DISABLED	PTD4	KBI0_P28						
57	45	30	PTD3	DISABLED	PTD3	KBI0_P27	SPI1_PCS					
58	46	31	PTD2	DISABLED	PTD2	KBI0_P26	SPI1_MISO					
59	47	32	PTA3	DISABLED	PTA3	KBI0_P3	UART0_TX	I2C0_SCL				
60	48	33	PTA2	DISABLED	PTA2	KBI0_P2	UART0_RX	I2C0_SDA				
61	49	34	PTA1	ADC0_SE1	PTA1	KBI0_P1	FTM0_CH1	I2C0_4WSDAOUT	ACMP0_IN1	ADC0_SE1		
62	50	35	PTA0	ADC0_SE0	PTA0	KBI0_P0	FTM0_CH0	I2C0_4WSCLOUT	ACMP0_IN0	ADC0_SE0		
63	51	36	PTC7	DISABLED	PTC7	KBI0_P23	UART1_TX					
64	52	37	PTC6	DISABLED	PTC6	KBI0_P22	UART1_RX					
65	—	—	PTI3	DISABLED	PTI3	IRQ						
66	—	—	PTI2	DISABLED	PTI2	IRQ						
67	53	—	PTE3	DISABLED	PTE3	KBI1_P3	SPI0_PCS					
68	54	38	PTE2	DISABLED	PTE2	KBI1_P2	SPI0_MISO	PWT_IN0				
69	—	—	VSS	VSS							VSS	
70	—	—	VDD	VDD							VDD	
71	55	—	PTG3	DISABLED	PTG3	KBI1_P19						
72	56	—	PTG2	DISABLED	PTG2	KBI1_P18						
73	57	—	PTG1	DISABLED	PTG1	KBI1_P17						
74	58	—	PTG0	DISABLED	PTG0	KBI1_P16						
75	59	39	PTE1	DISABLED	PTE1	KBI1_P1	SPI0_MOSI		I2C1_SCL			
76	60	40	PTE0	DISABLED	PTE0	KBI1_P0	SPI0_SCK	TCLK1	I2C1_SDA			
77	61	41	PTC5	DISABLED	PTC5	KBI0_P21		FTM1_CH1		RTC_CLKOUT		
78	62	42	PTC4	SWD_CLK	PTC4	KBI0_P20	RTC_CLKOUT	FTM1_CH0	ACMP0_IN2	SWD_CLK		
79	63	43	PTA5	RESET_b	PTA5	KBI0_P5	IRQ	TCLK0	RESET_b			
80	64	44	PTA4	SWD_DIO	PTA4	KBI0_P4		ACMP0_OUT	SWD_DIO			

## 8.2 Device pin assignment





**Figure 21. 80-pin LQFP package**

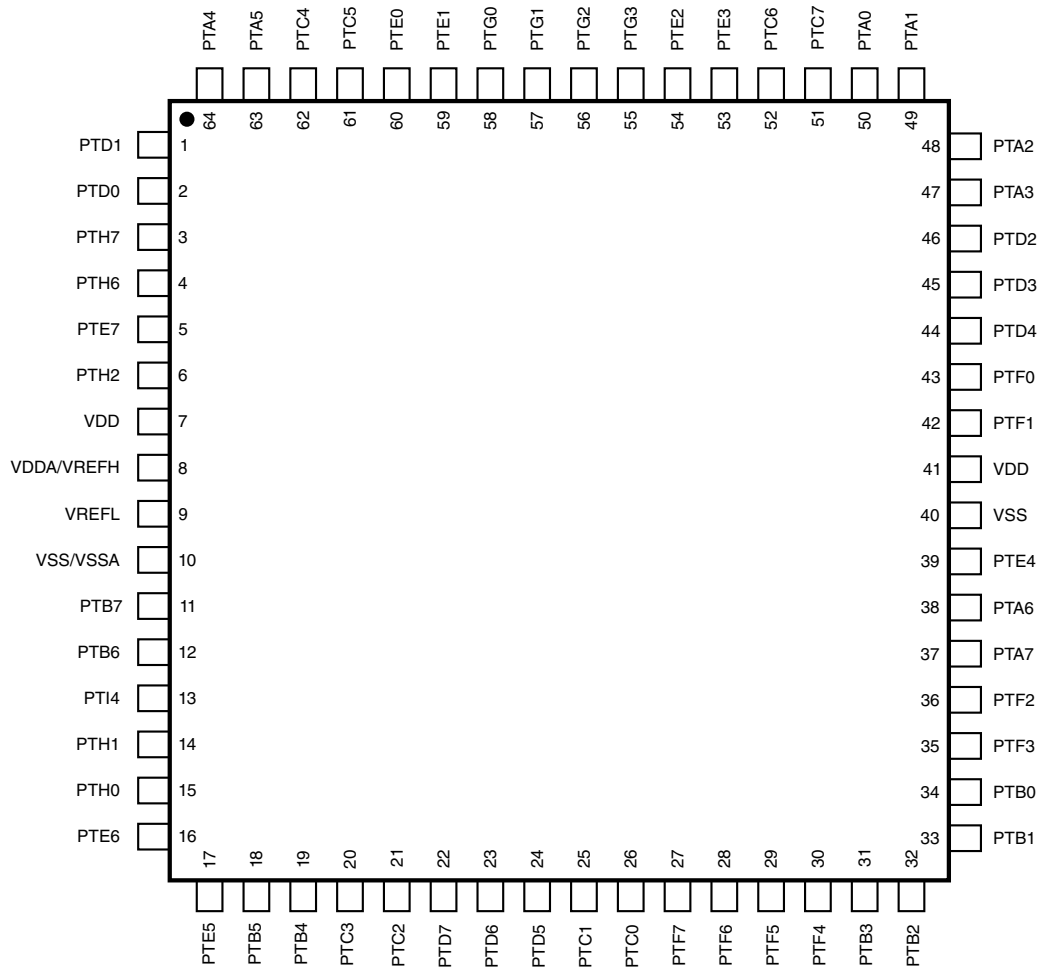


Figure 22. 64-pin QFP/LQFP packages

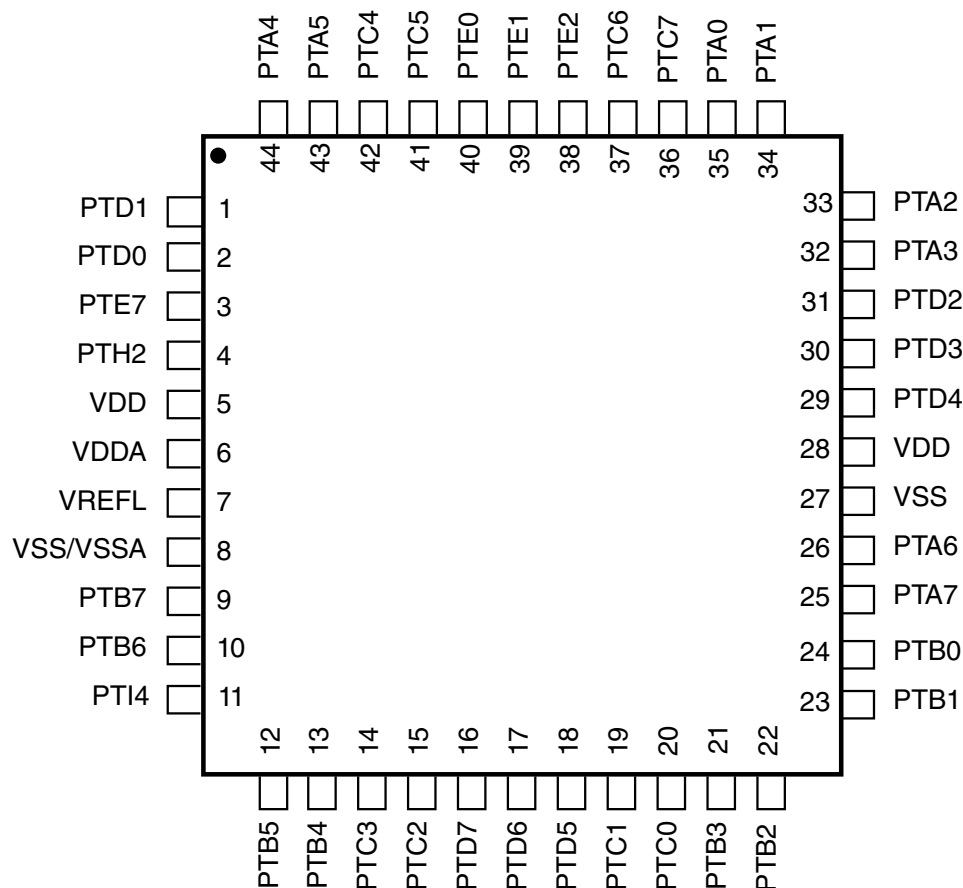


Figure 23. 44-pin LQFP package

## 9 Revision history

The following table provides a revision history for this document.

Table 19. Revision history

Rev. No.	Date	Substantial Changes
1	12/2013	Initial NDA release.
2	3/2014	Initial public release.
3	5/2014	<ul style="list-style-type: none"><li>Updated the Max. of <math>SI_{DD}</math>.</li><li>Updated footnote to the <math>V_{OH}</math>.</li><li>Corrected Unit in the FTM input timing table.</li></ul>
4	07/2016	<ul style="list-style-type: none"><li>Added a new section of <a href="#">Thermal operating requirements</a>.</li><li>Corrected pinout diagram for 44-pin LQFP in the <a href="#">Device pin assignment</a>.</li></ul>
5	01/2019	<ul style="list-style-type: none"><li>Added a footnote of "Max power supply ramp rate is 500 V/ms." to Operating voltage in the <a href="#">DC characteristics</a>.</li><li>Added a footnote to the <math>\Delta f_{int\_ft}</math> in the <a href="#">External oscillator (OSC) and ICS characteristics</a>.</li></ul>

Table continues on the next page...

**Table 19. Revision history (continued)**

Rev. No.	Date	Substantial Changes
6	04/2020	<ul style="list-style-type: none"><li>• Updated the footnote to Operating voltage in the <a href="#">DC characteristics</a>.</li><li>• Updated the timing assumptions in the <a href="#">SPI switching specifications</a>.</li></ul>

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