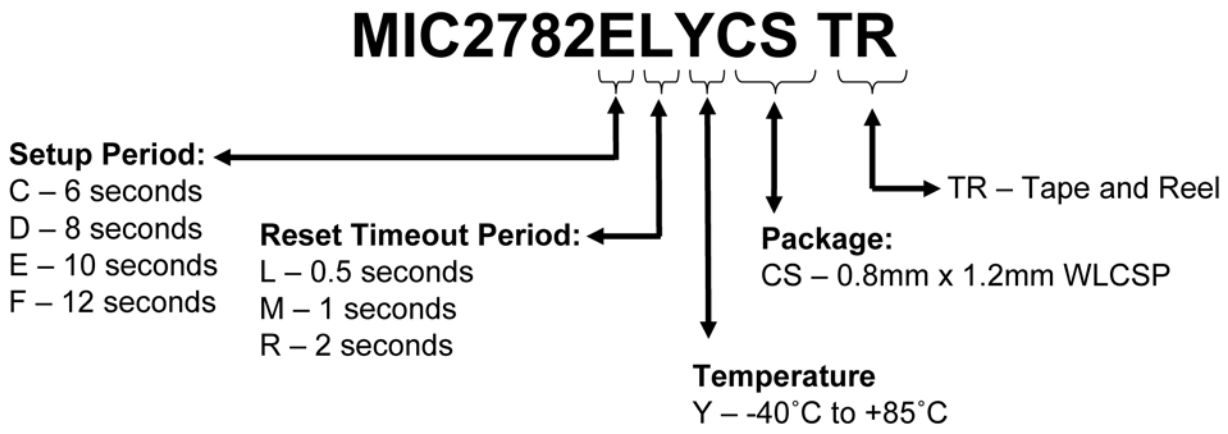
Ordering Information

Part Number	Part Marking	Setup Period (t_{SETUP}) (s)	Reset Timeout Period (t_{RESET}) (s)	Package
MIC2782CLYCS	UJA	6	0.5	6-bump, 0.4mm pitch, 0.8mm × 1.2mm WLCSP
MIC2782CMYCS[1]	-	6	1	6-bump, 0.4mm pitch, 0.8mm × 1.2mm WLCSP
MIC2782CRYCS	UJC	6	2	6-bump, 0.4mm pitch, 0.8mm × 1.2mm WLCSP
MIC2782DLYCS	UKU	8	0.5	6-bump, 0.4mm pitch, 0.8mm × 1.2mm WLCSP
MIC2782DMYCS[1]	-	8	1	6-bump, 0.4mm pitch, 0.8mm × 1.2mm WLCSP
MIC2782DRYCS	UJE	8	2	6-bump, 0.4mm pitch, 0.8mm × 1.2mm WLCSP
MIC2782ELYCS	UKW	10	0.5	6-bump, 0.4mm pitch, 0.8mm × 1.2mm WLCSP
MIC2782EMYCS	UKX	10	1	6-bump, 0.4mm pitch, 0.8mm × 1.2mm WLCSP
MIC2782ERYCS[1]	-	10	2	6-bump, 0.4mm pitch, 0.8mm × 1.2mm WLCSP
MIC2782FLYCS	UJF	12	0.5	6-bump, 0.4mm pitch, 0.8mm × 1.2mm WLCSP
MIC2782FMYCS[1]	-	12	1	6-bump, 0.4mm pitch, 0.8mm × 1.2mm WLCSP
MIC2782FRYCS	UKZ	12	2	6-bump, 0.4mm pitch, 0.8mm × 1.2mm WLCSP

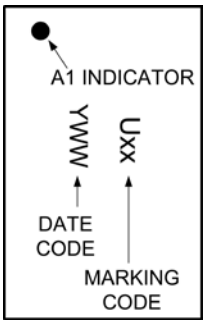
Notes:

1. Contact Factory for availability.

Ordering Guide

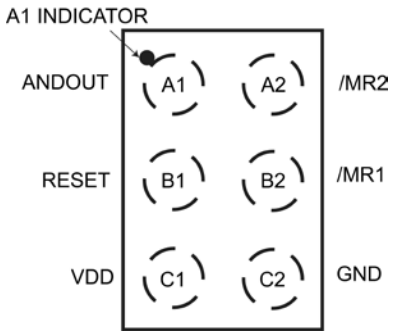


Chip Scale Package (CS) Bump Configuration

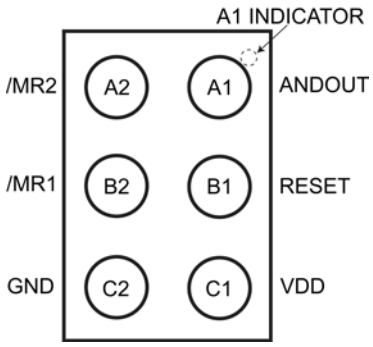


Y = Year Code
WW = Week Code

TOP VIEW



TOP VIEW (BUMP SIDE DOWN)



BOTTOM VIEW (BUMP SIDE UP)

6-Bump, 0.4mm pitch, 0.8mm x 1.2mm WLCSP

Pin Description

Bump Designation	Bump Name	Pin Function
A1	ANDOUT	NMOS Open-Drain output, Active-Low. Asserts low 1.5ms after /MR1 and /MR2 are both asserted low. Connect a resistor greater than 5kΩ from the ANDOUT pin to VDD in order to pull up the ANDOUT output voltage when inactive. No ESD diode from ANDOUT to VDD. Please see the Functional Description and Timing Diagram sections for further details of how the ANDOUT output functions.
A2	/MR2	Manual Reset Input 2, Active-Low. Internal 65kΩ (typical) Pull-Up Resistor to VDD. Pulling both manual reset inputs low for longer than the setup period causes one RESET output pulse for the reset timeout delay period.
B1	RESET	NMOS Open-Drain output, Active-Low. Asserts low after /MR1 and /MR2 have both asserted low for longer than setup period. Connect a resistor greater than 5kΩ from the RESET pin to VDD in order to pull up the RESET output voltage when inactive. No ESD diode from RESET to VDD. Please see the Functional Description and Timing Diagram sections for further details of how the RESET output functions.
B2	/MR1	Manual Reset Input 1, Active-Low. Internal 65kΩ (typical) Pull-Up Resistor to VDD. Pulling both manual reset inputs low for longer than the setup period causes one RESET output pulse for the reset timeout delay period.
C1	VDD	Supply Voltage. Bypass to ground with minimum 0.1µF capacitor.
C2	GND	Supply Ground.

Absolute Maximum Ratings [1]

Supply Voltage (V_{DD}).....GND to +6.0V
Input Voltage ($V_{/MR1}$, $V_{/MR2}$)……GND - 0.3V to V_{DD} + 0.3V
NMOS Output Voltage (V_{RESET}, V_{ANDOUT})…....GND - 0.3V to +6.0V
Lead Temperature (soldering, 10sec.)..... 260°C
Storage Temperature (Ts).....-55°C to +150°C
ESD Rating (Human Body Model)[3] 2kV
ESD Rating (Machine Model)……..200V

Operating Ratings [2]

Supply Voltage (V_{DD})..... +1.5V to +5.5V
Input Voltage ($V_{/MR1}$, $V_{/MR2}$)……..……0V to V_{DD}
NMOS Output Voltage (V_{RESET}, V_{ANDOUT})…….0V to +5.5V
Junction Temperature (T_J) .....–40°C to +85°C
Package Thermal Resistance
6-Bump, 0.4mm Pitch WLCSP (θ_{JA}).....125°C/W

Electrical Characteristics [4]

For typical values, V_{DD} = 3.3V, /MR1 = /MR2 = Open, T_J = 25°C, **bold** values indicate –40°C ≤ T_J ≤ +85°C; unless noted.

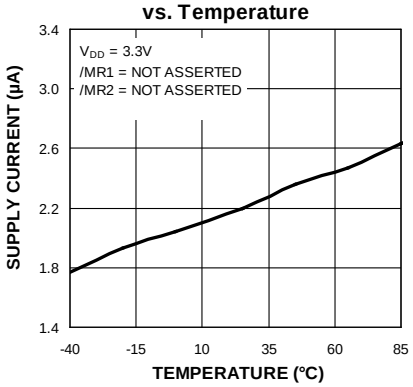
Parameter	Conditions	Min.	Typ.	Max.	Units
Power Supply Input					
Supply Voltage (V_{DD})	Reset Output Valid	**1.5**		**5.5**	V
Supply Current (I_{DD})	V_{DD} = 3.3V, /MR1 = /MR2 = VDD		2.2	**4.0**	µA
	V_{DD} = 5.0V, /MR1 = /MR2 = VDD		3.2	**5.0**	
	V_{DD} = 3.3V, /MR1 = /MR2 = GND		120		
Reset Time					
Setup Period (t_{SETUP})	Ordering Option: C	**5.4**	6	**6.6**	s
	Ordering Option: D	**7.2**	8	**8.8**	
	Ordering Option: E	**9.0**	10	**11**	
	Ordering Option: F	**10.8**	12	**13.2**	
Reset Timeout Period (t_{RESET})	Ordering Option: L	**0.4**	0.5	**0.6**	s
	Ordering Option: M	**0.9**	1	**1.1**	
	Ordering Option: R	**1.8**	2	**2.2**	
ANDOUT Debounce Time (t_{DB})	$V_{/MR1,2}$ < (V_{IL} – 100mV)	**1**	1.5	**2**	ms
Output Low Voltage (V_{OL})	V_{DD} = 4.5V, I_{SINK} = 1.6mA			**0.3**	V
	V_{DD} = 3.3V, I_{SINK} = 1.2mA			**0.3**	
	V_{DD} = 1.5V, I_{SINK} = 0.5mA			**0.3**	
Open-Drain Leakage Current ($I_{LEAKAGE}$)	RESET, ANDOUT Inactive V_{RESET}, V_{ANDOUT} = 5.5V			**300**	nA
/MR1, /MR2 Input					
Input High Voltage (V_{IH})		**1.2**			V
Input Low Voltage (V_{IL})				**0.4**	V
Internal Pull-Up Resistance (R_{PU})	For /MR1, /MR2	**55**	65	**75**	kΩ

Notes:

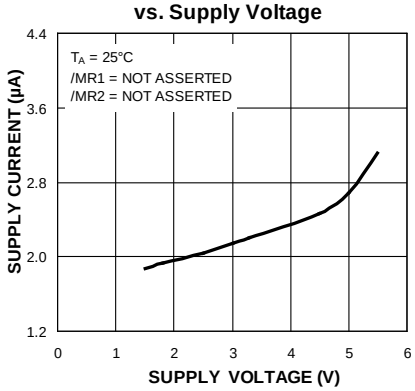
1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5kΩ in series with 100pF.
4. Specification for packaged product only.

Typical Characteristics

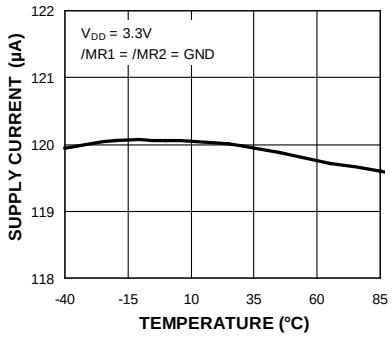
V_{DD} Supply Current vs. Temperature



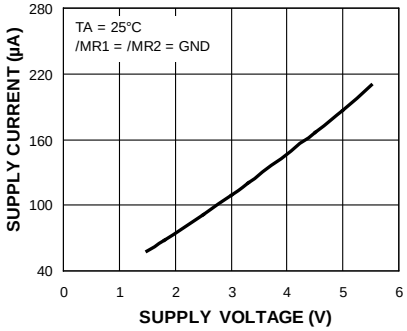
V_{DD} Supply Current vs. Supply Voltage



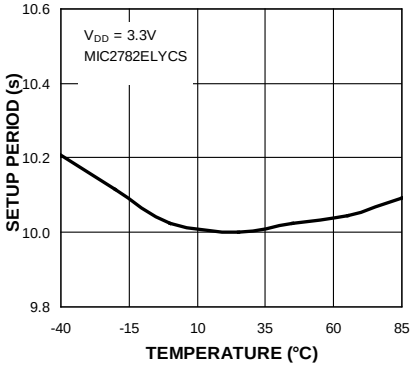
Supply Current for /MR1 and /MR2 Inputs Low vs. Temperature



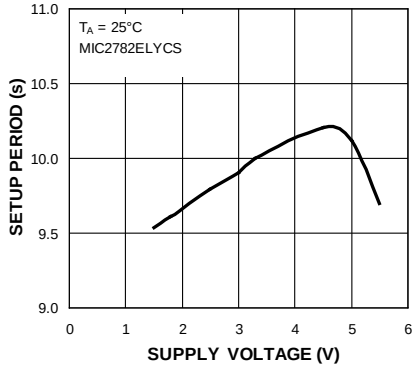
Supply Current for /MR1 and /MR2 Inputs Low vs. Supply Voltage



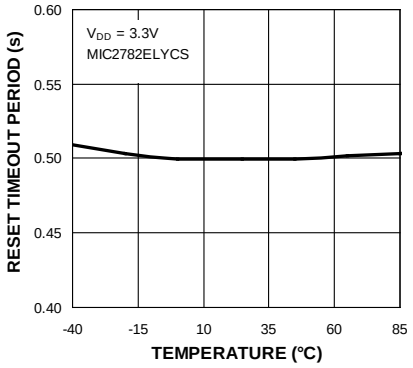
Setup Period vs. Temperature



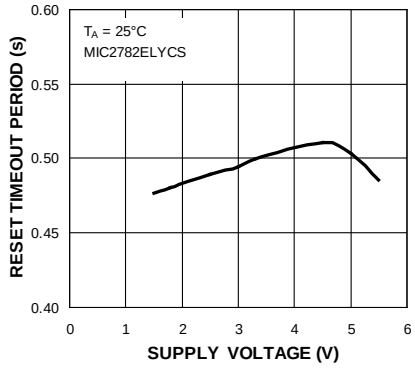
Setup Period vs. Supply Voltage



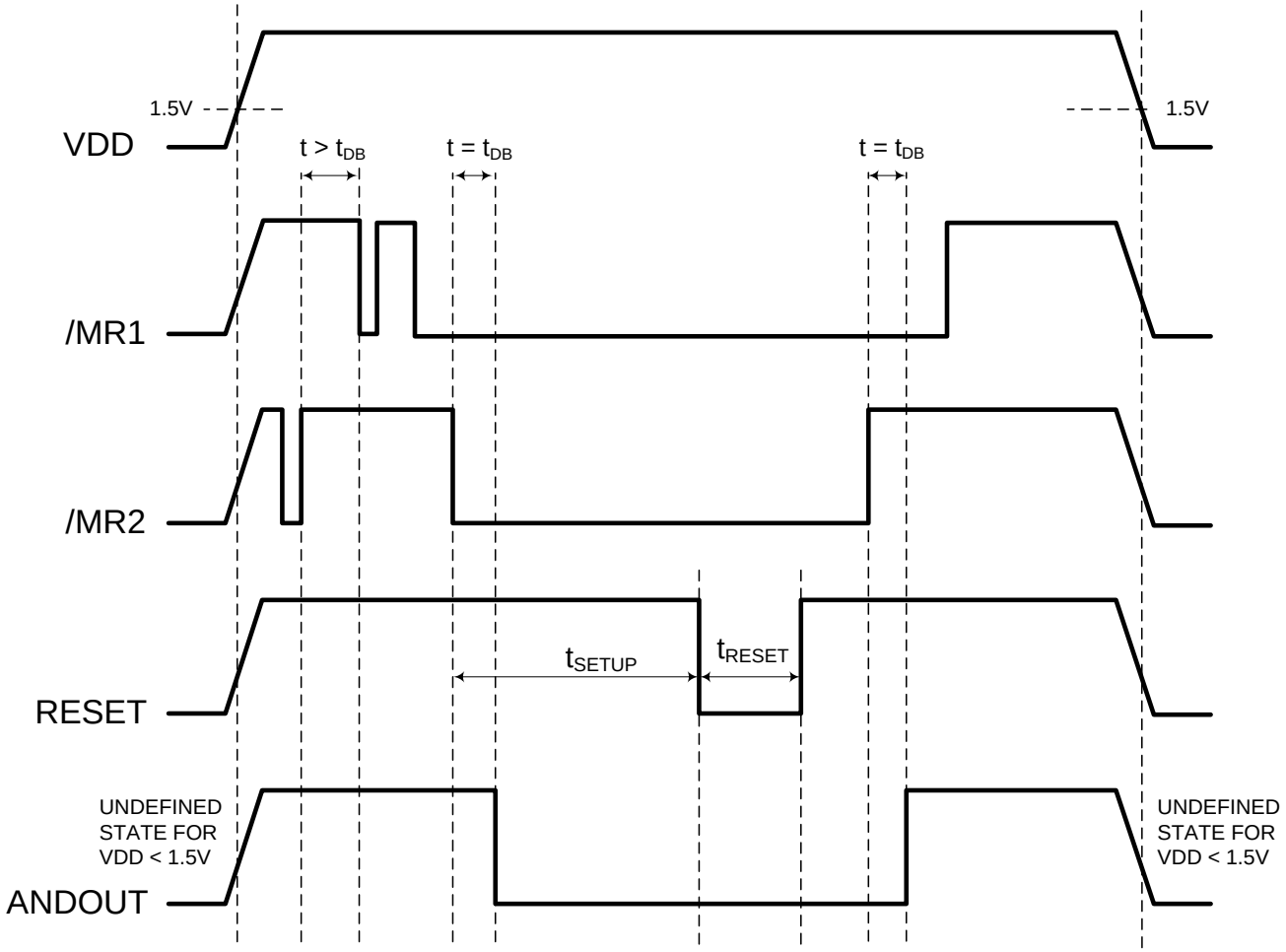
Reset Timeout Period vs. Temperature



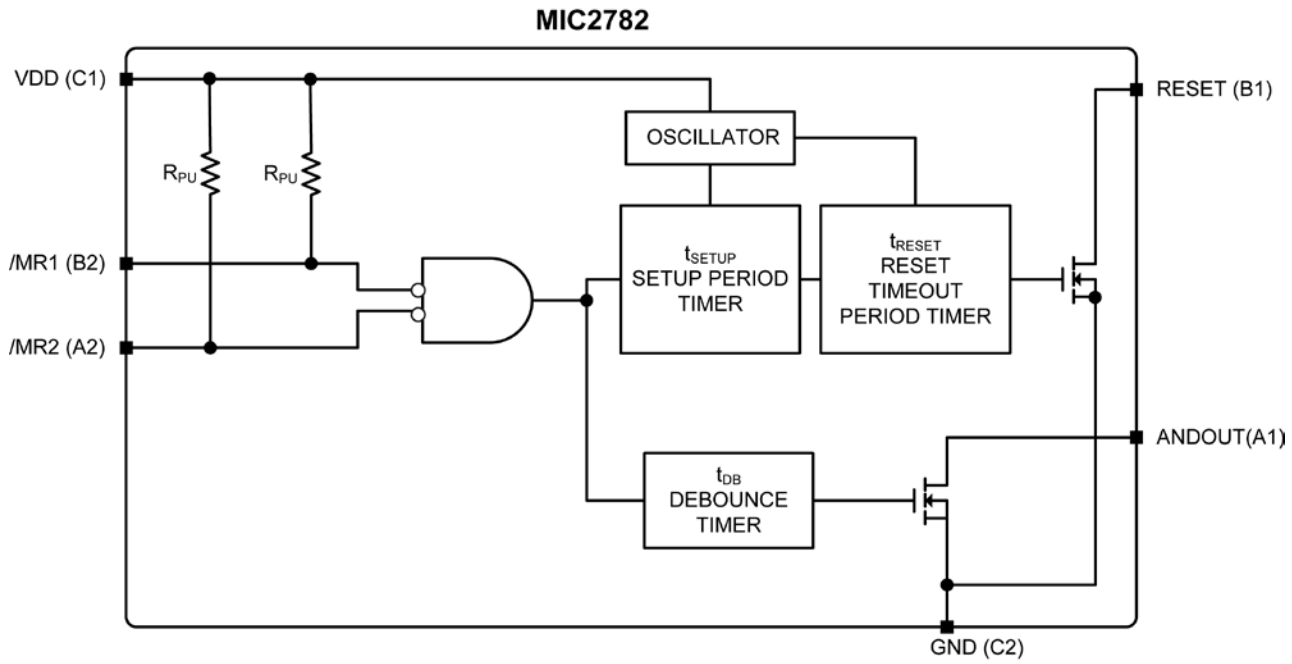
Reset Timeout Period vs. Supply Voltage



Timing Diagram



Functional Diagram



Functional Description

Design and Product Advantages

The MIC2782 is a dual push-button input reset IC with extended setup delay times. It is used for generating a hard reset for microcontrollers, PMICs or load disconnect switches. The dual manual reset inputs and long setup delay times help protect against accidental system resets. The fixed Reset Timeout period allows for more predictable phone or Tablet operation during hardware resets. It is used in applications such as smart phones, tablets, personal navigation devices, MP3 players and Set-Top Boxes (STB).

General Functionality

As shown in Figure 1, if both /MR1 and /MR2 are asserted low for longer than the Setup Period (t_{SETUP}), the RESET output will be asserted (logic-level low) for a Reset Timeout Period (t_{RESET}). During the Setup Period, if either of the /MR1 or /MR2 inputs are de-asserted high, then the Setup Period timer will be reset. To assert the RESET output low again, both the /MR1 and /MR2 inputs will have to be asserted low together for the full duration of the Setup period.

If both /MR1 and /MR2 are asserted low for longer than the Debounce Time (t_{DB}), then the ANDOUT output will be asserted, (logic-level low). ANDOUT will remain asserted low as long as both the /MR1 and /MR2 inputs are asserted low. If either the /MR1 or /MR2 are de-asserted for longer that the Debounce Time (t_{DB}), then the ANDOUT output will de-assert high.

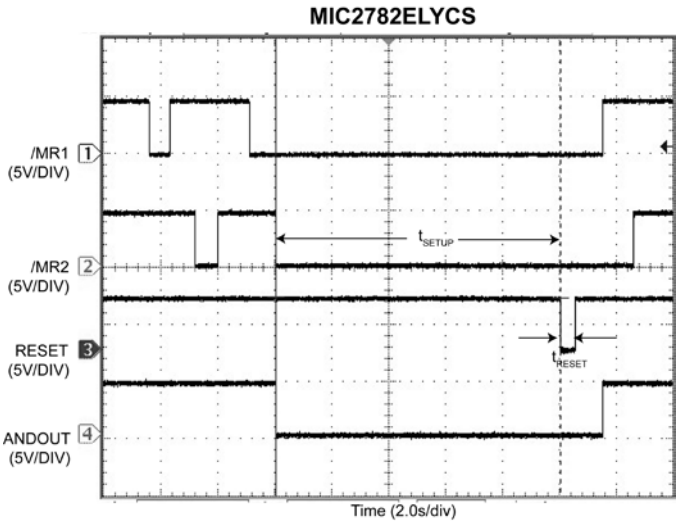


Figure 1. Manual Reset Function

Keeping both manual reset inputs low for a longer time does not generate additional RESET output pulses. De-asserting either manual reset input during the RESET pulse duration, will not reset the Setup Timer. After the RESET pin has de-asserted high, both the manual reset inputs must be held high for more than a Debounce Time to reset the Setup Timer.

ANDOUT Debounce Time is a de-glitch time, typically 1.5ms, that senses the asserting of both manual reset inputs low together. A de-glitch time is needed if the manual reset inputs come from noisy push-button sources. If either manual reset inputs are asserted (or de-asserted) for less than a Debounce Time, the ANDOUT output will not respond.

Dual Manual Reset Inputs (/MR1, /MR2)

The /MR1, /MR2 are active-low manual inputs that have integrated 65kΩ pull-up resistors to the VDD power supply. If both inputs are asserted (logic-level low) for a Setup Period (t_{SETUP}), only one reset pulse, of width t_{RESET}, is generated. The behavior of the RESET and ANDOUT outputs is independent of the order in which the /MR1, /MR2 inputs are driven low. The MIC2782 consumes only 2µA when /MR1 and /MR2 manual inputs are de-asserted (logic-level high) together. Current consumption is typically 120µA when both manual inputs are asserted low together and 55µA when only one of the manual inputs is asserted low while the other manual input is de-asserted high.

Outputs (RESET and ANDOUT)

The RESET and ANDOUT outputs are simple open-drain N-channel MOSFET structures that require a pull-up resistor. For most applications, the pull-up voltage will be the same as the power supply that supplies V_{DD} to the MIC2782. As shown in Figure 2, it is possible to tie this resistor to some other voltage, other than V_{DD}, thus enabling level-shifting of the RESET or ANDOUT outputs. The pull-up voltage must be limited to 5.5V to avoid damaging the MIC2782. The pull-up resistor must be small enough to supply current to the inputs and leakage paths that are driven by the RESET or ANDOUT outputs. A recommended value is 100kΩ.

Since the RESET and ANDOUT outputs are open-drain, several reset sources can be wire-ORed, in parallel, to allow resets from multiple sources.

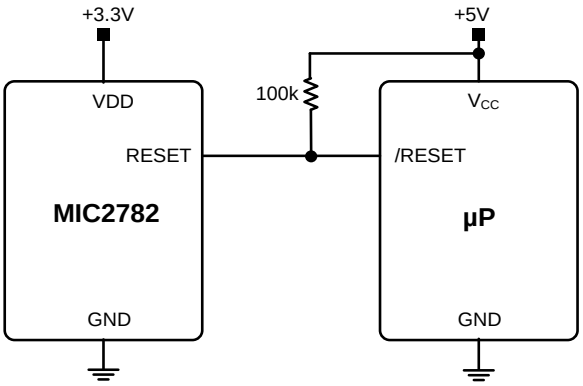


Figure 2. MIC2782 Used in Multiple Supply System

Bypass Capacitor from VDD to GND

A 0.1µF input bypass capacitor must be placed from VDD (Pin C1) to GND (Pin C2).

Typical Applications

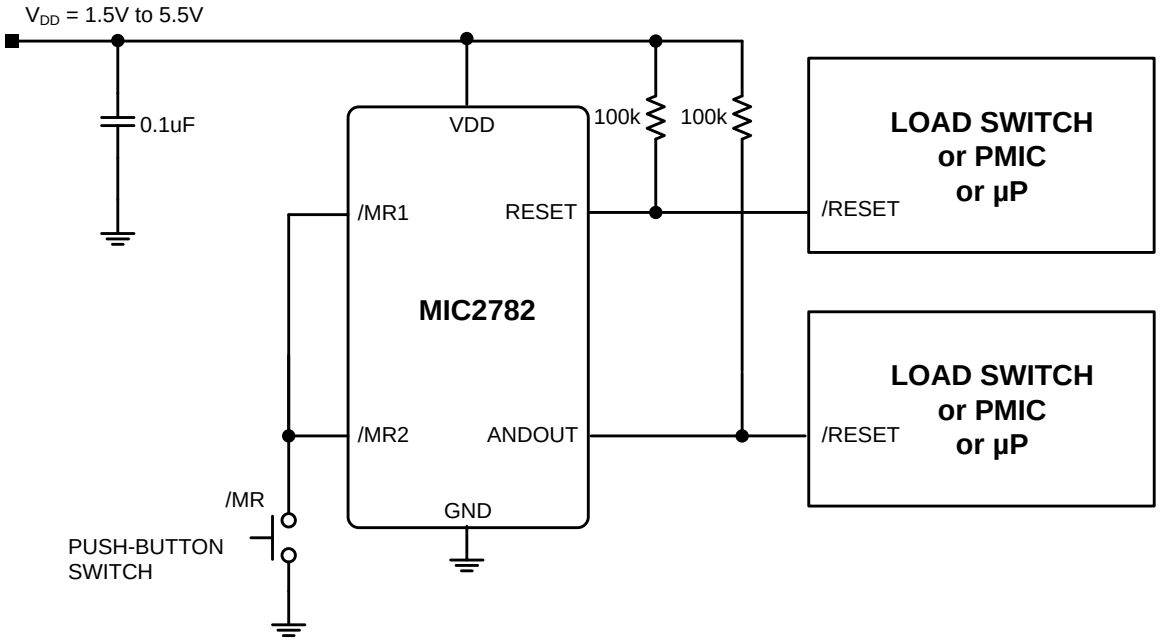


Figure 3. Single Button application for MIC2782 used for Microcontroller Reset

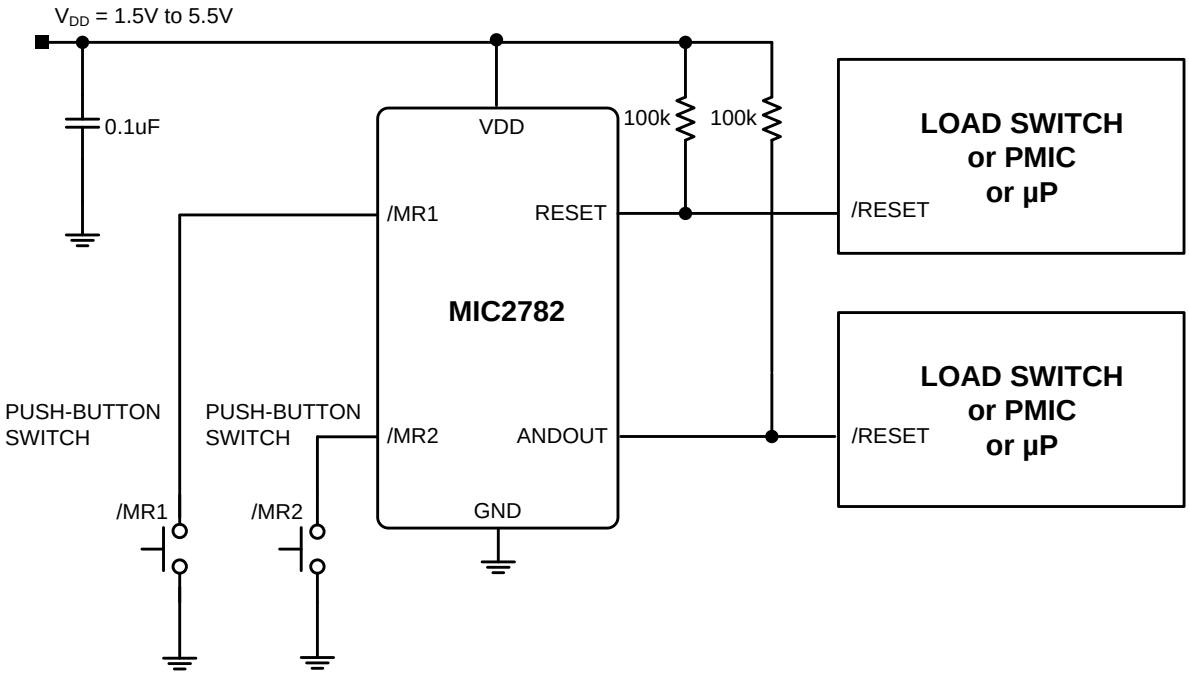
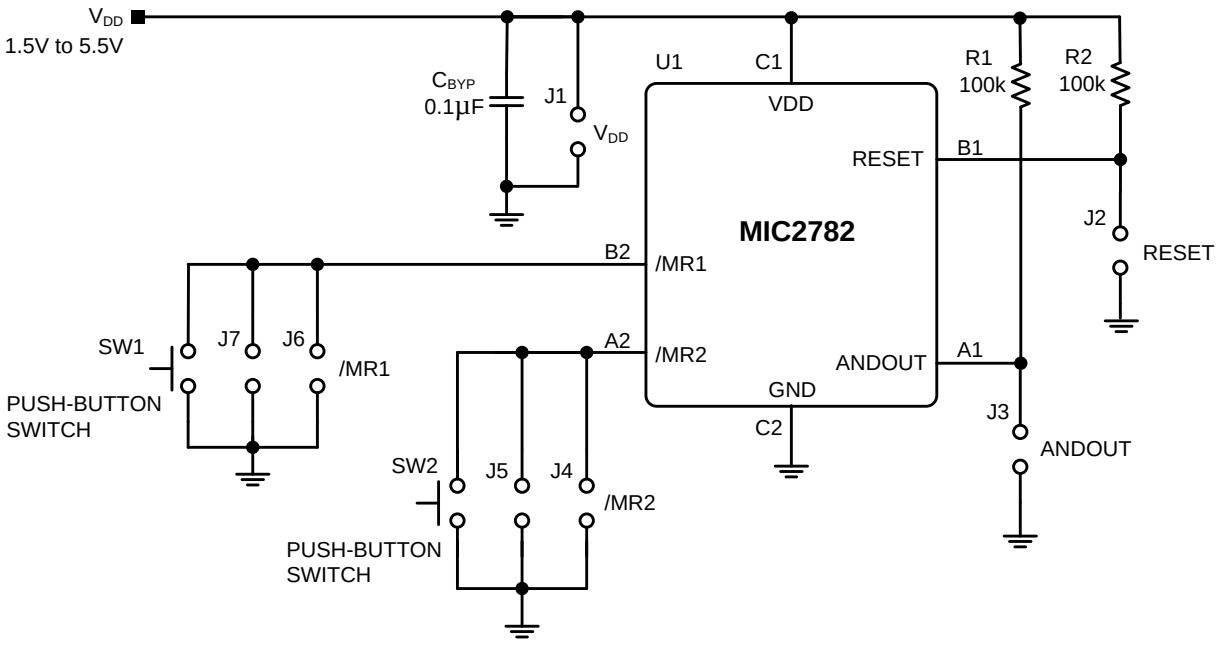


Figure 4. Dual Button application for MIC2782 used for Microcontroller Reset

Evaluation Board Schematic



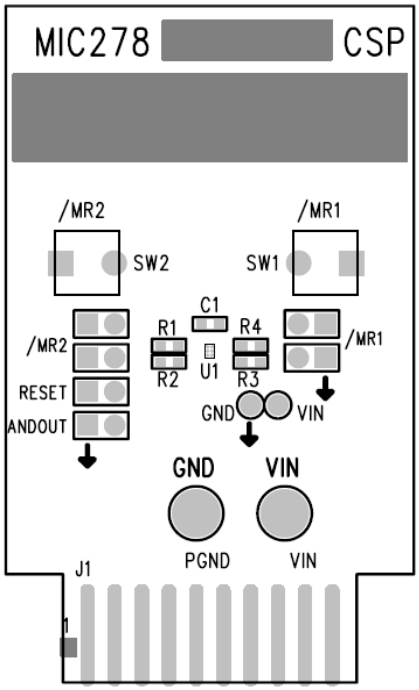
Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1	GRM188R71C104KA01D[1]	Murata	0.1µF, 16V capacitor, X7R, 0603	1
R1, R2	CRCW0603100KJNEA[2]	Vishay	100k, 5% resistor, 0603	2
U1	**MIC2782ELYCS[3]**	**Micrel, Inc.**	**Dual-Input Push Button Reset IC**	**1**

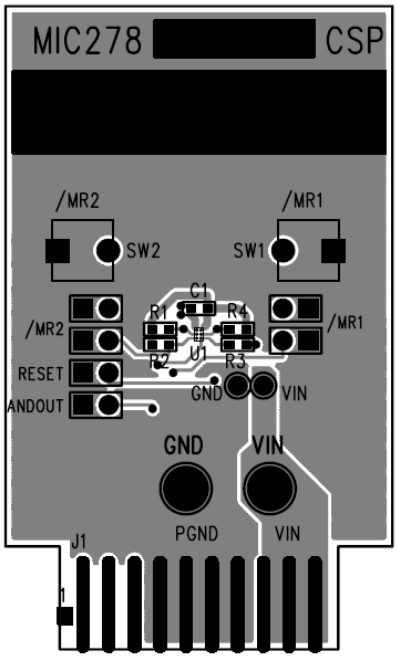
Notes:

1. Murata Tel: www.murata.com.
2. Vishay Tel: www.vishay.com.
3. **Micrel, Inc.: www.micrel.com.**

PCB Layout Recommendations

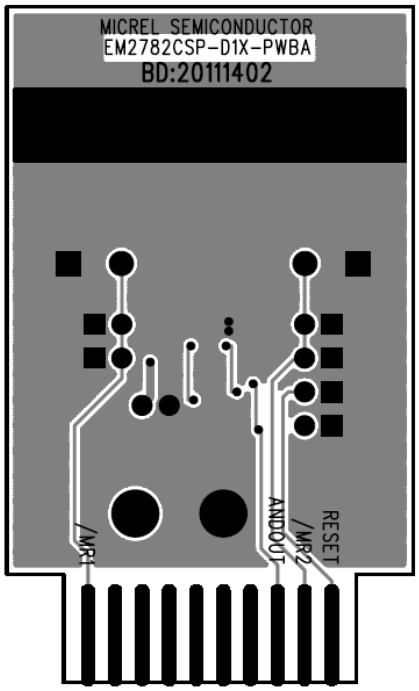


Top Silkscreen

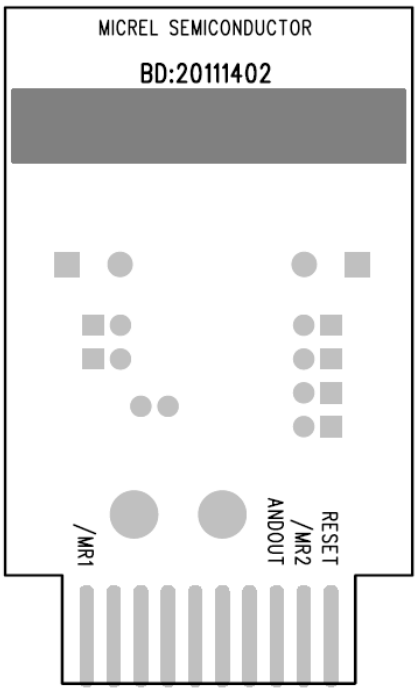


Copper Layer 1 (Top Layer)

PCB Layout Recommendations (Continued)

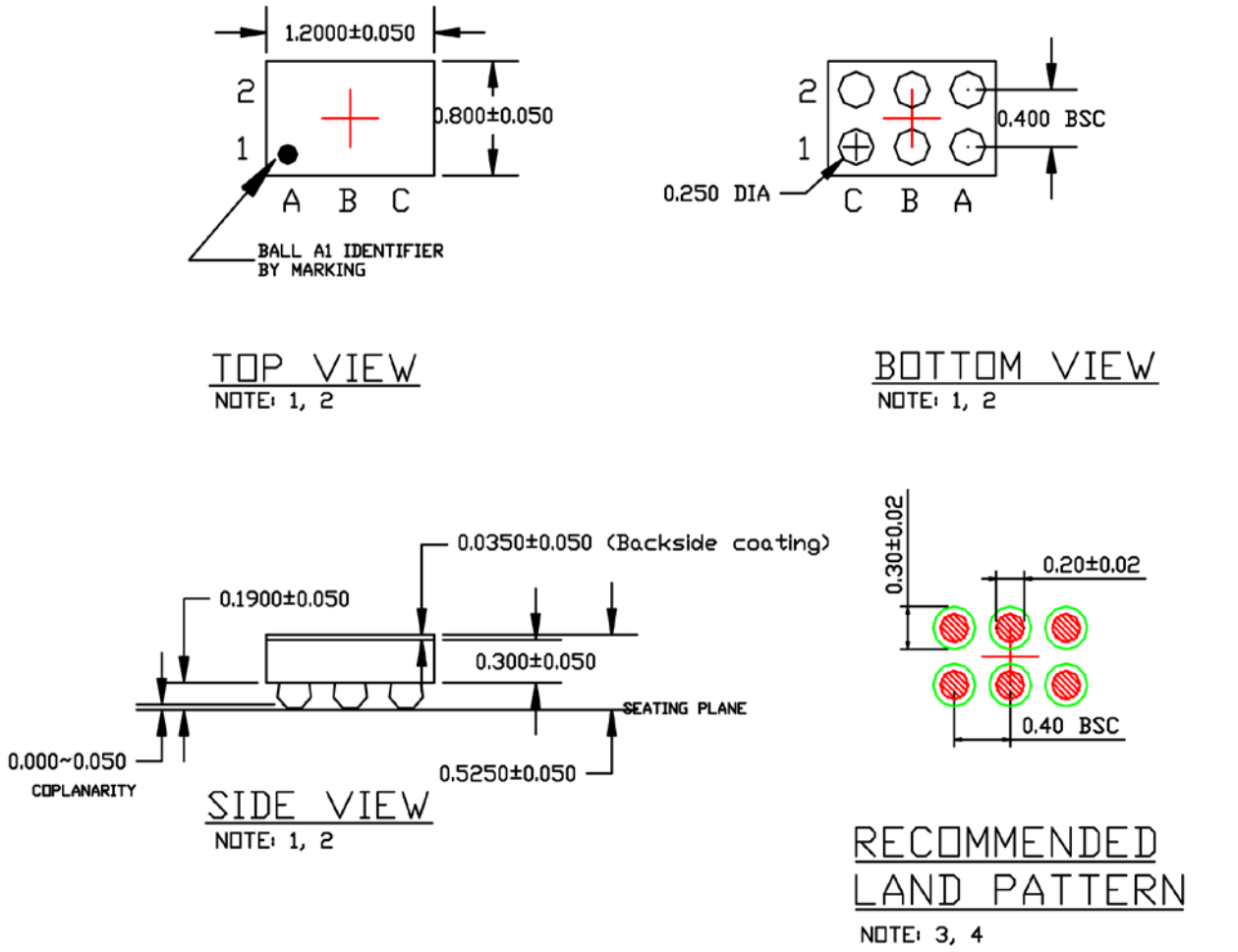


Copper Layer 2 (Bottom Layer)



Bottom Silkscreen

Package Information



NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. NON-SOLDERMASK DEFINED PADS ARE RECOMMENDED FOR BOARD LAYOUT
4. SHADED RED CIRCLES REPRESENT CONTACT PAD AREA. GREEN CIRCLES REPRESENT SOLDER MASK OPENING

6-Bump, 0.4mm Pitch 0.8mm × 1.2mm WLCSP (CS)

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http://www.micrel.com