

# MB89650AR Series

(Continued)

- 8-bit PWM timers: 2 channels (A maximum of 4 channels can be used for output.)
- 8/16-bit timer/counter: 4 channels (16 bits × 2 channels)
- 8-bit serial I/O: 1 channel
- 8-bit A/D converter: 8 channels
- External interrupt 1  
Four independent channels with edge detection function
- External interrupt 2 (wake-up function)  
Twelve "L" level-interrupt channels
- Watch prescaler
- LCD controller/driver: 16 to 32 segments × 2 to 4 commons
- Power-on reset function
- Low-power consumption modes (subclock mode, watch mode, sleep mode, and stop mode)
- LQFP-100 and QFP-100 packages

## ■ PRODUCT LINEUP

<div>Part number</div> <div>Parameter</div>	MB89653AR	MB89655AR	MB89656AR	MB89657AR	MB89P657A	MB89PV650A
Classification	Mass production products (mask ROM products)				One-time PROM product	Piggyback/ evaluation product (for evaluation and development)
ROM size	8 K × 8 bits (internal mask ROM)	16 K × 8 bits (internal mask ROM)	24 K × 8 bits (internal mask ROM)	32 K × 8 bits (internal mask ROM)	32 K × 8 bits (internal PROM, programming with general- purpose EPROM programmer)	32 K × 8 bits (external ROM)
RAM size	256 × 8 bits	512 × 8 bits	768 × 8 bits	1 K × 8 bits		
LCD display RAM	16 × 8 bits					
CPU functions	Number of instructions : 136 Instruction bit length : 8 bits Instruction length : 1 to 3 bytes Data bit length : 1, 8, 16 bits Minimum execution time : 0.4 μs/10 MHz to 6.4 μs/10 MHz, 61.0 μs/32.768 kHz Interrupt processing time : 3.6 μs/10 MHz to 57.6 μs/10 MHz, 549.3 μs/32.768 kHz					
Ports	Input ports : 8 (All also serve as peripherals.) Output ports : 8 (All also serve as peripherals.) I/O ports : 48 (All also serve as peripherals.) Total : 64					
8-bit timer 1, 8-bit timer 2	8-bit timer operation (toggled output capable, operating clock cycle: 0.8 to 12.8 μs) 16-bit timer operation (toggled output capable, operating clock cycle: 0.8 to 12.8 μs) 2 output channels are enabled when operating as an 8-bit timer.					

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# MB89650AR Series

(Continued)

Part number Parameter	MB89653AR	MB89655AR	MB89656AR	MB89657AR	MB89P657A	MB89PV650A
8-bit timer 3, 8-bit timer 4	8-bit timer operation (toggled output capable, operating clock cycle: 0.8 to 12.8 $\mu$ s) 16-bit timer operation (toggled output capable, operating clock cycle: 0.8 to 12.8 $\mu$ s) 2 output channels are enabled when operating as an 8-bit timer.					
Clock timer	21 bits $\times$ 1 (in main clock mode)/15 bits $\times$ 1 (at 32.768 kHz)					
8-bit PWM timer 1, 8-bit PWM timer 2	8-bit reload timer operation (toggled output capable, operating clock cycle: 0.4 $\mu$ s to 3.3 ms) 8-bit resolution PWM operation (conversion cycle: 102 $\mu$ s to 839 ms) Both 8-bit PWM timer 1 and 8-bit PWM timer 2 can output 2 channels.					
8-bit serial I/O	8 bits LSB first/MSB first selectability One clock selectable from four transfer clocks (one external shift clock, three internal shift clocks: 0.8 $\mu$ s, 3.2 $\mu$ s, 12.8 $\mu$ s)					
8-bit A/D converter	8-bit resolution $\times$ 8 channels A/D conversion mode (conversion time: 18 $\mu$ s) Sense mode (conversion time: 5 $\mu$ s) Continuous activation by an internal timer capable Reference voltage input					
External interrupt 1	4 independent channels (edge selection) Rising edge/falling edge selectability Used also for wake-up from stop/sleep mode. (Edge detection is also permitted in stop mode.)					
External interrupt 2 (wake-up function)	“L” level interrupt $\times$ 12 channels					
Standby mode	Subclock mode, sleep mode, watch mode, and stop mode					
Process	CMOS					
Operating voltage*	2.2 V to 6.0 V				2.7 V to 6.0 V	
EPROM for use	—					MBM27C256A- 20TVM

\* : Varies with conditions such as the operating frequency. (See section “■ Electrical Characteristics”.)  
In the case of the MB89PV650A, the voltage varies with the restrictions of the EPROM for use.

## ■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB89653AR MB89655AR MB89656AR MB89657AR MB89P657A	MB89PV650A
FPT-100P-M05	○	×
FPT-100P-M06	○	×
MQP-100C-P02	×	○

○ : Available    × : Not available

Note : For more information about each package, see section “■ Package Dimensions”.

# MB89650AR Series

## ■ DIFFERENCES AMONG PRODUCTS

### 1. Memory Size

Before evaluating using the piggyback product, verify its differences from the product that will actually be used. Take particular care on the following points:

- On the MB89653AR, the upper half of the register bank cannot be used.
- On the MB89P657A, the program area starts from address 8006<sub>H</sub> but on the MB89PV650A and MB89657AR starts from 8000<sub>H</sub>.

(On the MB89P657A, addresses 8000<sub>H</sub> to 8005<sub>H</sub> comprise the option setting area, option settings can be read by reading these addresses. On the MB89PV650A and MB89657A, addresses 8000<sub>H</sub> to 8005<sub>H</sub> could also be used as a program ROM. However, do not use these addresses in order to maintain compatibility of the MB89P657A.)

- The stack area, etc., is set at the upper limit of the RAM.

### 2. Current Consumption

- In the case of the MB89PV650A, add the current consumed by the EPROM which is connected to the top socket.
- When operated at low speed, the product with an OTPROM (one-time PROM) or an EPROM will consume more current than the product with a mask ROM.

However, the current consumption in sleep/stop modes is the same. (For more information, see sections “■ Electrical Characteristics” and “■ Example Characteristics.”)

### 3. Mask Options

Functions that can be selected as options and how to designate these options vary by the product.

Before using options check section “■ Mask Options.”

Take particular care on the following points:

- A pull-up resistor cannot be set for P70 to P75 on the MB89P657A. On this product, a pull-up resistor must be selected in a group of four bits for P14 to P17, P40 to P43, and P44 to P47.
- A pull-up resistor is not selectable for P30 to P37 and P40 to P47 if they are used as LCD pins.
- Options are fixed on the MB89PV650A.

### 4. Differences between the MB89650A and MB89650AR Series

- Electrical specifications/electrical characteristics

Electrical specifications of the MB89650AR series are the same with that of the MB89650A series.

Electrical characteristics of both series are much the same.

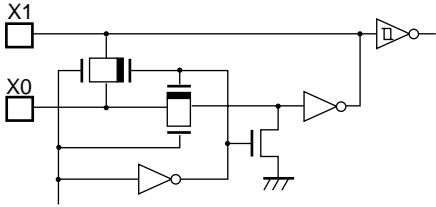
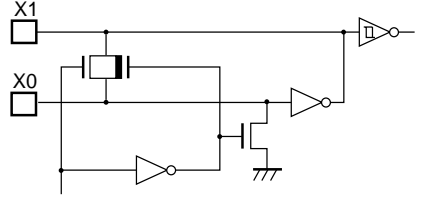
- Oscillation circuit type

In the MB89650A series, the circuit type of using an external clock differs from that of using a crystal or ceramic resonator as follows.

Circuit type of the MB89650AR series is a circuit type in using external clock even when crystal or ceramic resonator is selected.

- Memory access area and other specifications of both the MB89650A and MB89650AR series are the same.

## • I/O circuit type

Type	Circuit	Remarks
A	 <p>Standby control signal</p>	<ul style="list-style-type: none"> <li>Crystal or ceramic oscillation type (main clock) MB89PV650A and MB89P657A, external clock input selection versions of MB89653A/655A/656A/657A At an oscillation feedback resistor of approximately 1 M<math>\Omega</math>/5.0 V</li> <li>MB89653AR/655AR/656AR/657AR</li> </ul>
	 <p>Standby control signal</p>	<ul style="list-style-type: none"> <li>Crystal or ceramic oscillation type (main clock) Crystal or ceramic oscillation selection versions of MB89653A/655A/656A/657A At an oscillation feedback resistor of approximately 1 M<math>\Omega</math>/5.0 V</li> </ul>

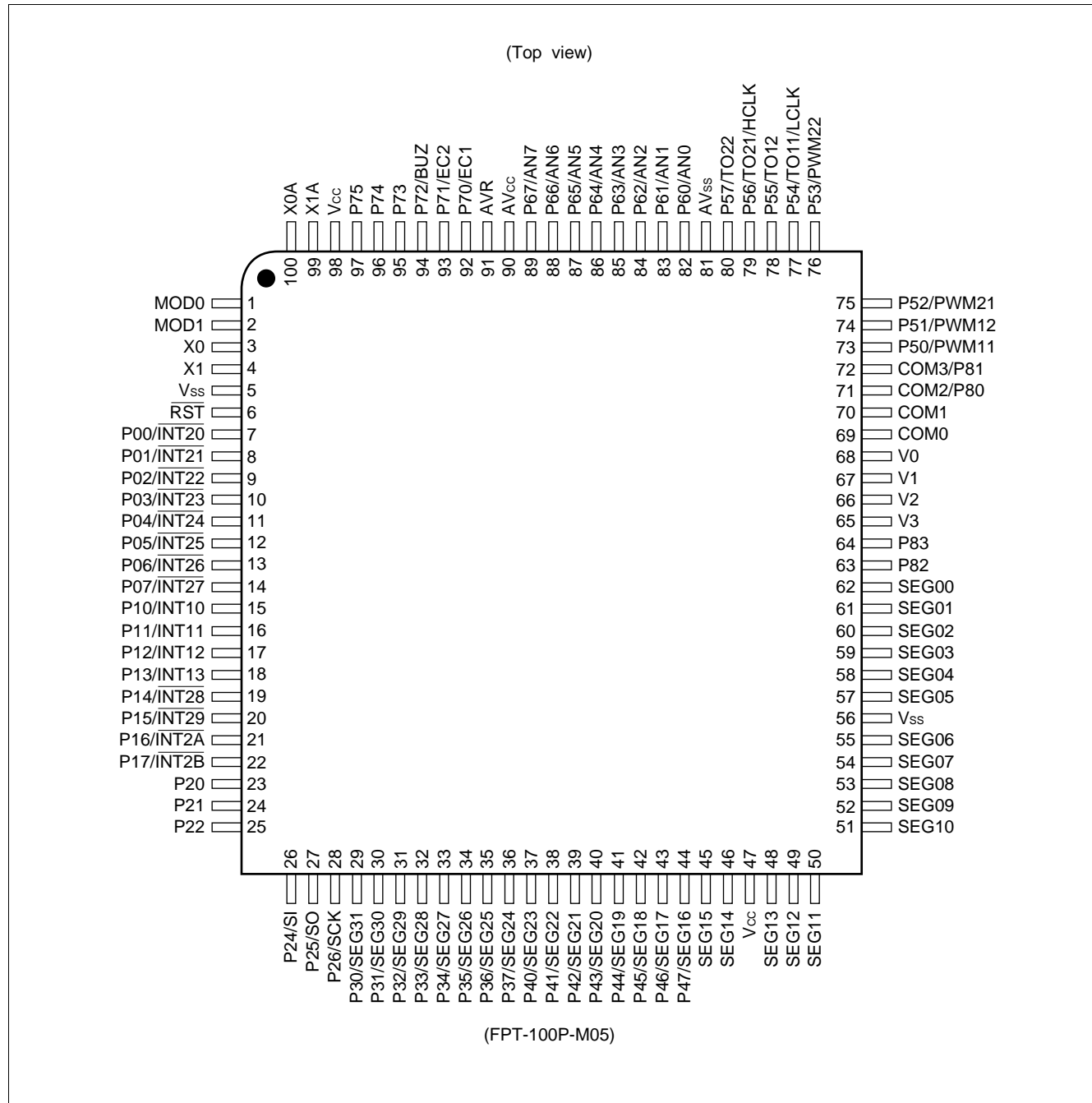
## ■ CORRESPONDENCE BETWEEN THE MB89650A AND MB89650AR SERIES

- The MB89650AR series is the reduction version of the MB89650A series.
- The MB89650A and MB89650AR series consist of the following products:

MB89650A series	MB89653A	MB89655A	MB89656A	MB89657A	MB89P657A	MB89PV650A
MB89650AR series	MB89653AR	MB89655AR	MB89656AR	MB89657AR		

# MB89650AR Series

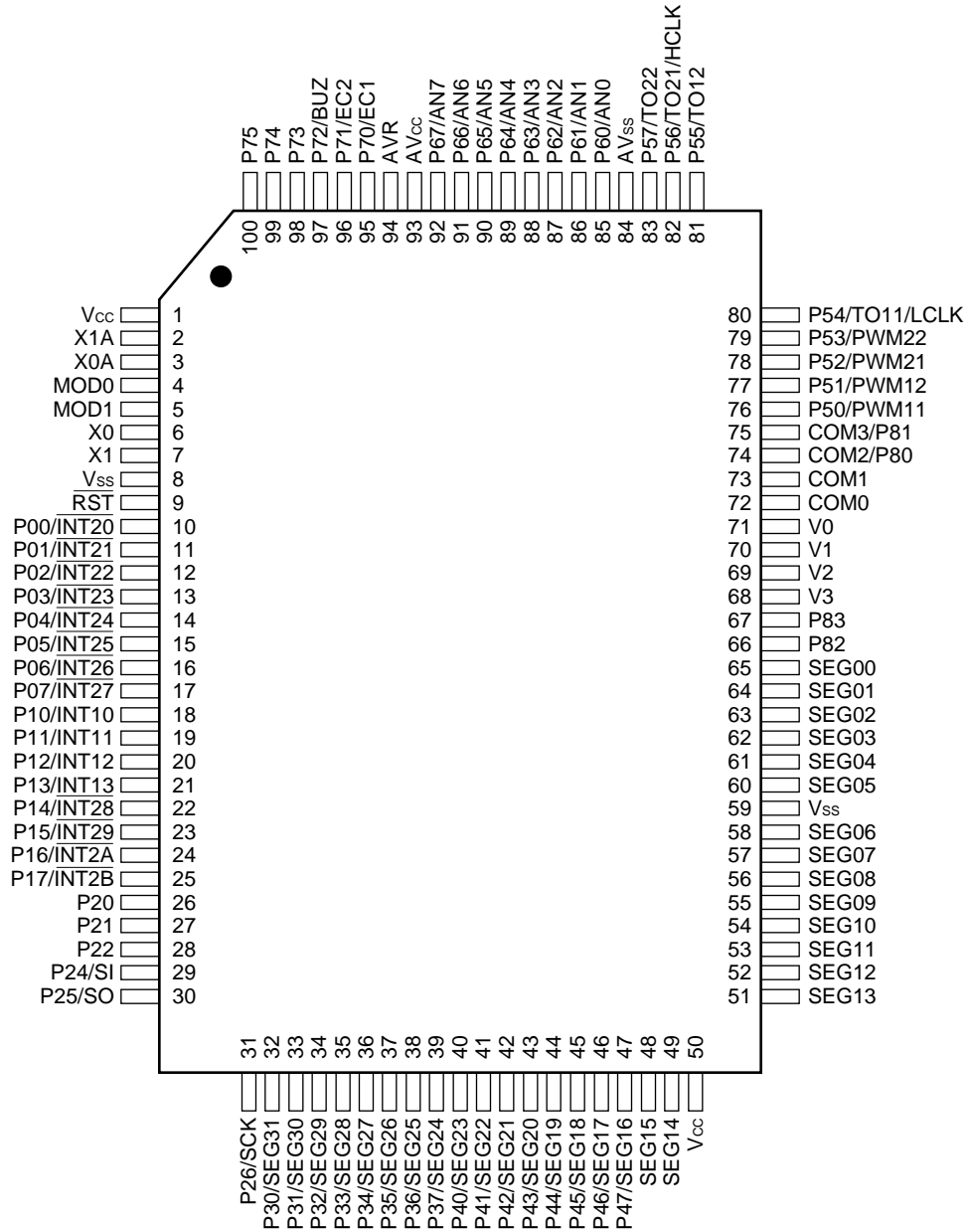
## PIN ASSIGNMENT



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# MB89650AR Series

(Top view)

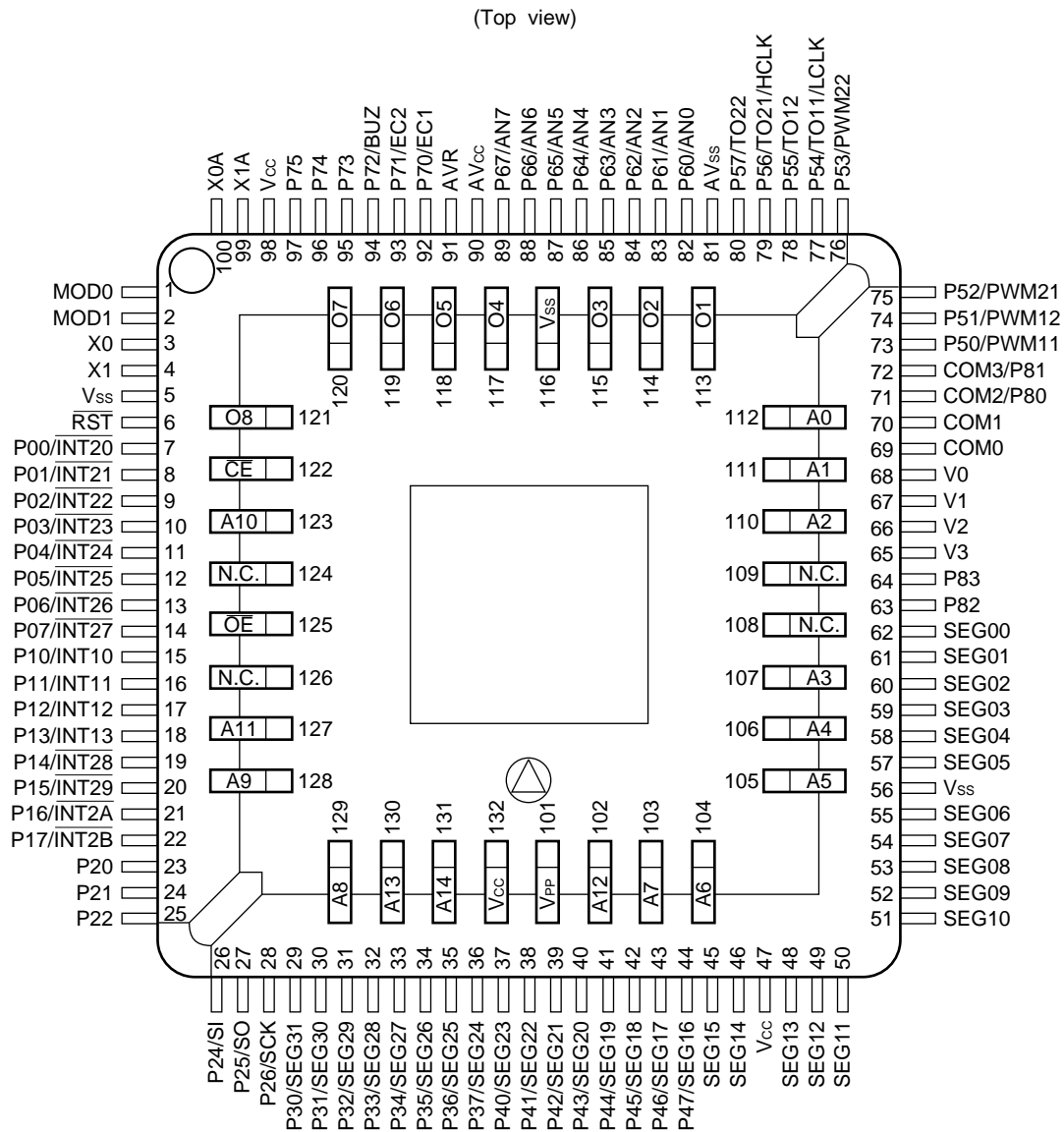


(FPT-100P-M06)

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# MB89650AR Series

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(MQP-100C-P02)

• Pin assignment on package top (MB89PV650A only)

Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name
101	V <sub>PP</sub>	109	N.C.	117	O4	125	$\overline{OE}$
102	A12	110	A2	118	O5	126	N.C.
103	A7	111	A1	119	O6	127	A11
104	A6	112	A0	120	O7	128	A9
105	A5	113	O1	121	O8	129	A8
106	A4	114	O2	122	$\overline{CE}$	130	A13
107	A3	115	O3	123	A10	131	A14
108	N.C.	116	V <sub>SS</sub>	124	N.C.	132	V <sub>CC</sub>

N.C.:Internally connected. Do not use.

## ■ PIN DESCRIPTION

Pin no.		Pin name	Circuit type	Function
QFP*1	MQFP*2 LQFP*3			
4	1	MOD0	J	Operating mode selection pins Connect to V <sub>SS</sub> (GND) when using.
5	2	MOD1		
6	3	X0	A	Main clock crystal oscillator pins (Max 10 MHz)
7	4	X1		
8	5	V <sub>SS</sub>	—	Power supply (GND) pin
9	6	RST	J	Reset input pin
10 to 17	7 to 14	P00/ $\overline{\text{INT20}}$ to P07/ $\overline{\text{INT27}}$	F	General-purpose I/O ports Also serve as an external interrupt 2 input (wake-up function). External interrupt 2 input ( $\overline{\text{INT20}}$ to $\overline{\text{INT27}}$ ) is hysteresis input while port input (P00 to P07) is CMOS input.
18 to 21	15 to 18	P10/INT10 to P13/INT13	F	General-purpose I/O ports Also serve as an external interrupt 1 input. External interrupt 1 input (INT10 to INT13) is hysteresis input while port input (P10 to P13) is CMOS input.
22 to 25	19 to 22	P14/ $\overline{\text{INT28}}$ to P15/ $\overline{\text{INT2B}}$	F	General-purpose I/O ports Also serve as an external interrupt 2 input (wake-up function). External interrupt 2 input ( $\overline{\text{INT28}}$ to $\overline{\text{INT2B}}$ ) is hysteresis input while port input (P14 to P17) is CMOS input.
26 to 28	23 to 25	P20 to P22	C	General-purpose I/O ports
29, 30, 31	26, 27, 28	P24/SI, P25/SO, P26/SCK	F	General-purpose I/O ports The output type can be switched between N-ch open-drain and CMOS. These ports also serve as an 8-bit serial I/O. The P26/SCK pin is a CMOS input type when it functions as the port input (P26) while the pin is a hysteresis input type when it functions as the serial clock input (SCK).
32 to 47	29 to 44	P36/SEG31 to P47/SEG26	H	General-purpose I/O ports Also serve as an LCD controller/driver segment output.
48, 49	45, 46	SEG15, SEG14	I	LCD controller/driver segment output pins

\*1 : FPT-100P-M06

\*2 : FPT-100P-M05

\*3 : MQP-100C-P02

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# MB89650AR Series

(Continued)

Pin no.		Pin name	Circuit type	Function
QFP*1	MQFP*2 LQFP*3			
50	47	V <sub>CC</sub>	—	Power supply pin
51 to 58	48 to 55	SEG13 to SEG06	I	LCD controller/driver segment output pins
59	56	V <sub>SS</sub>	—	Power supply (GND) pin
60 to 65	57 to 62	SEG05 to SEG00	I	LCD controller/driver segment output pins
66, 67	63, 64	P82, P83	C	General-purpose I/O ports
68 to 71	65 to 68	V3 to V0	—	LCD driving power supply pins
72, 73	69, 70	COM0, COM1	I	LCD controller/driver common output pins
74, 75	71, 72	COM2/P80, COM3/P81	H	General-purpose I/O ports Also serve as an LCD controller/driver common output.
76 to 79	73 to 76	P50/PWM11 to P53/PWM22	G	General-purpose output ports Also serve as an 8-bit PWM timer.
80, 81, 82, 83	77, 78, 79, 80	P54/TO11/LCLK, P55/TO12, P56/TO21/HCLK, P57/TO22	G	General-purpose output ports Also serve as an 8/16-bit timer. P54 and P56 also serve as a 32.768 kHz oscillation output/10 MHz divide-by-two output.
84	81	AV <sub>SS</sub>	—	A/D converter power supply (GND) pin
85 to 92	82 to 89	P60/AN0 to P67/AN7	E	General-purpose input ports Also serve as an analog input.
93	90	AV <sub>CC</sub>	—	A/D converter power supply pin
94	91	AVR	—	A/D converter reference voltage input pin
95, 96	92, 93	P70/EC1, P71/EC2	K	General-purpose N-ch open-drain I/O ports Also serve as an 8/16-bit timer to input hysteresis.
97, 98 to 100	94, 95 to 97	P72/BUZ, P73 to P75	D	General-purpose N-ch open-drain I/O ports P72 also serves as a buzzer output.
1	98	V <sub>CC</sub>	—	Power supply pin
2	99	X1A	B	Subclock crystal oscillator pins (32.768 kHz)
3	100	X0A		

\*1 : FPT-100P-M06

\*2 : FPT-100P-M05

\*3 : MQP-100C-P02

# MB89650AR Series

• External EPROM pins (MB89PV650A only)

Pin no.	Pin name	I/O	Function
101	V <sub>PP</sub>	O	"H" level output pin
102 103 104 105 106 107 110 111 112	A12 A7 A6 A5 A4 A3 A2 A1 A0	O	Address output pins
113 114 115	O1 O2 O3	I	Data input pins
116	V <sub>SS</sub>	O	Power supply (GND) pin
117 118 119 120 121	O4 O5 O6 O7 O8	I	Data input pins
122	$\overline{\text{CE}}$	O	ROM chip enable pin Outputs "H" during standby.
123	A10	O	Address output pin
125	$\overline{\text{OE}}$	O	ROM output enable pin Outputs "L" at all times.
127 128 129	A11 A9 A8	O	Address output pins
130	A13	O	Address output pin
131	A14	O	Address output pin
132	V <sub>CC</sub>	O	EPROM power supply pin
108 109 124 126	N.C.	—	Internally connected pins Be sure to leave them open.

# MB89650AR Series

### ■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A	<p>Standby control signal</p>	<ul style="list-style-type: none"> <li>Crystal or ceramic oscillation type (main clock)</li> <li>At an oscillation feedback resistor of approximately 1 MΩ/5.0 V</li> </ul>
B	<p>Standby control signal</p>	<ul style="list-style-type: none"> <li>Crystal or ceramic oscillation type (subclock)</li> <li>MB89PV650A, MB89P657A</li> <li>At an oscillation feedback resistor of approximately 4.5 MΩ/5.0 V</li> </ul>
	<p>Standby control signal</p>	<ul style="list-style-type: none"> <li>Crystal or ceramic oscillation type (subclock)</li> <li>MB89653AR/655AR/656AR/657AR</li> <li>At an oscillation feedback resistor of approximately 4.5 MΩ/5.0 V</li> </ul>
C		<ul style="list-style-type: none"> <li>CMOS I/O</li> <li>Pull-up resistor optional (except P82 and P83)</li> </ul>
D		<ul style="list-style-type: none"> <li>N-ch open-drain I/O</li> <li>CMOS input</li> <li>Pull-up resistor optional</li> </ul>
E		<ul style="list-style-type: none"> <li>A/D converter input</li> <li>CMOS input</li> <li>Pull-up resistor optional</li> </ul>

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Type	Circuit	Remarks
F		<ul style="list-style-type: none"> <li>CMOS I/O (when selected as general-purpose ports) P24 to P26 outputs can be switched between CMOS and N-ch open-drain.</li> <li>When toggled as hysteresis input peripherals. However, SI input excluded.</li> <li>Pull-up resistor optional</li> </ul>
G		<ul style="list-style-type: none"> <li>CMOS output</li> </ul>
H		<ul style="list-style-type: none"> <li>LCD controller/driver output</li> <li>CMOS I/O</li> <li>Pull-up resistor optional</li> </ul>
I		<ul style="list-style-type: none"> <li>LCD controller/driver output</li> </ul>
J		
K		<ul style="list-style-type: none"> <li>Hysteresis input</li> <li>N-ch open-drain output</li> <li>Pull-up resistor optional</li> </ul>

## ■ HANDLING DEVICES

### 1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than  $V_{CC}$  or lower than  $V_{SS}$  is applied to input and output pins other than medium- to high-voltage pins or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in section “■ Electrical Characteristics” is applied between  $V_{CC}$  and  $V_{SS}$ .

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog power supply ( $AV_{CC}$  and  $AVR$ ) and analog input from exceeding the digital power supply ( $V_{CC}$ ) when the analog system power supply is turned on and off.

### 2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

### 3. Treatment of Power Supply Pins on Microcontrollers with A/D and D/A Converters

Connect to be  $AV_{CC} = DAVC = V_{CC}$  and  $AV_{SS} = AVR = V_{SS}$  even if the A/D and D/A converters are not in use.

### 4. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

### 5. Power Supply Voltage Fluctuations

Although  $V_{CC}$  power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that  $V_{CC}$  ripple fluctuations (P-P value) will be less than 10% of the standard  $V_{CC}$  value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

### 6. Precautions when Using an External Clock

Even when an external clock is used, oscillation stabilization time is required for power-on reset (optional) and wake-up from stop mode.

## ■ PROGRAMMING TO THE EPROM ON THE MB89P657A

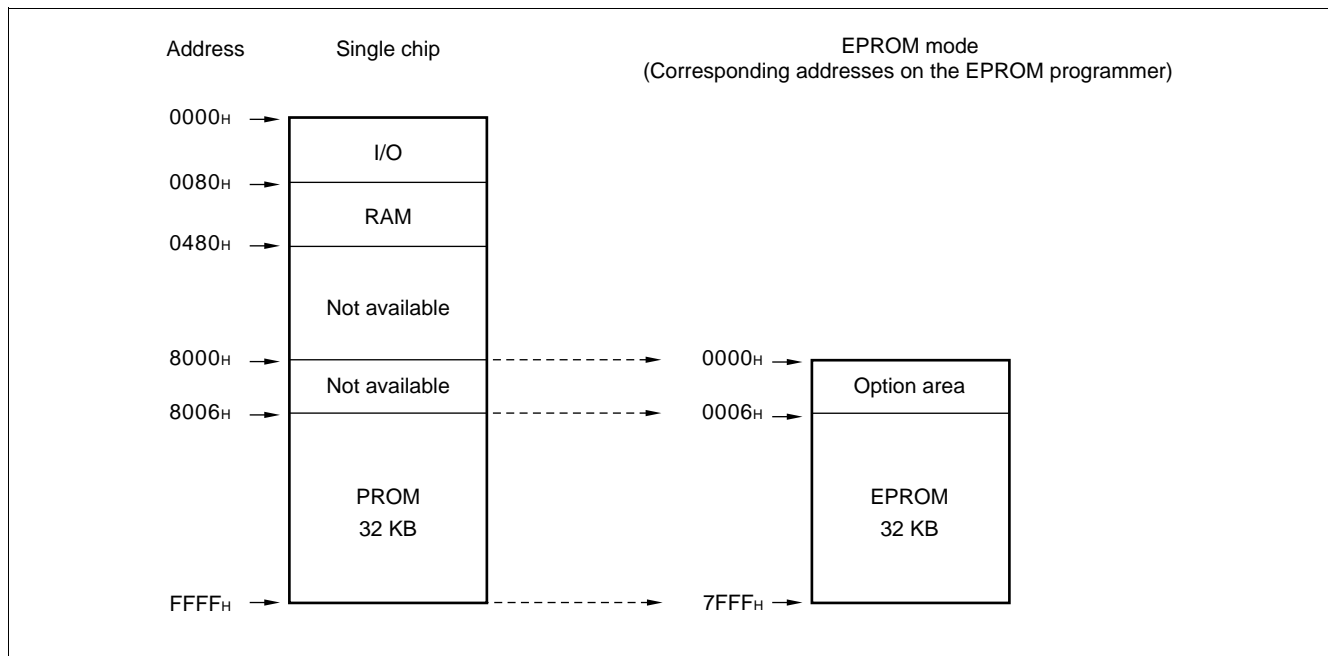
The MB89P657A is an OTPROM version of the MB89650A series.

### 1. Features

- 32-Kbyte PROM on chip
- Options can be set using the EPROM programmer.
- Equivalency to the MBM27C256A in EPROM mode (when programmed with the EPROM programmer)

### 2. Memory Space

Memory space in each mode such as 32-Kbyte PROM, option area is diagrammed below.



### 3. Programming to the EPROM

In EPROM mode, the MB89P657A functions equivalent to the MBM27C256A. This allows the PROM to be programmed with a general-purpose EPROM programmer (the electronic signature mode cannot be used) by using the dedicated socket adapter.

When the operating ROM area for a single chip is 32 Kbytes (8006<sub>H</sub> to FFFF<sub>H</sub>) the PROM can be programmed as follows:

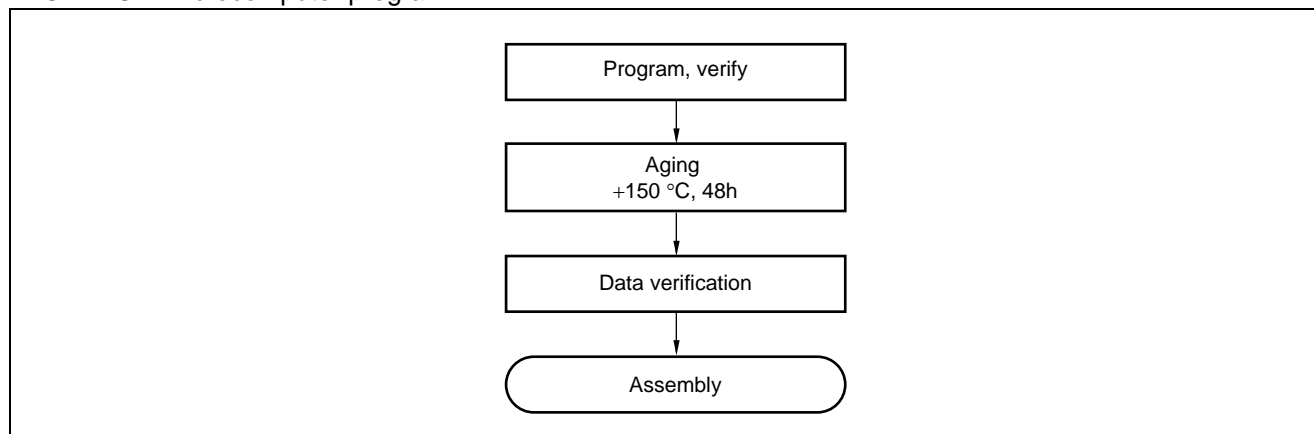
#### • Programming procedure

- (1) Set the EPROM programmer to the MBM27C256A.
- (2) Load program data into the EPROM programmer at 0006<sub>H</sub> to 7FFF<sub>H</sub> (note that addresses 8006<sub>H</sub> to FFFF<sub>H</sub> while operating as a single chip assign to 0006<sub>H</sub> to 7FFF<sub>H</sub> in EPROM mode).  
Load option data into addresses 0000<sub>H</sub> to 0005<sub>H</sub> of the EPROM programmer. (For information about each corresponding option, see "7. Setting OTPROM Options.")
- (3) Program to 0000<sub>H</sub> to 7FFF<sub>H</sub> with the EPROM programmer.

# MB89650AR Series

## 4. Recommended Screening Conditions

High-temperature aging is recommended as the pre-assembly screening procedure for a product with a blanked OTPROM microcomputer program.



## 5. Programming Yield

All bits cannot be programmed at Fujitsu Microelectronics shipping test to a blanked OTPROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

## 6. EPROM Programmer Socket Adapter

Package	Compatible socket adapter
FPT-100P-M05	ROM-100SQF-28DP-8L
FPT-100P-M06	ROM-100QF-28DP-8L2

Inquiry: Sun Hayato Co., Ltd.: TEL 81-3-3802-5760

Note : Connect the ROM-100SQF-28DP-8L jumper pin to  $V_{SS}$  when using.

Depending on the EPROM programmer, inserting a capacitor of about 0.1  $\mu F$  between  $V_{PP}$  and  $V_{SS}$  or  $V_{CC}$  and  $V_{SS}$  can stabilize programming operations.

## 7. Setting OTPROM Options

The programming procedure is the same as that for the PROM. Options can be set by programming values at the addresses shown on the memory map. The relationship between bits and options is shown on the following bit map:

### • OTPROM option bit map

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0000 <sub>H</sub>	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	P81 Pull-up 1: No 0: Yes	P80 Pull-up 1: No 0: Yes	Single/dual- clock system 1: Dual clock 2: Single clock
0001 <sub>H</sub>	P07 Pull-up 1: No 0: Yes	P06 Pull-up 1: No 0: Yes	P05 Pull-up 1: No 0: Yes	P04 Pull-up 1: No 0: Yes	P03 Pull-up 1: No 0: Yes	P02 Pull-up 1: No 0: Yes	P01 Pull-up 1: No 0: Yes	P00 Pull-up 1: No 0: Yes
0002 <sub>H</sub>	P37 Pull-up 1: No 0: Yes	P36 Pull-up 1: No 0: Yes	P35 Pull-up 1: No 0: Yes	P34 Pull-up 1: No 0: Yes	P33 Pull-up 1: No 0: Yes	P32 Pull-up 1: No 0: Yes	P31 Pull-up 1: No 0: Yes	P30 Pull-up 1: No 0: Yes
0003 <sub>H</sub>	P67 Pull-up 1: No 0: Yes	P66 Pull-up 1: No 0: Yes	P65 Pull-up 1: No 0: Yes	P64 Pull-up 1: No 0: Yes	P63 Pull-up 1: No 0: Yes	P62 Pull-up 1: No 0: Yes	P61 Pull-up 1: No 0: Yes	P60 Pull-up 1: No 0: Yes
0004 <sub>H</sub>	P47 to P44 Pull-up 1: No 0: Yes	P43 to P40 Pull-up 1: No 0: Yes	P26 Pull-up 1: No 0: Yes	P25 Pull-up 1: No 0: Yes	P24 Pull-up 1: No 0: Yes	P22 Pull-up 1: No 0: Yes	P21 Pull-up 1: No 0: Yes	P20 Pull-up 1: No 0: Yes
0005 <sub>H</sub>	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	P17 to P14 Pull-up 1: No 0: Yes	P13 Pull-up 1: No 0: Yes	P12 Pull-up 1: No 0: Yes	P11 Pull-up 1: No 0: Yes	P10 Pull-up 1: No 0: Yes

Notes : • Set each bit to 1 to erase.

- Do not write 0 to the vacant bit.

The read value of the vacant bit is 1, unless 0 is written to it.



# MB89650AR Series

## ■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE

### 1. EPROM for Use

MBM27C256A-20TVM

### 2. Programming Socket Adapter

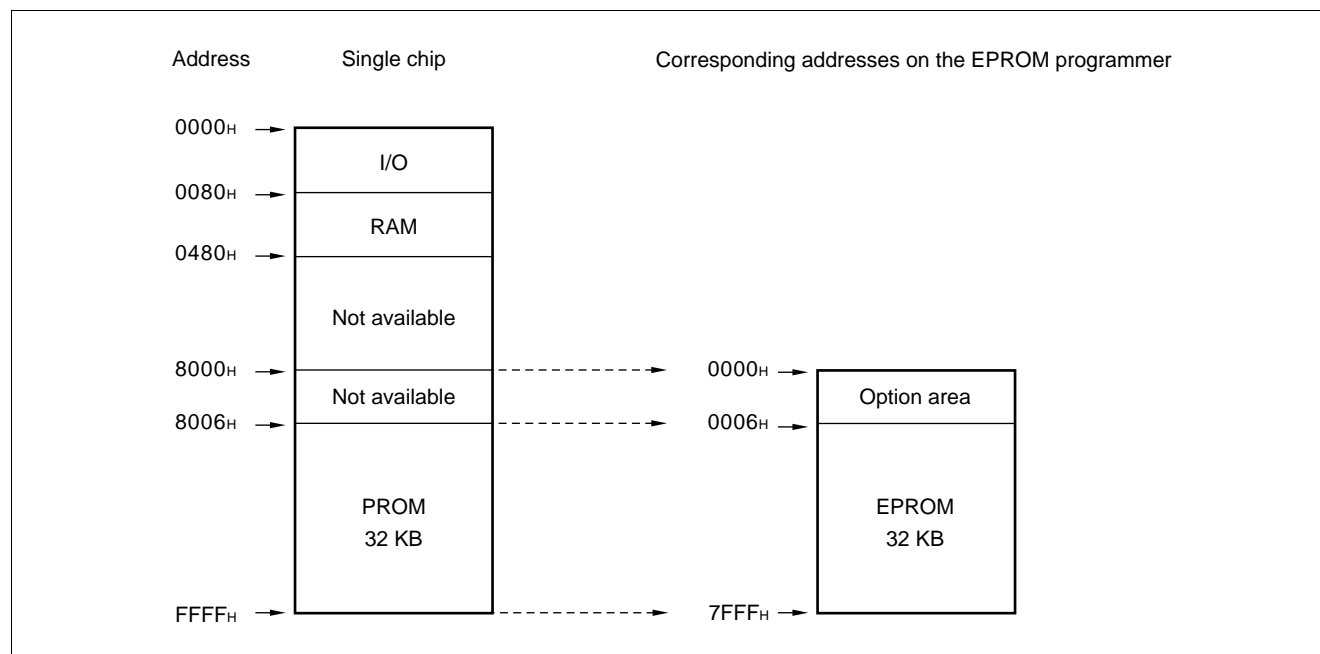
To program to the PROM using an EPROM programmer, use the socket adapter (manufacturer: Sun Hayato Co., Ltd.) listed below.

Package	Adapter socket part number
LCC-32(Rectangle)	ROM-32LC-28DP-YG
LCC-32(Square)	ROM-32LC-28DP-S

Inquiry: Sun Hayato Co., Ltd.: TEL 81-3-3802-5760

### 3. Memory Space

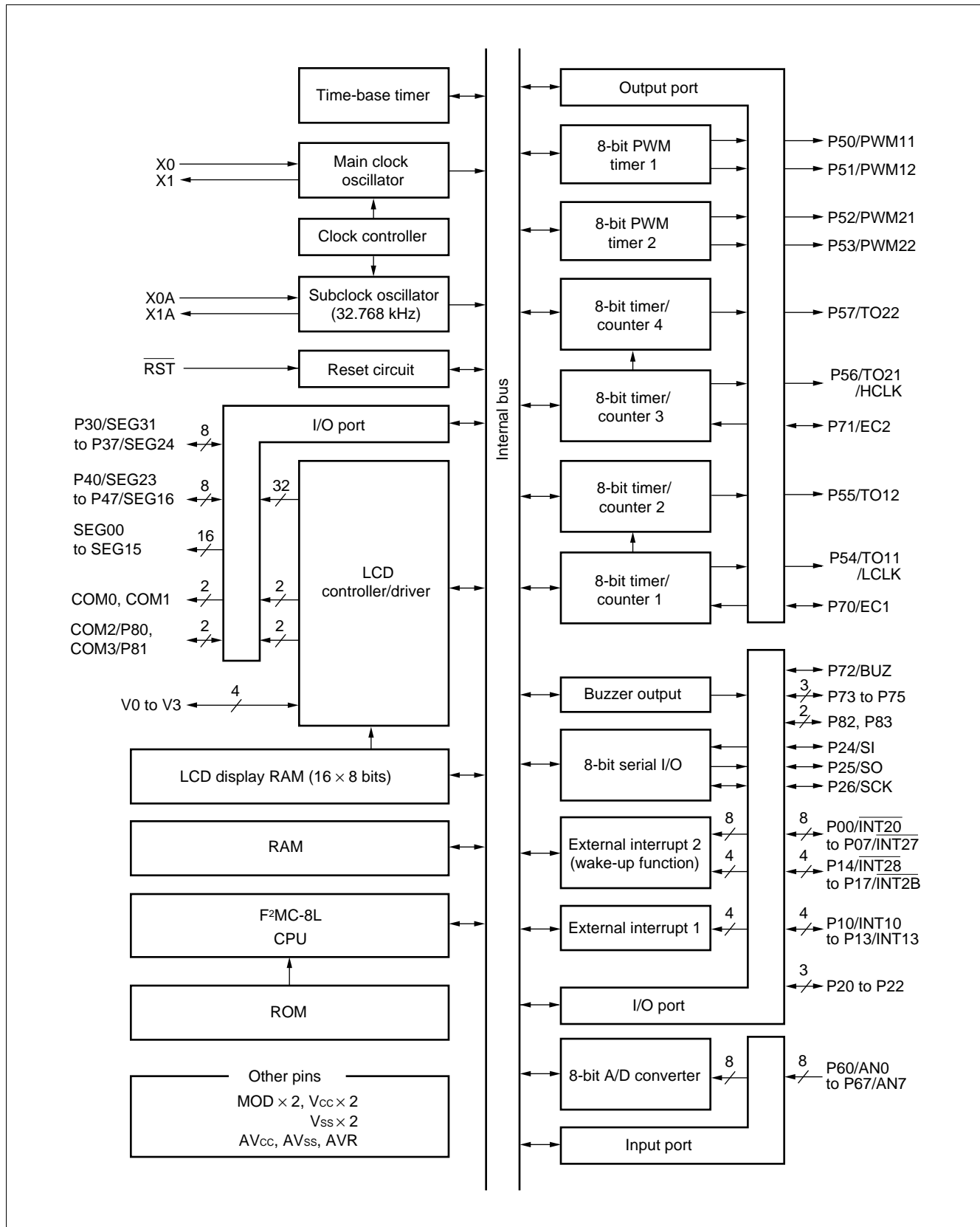
Memory space in each mode, such as 32-Kbyte PROM, option area is diagrammed below.



### 4. Programming to the EPROM

- (1) Set the EPROM programmer to the MBM27C256A.
- (2) Load program data into the EPROM programmer at 0006<sub>H</sub> to 7FFF<sub>H</sub>.
- (3) Program to 0000<sub>H</sub> to 7FFF<sub>H</sub> with the EPROM programmer.

## ■ BLOCK DIAGRAM



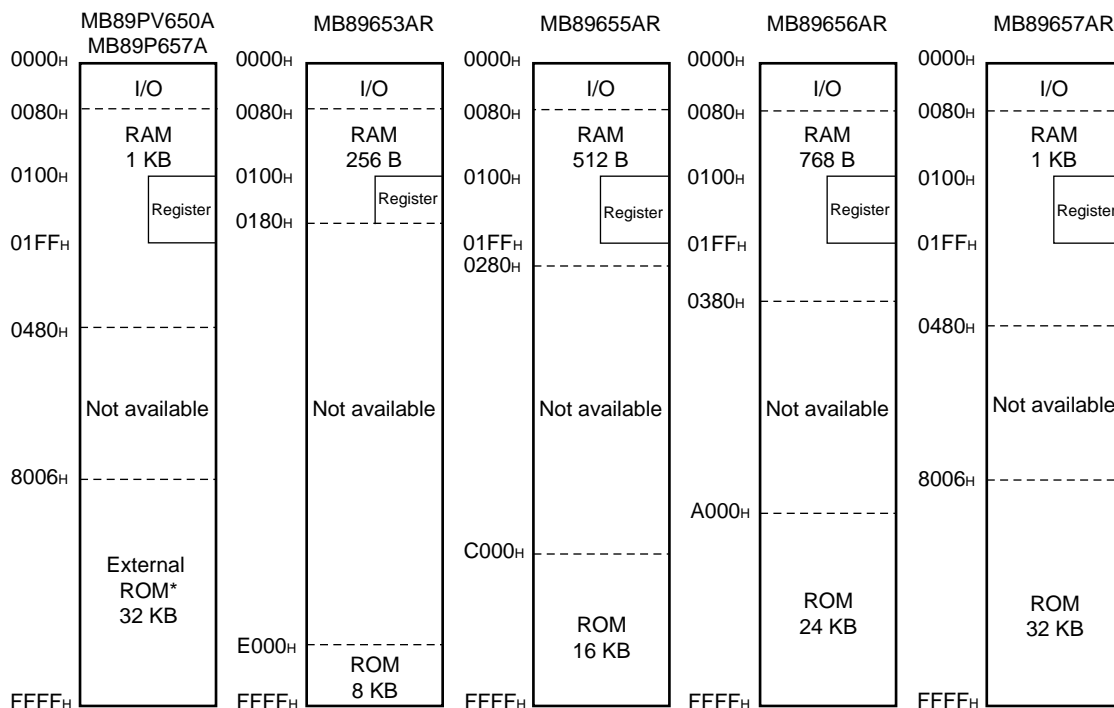
# MB89650AR Series

## ■ CPU CORE

### 1. Memory Space

The microcontrollers of the MB89650AR series offer a memory space of 64 Kbytes for storing all of I/O, data, and program areas. The I/O area is located at the lowest address. The data area is provided immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is located at exactly the opposite end, that is, near the highest address. Provide the tables of interrupt reset vectors and vector call instructions toward the highest address within the program area. The memory space of the MB89650AR series is structured as illustrated below.

#### Memory Space



\*: This is an internal PROM on the MB89P657A.

Since addresses 8000H to 8005H for the MB89P657A comprise an option area, do not use this area for the MB89PV650A.

## 2. Registers

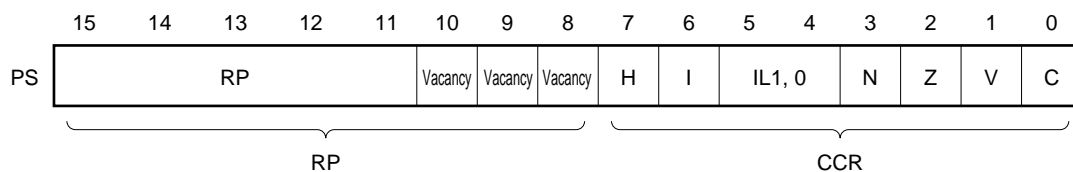
The F<sup>2</sup>MC-8L family has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following dedicated registers are provided:

Program counter (PC):	A 16-bit register for indicating instruction storage positions
Accumulator (A):	A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.
Temporary accumulator (T):	A 16-bit register which performs arithmetic operations with the accumulator When the instruction is an 8-bit data processing instruction, the lower byte is used.
Index register (IX):	A 16-bit register for index modification
Extra pointer (EP):	A 16-bit pointer for indicating a memory address
Stack pointer (SP):	A 16-bit register for indicating a stack area
Program status (PS):	A 16-bit register for storing a register pointer, a condition code

16 bits		Initial value
PC	: Program counter	FFFD <sub>H</sub>
A	: Accumulator	Undefined
T	: Temporary accumulator	Undefined
IX	: Index register	Undefined
EP	: Extra pointer	Undefined
SP	: Stack pointer	Undefined
PS	: Program status	I-flag = 0, IL1, 0 = 11 Other bits are undefined.

The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)

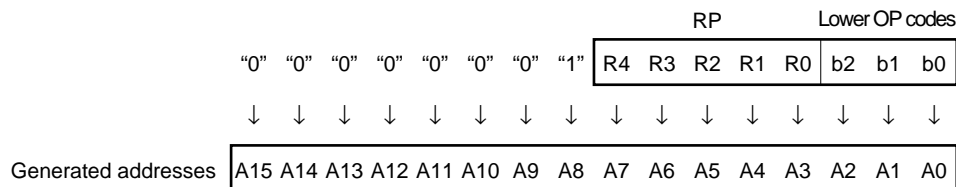
### Structure of the Program Status Register



# MB89650AR Series

The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

### Rule for Conversion of Actual Addresses of the General-purpose Register Area




The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

**H-flag:** Set when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared otherwise. This flag is for decimal adjustment instructions.

**I-flag:** Interrupt is allowed when this flag is set to 1. Interrupt is prohibited when the flag is set to 0. Set to 0 when reset.

IL1, 0: Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	High-low
0	0	1	<div style="text-align: center;">           High              Low = no interrupt         </div>
0	1		
1	0	2	
1	1	3	

N-flag: Set if the MSB is set to 1 as the result of an arithmetic operation. Cleared when the bit is set to 0.

**Z-flag:** Set when an arithmetic operation results in 0. Cleared otherwise.

**V-flag:** Set if the complement on 2 overflows as a result of an arithmetic operation. Reset if the overflow does not occur.

**C-flag:** Set when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared otherwise.  
Set to the shift-out value in the case of a shift instruction.

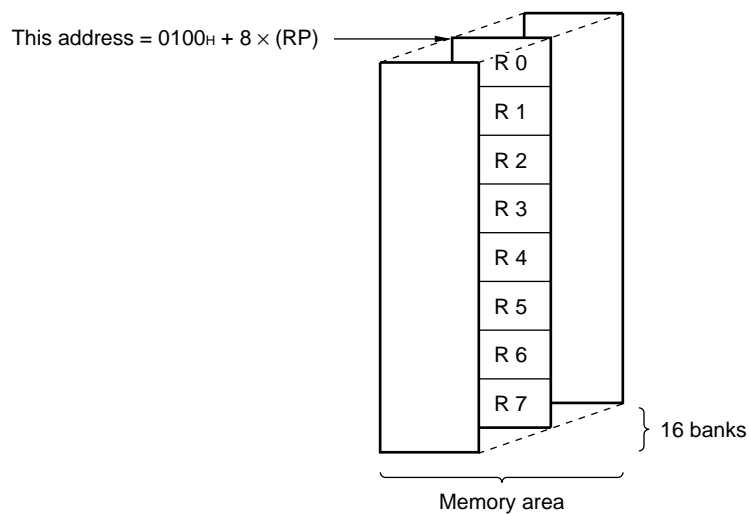
The following general-purpose registers are provided:

General-purpose registers: An 8-bit register for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers and up to a total of 16 banks can be used on the MB89653AR (RAM  $256 \times 8$  bits). The bank currently in use is indicated by the register bank pointer (RP).

Note: The number of register banks that can be used varies with the RAM size. Up to a total of 32 banks can be used on other than the MB89653AR.

## Register Bank Configuration



# MB89650AR Series

## ■ I/O MAP

Address	Read/write	Register name	Register description
00 <sub>H</sub>	(R/W)	PDR0	Port 0 data register
01 <sub>H</sub>	(W)	DDR0	Port 0 data direction register
02 <sub>H</sub>	(R/W)	PDR1	Port 1 data register
03 <sub>H</sub>	(W)	DDR1	Port 1 data direction register
04 <sub>H</sub>	(R/W)	PDR2	Port 2 data register
05 <sub>H</sub>	(R/W)	DDR2	Port 2 data direction register
06 <sub>H</sub>			Vacancy
07 <sub>H</sub>	(R/W)	SCC	System clock control register
08 <sub>H</sub>	(R/W)	SMC	System mode control register
09 <sub>H</sub>	(R/W)	WDTC	Watchdog time control register
0A <sub>H</sub>	(R/W)	TBTC	Time-base timer control register
0B <sub>H</sub>	(R/W)	WCR	Watch prescaler control register
0C <sub>H</sub>	(R/W)	PDR3	Port 3 data register
0D <sub>H</sub>	(R/W)	DDR3	Port 3 data direction register
0E <sub>H</sub>	(R/W)	PDR4	Port 4 data register
0F <sub>H</sub>	(R/W)	DDR4	Port 4 data direction register
10 <sub>H</sub>	(R/W)	T4CR	Timer 4 control register
11 <sub>H</sub>	(R/W)	T3CR	Timer 3 control register
12 <sub>H</sub>	(R/W)	T4DR	Timer 4 data register
13 <sub>H</sub>	(R/W)	T3DR	Timer 3 data register
14 <sub>H</sub>			Vacancy
15 <sub>H</sub>			Vacancy
16 <sub>H</sub>	(R/W)	PDR5	Port 5 data register
17 <sub>H</sub>			Vacancy
18 <sub>H</sub>			Vacancy
19 <sub>H</sub>			Vacancy
1A <sub>H</sub>	(W)	ICR6	Port 6 input control register
1B <sub>H</sub>	(R)	PDR6	Port 6 data register
1C <sub>H</sub>	(R/W)	PDR7	Port 7 data register
1D <sub>H</sub>	(R/W)	CHG2	Port 2 switching register
1E <sub>H</sub>	(R/W)	CNTR1	PWM 0/1 control register
1F <sub>H</sub>	(W)	COMP1	PWM 0/1 compare register

(Continued)

(Continued)

Address	Read/write	Register name	Register description
20 <sub>H</sub>	(R/W)	CNTR2	PWM 2/3 control register
21 <sub>H</sub>	(W)	COMP2	PWM 2/3 compare register
22 <sub>H</sub>			Vacancy
23 <sub>H</sub>			Vacancy
24 <sub>H</sub>	(R/W)	T2CR	Timer 2 control register
25 <sub>H</sub>	(R/W)	T1CR	Timer 1 control register
26 <sub>H</sub>	(R/W)	T2DR	Timer 2 data register
27 <sub>H</sub>	(R/W)	T1DR	Timer 1 data register
28 <sub>H</sub>	(R/W)	SMR	Serial mode register
29 <sub>H</sub>	(R/W)	SDR	Serial data register
2A <sub>H</sub>			Vacancy
2B <sub>H</sub>			Vacancy
2C <sub>H</sub>			Vacancy
2D <sub>H</sub>	(R/W)	ADC1	A/D converter control register 1
2E <sub>H</sub>	(R/W)	ADC2	A/D converter control register 2
2F <sub>H</sub>	(R/W)	ADCD	A/D converter data register
30 <sub>H</sub>	(R/W)	EIE1	External interrupt 1 enable register
31 <sub>H</sub>	(R/W)	EIF1	External interrupt 1 flag register
32 <sub>H</sub>	(R/W)	EIE2	External interrupt 2 enable register
33 <sub>H</sub>	(R/W)	EIF2	External interrupt 2 flag register
34 <sub>H</sub> to 5F <sub>H</sub>			Vacancy
60 <sub>H</sub> to 6F <sub>H</sub>	(R/W)	VRAM	Display data RAM
70 <sub>H</sub>	(R/W)	LCR1	LCD controller/driver control register 1
71 <sub>H</sub>	(R/W)	LCR2	LCD controller/driver control register 2
72 <sub>H</sub>	(R/W)	PDR8	Port 8 data register
73 <sub>H</sub>	(W)	DDR8	Port 8 data direction register
74 <sub>H</sub> to 7B <sub>H</sub>			Vacancy
7C <sub>H</sub>	(W)	ILR1	Interrupt level setting register 1
7D <sub>H</sub>	(W)	ILR2	Interrupt level setting register 2
7E <sub>H</sub>	(W)	ILR3	Interrupt level setting register 3
7F <sub>H</sub>			Vacancy

Note : Do not use vacancies.



# MB89650AR Series

## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Ratings

( $AV_{SS} = V_{SS} = 0.0\text{ V}$ )

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	$V_{CC}$ $AV_{CC}$	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	*1
A/D converter reference input voltage	AVR	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	
LCD power supply voltage	V0 to V3	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	V0 to V3 must not exceed $V_{CC}$ .
Input voltage	$V_I$	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	Except P70 to P75*2
	$V_{I2}$	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	P70 to P75
Output voltage	$V_O$	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	Except P70 to P75*2
	$V_{O2}$	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	P70 to P75
"L" level maximum output current	$I_{OL}$	—	20	mA	
"L" level average output current	$I_{OLAV}$	—	4	mA	Average value (operating current × operating rate)
"L" level total maximum output current	$\Sigma I_{OL}$	—	100	mA	
"L" level total average output current	$\Sigma I_{OLAV}$	—	40	mA	Average value (operating current × operating rate)
"H" level maximum output current	$I_{OH}$	—	-20	mA	
"H" level average output current	$I_{OHAV}$	—	-4	mA	Average value (operating current × operating rate)
"H" level total maximum output current	$\Sigma I_{OH}$	—	-50	mA	
"H" level total average output current	$\Sigma I_{OHAV}$	—	-20	mA	Average value (operating current × operating rate)
Power consumption	$P_D$	—	300	mW	
Operating temperature	$T_A$	-40	+85	°C	
Storage temperature	$T_{stg}$	-55	+150	°C	

\*1 : Use  $AV_{CC}$  and  $V_{CC}$  set at the same voltage.

Take care so that AVR does not exceed  $AV_{CC} + 0.3\text{ V}$  and  $AV_{CC}$  does not exceed  $V_{CC}$ , such as when power is turned on.

\*2 :  $V_I$  and  $V_O$  must not exceed  $V_{CC} + 0.3\text{ V}$ .

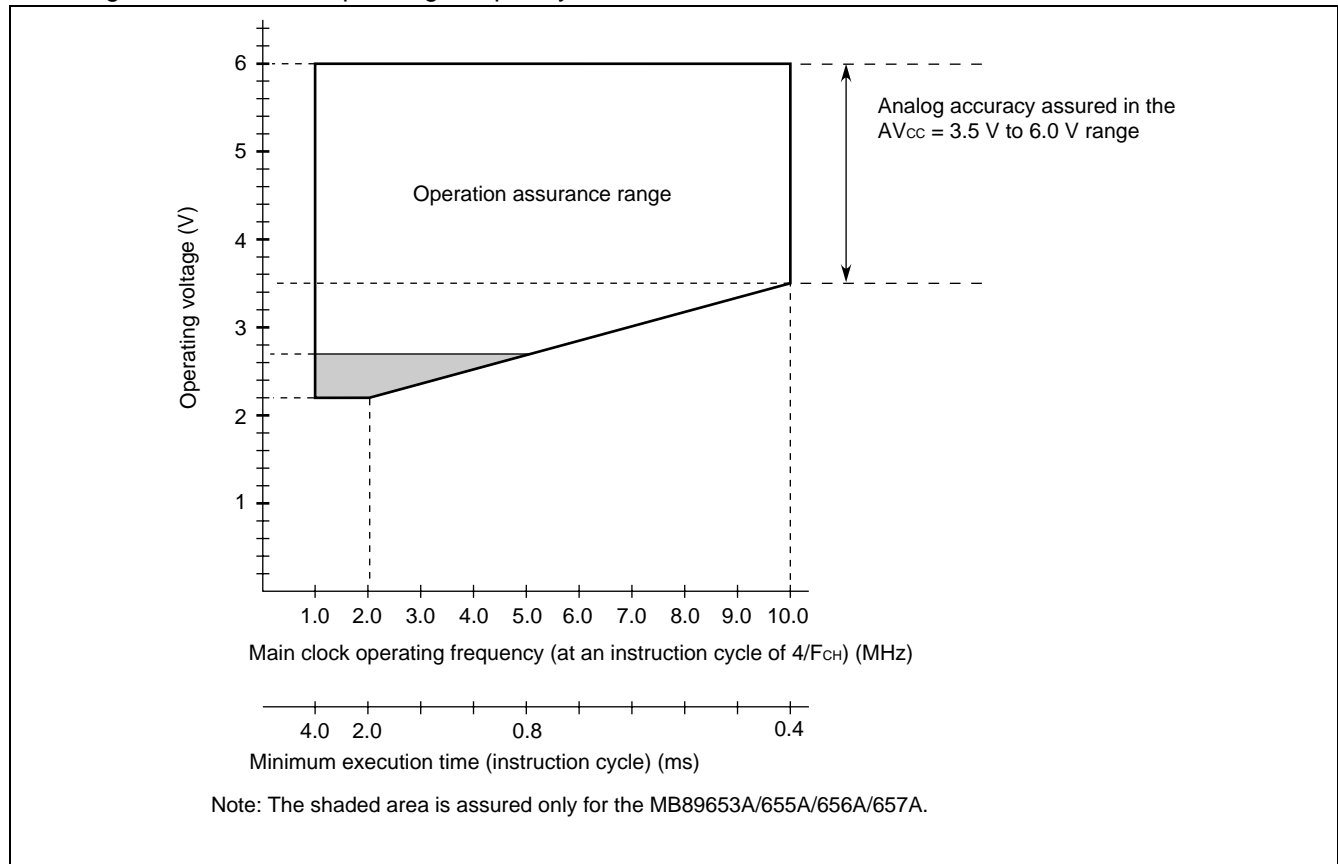
**WARNING:** Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## 2. Recommended Operating Conditions

( $AV_{SS} = V_{SS} = 0.0\text{ V}$ )

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	$V_{CC}$ $AV_{CC}$	2.2*	6.0*	V	Normal operation assurance range* MB89653AR/655AR/656AR/657AR
		2.7*	6.0*	V	Normal operation assurance range* MB89PV650A/P657A
		1.5	6.0	V	Retains the RAM state in stop mode
A/D converter reference input voltage	AVR	0.0	$AV_{CC}$	V	
LCD power supply voltage	V0 to V3	$V_{SS}$	$V_{CC}$	V	LCD power supply range (The optimum value is dependent on the LCD element in use.)
Operating temperature	$T_A$	-40	+85	°C	

\* : These values vary with the operating frequency, instruction cycle, and analog assurance range. See "Operating Voltage vs. Main Clock Operating Frequency" and "5. A/D Converter Electrical Characteristics."



### Operating Voltage vs. Main Clock Operating Frequency

"Operating Voltage vs. Main Clock Operating Frequency" indicates the operating frequency of the external oscillator at an instruction cycle of  $4/F_{CH}$ .

Since the operating voltage range is dependent on the instruction cycle, see minimum execution time if the operating speed is switched using a gear.

# MB89650AR Series

**WARNING:** The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

## 3. DC Characteristics

( $V_{CC} = V_{CC} = 5.0\text{ V}$ ,  $V_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
“H” level input voltage	$V_{IH1}$	P20 to P26, P30 to P37, P40 to P47, P60 to P67, P80 to P83	—	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	
	$V_{IH2}$	P72 to P75	—	$0.7 V_{CC}$	—	$V_{SS} + 6.0$	V	Without pull-up resistor
	$V_{IHS}$	P00 to P07, P10 to P17, $\overline{RST}$ , MOD0, MOD1, P26 (at SC input)	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	
	$V_{IHS2}$	P70, P71	—	$0.8 V_{CC}$	—	$V_{SS} + 6.0$	V	Without pull-up resistor
“L” level input voltage	$V_{IL}$	P20 to P26, P30 to P37, P40 to P47, P60 to P67, P72 to P75, P80 to P83	—	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	
	$V_{IS}$	P00 to P07, P10 to P17, P26 (at SC input), P70, P71, $\overline{RST}$ , MOD0, MOD1	—	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	
Open-drain output pin application voltage	$V_D$	P24 to P26	—	$V_{SS} - 0.3$	—	$V_{SS} + 0.3$	V	N-ch open-drain
	$V_{D2}$	P70 to P75	—	$V_{SS} - 0.3$	—	$V_{SS} + 6.0$	V	
“H” level output voltage	$V_{OH}$	P00 to P07, P10 to P17, P20 to P26, P30 to P37, P40 to P47, P50 to P57, P80 to P83	$I_{OH} = -2.0\text{ mA}$	4.0	—	—	V	
“L” level output voltage	$V_{OL}$	P00 to P07, P10 to P17, P20 to P26, P30 to P37, P40 to P47, P50 to P57, P70 to P75, P80 to P83	$I_{OL} = 4.0\text{ mA}$	—	—	0.4	V	
Input leakage current (Hi-z output leakage current)	$I_{LI}$	P00 to P07, P10 to P17, P20 to P26, P30 to P37, P40 to P47, P60 to P67, P70 to P75, P80 to P83, MOD0, MOD1, $\overline{RST}$	$0.0\text{ V} < V_I < V_{CC}$	—	—	$\pm 5$	$\mu\text{A}$	Without pull-up resistor
Pull-up resistance	$R_{PULL}$	P00 to P07, P10 to P17, P20 to P26, P30 to P37, P40 to P47, P60 to P67, P70 to P75, P80 to P81	$V_I = 0.0\text{ V}$	25	50	100	$k\Omega$	With pull-up resistor

(Continued)

# MB89650AR Series

( $AV_{CC} = V_{CC} = 5.0\text{ V}$ ,  $AV_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*1	$I_{CC1}$	$V_{CC}$	$F_{CH} = 10\text{ MHz}$ $V_{CC} = 5.0\text{ V}$ $t_{inst}^{*2} = 0.4\text{ }\mu\text{s}$	—	12	20	mA	
	$I_{CC2}$		$F_{CH} = 10\text{ MHz}$ $V_{CC} = 3.0\text{ V}$ $t_{inst}^{*2} = 6.4\text{ }\mu\text{s}$	—	1.0	2	mA	MB89653AR/ 655AR/656AR/ 657AR/ PV650A
				—	1.5	2.5	mA	MB89P657A
	$I_{CCS1}$		Sleep mode $F_{CH} = 10\text{ MHz}$ $V_{CC} = 5.0\text{ V}$ $t_{inst}^{*2} = 0.4\text{ }\mu\text{s}$	—	3	7	mA	
	$I_{CCS2}$			—	0.5	1.5	mA	
	$I_{CCL}$		$F_{CL} = 32.768\text{ kHz}$ , $V_{CC} = 3.0\text{ V}$ Subclock mode	—	50	100	$\mu\text{A}$	MB89653AR/ 655AR/656AR/ 657AR/ PV650A
				—	500	700	$\mu\text{A}$	MB89P657A
	$I_{CCLS}$		$F_{CL} = 32.768\text{ kHz}$ , $V_{CC} = 3.0\text{ V}$ Subclock sleep mode	—	15	50	$\mu\text{A}$	
	$I_{CCT}$		$F_{CL} = 32.768\text{ kHz}$ , $V_{CC} = 3.0\text{ V}$ • Watch mode • Main clock stop mode at dual- clock system	—	3	15	$\mu\text{A}$	
	$I_{CCH}$		$T_A = +25^\circ\text{C}$ • Subclock stop mode • Main clock stop mode at single- clock system	—	—	1	$\mu\text{A}$	
	$I_A$	$AV_{CC}$	$F_{CH} = 10\text{ MHz}$ , when A/D conversion is activated	—	1.5	3	mA	
	$I_{AH}$		$F_{CH} = 10\text{ MHz}$ , $T_A = +25^\circ\text{C}$ , when A/D conversion is stopped	—	—	1	$\mu\text{A}$	

(Continued)

# MB89650AR Series

(Continued)

( $AV_{CC} = V_{CC} = 5.0\text{ V}$ ,  $AV_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ )

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
LCD divided resistance	$R_{LCD}$	—	Between $V_{CC}$ and $V_0$ at $V_{CC} = 5.0\text{ V}$	300	500	750	$k\Omega$	
COM0 to COM3 output impedance	$R_{VCOM}$	COM0 to COM03	$V_1$ to $V_3 = 5.0\text{ V}$	—	—	2.5	$k\Omega$	
SEG0 to SEG31 output impedance	$R_{VSEG}$	SEG0 to SEG31		—	—	15	$k\Omega$	
LCD controller/driver leakage current	$I_{LCDL}$	$V_0$ to $V_3$ , COM0 to 3, SEG0 to SEG31	—	—	—	$\pm 1$	$\mu\text{A}$	
Input capacitance	$C_{IN}$	Other than $AV_{CC}$ , $AV_{SS}$ , $V_{CC}$ , and $V_{SS}$	$f = 1\text{ MHz}$	—	10	—	$\text{pF}$	

\*1 : The power supply current is measured at the external clock.

\*2 : For information on  $t_{inst}$ , see “(4) Instruction Cycle” in “4. AC Characteristics.”

Note : For pins which serve as the LCD and ports (P30 to P37, P40 to P47, and P80 to P81), see the port parameter when these pins are used as ports and the LCD parameter when they are used as LCD pins.

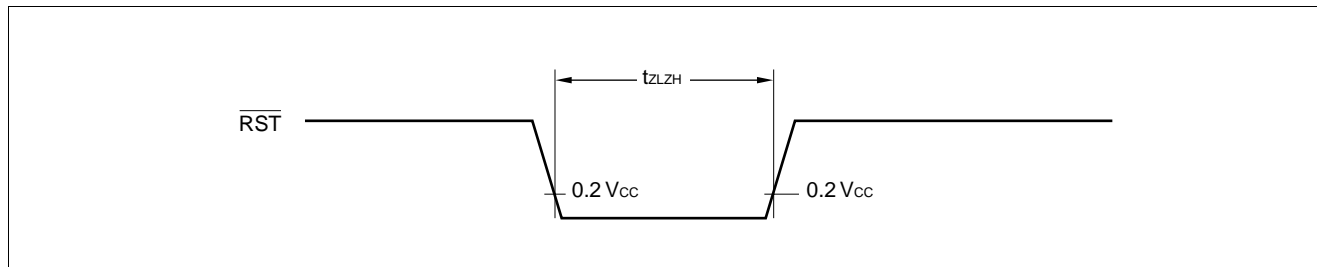
# MB89650AR Series

## 4. AC Characteristics

### (1) Reset Timing

( $V_{CC} = +5.0\text{ V} \pm 10\%$ ,  $AV_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
$\overline{\text{RST}}$ "L" pulse width	$t_{ZLZH}$	—	48 $t_{HCL}$	—	ns	



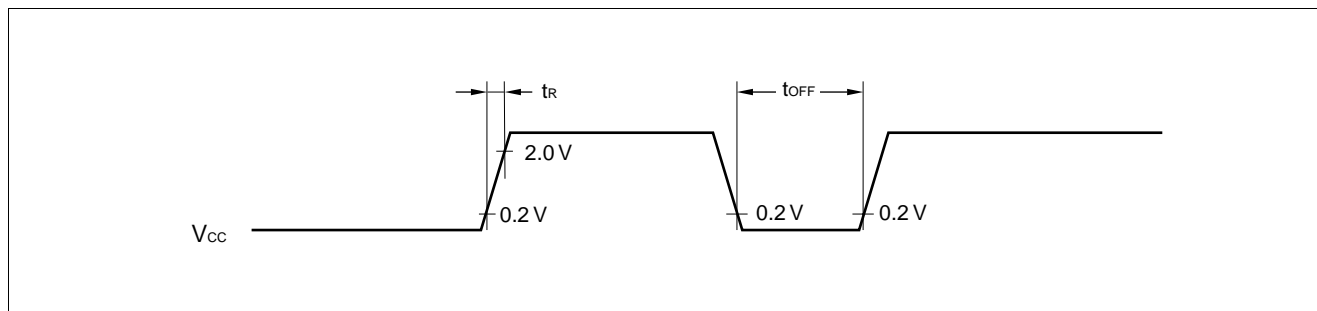
### (2) Power-on Reset

( $AV_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Power supply rising time	$t_R$	—	—	50	ms	Power-on reset function only
Power supply cut-off time	$t_{OFF}$	—	1	—	ms	Due to repeated operations

Note : Make sure that power supply rises within the selected oscillation stabilization time.

If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.

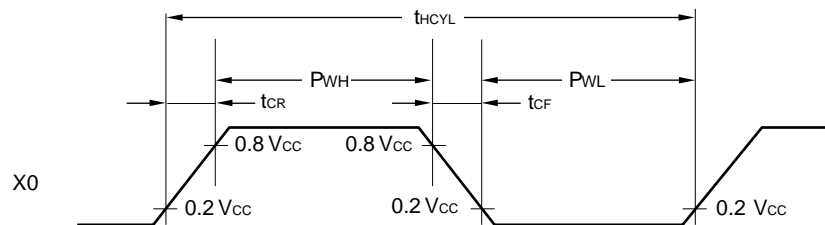


## (3) Clock Timing

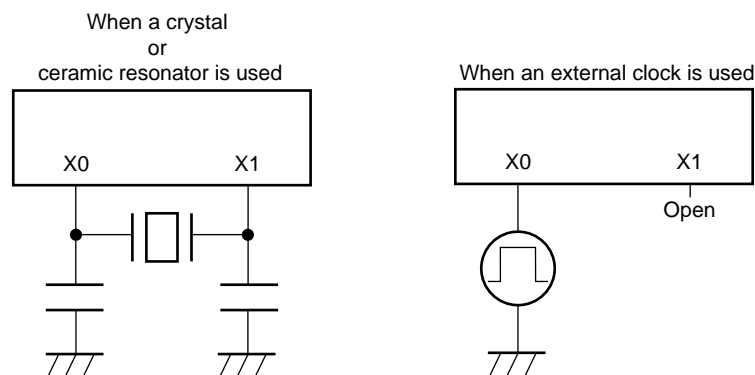
( $V_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	$F_{CH}$	X0, X1	—	1	—	10	MHz	
	$F_{CL}$	X0A, X1A		—	32.768	—	kHz	
Clock cycle time	$t_{HCL}$	X0, X1		100	—	1000	ns	
	$t_{LCL}$	X0A, X1A		—	30.5	—	$\mu\text{s}$	
Input clock pulse width	$P_{WH}$ $P_{WL}$	X0		20	—	—	ns	External clock
	$P_{WLH}$ $P_{WLL}$	X0A		—	15.2	—	$\mu\text{s}$	External clock
Input clock rising/falling time	$t_{CR}$ $t_{CF}$	X0		—	—	10	ns	External clock

### X0 and X1 Timing and Conditions



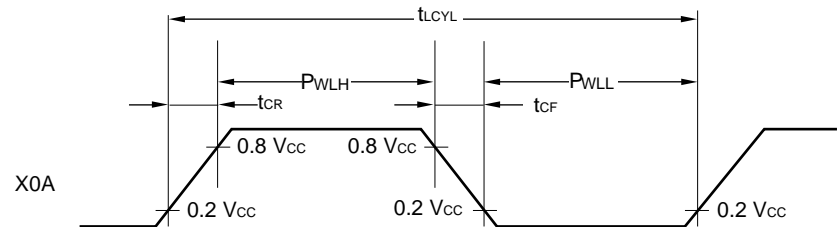
### Main Clock Conditions



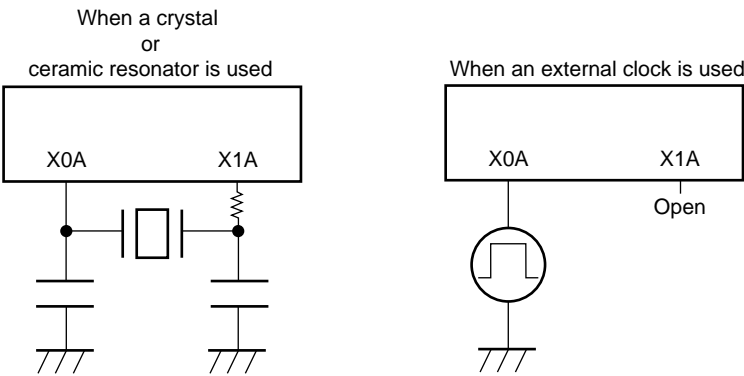


# MB89650AR Series

## X0A and X1A Timing and Conditions



## Subclock Conditions



## (4) Instruction Cycle

Parameter	Symbol	Value (typical)	Unit	Remarks
Instruction cycle (minimum execution time)	t <sub>inst</sub>	4/F <sub>CH</sub> , 8/F <sub>CH</sub> , 16/F <sub>CH</sub> , 64/F <sub>CH</sub>	μs	(4/F <sub>CH</sub> ) t <sub>inst</sub> = 0.4 μs when operating at F <sub>CH</sub> = 10 MHz
		2/F <sub>CL</sub>	μs	t <sub>inst</sub> = 61.036 μs when operating at F <sub>CL</sub> = 32.768 kHz

Note : When operating at 10 MHz, the cycle varies with the set execution time.

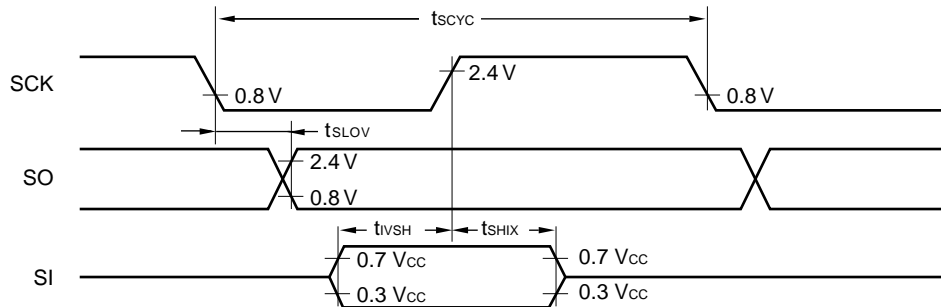
## (5) Serial I/O Timing

( $V_{CC} = +5.0\text{ V} \pm 10\%$ ,  $AV_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

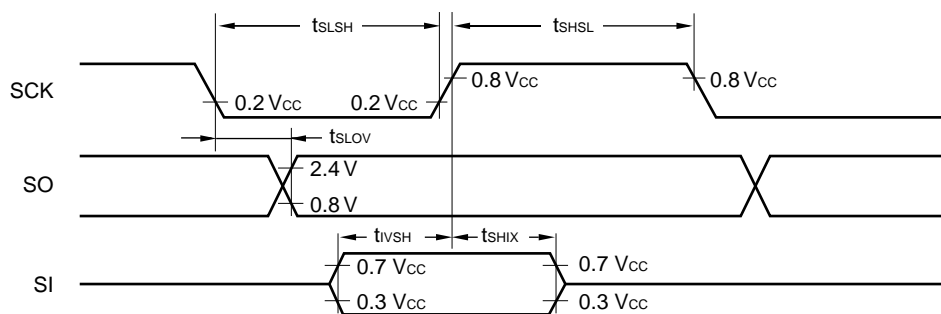
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	$t_{SCYC}$	SCK	Internal shift clock mode	$2\ t_{inst}^*$	—	$\mu\text{s}$	
SCK $\downarrow \rightarrow$ SO time	$t_{SLOV}$	SCK, SO		-200	200	ns	
Valid SI $\rightarrow$ SCK $\uparrow$	$t_{IVSH}$	SI, SCK		$1/2\ t_{inst}^*$	—	$\mu\text{s}$	
SCK $\uparrow \rightarrow$ valid SI hold time	$t_{SHIX}$	SCK, SI		$1/2\ t_{inst}^*$	—	$\mu\text{s}$	
Serial clock "H" pulse width	$t_{SHSL}$	SCK	External shift clock mode	$1\ t_{inst}^*$	—	$\mu\text{s}$	
Serial clock "L" pulse width	$t_{SLSH}$			$1\ t_{inst}^*$	—	$\mu\text{s}$	
SCK $\downarrow \rightarrow$ SO time	$t_{SLOV}$	SCK, SO		0	200	ns	
Valid SI $\rightarrow$ SCK $\uparrow$	$t_{IVSH}$	SI, SCK		$1/2\ t_{inst}^*$	—	$\mu\text{s}$	
SCK $\uparrow \rightarrow$ valid SI hold time	$t_{SHIX}$	SCK, SI		$1/2\ t_{inst}^*$	—	$\mu\text{s}$	

\* : For information on  $t_{inst}$ , see "(4) Instruction Cycle."

### Internal Shift Clock Mode



### External Shift Clock Mode



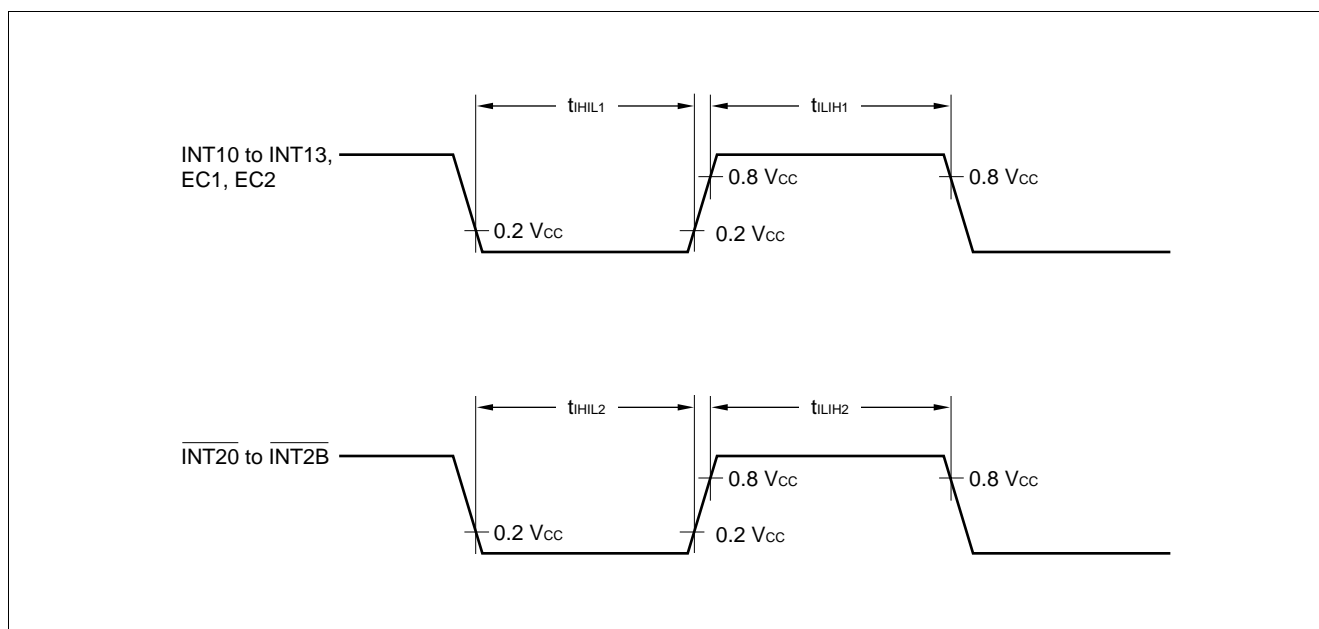
# MB89650AR Series

## (6) Peripheral Input Timing

( $V_{CC} = +5.0\text{ V} \pm 10\%$ ,  $AV_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

Parameter	Symbol	Pin	Value		Unit	Remarks
			Min	Max		
Peripheral input "H" pulse width 1	$t_{LIH1}$	INT10 to INT13, EC1, EC2	1 $t_{inst}^*$	—	$\mu\text{s}$	
Peripheral input "L" pulse width 1	$t_{IHIL1}$		1 $t_{inst}^*$	—	$\mu\text{s}$	
Peripheral input "H" pulse width 2	$t_{LIH2}$	$\overline{\text{INT20}}$ to $\overline{\text{INT2B}}$	2 $t_{inst}^*$	—	$\mu\text{s}$	
Peripheral input "L" pulse width 2	$t_{IHIL2}$		2 $t_{inst}^*$	—	$\mu\text{s}$	

\* : For information on  $t_{inst}$ , see "(4) Instruction Cycle."



## 5. A/D Converter Electrical Characteristics

( $AV_{CC} = V_{CC} = +3.5 \text{ V to } +6.0 \text{ V}$ ,  $AV_{SS} = V_{SS} = 0.0 \text{ V}$ ,  $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ )

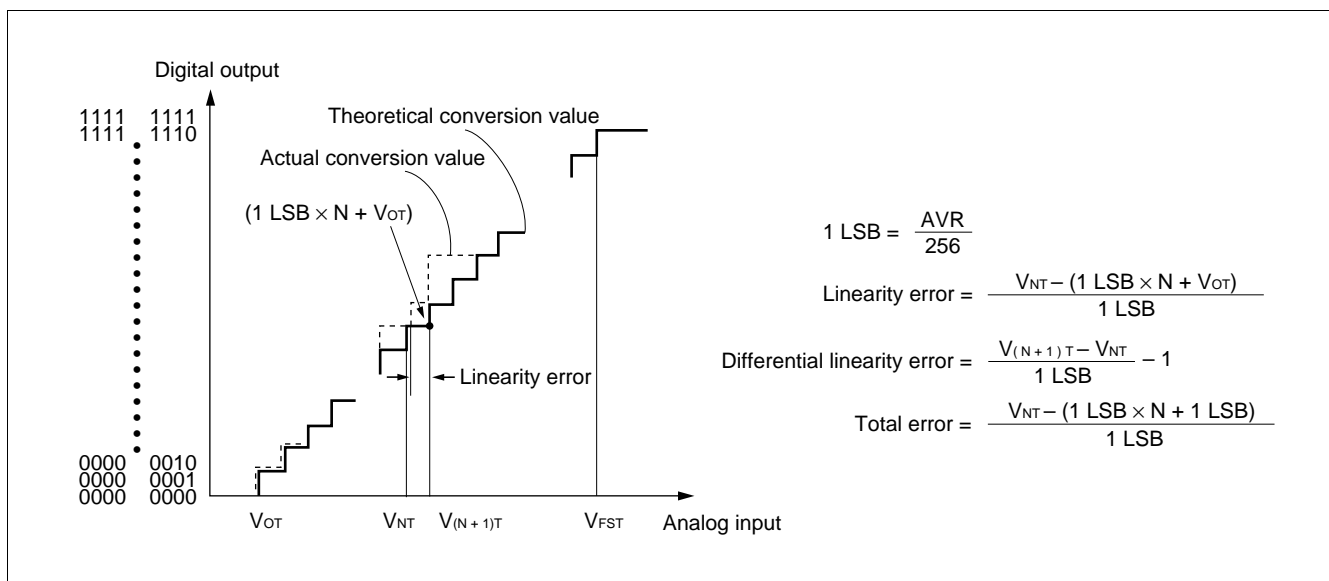
Parameter	Sym- bol	Pin	Condition	Value			Unit	Remarks	
				Min	Typ	Max			
Resolution	—	—	—	—	—	8	bit		
Total error			—	—	±1.5	LSB			
Linearity error			—	—	±1.0	LSB			
Differential linearity error			—	—	±0.9	LSB			
Zero transition voltage	V <sub>OT</sub>		—	AVR = AV <sub>CC</sub>	AV <sub>SS</sub> – 1.0 LSB	AV <sub>SS</sub> + 0.5 LSB	AV <sub>SS</sub> + 2.0 LSB	mV	
Full-scale transition voltage	V <sub>FST</sub>				AVR – 3.0 LSB	AVR – 1.5 LSB	AVR	mV	
Interchannel disparity	—				—	—	0.5	LSB	
A/D mode conversion time			—	—	44 t <sub>inst</sub> <sup>*</sup>	—	μs		
Sense mode conversion time				—	12 t <sub>inst</sub> <sup>*</sup>	—	μs		
Analog port input current	I <sub>AIN</sub>	AN0 to AN7	—	—	—	10	μA		
Analog input voltage	—			0.0	—	AVR	V		
Reference voltage	—	AVR		AVR = 5.0V, when A/D conversion is activated	0.0	—	AV <sub>CC</sub>	V	
Reference voltage supply current	I <sub>R</sub>		—		100	—	μA		
	I <sub>RH</sub>		AVR = 5.0V, when A/D conversion is stopped		—	—	1	μA	

\* : For information on  $t_{inst}$ , see “(4) Instruction Cycle” in “4. AC Characteristics.”

# MB89650AR Series

## (1) A/D Glossary

- Resolution  
Analog changes that are identifiable with the A/D converter.  
When the number of bits is 8, analog voltage can be divided into  $2^8 = 256$ .
- Linearity error (unit: LSB)  
The deviation of the straight line connecting the zero transition point ("0000 0000" ↔ "0000 0001") with the full-scale transition point ("1111 1111" ↔ "1111 1110") from actual conversion characteristics
- Differential linearity error (unit: LSB)  
The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value
- Total error (unit: LSB)  
The difference between theoretical and actual conversion values



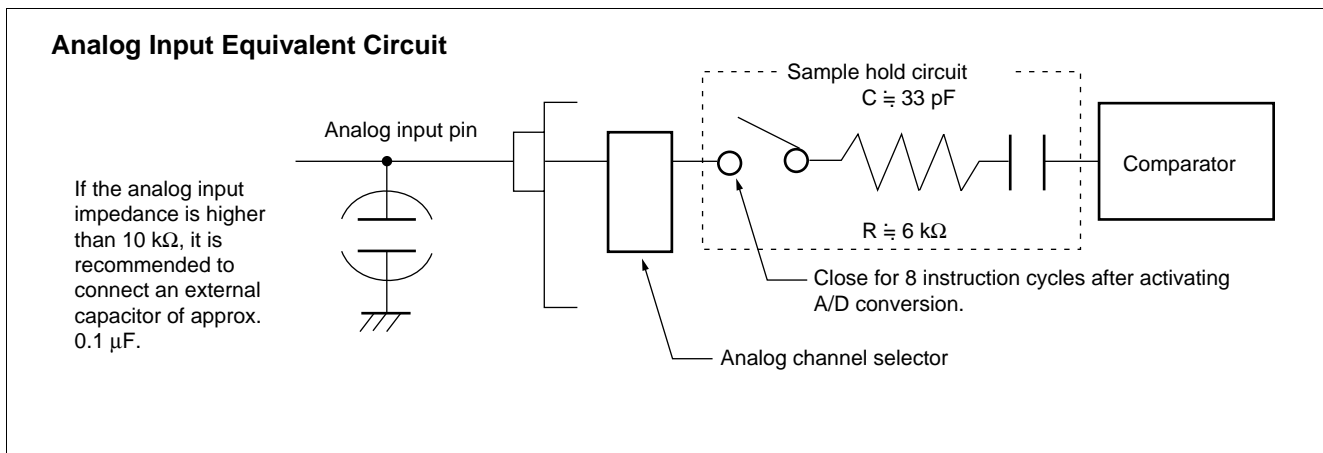
## (2) Precautions

### • Input impedance of the analog input pins

The A/D converter used for the MB89650AR series contains a sample hold circuit as illustrated below to fetch analog input voltage into the sample hold capacitor for eight instruction cycles after activating A/D conversion.

For this reason, if the output impedance of the external circuit for the analog input is high, analog input voltage might not stabilize within the analog input sampling period. Therefore, it is recommended to keep the output impedance of the external circuit low (below 10 k $\Omega$ ).

Note that if the impedance cannot be kept low, it is recommended to connect an external capacitor of about 0.1  $\mu$ F for the analog input pin.



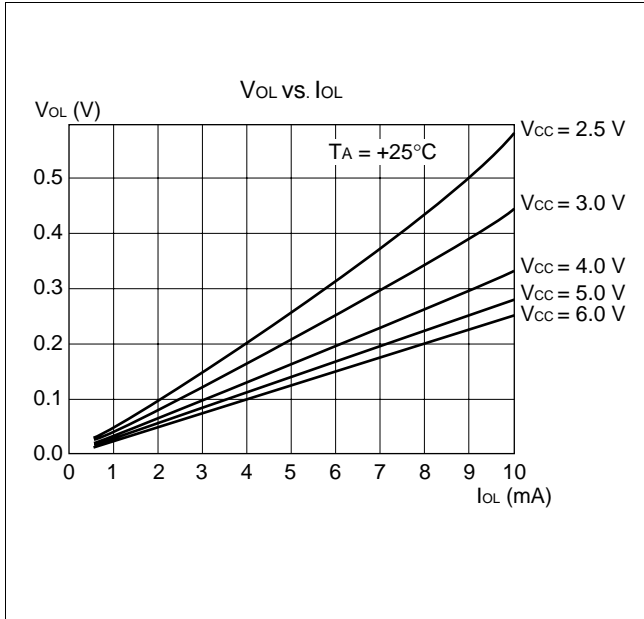
### • Error

The smaller the  $|AVR - AV_{SS}|$ , the greater the error would become relatively.

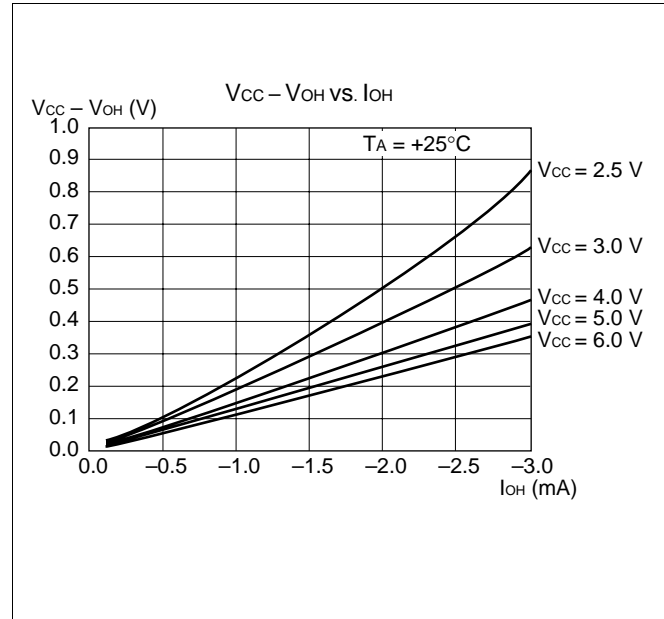
# MB89650AR Series

## ■ EXAMPLE CHARACTERISTICS

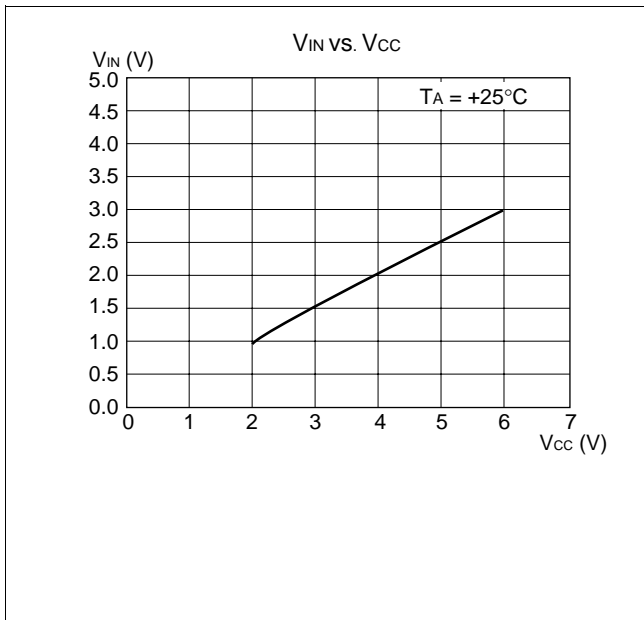
(1) "L" Level Output Voltage



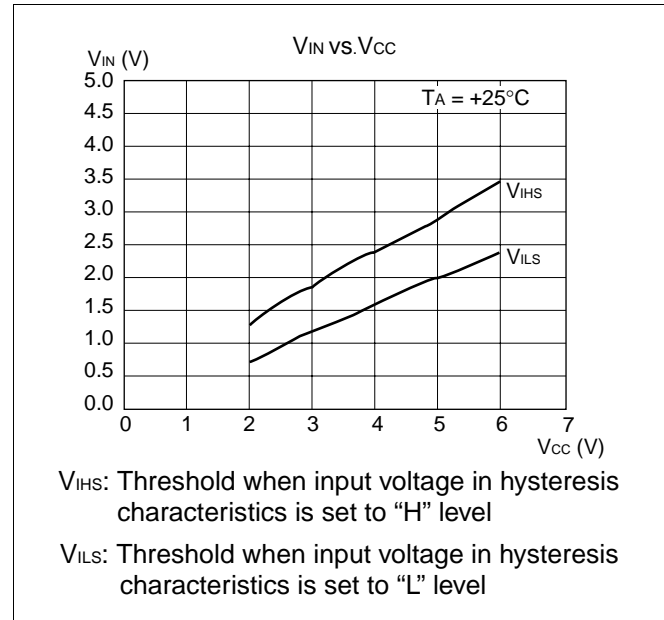
(2) "H" Level Output Voltage



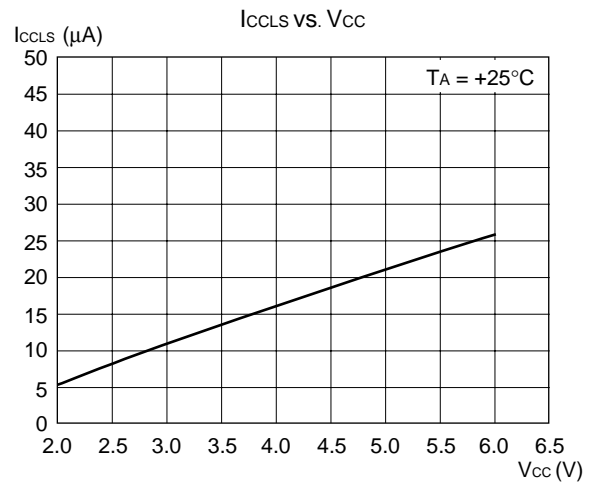
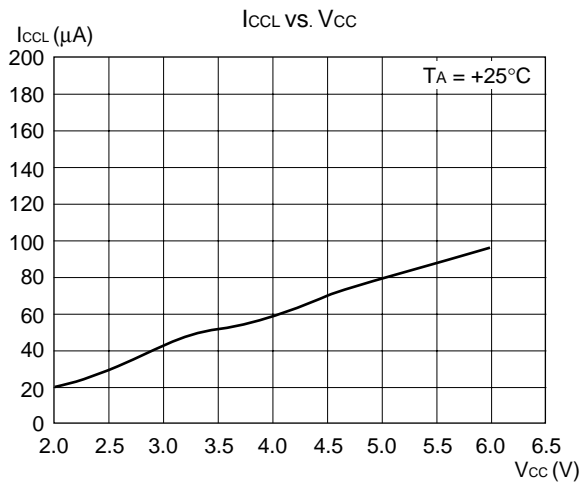
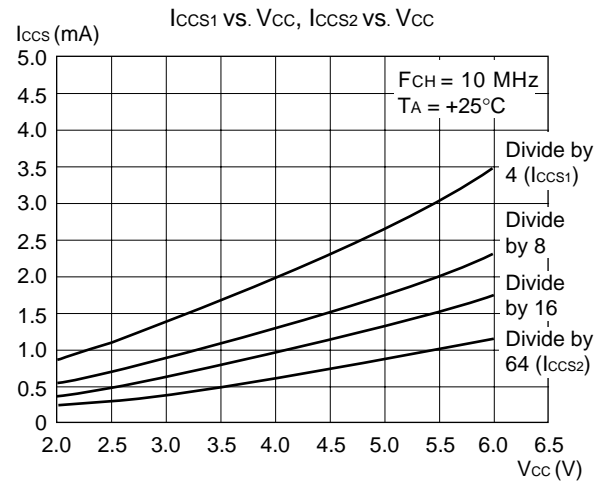
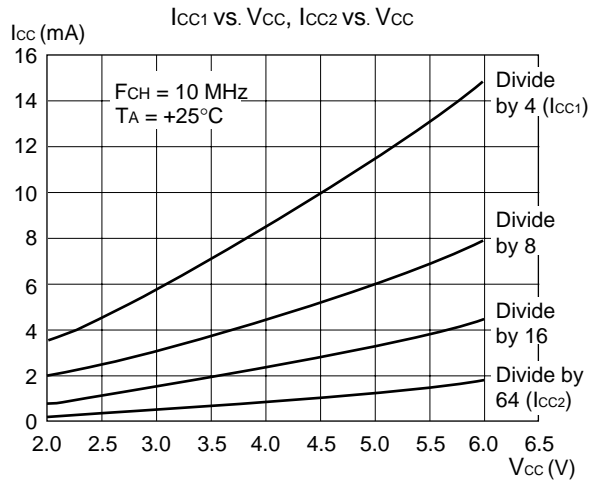
(3) "H" Level Input Voltage/"L" Level Input Voltage (CMOS Input)



(4) "H" Level Input Voltage/"L" Level Input Voltage (Hysteresis Input)



## (5) Power Supply Current (External Clock)

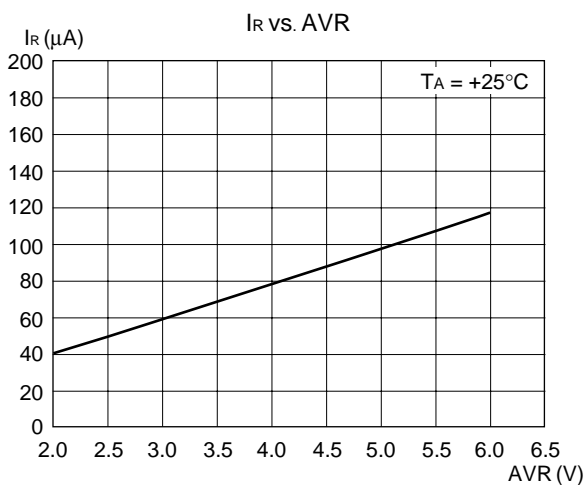
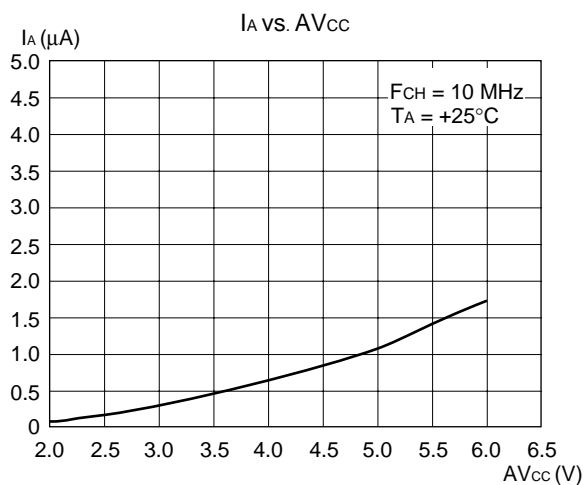
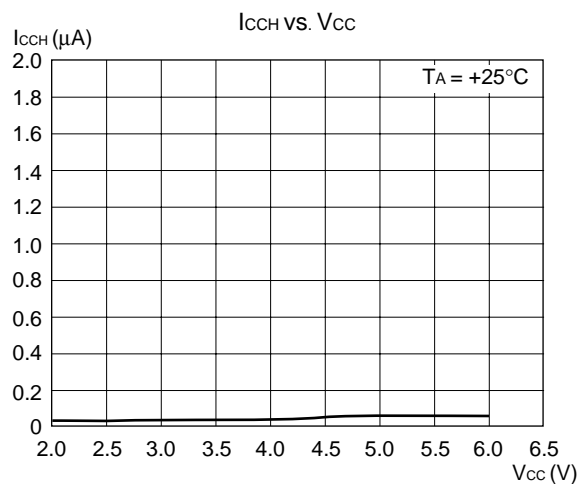
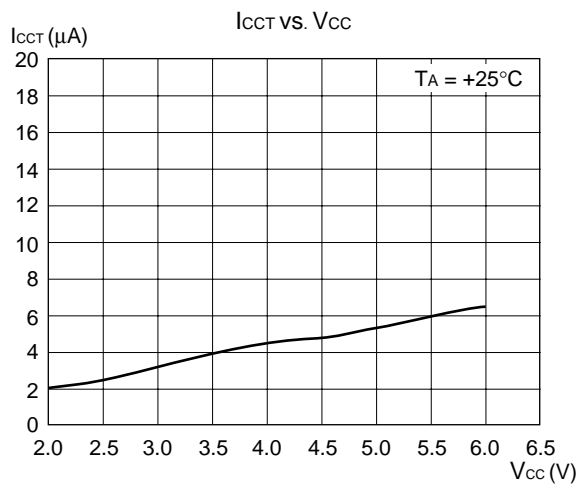


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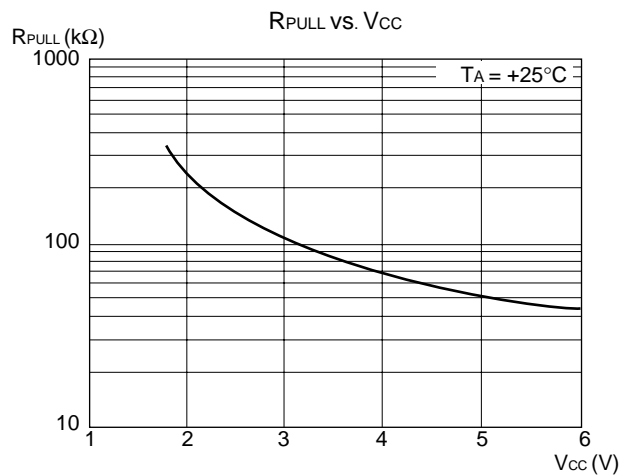


# MB89650AR Series

(Continued)



## (6) Pull-up Resistance



## ■ MASK OPTIONS

No.	Part number	MB89653AR MB89655AR MB89656AR MB89657AR	MB89P657A	MB89PV650A
	Specifying procedure	Specify when ordering masking	Set with EPROM programmer	Setting not possible
1	Pull-up resistors <div> <div>P00 to P07, P10 to P17, P20 to P22, P24 to P26, P30 to P37, P40 to P47, P60 to P67, P70 to P75, P80 to P81</div> </div>	Specify by pin	Can be set per pin. (Select in a group of four bits for P14 to P17, P40 to P43, and P40 to P47.) (P75 to P70 are available only for without a pull-up resistor.)	Fixed to without pull-up resistor
2	Power-on reset selection <div> <div>With power-on reset</div> <div>Without power-on reset</div> </div>	Selectable	With power-on reset	Fixed to with power-on reset
3	Selection of the oscillation stabilization time initial value <div> <div>Crystal oscillator: <math>2^{18}/F_{CH}</math> (Approx. 26.2 ms<sup>*1</sup>)</div> <div>Ceramic oscillator: <math>2^{13}/F_{CH}</math> (Approx. 26.2 ms<sup>*1</sup>)</div> </div>	Selectable	$2^{18}/F_{CH}$ (Approx. 26.2 ms <sup>*1</sup> )	Fixed to $2^{18}/F_{CH}$ (Approx. 26.2 ms <sup>*1</sup> )
4	Selection either single- or dual-clock system <div> <div>Single clock</div> <div>Dual clock</div> </div>	Selectable	Setting possible	Fixed to dual-clock system
5	Selection of a built-in booster*2 <div> <div>Without booster</div> <div>With booster (Segment output switching)</div> <div>16 segments: Selection of P30 to P37 and P40 to P47</div> <div>20 segments: Selection of P30 to P37 and P40 to P43</div> <div>24 segments: Selection of P30 to P37</div> <div>28 segments: Selection of P30 to P33</div> <div>32 segments: No port selection</div> </div>	Selectable	Can be selected from the following six options: -101: Without booster -102: 16 segments -103: 20 segments -104: 24 segments -105: 28 segments -106: 32 segments	Fixed to without booster

\*1 : The value at  $F_{CH} = 10 \text{ MHz}$

\*2 : On microcontrollers with a built-in booster, only 1/3 bias can be used. The 1/2 duty cannot be used.

Note : Reset is input asynchronized with the internal clock whether with or without power-on reset.

# MB89650AR Series

## ■ ORDERING INFORMATION

Part number	Package	Remarks
MB89653APFV MB89655APFV MB89656APFV MB89657APFV MB89P657APFV-101 MB89P657APFV-102 MB89P657APFV-103 MB89P657APFV-104 MB89P657APFV-105 MB89P657APFV-106	100-pin Plastic LQFP (FPT-100P-M05)	
MB89653APF MB89655APF MB89656APF MB89657APF MB89P657APF-101 MB89P657APF-102 MB89P657APF-103 MB89P657APF-104 MB89P657APF-105 MB89P657APF-106	100-pin Plastic QFP (FPT-100P-M06)	
MB89PV650ACF	100-pin Ceramic MQFP (MQP-100C-P02)	

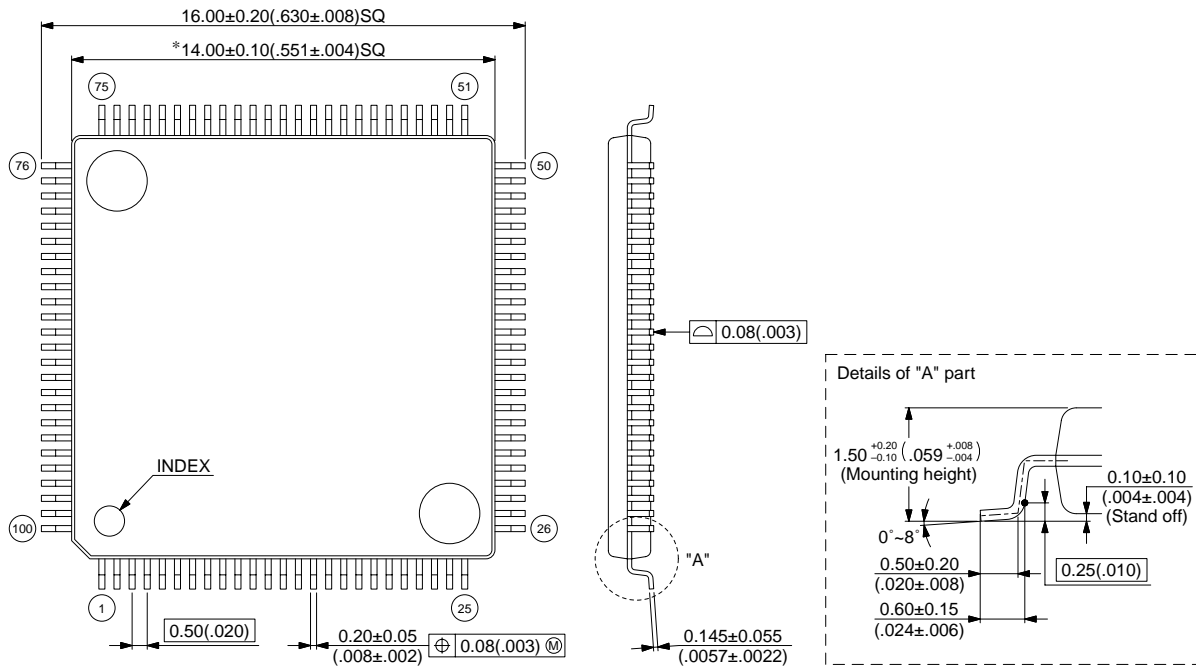
## ■ PACKAGE DIMENSIONS

100-pin plastic LQFP  
(FPT-100P-M05)

Note 1) \* : These dimensions do not include resin protrusion.

Note 2) Pins width and pins thickness include plating thickness.

Note 3) Pins width do not include tie bar cutting remainder.



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Dimensions in mm (inches) .

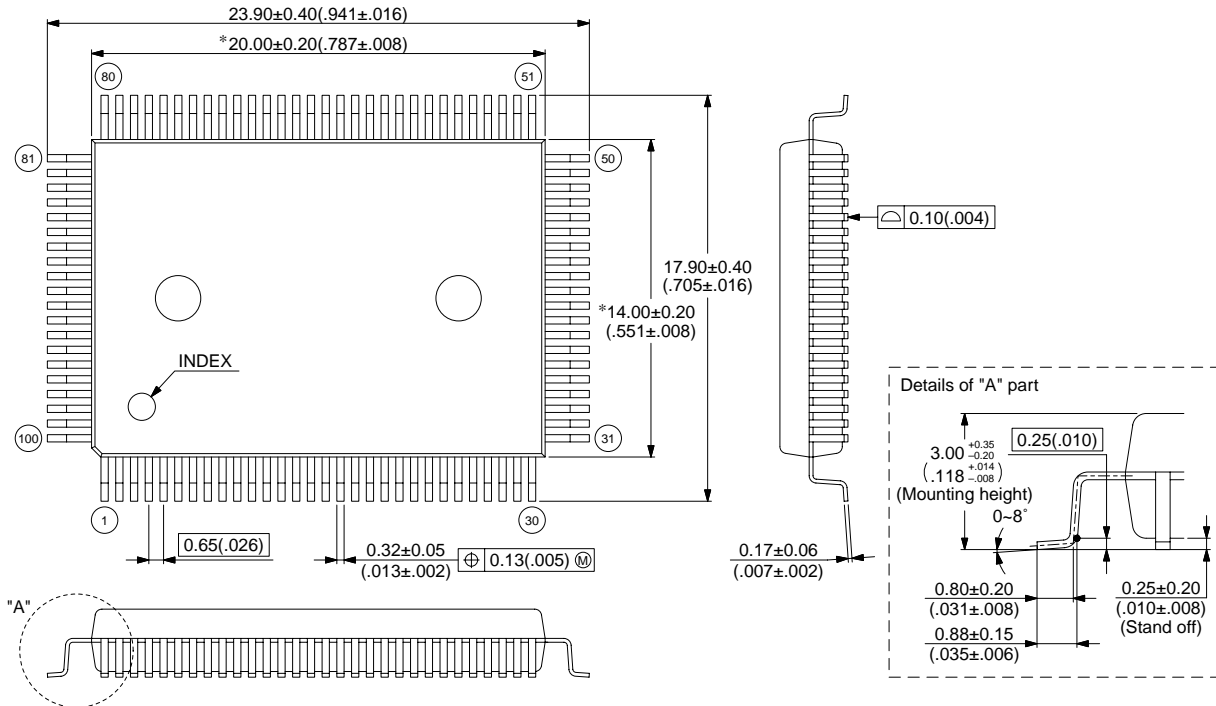
Note : The values in parentheses are reference values.

(Continued)

# MB89650AR Series

100-pin plastic QFP  
(FPT-100P-M06)

Note 1) \* : These dimensions do not include resin protrusion.  
Note 2) Pins width and pins thickness include plating thickness.  
Note 3) Pins width do not include tie bar cutting remainder.



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Dimensions in mm (inches) .

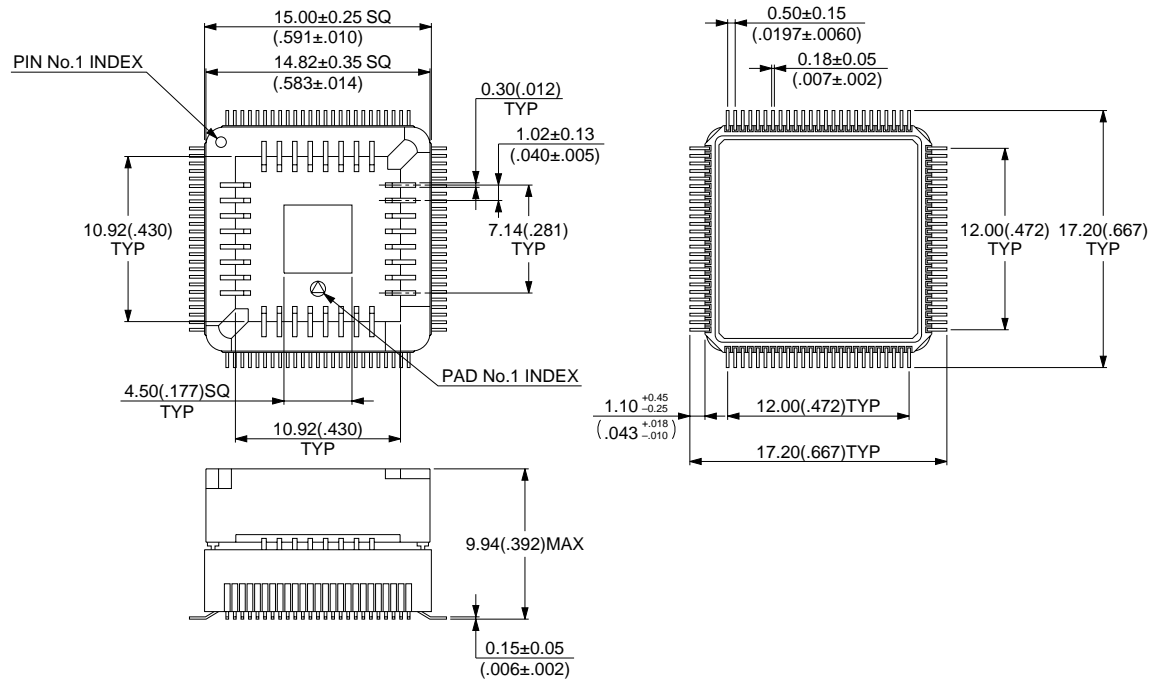
Note : The values in parentheses are reference values.

(Continued)

## MB89650AR Series

(Continued)

100-pin Ceramic MQFP  
(MQP-100C-P02)



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Dimensions in mm (inches) .

Note : The values in parentheses are reference values.

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