

Absolute Maximum Ratings

Supply Voltage (V_{DD} to GND).....	-0.3V to +22V
Any Other Pin to GND.....	-0.3V to (V_{DD} + 0.3V)
IN_+/IN_- (current)	±20mA
OUT_ (current)	1.3A
Continuous Power Dissipation (T_A = +70°C)	
SOT23 (derate 3.7mW/°C above +70°C).....	297.4mW
μMAX-EP (derate 12.9mW/°C	
above +70°C)	1030.9mW
TDFN-EP (derate 23.8mW/°C	
above +70°C)	1951.2mW

Operating Temperature Range.....	-40°C to +125°C
Junction Temperature.....	+150°C
Storage Temperature Range.....	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Soldering Temperature (reflow).....	+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

SOT23

Package Code	Z5+2A
Outline Number	21-0113
Land Pattern Number	90-0241
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	146.4
Junction to Case (θ_{JC})	93.5

μMAX®-EP

Package Code	U8E+2
Outline Number	21-0107
Land Pattern Number	90-0145
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	97
Junction to Case (θ_{JC})	5
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	77.6
Junction to Case (θ_{JC})	5

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Package Information (continued)

TDFN-EP

Package Code	T833+2
Outline Number	21-0137
Land Pattern Number	90-0059
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	54
Junction to Case (θ_{JC})	8
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	41
Junction to Case (θ_{JC})	8

Electrical Characteristics

($V_{DD} = 19V$, $V_{GND} = 0V$, $V_{CM} = V_{OUT} = V_{DD}/2$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{DD}	Guaranteed by PSRR	6		20	V
Quiescent Current	I_{DD}	Per channel		3.7	8	mA
High Output Voltage	V_{OH}	$I_H = +5mA$, $V_{IN} = V_{DD}$	$V_{DD} - 0.30$	$V_{DD} - 0.05$		V
Low Output Voltage	V_{OL}	$I_L = -5mA$, $V_{IN} = 0V$		0.05	0.30	V
Input Offset Voltage	V_{OS}	$T_A = +25^\circ C$	-14	3.5	+14	mV
		$T_A = -40^\circ C$ to $+125^\circ C$	-17		+17	
Load Regulation	LR	$I_{OUT} = 0mA$ to $-80mA$		+0.2		mV/mA
		$I_{OUT} = 0mA$ to $+80mA$		-0.2		
Input Bias Current	I_{FB}	At $V_{IN} = 9.5V$		0.01	1	μA
Voltage Gain	A_V	$R_L = 10k\Omega$, $C_L = 50pF$	0.99		1.01	V/V
Power-Supply Rejection Ratio	PSRR	$V_{DD} = 6V$ to $20V$, $V_{CM} = V_{OUT} = 3V$	70	95		dB
Common-Mode Input Voltage Range	CMVR	Inferred from CMRR test	0.5		$V_{DD} - 0.5$	V
Common-Mode Rejection Ratio	CMRR	$0.5V \leq V_{CM} \leq V_{DD} - 0.5V$	60	80		dB
Continuous Output Current	I_O	$V_{OUT} = 9.5V$ (Note 2)	MAX9650AZK+		20	mA
			MAX9650AUA+		80	
		$V_{DD} = 15V$, $V_{OUT} = 7.5V$	MAX9650ATA+		± 350	
Transient Peak Output Current	I_{PK}	(Note 3)		± 1.3		A
Bandwidth	BW	-3dB		35		MHz

Electrical Characteristics (continued)

($V_{DD} = 19V$, $V_{GND} = 0V$, $V_{CM} = V_{OUT} = V_{DD}/2$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Slew Rate	SR	4V step, $C_L = 50pF$, $R_L = 10k\Omega$, $A_V = +1V/V$		40		V/ μs
Settling Time	t_S	Settling to 0.1% of V_{OUT} , $I_L = 0$ to 1000mA, $R_S = 2.2\Omega$, $C_S = 0.1\mu F$ (Figure 1)		2.0		μs
Maximum Load Capacitance	C_{LOAD}	(Note 4)		150		nF
Noninverting Input Resistance	R_{IN+}	(Note 5)		100		M Ω
Inverting Input Resistance	R_{IN-}	(Note 5)		100		M Ω
Input Capacitance	C_{IN}			3		pF
Thermal Shutdown				+170		$^\circ C$
Thermal Shutdown Hysteresis				15		$^\circ C$

Note 1: All devices are 100% production tested at $T_A = +25^\circ C$. All temperature limits are guaranteed by design.

Note 2: Continuous output current is tested with one output at a time.

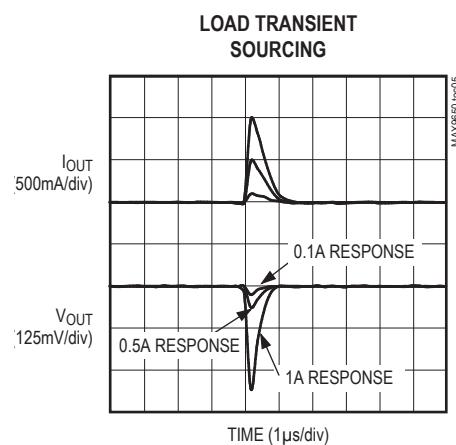
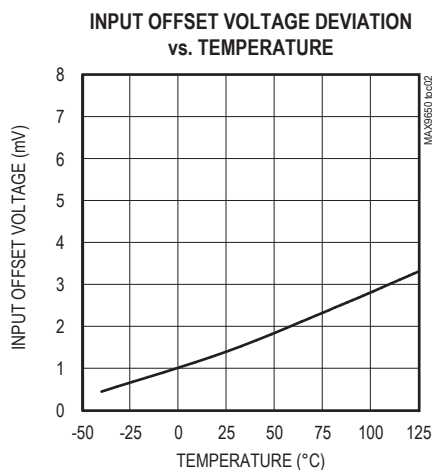
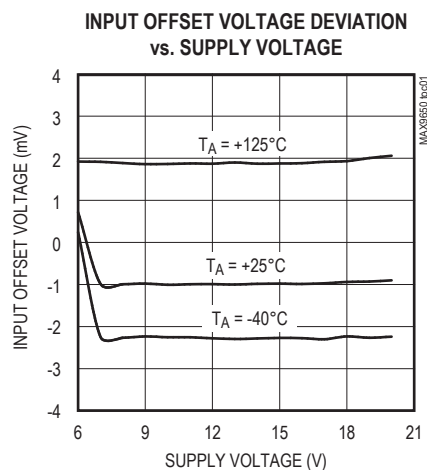
Note 3: See the [Thermal Shutdown with Temperature Hysteresis](#) section.

Note 4: A series resistor can extend load capacitance range. The settling time can be optimized by a small series resistance. See the [Applications Information](#) section for more information.

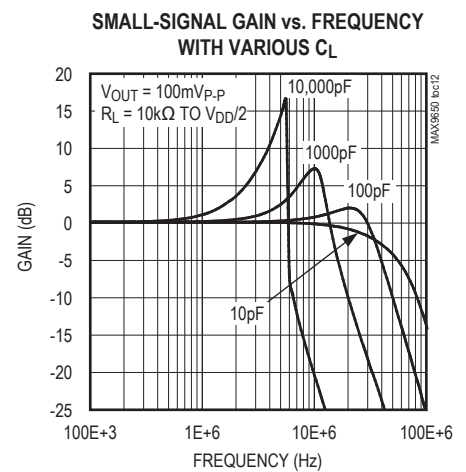
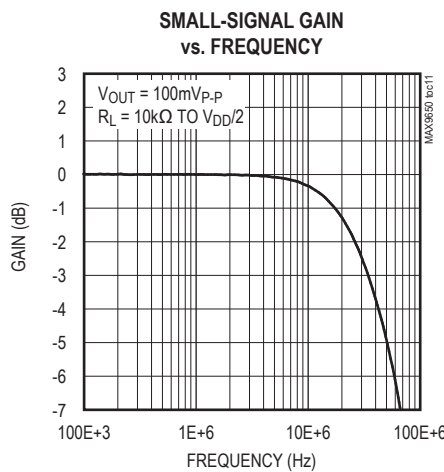
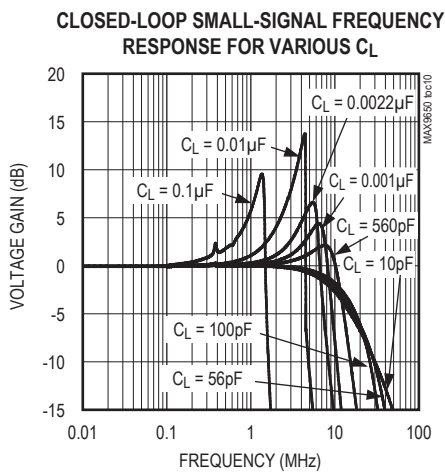
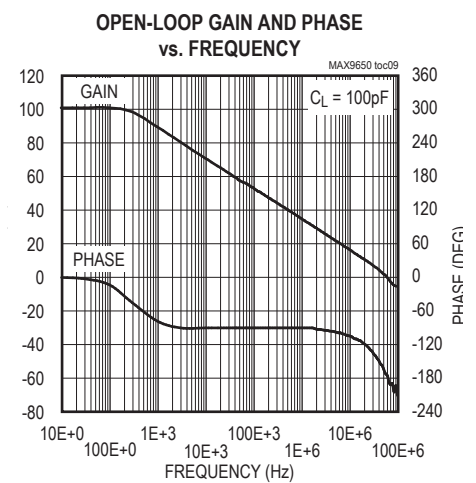
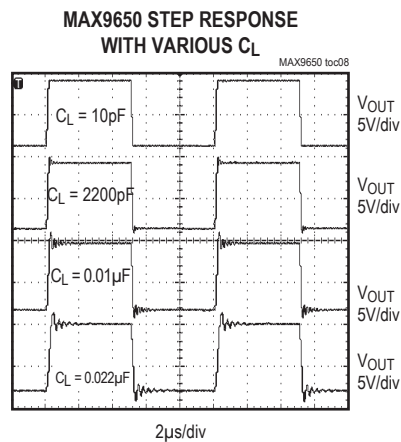
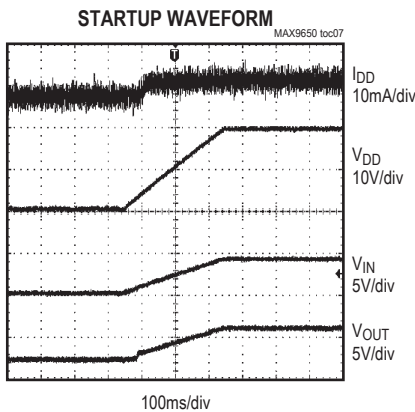
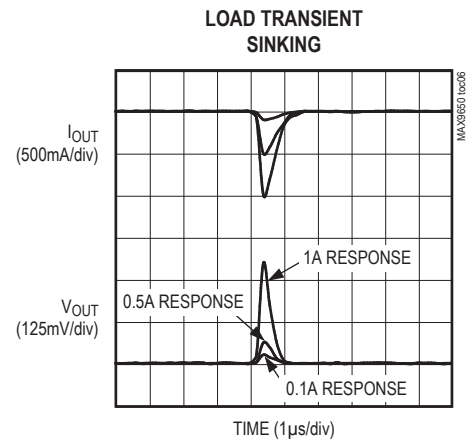
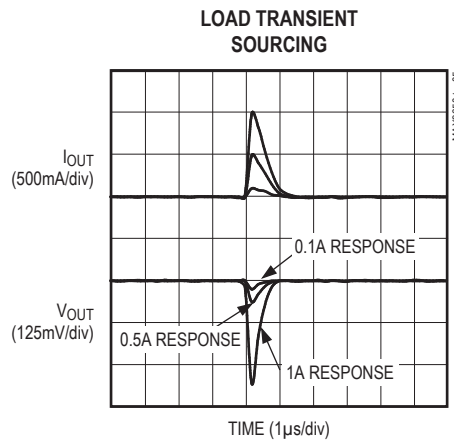
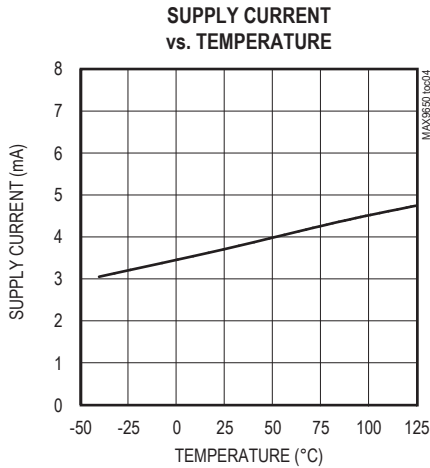
Note 5: Inputs are protected by back-to-back diodes.

Typical Operating Characteristics

($V_{DD} = 19V$, $GND = 0$, $V_{CM} = V_{OUT} = V_{DD}/2$, $T_A = +25^\circ C$, unless otherwise specified.)



Typical Operating Characteristics (continued)

(V_{DD} = 19V, GND = 0, V_{CM} = V_{OUT} = V_{DD}/2, T_A = +25°C, unless otherwise specified.)

Pin Description

PIN			NAME	FUNCTION
MAX9650		MAX9651 (μMAX-EP, TDFN-EP)		
SOT23	μMAX-EP, TDFN-EP			
1	6	1	OUTA	VCOM Output A
2	4	4	GND	Ground
3	3	3	INA+	Positive Input A
4	2	2	INA-	Negative Input A
5	7	8	V _{DD}	Positive-Supply Input. Bypass V _{DD} to GND with a 0.1μF capacitor as close as possible to the device.
—	—	5	INB+	Positive Input B
—	—	6	INB-	Negative Input B
—	—	7	OUTB	VCOM Output B
—	1, 5, 8	—	N.C.	No Connection. Not internally connected.
—	—	—	EP	Exposed Pad (μMAX and TDFN Only). EP is internally connected to GND. Connect EP to GND.

Detailed Description

The MAX9650/MAX9651 operational rail-to-rail input/output amplifiers hold the VCOM voltage stable while providing the ability to source and sink a high current quickly (1.3A) into a capacitive load such as the backplane of a TFT-LCD panel.

Thermal Shutdown with Temperature Hysteresis

The MAX9650/MAX9651 are capable of high output currents and feature thermal-shutdown protection with temperature hysteresis. When the die temperature reaches +170°C, the device shuts down. When the die cools down by 15°C, the device turns on again. In a TFT-LCD application, the duty cycle is very low. Even with high values of voltage and current, the power dissipation is low and the chip does not shut down.

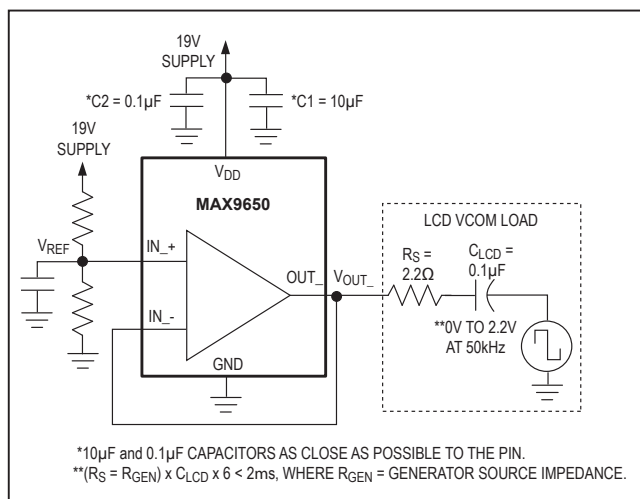


Figure 1. Settling Time Test Circuit

Applications Information

Output Load

The MAX9650/MAX9651 are designed to drive capacitive loads. A small value of series resistance improves the performance of the device to ensure stability and fast settling with very large or very small capacitive loads. In many cases, this resistance is already present due to connection resistance in the wiring and no additional physical resistor is necessary. For minimum series resistance required for stability with capacitive loading, see [Figure 2](#).

Power Supplies and Bypass Capacitors

The MAX9650/MAX9651 operate from a 6V to 20V single supply or from $\pm 4.5\text{V}$ to $\pm 10\text{V}$ dual supplies. Proper supply bypassing ensures stability while driving high

transient loads. The MAX9650/MAX9651 require a minimum $10\mu\text{F}$ (C1) and $0.1\mu\text{F}$ (C2) power-supply bypass capacitors placed as close as possible to the power-supply pin (V_{DD}). See [Figure 3](#). For dual-supply operation, use $10\mu\text{F}$ and $0.1\mu\text{F}$ bypass capacitors on both supplies (V_{DD} and GND) with each capacitor placed as close as possible to V_{DD} and GND.

Layout and Grounding

The exposed pad on the μMAX and TDFN packages provides a low thermal resistance for heat dissipation. Solder the exposed pad to a ground plane for best thermal performance. Do not route traces under these packages. For dual-supply operation, the exposed pad (EP) can be electrically connected to the negative supply or it can be left unconnected.

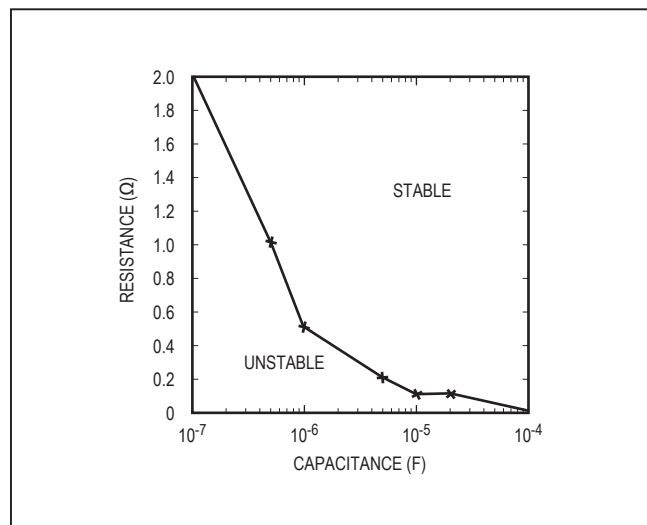


Figure 2. Minimum Combined ESR/Series/Trace Resistance Required for Stability of the MAX9650 in Response to Capacitive Loads

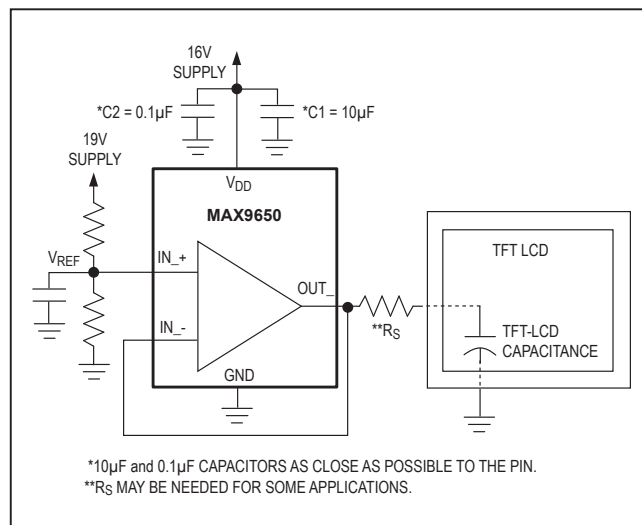
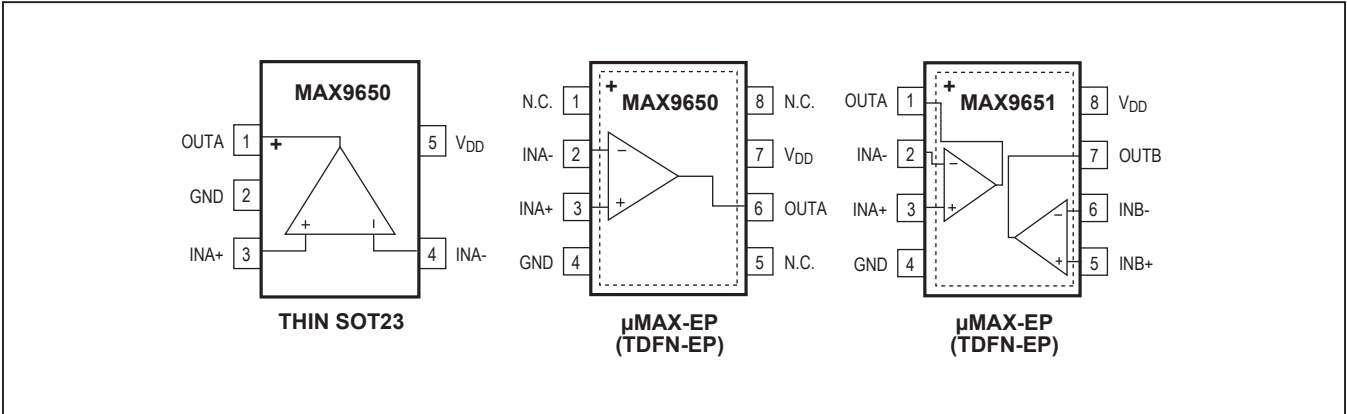


Figure 3. Typical TFT-LCD Backplane Drive Circuit

Pin Configurations



Ordering Information

PART	AMPS PER PACKAGE	PIN-PACKAGE	TOP MARK
MAX9650AZK+	1	5 SOT23	ADSI
MAX9650AZK/V+	1	5 SOT23	ADSK
MAX9650AUA+	1	8 μMAX-EP*	AABI
MAX9650ATA+	1	8 TDFN-EP*	BKX
MAX9651AUA+	2	8 μMAX-EP*	AABH
MAX9651ATA+	2	8 TDFN-EP*	BKY

Note: All devices are specified over the -40°C to +125°C operating range.

+Denotes a lead(Pb)-free/RoHS-compliant package.

/V denotes an automotive qualified part.

*EP = Exposed pad.

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/08	Initial release	—
1	10/08	Updated slew rate and added TDFN-EP package	1, 2, 6, 10, 11
2	5/09	Updated continuous output current specification	2
3	2/10	Added automotive part to Ordering Information , corrected units for input offset voltage, and added figure for minimum series resistance	1, 2, 5, 6
4	7/10	Removed extraneous information in the Electrical Characteristics table and corrected typo in TOC 5	2, 4
5	11/12	Corrected lead pattern number	8
6	3/18	Added new Package Information tables, deleted Package Information table/diagrams from end of data sheet, and moved Ordering Information to end of data sheet	1, 2, 8–12
7	12/18	Updated Package Information table for SOT23	2
8	1/19	Updated Package Information table for SOT23	2

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

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