Quad Bus LVDS Driver with Flow-Through Pinout

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +4.0V
IN_, EN, $\overline{EN}$ to GND.....-0.3V to (V_{CC} + 0.3V)
OUT_+, OUT_- to GND.....-0.3V to +4.0V
Short-Circuit Duration (OUT_+, OUT_-) .....Continuous
Continuous Power Dissipation (T_A = +70°C)
16-Pin QFN (derate 18.5mW/°C above +70°C) 1481mW
16-Pin TSSOP (derate 9.4mW/°C above +70°C) 755mW
Storage Temperature Range .....-65°C to +150°C
Maximum Junction Temperature .....+150°C
Operating Temperature Range .....-40°C to +85°C
ESD Protection
Human Body Model, OUT_+, OUT_- .....±8kV
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, R_L = 27Ω ±1%, EN = high, $\overline{EN}$ = low, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BLVDS OUTPUTS (OUT_+, OUT_-)						
Differential Output Voltage	V_{OD}	Figure 1	250	371	450	mV
Change in Magnitude of V_{OD} Between Complementary Output States	ΔV_{OD}	Figure 1		1	25	mV
Offset Voltage	V_{OS}	Figure 1	1.125	1.29	1.375	V
Change in Magnitude of V_{OS} Between Complementary Output States	ΔV_{OS}	Figure 1		5	25	mV
Output High Voltage	V_{OH}			1.465	1.6	V
Output Low Voltage	V_{OL}		0.90	1.085		V
Differential Output Short-Circuit Current	I_{OSD}	V_{OD} = 0			20	mA
Output Short-Circuit Current	I_{OS}	OUT_+ = 0 at IN_ = V_{CC} or OUT_- = 0 at IN_ = 0			-20	mA
Output High-Impedance Current	I_{OZ}	Disabled, OUT_+ = 0 or V_{CC}, OUT_- = 0 or V_{CC}	-1		1	µA
Power-Off Output Current	I_{OFF}	V_{CC} = 0 or open, EN = $\overline{EN}$ = IN_ = 0, OUT_+ = 0 or 3.6V, OUT_- = 0 or 3.6V	-1		1	µA
Output Capacitance	C_{OUT}	Capacitance from OUT_+ or OUT_- to GND		4.3		pF
INPUTS (IN_, EN, $\overline{EN}$)						
High-Level Input Voltage	V_{IH}		2.0		V_{CC}	V
Low-Level Input Voltage	V_{IL}		GND		0.8	V
Input Current	I_{IN}	IN_, EN, $\overline{EN}$ = 0 or V_{CC}	-15		15	µA
SUPPLY CURRENT						
Supply Current	I_{CC}	R_L = 27Ω, IN_ = V_{CC} or 0 for all channels		58	70	mA
Disabled Supply Current	I_{CCZ}	Disabled		3.2	5	mA

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AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, R_L = 27Ω ±1%, C_L = 15pF, EN = high, $\overline{EN}$ = low, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.) (Notes 3, 4, 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Differential Propagation Delay High to Low	t_{PHLD}	Figures 2 and 3		1.0	1.98	3.0	ns
Differential Propagation Delay Low to High	t_{PLHD}	Figures 2 and 3		1.0	1.92	3.0	ns
Differential Pulse Skew (Note 6)	t_{SKD1}	Figures 2 and 3				300	ps
Differential Channel-to-Channel Skew (Note 7)	t_{SKD2}	Figures 2 and 3				450	ps
Differential Part-to-Part Skew (Note 8)	t_{SKD3}	Figures 2 and 3				1.2	ns
Differential Part-to-Part Skew (Note 9)	t_{SKD4}	Figures 2 and 3				2.0	ns
Rise Time	t_{TLH}	Figures 2 and 3	MAX9129EGE	0.60	1.19	1.55	ns
			MAX9129EUE	0.60	1.09	1.40	
Fall Time	t_{THL}	Figures 2 and 3	MAX9129EGE	0.60	1.12	1.55	ns
			MAX9129EUE	0.60	1.02	1.40	
Disable Time High to Z	t_{PHZ}	Figures 4 and 5				8	ns
Disable Time Low to Z	t_{PLZ}	Figures 4 and 5				8	ns
Enable Time Z to High	t_{PZH}	Figures 4 and 5				10	ns
Enable Time Z to Low	t_{PZL}	Figures 4 and 5				10	ns
Maximum Operating Frequency (Note 10)	f_{MAX}	Figure 2		100			MHz

Note 1: Maximum and minimum limits over temperature are guaranteed by design and characterization. Devices are 100% tested at T_A = +25°C.

Note 2: Current into the device is defined as positive, and current out of the device is defined as negative. All voltages are referenced to ground except V_{OD} and ΔV_{OD}.

Note 3: AC parameters are guaranteed by design and characterization.

Note 4: C_L includes probe and jig capacitance.

Note 5: Signal generator conditions: V_{OL} = 0, V_{OH} = V_{CC}, f = 100MHz, 50% duty cycle, R_O = 50Ω, t_R = t_F = 1ns (10% to 90%).

Note 6: t_{SKD1} is the magnitude difference of differential propagation delays. t_{SKD1} = | t_{PHLD} - t_{PLHD} |.

Note 7: t_{SKD2} is the magnitude difference of t_{PHLD} or t_{PLHD} of one channel to the t_{PHLD} or t_{PLHD} of another channel on the same device.

Note 8: t_{SKD3} is the magnitude difference of any differential propagation delays between devices at the same V_{CC} and within 5°C of each other.

Note 9: t_{SKD4} is the magnitude difference of any differential propagation delays between devices operating over the rated supply and temperature ranges.

Note 10: Signal generator conditions: V_{OL} = 0, V_{OH} = V_{CC}, f = 100MHz, 50% duty cycle, R_O = 50Ω, t_R = t_F = 1ns (10% to 90%). MAX9129 output criteria: duty cycle = 45% to 55%, V_{OD} ≥ 250mV, all channels switching.

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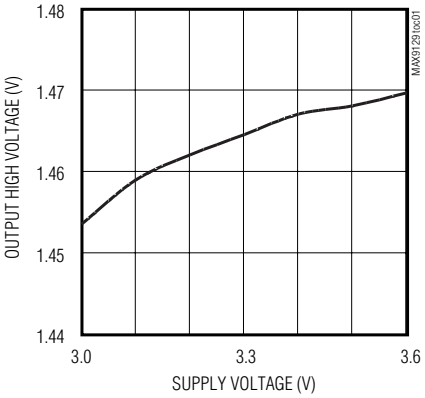
Quad Bus LVDS Driver with Flow-Through Pinout

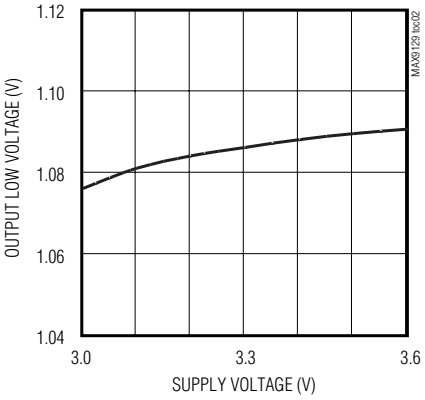
Typical Operating Characteristics

(MAX9129EUE (TSSOP package), V_{CC} = +3.3V, R_L = 27Ω, C_L = 15pF, T_A = +25°C, unless otherwise noted.) (Note 5)

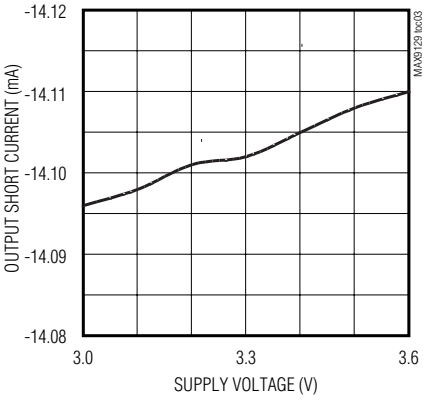
OUTPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



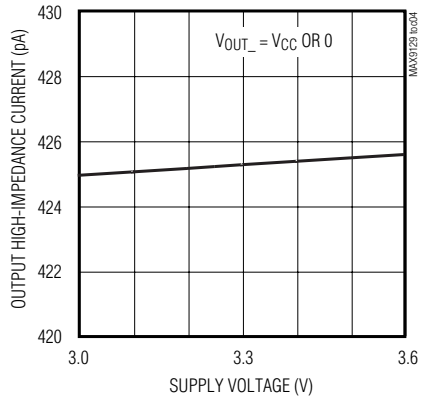
OUTPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



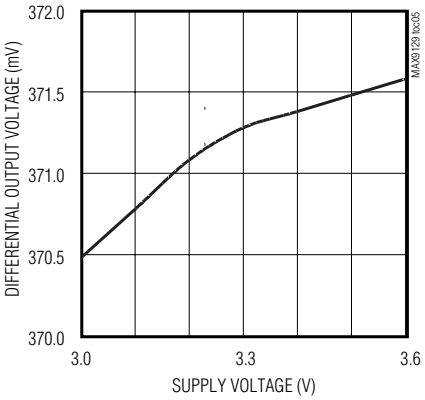
OUTPUT SHORT CURRENT (I_{OS}) vs. SUPPLY VOLTAGE



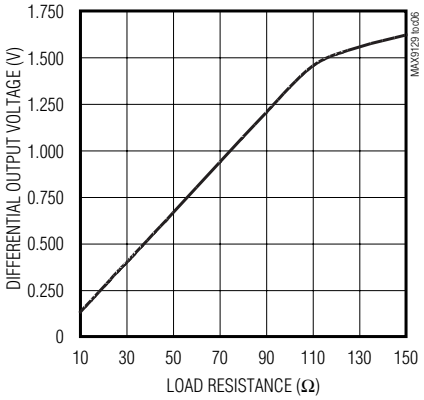
OUTPUT HIGH-IMPEDANCE CURRENT vs. SUPPLY VOLTAGE



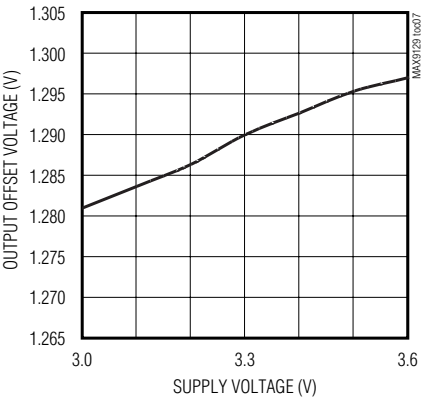
DIFFERENTIAL OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



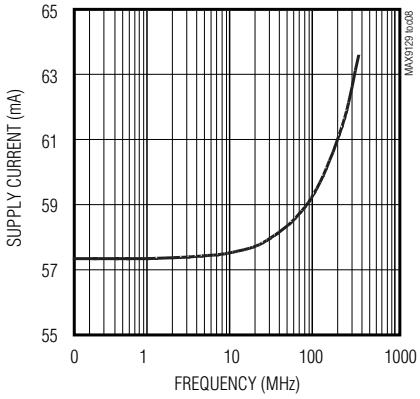
DIFFERENTIAL OUTPUT VOLTAGE vs. LOAD RESISTANCE



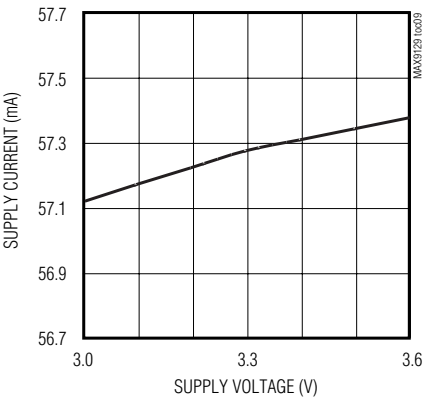
OUTPUT OFFSET VOLTAGE vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. FREQUENCY



SUPPLY CURRENT vs. SUPPLY VOLTAGE



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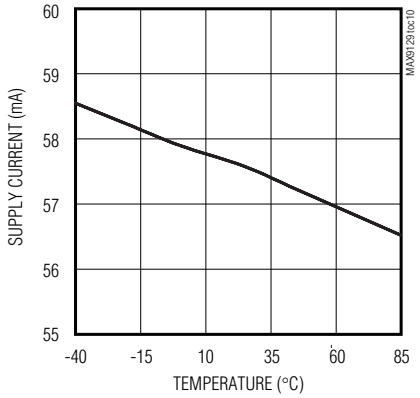
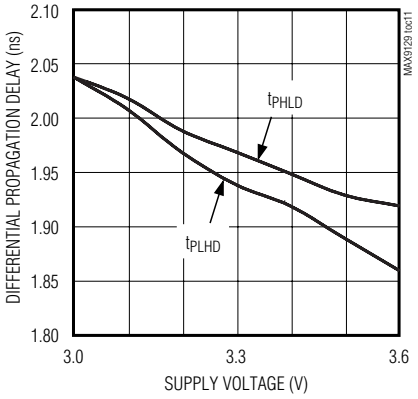
Typical Operating Characteristics (continued)

(MAX9129EUE (TSSOP package), V_{CC} = +3.3V, R_L = 27Ω, C_L = 15pF, T_A = +25°C, unless otherwise noted.) (Note 5)

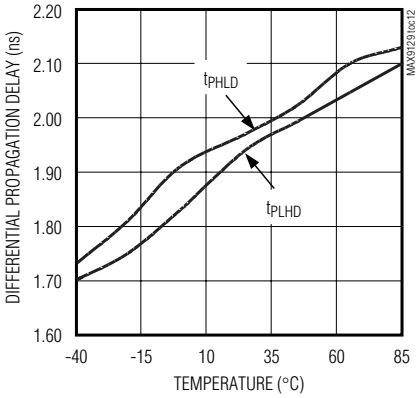
SUPPLY CURRENT vs. TEMPERATURE



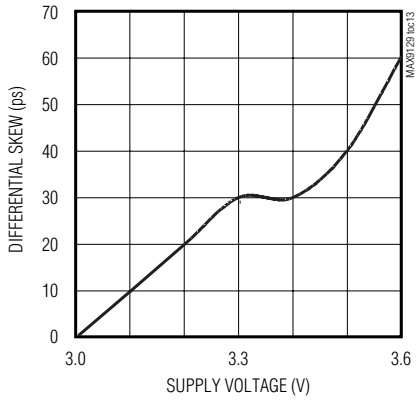
DIFFERENTIAL PROPAGAION DELAY vs. SUPPLY VOLTAGE



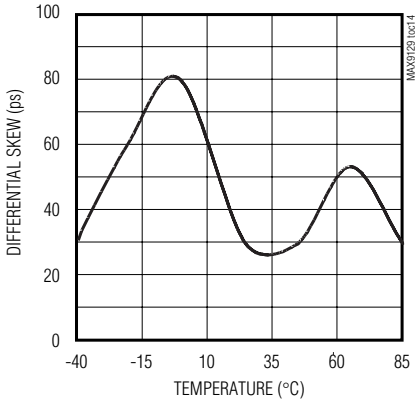
DIFFERENTIAL PROPAGATION DELAY vs. TEMPERATURE



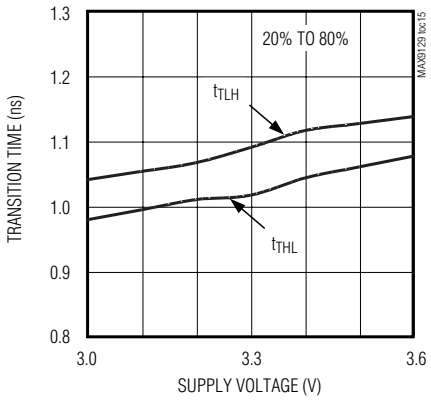
DIFFERENTIAL SKEW vs. SUPPLY VOLTAGE



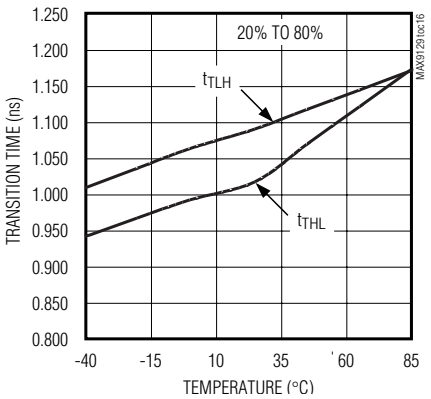
DIFFERENTIAL SKEW vs. TEMPERATURE



TRANSITION TIME vs. SUPPLY VOLTAGE



TRANSITION TIME vs. TEMPERATURE



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Quad Bus LVDS Driver with Flow-Through Pinout

Pin Description

PIN		NAME	FUNCTION
QFN	TSSOP		
15	1	EN	LVTTL/LVCMOS Enable Input. The driver is disabled when EN is low. EN is internally pulled down. When EN = high and $\overline{EN}$ = low or open, the outputs are active. For other combinations of EN and $\overline{EN}$, the outputs are disabled and are high impedance.
1, 4, 5, 16	2, 3, 6, 7	IN_	LVTTL/LVCMOS Driver Inputs
2	4	V_{CC}	Power-Supply Input. Bypass V_{CC} to GND with 0.1µF and 0.001µF ceramic capacitors.
3	5	GND	Ground
6	8	$\overline{EN}$	LVTTL/LVCMOS Enable Input. The driver is disabled when $\overline{EN}$ is high. $\overline{EN}$ is internally pulled down.
7, 10, 11, 14	9, 12, 13, 16	OUT_-	Inverting BLVDS Driver Outputs
8, 9, 12, 13	10, 11, 14, 15	OUT_+	Noninverting BLVDS Driver Outputs

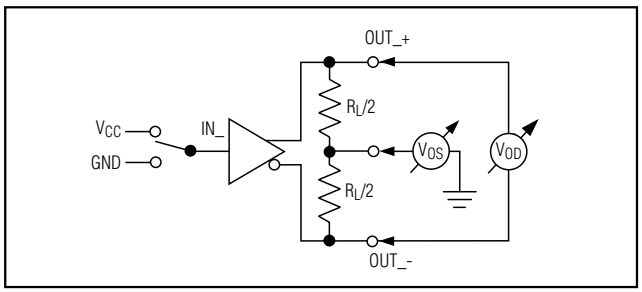

Figure 1. Driver V_{OD} and V_{OS} Test Circuit

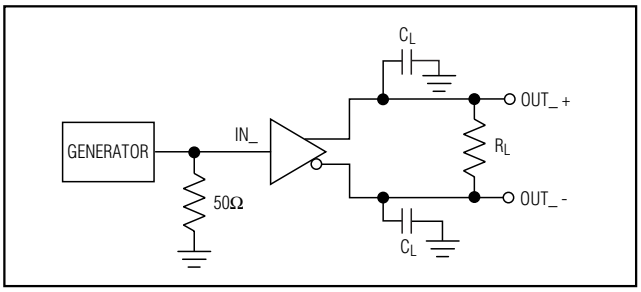

Figure 2. Driver Propagation Delay and Transition Time Test Circuit

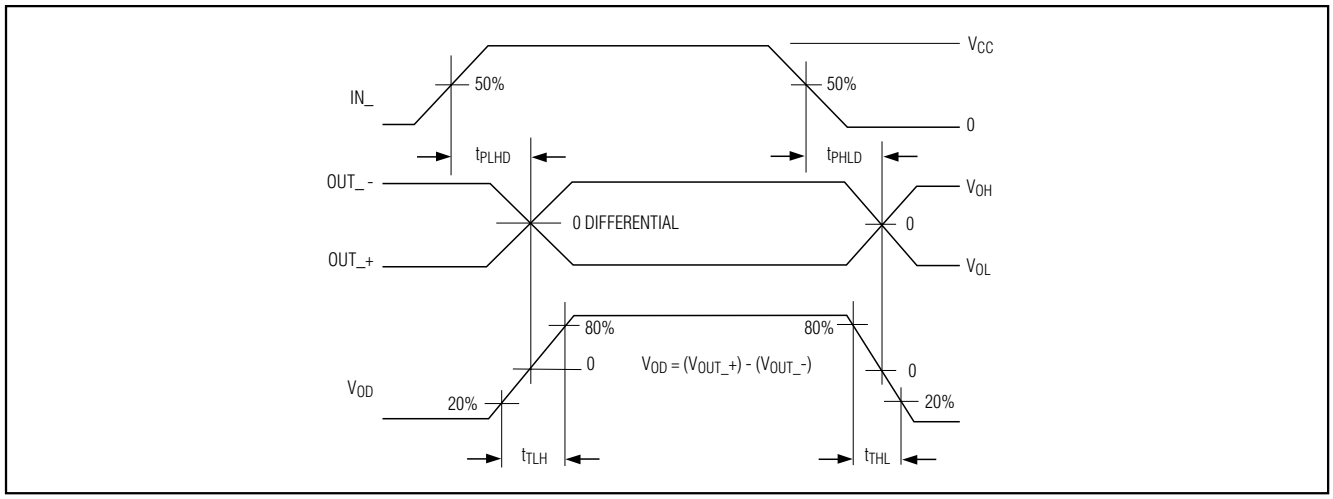

Figure 3. Driver Propagation Delay and Transition Time Waveforms

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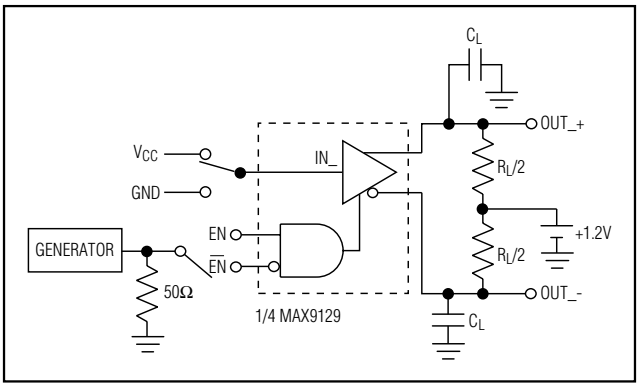

Figure 4. Driver High-Impedance Delay Test Circuit

Table 1. Input/Output Function Table

ENABLES		INPUTS	OUTPUTS	
EN	$\overline{EN}$	IN_	OUT_+	OUT_ -
H	L or open	L	L	H
		H	H	L
All other combinations of EN and $\overline{EN}$		X	Z	Z

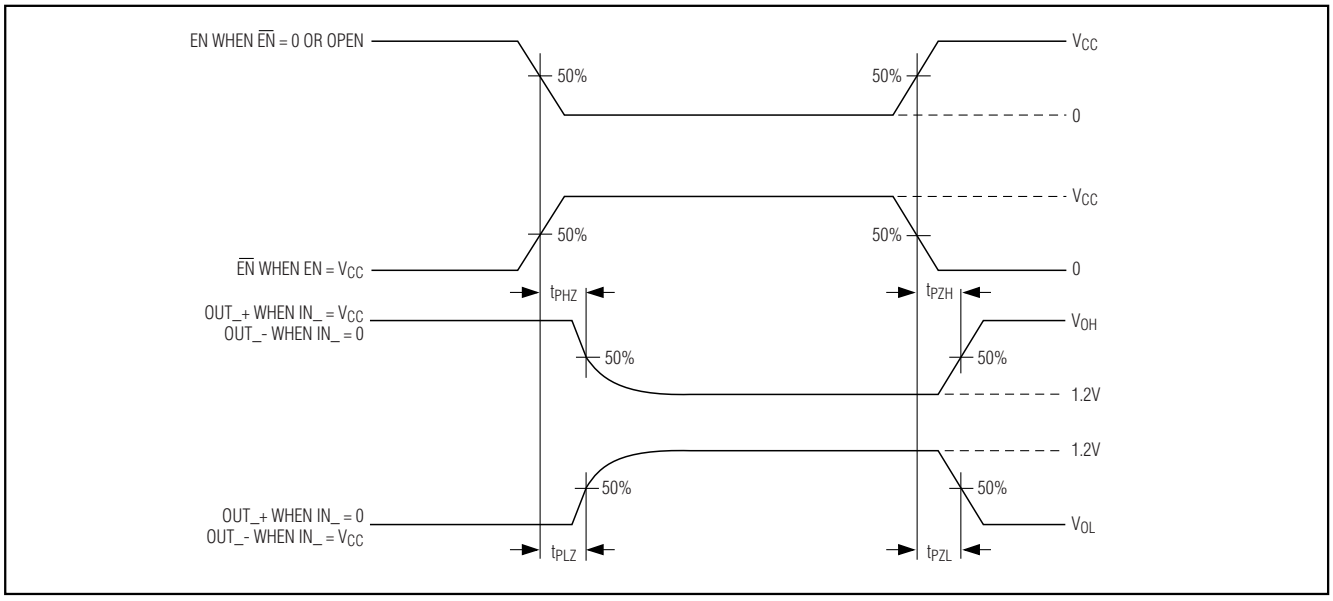

Figure 5. Driver High-Impedance Delay Waveform

Detailed Description

The MAX9129 is a 200Mbps quad differential BLVDS driver designed for multipoint, heavily loaded backplane applications. This device accepts LVTTL/LVCMOS input levels and translates them to output levels of 250mV to 450mV into a 27Ω load. The flow-through pinout simplifies board layout and reduces the potential for crosstalk between single-ended inputs and differential outputs. Transition times are designed to reduce reflections, yet enable high data rates. The MAX9129 can be used in conjunction with standard quad LVDS receivers, such as the MAX9121, to implement full-duplex multipoint buses more efficiently than with transceivers.

Effect of Capacitive Loading

The characteristic impedance of a differential PC board trace is uniformly reduced when equal capacitive loads are attached at equal intervals (provided the transition time of the signal being driven on the trace is longer than the delay between loads). This kind of loading is typical of multipoint buses where cards are attached at 1in or 0.8in intervals along the length of a backplane.

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Quad Bus LVDS Driver with Flow-Through Pinout

The reduction in characteristic impedance is approximated by the following formula:

$$Z_{DIFF\text{-}loaded} = Z_{DIFF\text{-}unloaded} \times SQRT\ [C_O / (C_O + N \times C_L / L)]$$

where:

$Z_{DIFF\text{-}unloaded}$ = unloaded differential characteristic impedance

C_O = unloaded trace capacitance (pF/unit length)

C_L = value of each capacitive load (pF)

N = number of capacitive loads

L = trace length

For example, if C_O = 2.5pF/in, C_L = 10pF, N = 18, L = 18in, and $Z_{DIFF\text{-}unloaded}$ = 120Ω, the loaded differential impedance is:

$$Z_{DIFF\text{-}loaded} = 120\Omega \times SQRT\ [2.5pF / (2.5pF + 18 \times 10pF/18in)]$$

$$Z_{DIFF\text{-}loaded} = 54\Omega$$

In this example, capacitive loading reduces the characteristic impedance from 120Ω to 54Ω. The load seen by a driver located on a card in the middle of the bus is 27Ω because the driver sees two 54Ω loads in parallel. A typical LVDS driver (rated for a 100Ω load) would not develop a large enough differential signal to be reliably detected by an LVDS receiver. Maxim's BLVDS driver is designed and specified to drive a 27Ω load to differential voltage levels of 250mV to 450mV (which are standard LVDS driver levels). A standard LVDS receiver is able to detect this level of differential signal.

Short extensions off the bus, called stubs, contribute to capacitive loading. Keep stubs less than 1in for a good balance between ease of component placement and good signal integrity.

The MAX9129 is a current source driver and drives larger differential signal levels into loads higher than 27Ω and smaller levels into loads less than 27Ω (see typical operating curves). To keep loading from reducing bus impedance below the rated 27Ω load, PC board traces can be designed for higher unloaded characteristic impedance.

Effect of Transition Time

For transition times (measured from 0% to 100%) shorter than the delay between capacitive loads, the loads are seen as low-impedance discontinuities from which the driven signal is reflected. Reflections add and subtract from the signal being driven and cause decreased noise margin and jitter. The MAX9129 is designed for a minimum transition time of 1ns (rated 0.6ns from 20% to 80%, or about 1ns 0% to 100%) to reduce reflections while being fast enough for high-speed backplane data transmission.

Power-On Reset

The power-on reset voltage of the MAX9129 is typically 2.25V. When the supply falls below this voltage, the device is disabled and the outputs are in high impedance.

Applications Information

Power-Supply Bypassing

Bypass V_{CC} with high-frequency, surface-mount ceramic 0.1µF and 0.001µF capacitors in parallel as close to the device as possible, with the smaller valued capacitor closest to V_{CC}.

Termination

In the example above, the loaded differential impedance of the bus is reduced to 54Ω. Since it can be driven from any card position, the bus must be terminated at each end. A parallel termination of 54Ω at each end of the bus placed across the traces that make up the differential pair provides a proper termination. The total load seen by the driver is 27Ω.

The MAX9129 drives higher differential signal levels into lighter loads. A multidrop bus with the driver at one end and receivers connected at regular intervals along the bus has a lowered impedance due to capacitive loading. Assuming the same impedance calculated in the multidrop example above (54Ω), the multidrop bus can be terminated with a single, parallel-connected 54Ω resistor at the far end from the driver. Only a single resistor is required because the driver sees one 54Ω differential trace. The signal swing is larger with a 54Ω load.

In general, parallel terminate each end of the bus with a resistor matching the differential impedance of the bus (taking into account any reduced impedance due to loading).

Board Layout

A four-layer PC board that provides separate power, ground, input, and output signals is recommended. Keep the LVTTL/LVCMOS and BLVDS signals separated to prevent coupling as shown in the suggested layout for the QFN package (not drawn to scale) (Figure 6).

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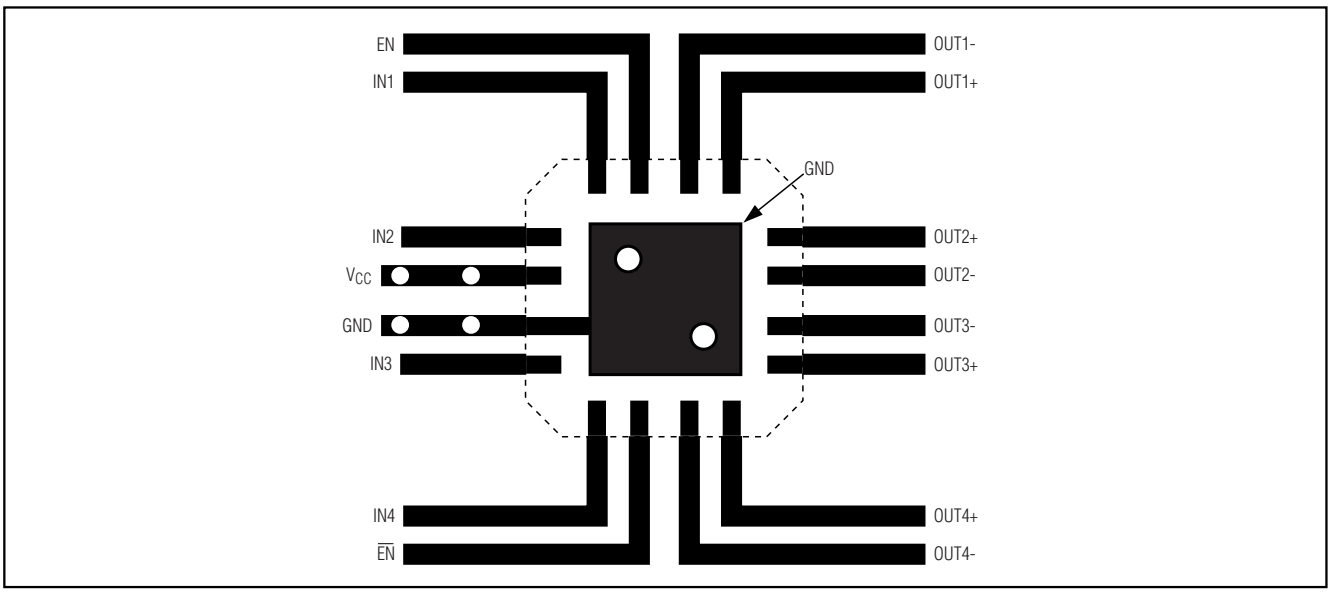

Figure 6. Suggested Layout for QFN Package

Chip Information

TRANSISTOR COUNT: 948

PROCESS: CMOS

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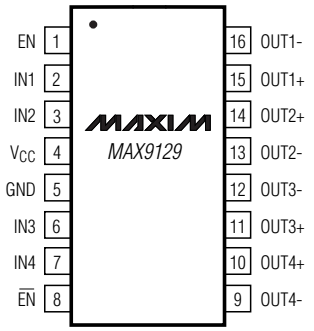
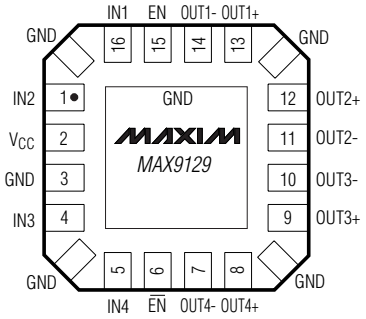
Quad Bus LVDS Driver with Flow-Through Pinout

Pin Configurations

TOP VIEW



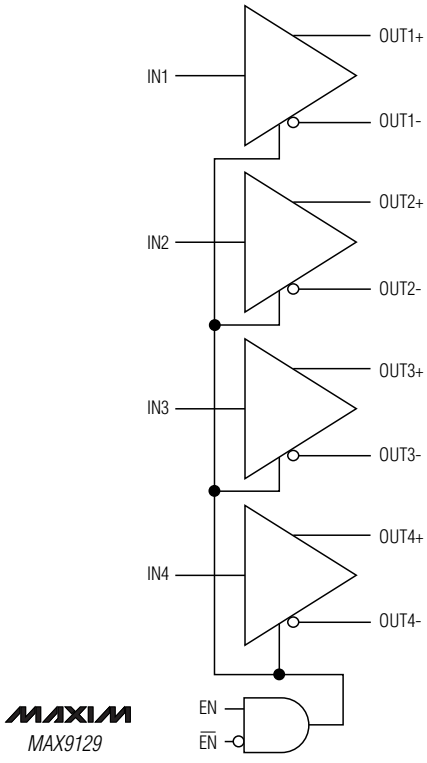
TSSOP



QFN
(4mm x 4mm)

(CONTACTS UNDER QFN)

Functional Diagram



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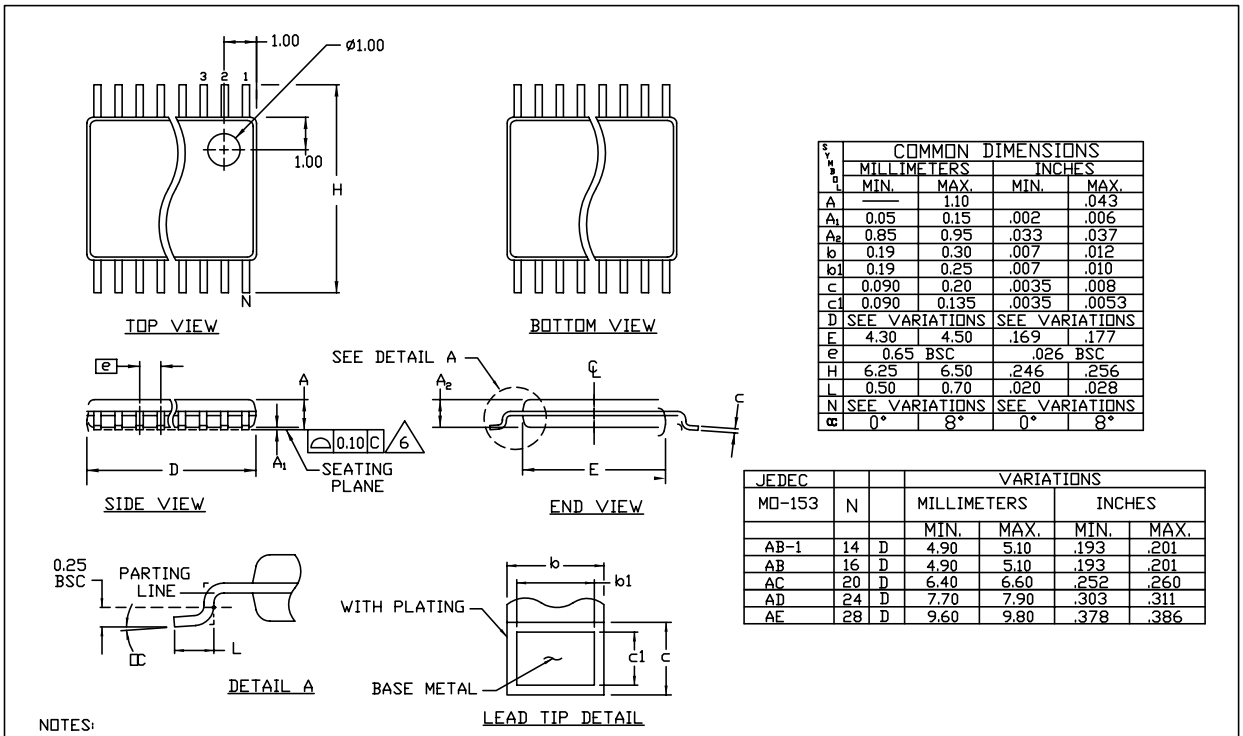
Quad Bus LVDS Driver with Flow-Through Pinout

Package Information

TSSOP,NO PADS.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	———	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b1	0.19	0.25	.007	.010
c	0.090	0.20	.0035	.008
c1	0.090	0.135	.0035	.0053
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.50	.246	.256
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE.
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED.

MAXIM
PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, TSSOP, 4.40 MM BODY

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0066	E	1/1

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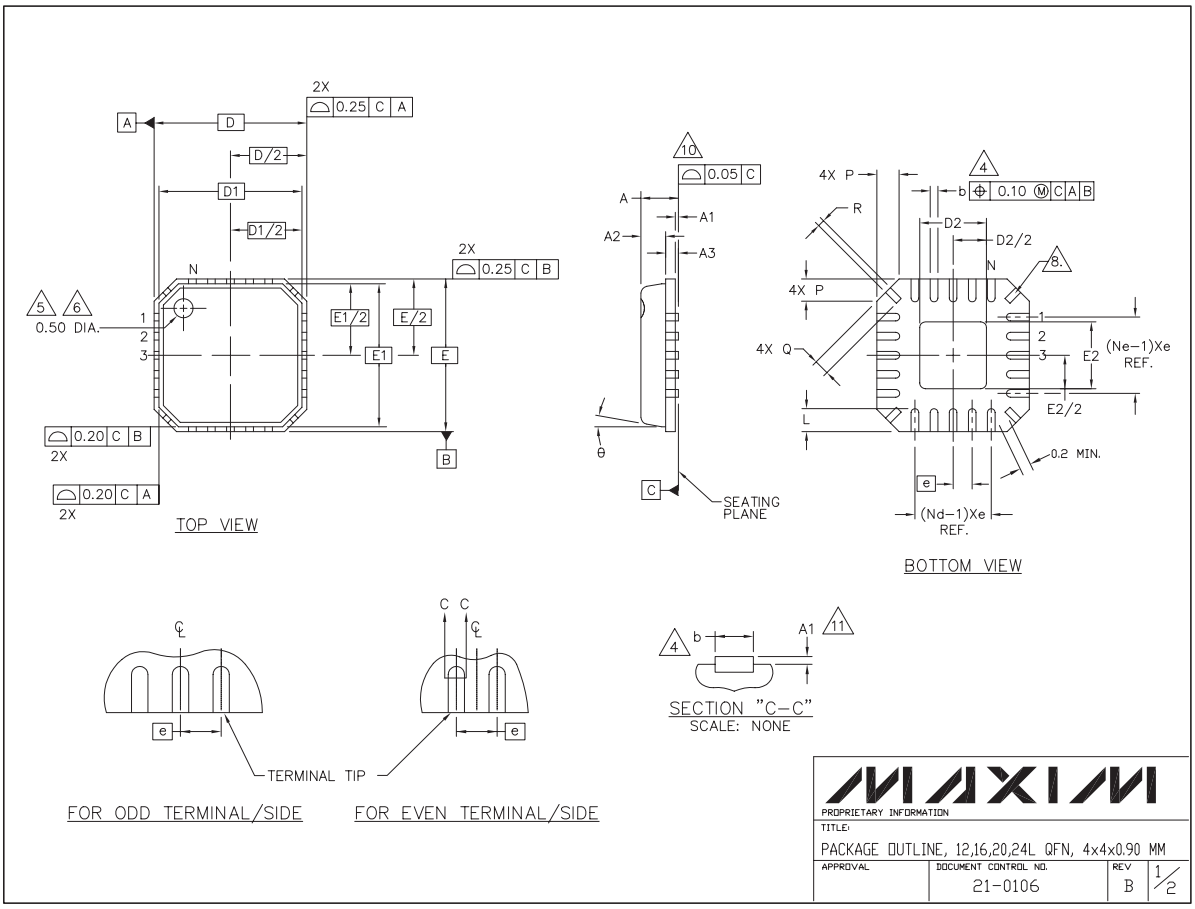
Quad Bus LVDS Driver with Flow-Through Pinout

Package Information (continued)



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Package Information (continued)

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM MUST TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X–DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y–DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. THE SHAPE SHOWN ON FOUR CORNERS ARE NOT ACTUAL I/O.
9. PACKAGE WARPAGE MAX 0.05mm.
10. APPLIED FOR EXPOSED PAD AND TERMINALS.
    EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
11. APPLIED ONLY FOR TERMINALS.
12. MEETS JEDEC MO220.

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	–	0.85	1.00	
A1	0.00	0.01	0.05	11
A2	–	0.65	0.80	
A3		0.20 REF.		
D		4.00 BSC		
D1		3.75 BSC		
E		4.00 BSC		
E1		3.75 BSC		
θ			12°	
P	0.24	0.42	0.60	
R	0.13	0.17	0.23	

SYMBOL	PITCH VARIATION A			NOTE
	MIN.	NOM.	MAX.	
e		0.80 BSC		
N		12		3
Nd		3		3
Ne		3		3
L	0.50	0.60	0.75	
b	0.28	0.33	0.40	4
Q	0.30	0.40	0.65	
D2	SEE EXPOSED PAD VARIATION: A, B			
E2	SEE EXPOSED PAD VARIATION: A, B			

SYMBOL	PITCH VARIATION B			NOTE
	MIN.	NOM.	MAX.	
e		0.65 BSC		
N		16		3
Nd		4		3
Ne		4		3
L	0.50	0.60	0.75	
b	0.23	0.28	0.35	4
Q	0.30	0.40	0.65	
D2	SEE EXPOSED PAD VARIATION: A, B			
E2	SEE EXPOSED PAD VARIATION: A, B			

SYMBOL	PITCH VARIATION C			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		20		3
Nd		5		3
Ne		5		3
L	0.50	0.60	0.75	
b	0.18	0.23	0.30	4
Q	0.30	0.40	0.65	
D2	SEE EXPOSED PAD VARIATION: A, B			
E2	SEE EXPOSED PAD VARIATION: A, B			

SYMBOL	PITCH VARIATION D			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		24		3
Nd		6		3
Ne		6		3
L	0.30	0.40	0.55	
b	0.18	0.23	0.30	4
Q	0.00	0.20	0.45	
D2	SEE EXPOSED PAD VARIATION: A			
E2	SEE EXPOSED PAD VARIATION: A			

SYMBOLS		D2			E2			NOTE
		MIN	NOM	MAX	MIN	NOM	MAX	
EXPOSED PAD VARIATIONS	A	1.95	2.10	2.25	1.95	2.10	2.25	
	B	1.55	1.70	1.85	1.55	1.70	1.85	

EXAMPLE: WE CAN CALL VARIATION "BB" FOR 16 TERMINAL QFN WITH 1.70x1.70 mm NOMINAL EXPOSED PAD DIMENSION. THE FORMER ONE IN VARIATION IS FOR PITCH VARIATION AND THE LATTER ONE IS FOR EXPOSED PAD VARIATION.

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PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 12,16,20,24L QFN, 4x4x0.90 MM

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0106	B	2/2

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