

# Overvoltage Protection Controllers with Status FLAG

## ABSOLUTE MAXIMUM RATINGS

IN to GND .....-0.3V to +30V  
 GATE to GND .....-0.3V to +12V  
 EN, FLAG to GND .....-0.3V to +6V  
 Continuous Power Dissipation ( $T_A = +70^\circ\text{C}$ )  
     6-Pin SC70 (derate 3.1mW/ $^\circ\text{C}$  above  $+70^\circ\text{C}$ ) .....245mW

Operating Temperature Range .....-40 $^\circ\text{C}$  to +85 $^\circ\text{C}$   
 Junction Temperature ..... +150 $^\circ\text{C}$   
 Storage Temperature Range .....-65 $^\circ\text{C}$  to +150 $^\circ\text{C}$   
 Lead Temperature (soldering, 10s) .....+300 $^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

( $V_{IN} = +5\text{V}$  (MAX4838–MAX4841),  $V_{IN} = +4\text{V}$  (MAX4842),  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ\text{C}$ .) (Note 1)

| PARAMETER                             | SYMBOL     | CONDITIONS                                                                                     |                  | MIN  | TYP  | MAX  | UNITS         |
|---------------------------------------|------------|------------------------------------------------------------------------------------------------|------------------|------|------|------|---------------|
| Input Voltage Range                   | $V_{IN}$   |                                                                                                |                  | 1.2  |      | 28.0 | V             |
| Undervoltage Lockout Threshold        | UVLO       | $V_{IN}$ falling                                                                               | MAX4838–MAX4841  | 3.0  | 3.25 | 3.5  | V             |
|                                       |            |                                                                                                | MAX4842          | 2.8  | 3.0  | 3.2  |               |
| Undervoltage Lockout Hysteresis       |            |                                                                                                |                  |      | 50   |      | mV            |
| Overvoltage Trip Level                | OVLO       | MAX4838/MAX4839                                                                                |                  | 7.0  | 7.4  | 7.8  | V             |
|                                       |            | MAX4840/MAX4841                                                                                |                  | 5.5  | 5.8  | 6.1  |               |
|                                       |            | MAX4842                                                                                        |                  | 4.4  | 4.7  | 5.0  |               |
| Overvoltage Trip Level Hysteresis     |            | MAX4838/MAX4839                                                                                |                  |      | 100  |      | mV            |
|                                       |            | MAX4840/MAX4841                                                                                |                  |      | 80   |      |               |
|                                       |            | MAX4842                                                                                        |                  |      | 50   |      |               |
| IN Supply Current                     | $I_{IN}$   | No load, $\overline{EN} = \text{GND}$ or 5.5V,<br>$V_{IN} = 5.4\text{V}$ (MAX4838–MAX4841)     |                  |      | 140  | 240  | $\mu\text{A}$ |
|                                       |            | No load, $\overline{EN} = \text{GND}$ or 4.4V,<br>$V_{IN} = 4.3\text{V}$ (MAX4842)             |                  |      | 130  | 220  |               |
| UVLO Supply Current                   |            | $V_{IN} = 2.9\text{V}$ (MAX4838–MAX4841),<br>$V_{IN} = 2.7\text{V}$ (MAX4842)                  |                  |      |      | 150  | $\mu\text{A}$ |
| GATE Voltage                          | $V_{GATE}$ | $I_{GATE}$ sourcing 1 $\mu\text{A}$                                                            | MAX4838–MAX4841  | 9    |      | 10   | V             |
|                                       |            |                                                                                                | MAX4842          | 7.5  |      | 8.0  |               |
| GATE Pulldown Current                 | $I_{PD}$   | $V_{IN} > V_{OVLO}$ , $V_{GATE} = 5.5\text{V}$                                                 |                  |      | 60   |      | mA            |
| $\overline{FLAG}$ Output Low Voltage  | $V_{OL}$   | $1.2\text{V} \leq V_{IN} < V_{UVLO}$ , $I_{SINK} = 50\mu\text{A}$                              |                  |      |      | 0.4  | V             |
|                                       |            | $V_{IN} \geq V_{OVLO}$ , $I_{SINK} = 1\text{mA}$                                               |                  |      |      | 0.4  |               |
| $\overline{FLAG}$ Output High Voltage | $V_{OH}$   | $I_{SOURCE} = 100\mu\text{A}$ , $\overline{FLAG}$ deasserted,<br>MAX4839/MAX4841               |                  | 2.4  |      |      | V             |
| $\overline{FLAG}$ Output High Leakage | $I_{OH}$   | $V_{\overline{FLAG}} = 5.5\text{V}$ , $\overline{FLAG}$ deasserted,<br>MAX4838/MAX4840/MAX4842 |                  |      |      | 1    | $\mu\text{A}$ |
| $\overline{EN}$ Input High Voltage    | $V_{IH}$   | MAX4838/MAX4840/MAX4842                                                                        |                  | 1.47 |      |      | V             |
| $\overline{EN}$ Input Low Voltage     | $V_{IL}$   | MAX4838/MAX4840/MAX4842                                                                        |                  |      |      | 0.65 | V             |
| $\overline{EN}$ Input Leakage         | $I_{LKG}$  | MAX4838/MAX4840/MAX4842,<br>$\overline{EN} = \text{GND}$ or 5.5V                               |                  |      |      | 1    | $\mu\text{A}$ |
| IN ESD rating                         |            | $C_{IN} \geq 1\mu\text{F}$                                                                     | Human Body Model |      | 15   |      | kV            |
|                                       |            |                                                                                                | IEC 1000-4-2     |      | 15   |      |               |

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MAX4838-MAX4842

## ELECTRICAL CHARACTERISTICS (continued)

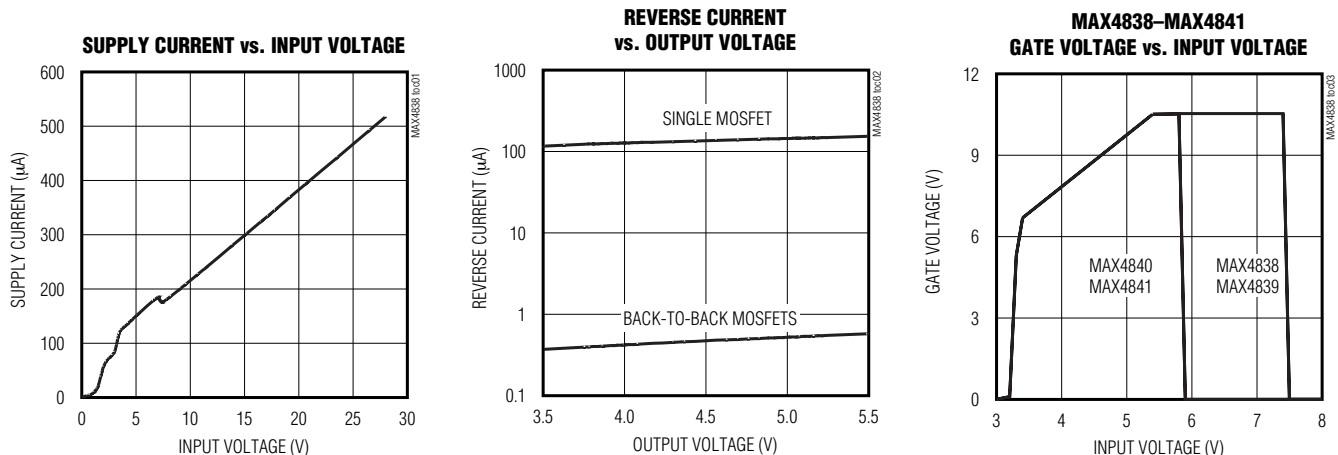
( $V_{IN} = +5V$  (MAX4838-MAX4841),  $V_{IN} = +4V$  (MAX4842),  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .) (Note 1)

| PARAMETER                       | SYMBOL      | CONDITIONS                                                                                                                                                                               | MIN | TYP | MAX | UNITS   |
|---------------------------------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|---------|
| <b>TIMING</b>                   |             |                                                                                                                                                                                          |     |     |     |         |
| Startup Delay                   | $t_{START}$ | $V_{IN} > V_{UVLO}$ , $V_{GATE} > 0.3V$ , Figure 1                                                                                                                                       | 20  | 50  | 80  | ms      |
| FLAG Blanking Time              | $t_{BLANK}$ | $V_{GATE} = 0.3V$ , $V_{FLAG} = 2.4V$ , Figure 1                                                                                                                                         | 20  | 50  | 80  | ms      |
| GATE Turn-On Time               | $t_{GON}$   | $V_{GATE} = 0.3V$ to $8V$ (MAX4838-MAX4841), $V_{GATE} = 0.3V$ to $6V$ (MAX4842), $C_{GATE} = 1500pF$ , Figure 1                                                                         |     | 10  |     | ms      |
| GATE Turn-Off Time              | $t_{GOFF}$  | $V_{IN}$ increasing from $5V$ to $8V$ at $3V/\mu s$ (MAX4838-MAX4841), $V_{IN}$ increasing from $4V$ to $6V$ at $2V/\mu s$ (MAX4842), $V_{GATE} = 0.3V$ , $C_{GATE} = 1500pF$ , Figure 2 |     | 6   | 20  | $\mu s$ |
| FLAG Assertion Delay            | $t_{FLAG}$  | $V_{IN}$ increasing from $5V$ to $8V$ at $3V/\mu s$ (MAX4838-MAX4841), $V_{IN}$ increasing from $4V$ to $6V$ at $2V/\mu s$ (MAX4842), $V_{FLAG} = 0.4V$ , Figure 2                       |     | 5.8 |     | $\mu s$ |
| Initial Overvoltage Fault Delay | $t_{OVP}$   | $V_{IN}$ increasing from $0$ to $8V$ (MAX4838-MAX4841), $V_{IN}$ increasing from $0V$ to $6V$ (MAX4842), $I_{GATE} = 80\%$ of $I_{PD}$ , Figure 3                                        |     | 100 |     | ns      |
| Disable Time                    | $t_{DIS}$   | $V_{EN} = 2.4V$ , $V_{GATE} = 0.3V$ , MAX4838/MAX4840/MAX4842, Figure 4                                                                                                                  |     | 580 |     | ns      |

**Note 1:** All parts are 100% tested at  $+25^{\circ}C$ . Electrical limits across the full temperature range are guaranteed by design and correlation.

## Typical Operating Characteristics

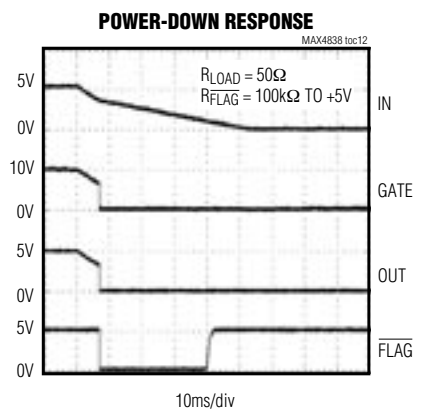
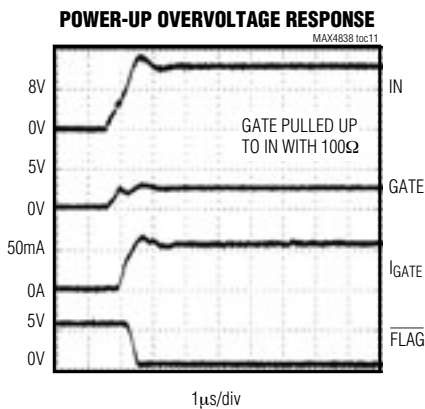
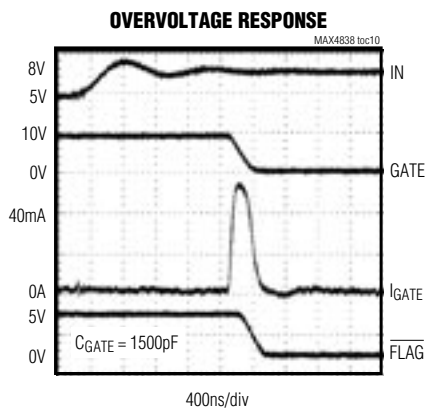
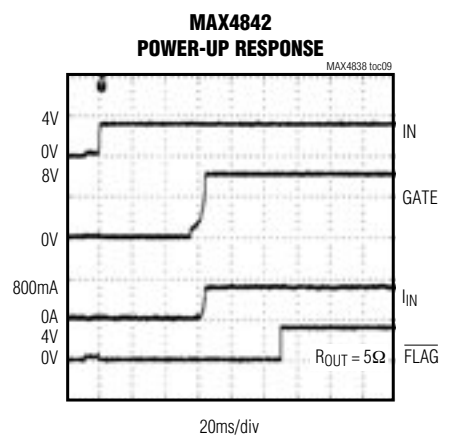
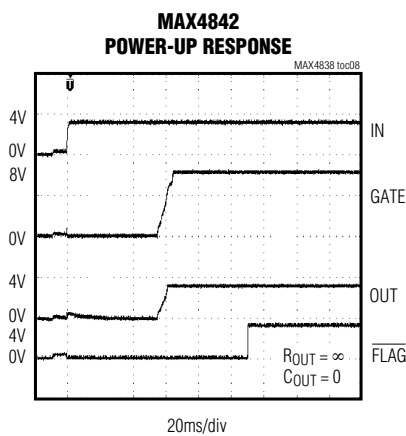
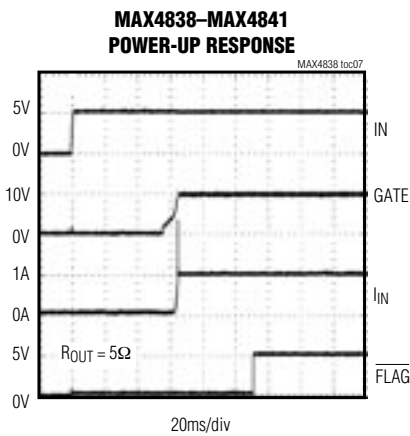
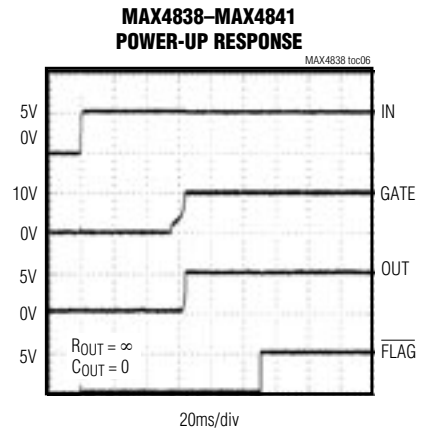
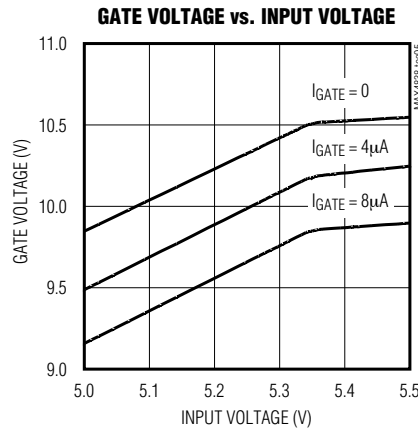
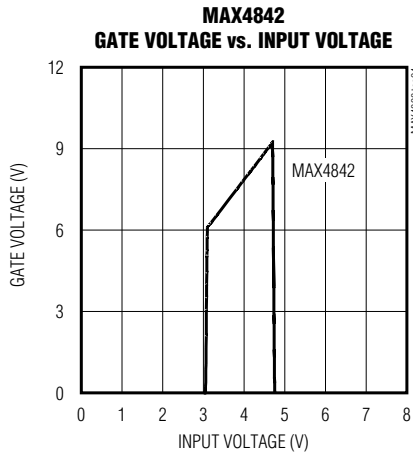
( $V_{IN} = +5V$ , MAX4838; Si9936DY external MOSFET in back-to-back configuration;  $T_A = +25^{\circ}C$ , unless otherwise noted.)



# Overvoltage Protection Controllers with Status FLAG

## Typical Operating Characteristics (continued)

( $V_{IN} = +5V$ , MAX4838; Si9936DY external MOSFET in back-to-back configuration;  $T_A = +25^\circ C$ , unless otherwise noted.)



# Overvoltage Protection Controllers with Status FLAG

MAX4838-MAX4842

## Pin Description

| PIN                             |                     | NAME                     | FUNCTION                                                                                                                                                                                                                                                                                                                   |
|---------------------------------|---------------------|--------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MAX4838/<br>MAX4840/<br>MAX4842 | MAX4839/<br>MAX4841 |                          |                                                                                                                                                                                                                                                                                                                            |
| 1                               | 1                   | IN                       | Input. IN is both the power-supply input and the overvoltage sense input. Bypass IN to GND with a 1 $\mu$ F capacitor or larger.                                                                                                                                                                                           |
| 2                               | 2                   | GND                      | Ground                                                                                                                                                                                                                                                                                                                     |
| 3                               | 3                   | $\overline{\text{FLAG}}$ | Fault Indication Output, Active Low. $\overline{\text{FLAG}}$ is asserted low during undervoltage lockout and overvoltage lockout conditions. $\overline{\text{FLAG}}$ is deasserted during normal operation. $\overline{\text{FLAG}}$ is open-drain on the MAX4838/MAX4840/MAX4842, and push-pull on the MAX4839/MAX4841. |
| 4                               | 4                   | GATE                     | Gate-Drive Output. GATE is the output of an on-chip charge pump. When $V_{\text{UVLO}} < V_{\text{IN}} < V_{\text{OVLO}}$ , GATE is driven high to turn on the external N-channel MOSFET(s).                                                                                                                               |
| 5                               | 5, 6                | N.C.                     | No Connection. Can be connected to GND.                                                                                                                                                                                                                                                                                    |
| 6                               | —                   | $\overline{\text{EN}}$   | Device Enable Input, Active Low. Drive $\overline{\text{EN}}$ low or connect to ground to allow normal device operation. Drive $\overline{\text{EN}}$ high to turn off the external MOSFET.                                                                                                                                |

## Timing Diagrams

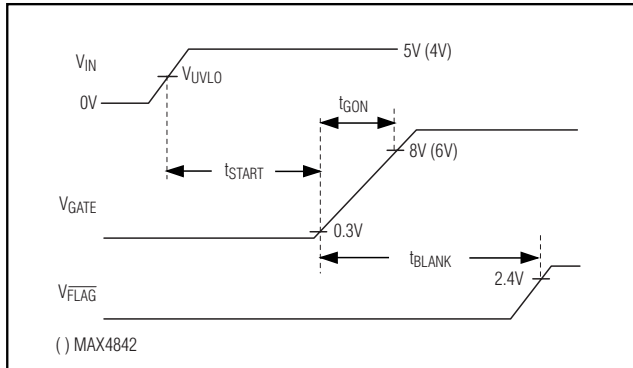


Figure 1. Startup Timing Diagram

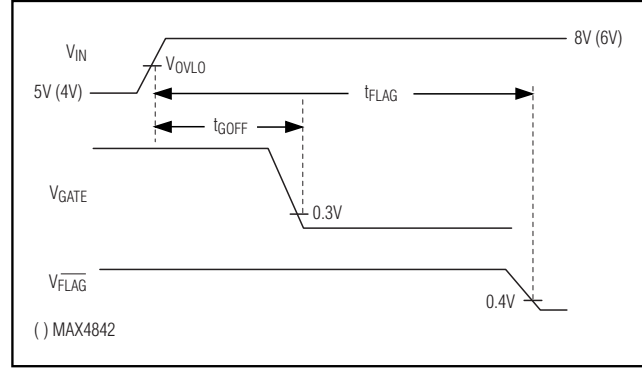


Figure 2. Shutdown Timing Diagram

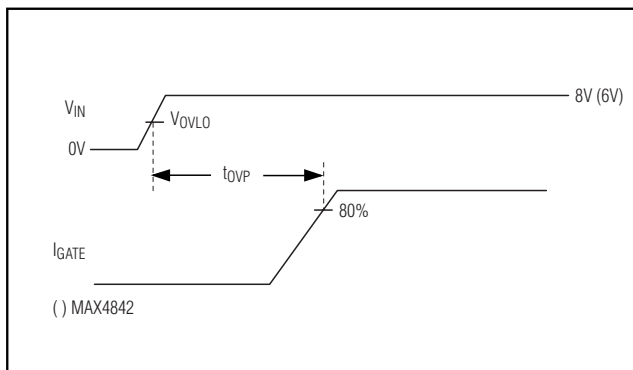


Figure 3. Power-Up Overvoltage Timing Diagram

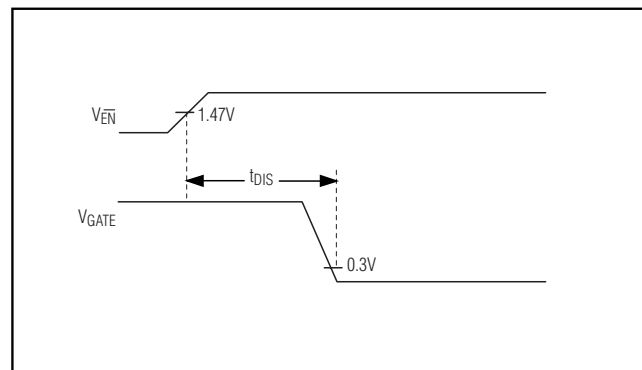


Figure 4. Disable Timing Diagram

# Overvoltage Protection Controllers with Status *FLAG*

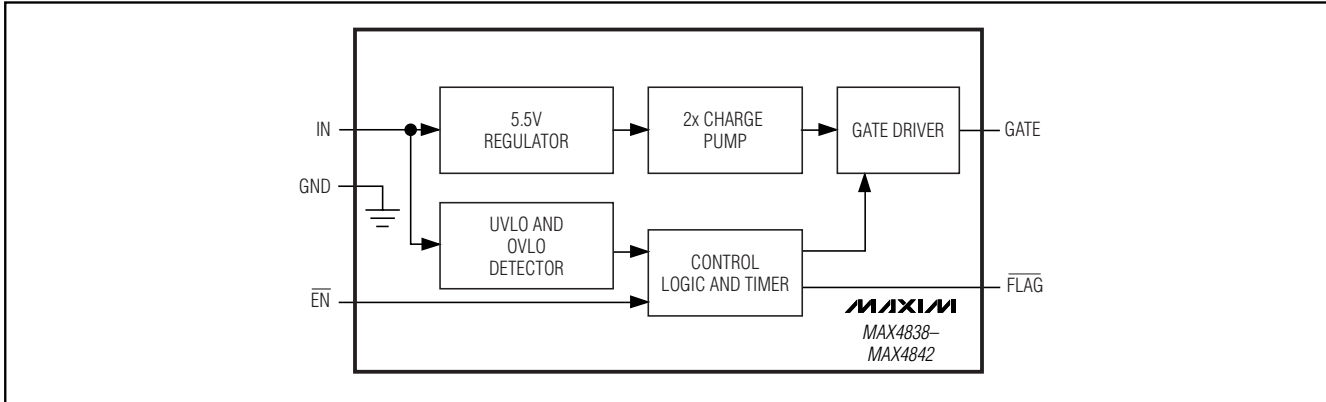


Figure 5. Functional Diagram

## Detailed Description

The MAX4838–MAX4842 provide up to 28V overvoltage protection for low-voltage systems. When the input voltage exceeds the overvoltage trip level, the MAX4838–MAX4842 turn off a low-cost external n-channel FET(s) to prevent damage to the protected components. An internal charge pump (Figure 5) drives the FET gate for a simple, robust solution.

### Undervoltage Lockout (UVLO)

The MAX4838–MAX4841 have a fixed 3.25V typical undervoltage lockout level (UVLO) while the MAX4842 has a 3.0V typical UVLO. When  $V_{\text{IN}}$  is less than the UVLO, the GATE driver is held low and  $\overline{\text{FLAG}}$  is asserted.

### Overvoltage Lockout (OVLO)

The MAX4838/MAX4839 have a 7.4V typical overvoltage threshold (OVLO), and the MAX4840/MAX4841 have a 5.8V typical overvoltage threshold. The MAX4842 has a 4.7V typical overvoltage threshold. When  $V_{\text{IN}}$  is greater than OVLO, the GATE driver is held low and  $\overline{\text{FLAG}}$  is asserted.

### $\overline{\text{FLAG}}$ Output

The  $\overline{\text{FLAG}}$  output is used to signal the host system there is a fault with the input voltage.  $\overline{\text{FLAG}}$  asserts immediately to an overvoltage fault.  $\overline{\text{FLAG}}$  is held low for 50ms after GATE turns on before deasserting.

The MAX4839 and MAX4841 have a push-pull  $\overline{\text{FLAG}}$  output. The output high voltage is proportional to  $V_{\text{IN}}$  for  $V_{\text{IN}}$  up to 5.5V, and fixed at 5.5V when  $V_{\text{IN}} > 5.5\text{V}$ .

The MAX4838/MAX4840/MAX4842 have an open-drain  $\overline{\text{FLAG}}$  output. Connect a pullup resistor from  $\overline{\text{FLAG}}$  to the logic I/O voltage of the host system.

### $\overline{\text{EN}}$ Enable Input

$\overline{\text{EN}}$  is an active-low enable input on the MAX4838/MAX4840/MAX4842 only. Drive  $\overline{\text{EN}}$  low or connect to ground to enable normal device operation. Drive  $\overline{\text{EN}}$  high to force the external MOSFET(s) off.  $\overline{\text{EN}}$  does not override an OVLO or UVLO fault.

### GATE Driver

An on-chip charge pump is used to drive GATE above  $V_{\text{IN}}$ , allowing the use of low-cost n-channel MOSFETs. The charge pump operates from the internal 5.5V regulator.

The actual GATE output voltage tracks approximately two times  $V_{\text{IN}}$  until  $V_{\text{IN}}$  exceeds 5.5V or the OVLO trip level is exceeded, whichever comes first. The MAX4838/MAX4839 have a 7.4V typical OVLO, therefore GATE remains relatively constant at about 10.5V for  $5.5\text{V} < V_{\text{IN}} < 7.4\text{V}$ . The MAX4840/MAX4841 have a 5.8V typical OVLO, but this can be as low as 5.5V. The MAX4840/MAX4841 in practice may never actually achieve the full 10.5V GATE output. The MAX4842 has a 4.7V (typ) OVLO and the GATE output voltage is 2x the input voltage. The GATE output voltage as a function of input voltage is shown in the *Typical Operating Characteristics*.

### Device Operation

The MAX4838–MAX4842 have an on-board state machine to control device operation. A flowchart is shown in Figure 6. On initial power-up, if  $V_{\text{IN}} < \text{UVLO}$  or if  $V_{\text{IN}} > \text{OVLO}$ , GATE is held at 0V, and  $\overline{\text{FLAG}}$  is low.

If  $\text{UVLO} < V_{\text{IN}} < \text{OVLO}$  and  $\overline{\text{EN}}$  is low, the device enters startup after a 50ms internal delay. The internal charge pump is enabled, and GATE begins to be driven above  $V_{\text{IN}}$  by the internal charge pump.  $\overline{\text{FLAG}}$  is held low during startup until the  $\overline{\text{FLAG}}$  blanking period expires, typi-

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MAX4838-MAX4842

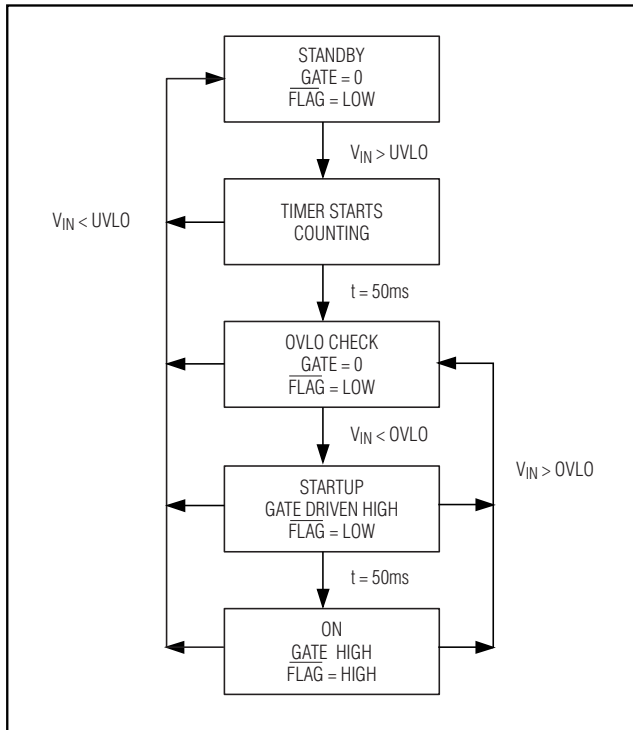


Figure 6. State Diagram

cally 50ms after the GATE starts going high. At this point the device is in its on state.

At any time if  $V_{IN}$  drops below UVLO,  $\overline{FLAG}$  is driven low and GATE is driven to ground.

## Applications Information

### MOSFET Configuration

The MAX4838-MAX4842 can be used with either a single MOSFET configuration as shown in the *Typical Operating Circuit*, or can be configured with a back-to-back MOSFET as shown in Figure 7.

The MAX4838-MAX4842 can drive either a single MOSFET or back-to-back MOSFETs. The back-to-back configuration has almost zero reverse current when the input supply is below the output.

If reverse current leakage is not a concern, a single MOSFET can be used. This approach has half the loss of the back-to-back configuration when used with similar MOSFET types, and is a lower cost solution. Note that if the input is actually pulled low, the output is pulled low as well due to the parasitic body diode in the

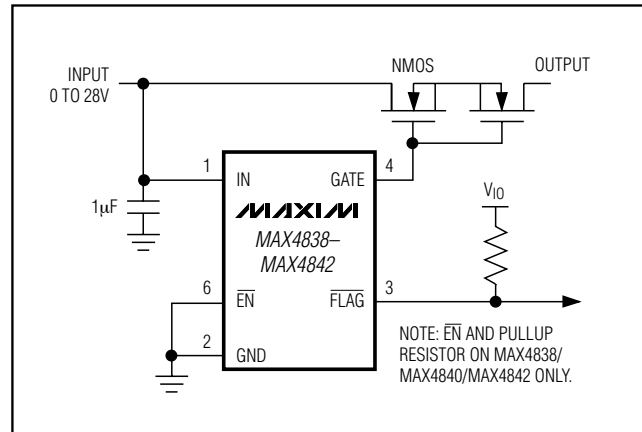


Figure 7. Back-to-Back External MOSFET Configuration

MOSFET. If this is a concern, then the back-to-back configuration should be used.

### MOSFET Selection

The MAX4838-MAX4842 are designed for use with either a single n-channel MOSFET or dual back-to-back n-channel MOSFETs. In most situations, MOSFETs with  $R_{DS(ON)}$  specified for a  $V_{GS}$  of 4.5V work well. If the input supply is near the UVLO maximum of 3.5V consider using a MOSFET specified for a lower  $V_{GS}$  voltage. Also the  $V_{DS}$  should be 30V for the MOSFET to withstand the full 28V IN range of the MAX4838-MAX4842. Table 1 shows a selection of MOSFETs appropriate for use with the MAX4838-MAX4842.

### IN Bypass Considerations

For most applications, bypass IN to GND with a 1µF ceramic capacitor. If the power source has significant inductance due to long lead length, take care to prevent overshoots due to the LC tank circuit and provide protection if necessary to prevent exceeding the 30V absolute maximum rating on IN.

The MAX4838-MAX4842 provide protection against voltage faults up to 28V, but this does not include negative voltages. If negative voltages are a concern, connect a Schottky diode from IN to GND to clamp negative input voltages.

### ESD Test Conditions

ESD performance depends on a number of conditions. The MAX4838-MAX4842 are specified for 15kV typical ESD resistance on IN when IN is bypassed to ground with a 1µF ceramic capacitor. Contact Maxim for a reli-

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Table 1. MOSFET Suggestions

| PART      | CONFIGURATION/<br>PACKAGE | V <sub>DS</sub> MAX (V) | R <sub>ON</sub> AT 4.5V (mΩ) | MANUFACTURER                                                     |
|-----------|---------------------------|-------------------------|------------------------------|------------------------------------------------------------------|
| Si5902DC  | Dual/1206-8               | 30                      | 143                          | Vishay Siliconix<br>www.vishay.com<br>402-563-6866               |
| Si1426DH  | Single/SC70-6             | 30                      | 115                          |                                                                  |
| FDC6305N  | Dual/SSOT-6               | 20                      | 80                           | Fairchild Semiconductor<br>www.fairchildsemi.com<br>207-775-8100 |
| FDC6561AN | Dual/ SSOT-6              | 30                      | 145                          |                                                                  |
| FDG315N   | Single/SC70-6             | 30                      | 160                          |                                                                  |

ability report that documents test setup, methodology, and results.

### Human Body Model

Figure 8 shows the Human Body Model and Figure 9 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

### IEC 1000-4-2

Since January 1996, all equipment manufactured and/or sold in the European community has been required to meet the stringent IEC 1000-4-2 specification. The IEC 1000-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to

integrated circuits. The MAX4838-MAX4842 help users design equipment that meets Level 3 of IEC 1000-4-2, without additional ESD-protection components.

The main difference between tests done using the Human Body Model and IEC 1000-4-2 is higher peak current in IEC 1000-4-2. Because series resistance is lower in the IEC 1000-4-2 ESD test model (Figure 10), the ESD-withstand voltage measured to this standard is generally lower than that measured using the Human Body Model. Figure 11 shows the current waveform for the ±8kV IEC 1000-4-2 Level 4 ESD Contact Discharge test. The Air-Gap test involves approaching the device with a charger probe. The Contact Discharge method connects the probe to the device before the probe is energized.

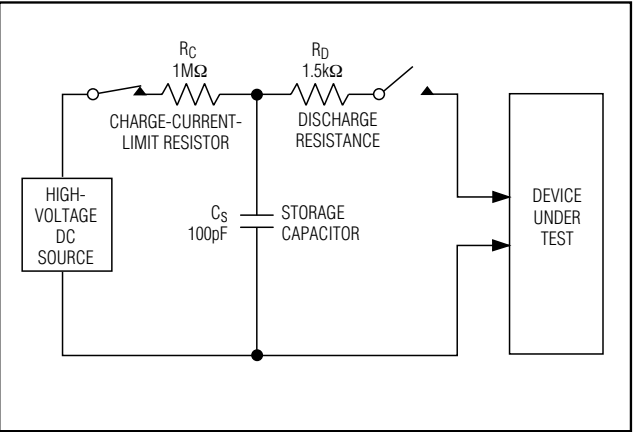


Figure 8. Human Body ESD Test Model

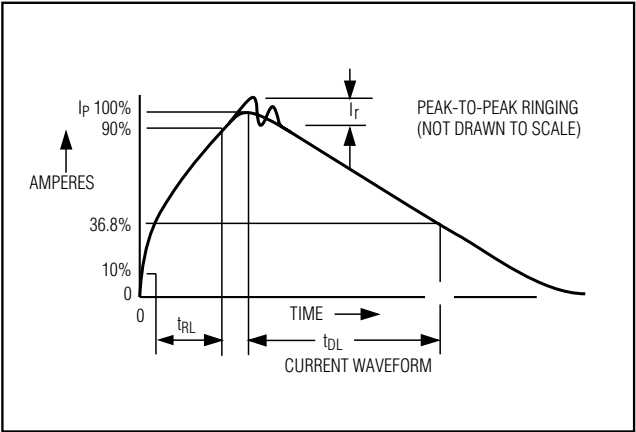


Figure 9. Human Body Model Current Waveform

# Overvoltage Protection Controllers with Status FLAG

MAX4838-MAX4842

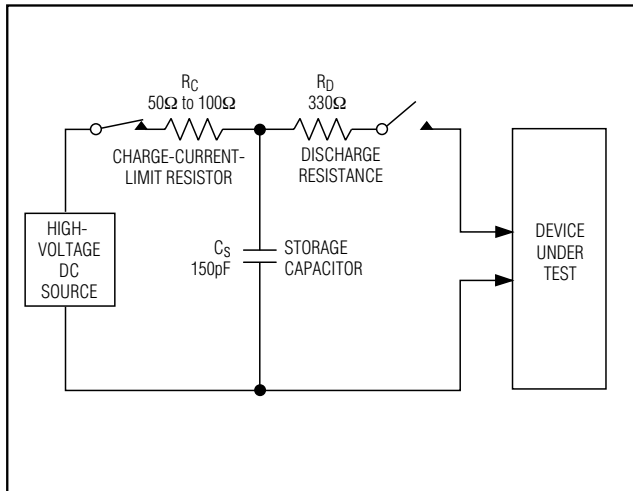


Figure 10. IEC 1000-4-2 ESD Test Model

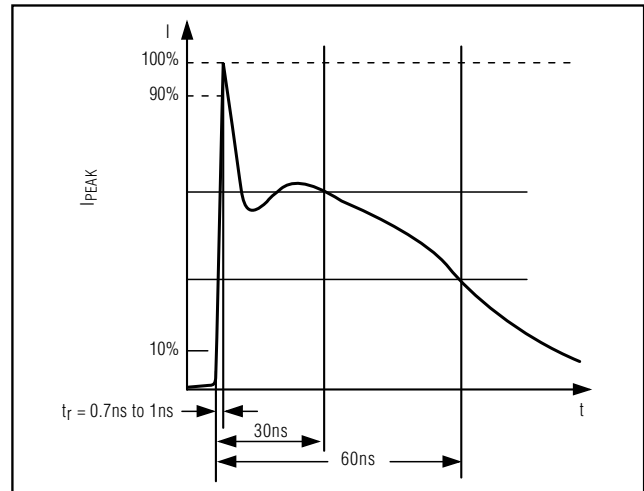
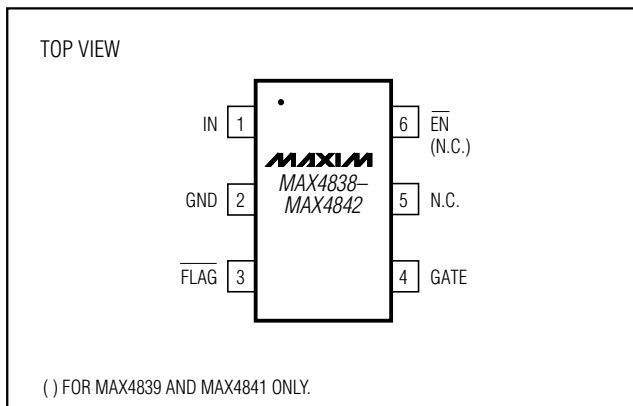


Figure 11. IEC 1000-4-2 ESD Generator Current

## Pin Configuration



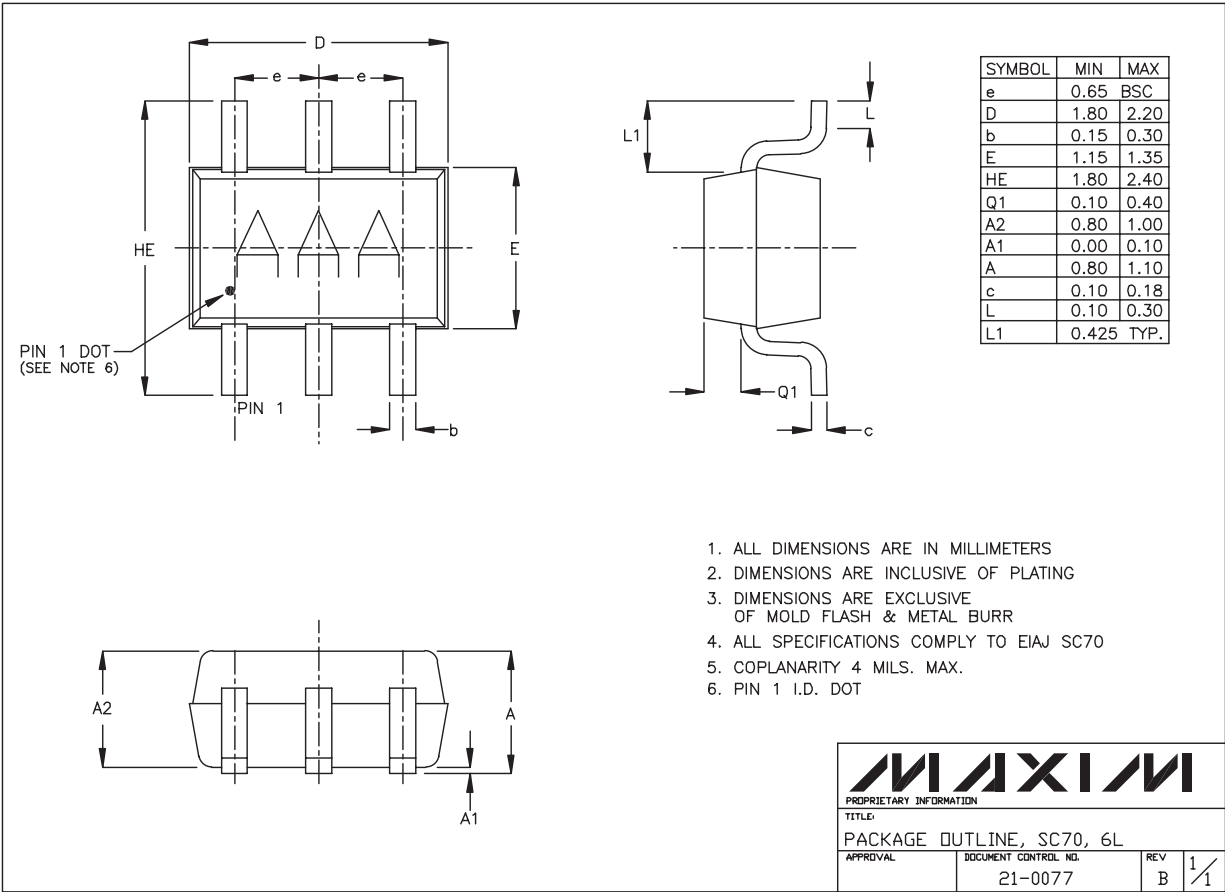
## Chip Information

TRANSISTOR COUNT: 737  
PROCESS: BiCMOS

# Overvoltage Protection Controllers with Status FLAG

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)



SC70, 6LEPS

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