Low-Voltage, Low-On-Resistance, SPST, CMOS Analog Switches

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND.)

V+ .....-0.3V, +13V
Voltage into Any Terminal (Note 1).....-0.3V to (V+ + 0.3V)
or ±20mA (whichever occurs first)
Continuous Current into Any Terminal.....±20mA
Peak Current, NO_ or COM_
(pulsed at 1ms,10% duty cycle).....±30mA
ESD per Method 3015.7 .....>2000V
Continuous Power Dissipation (T_A = +70°C)
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
8-Pin SO (derate 5.88mW/°C above +70°C).....471mW
5-Pin SOT23-5 (derate 7.1mW/°C above +70°C) 571mW
8-Pin CERDIP (derate 8.00mW/°C above +70°C).....640mW
Operating Temperature Ranges
MAX4514C_ _/MAX4515C_ _ .....0°C to +70°C
MAX4514E_ _/MAX4515E_ _.....-40°C to +85°C
MAX4514MJA/MAX4515MJA .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: Voltages exceeding V+ or GND on any signal terminal are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—+5V Supply

(V+ = +4.5V to +5.5V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH								
Analog Signal Range	V_{COM}, V_{NO}, V_{NC}				0		V+	V
COM to NO or NC On-Resistance	R_{ON}	V+ = 5V, V_{COM} = 3.5V, I_{COM} = 1mA	T_A = +25°C			10	20	Ω
			T_A = T_{MIN} to T_{MAX}				25	
COM to NO or NC On-Resistance Flatness	ΔR_{ON}	V_{COM} = 1V, 2V, 3V; I_{COM} = 1mA	T_A = +25°C			1	3	Ω
			T_A = T_{MIN} to T_{MAX}				5	
NO or NC Off-Leakage Current (Note 3)	$I_{NO(OFF)}$ $I_{NC(OFF)}$	V+ = 5.5V, V_{COM} = 1V, V_{NO} or V_{NC} = 4.5V	T_A = +25°C		-1	0.01	1	nA
			T_A = T_{MIN} to T_{MAX}	C, E	-20		20	
				M	-100		100	
COM Off-Leakage Current (Note 3)	$I_{COM(OFF)}$	V+ = 5.5V, V_{COM} = 4.5V, V_{NO} or V_{NC} = 1V	T_A = +25°C		-1	0.01	1	nA
			T_A = T_{MIN} to T_{MAX}	C, E	-20		20	
				M	-100		100	
COM On-Leakage Current (Note 3)	$I_{COM(ON)}$	V+ = 5.5V, V_{COM} = 4.5V, V_{NO} or V_{NC} = 4.5V	T_A = +25°C		-2	0.01	2	nA
			T_A = T_{MIN} to T_{MAX}	C, E	-40		40	
				M	-200		200	
DIGITAL I/O								
Input Logic High	V_{IH}				2.4		V+	V
Input Logic Low	V_{IL}				0		0.8	V
Input Current Logic High or Low	I_{IH}, I_{IL}	V_{IN} = V+, 0V			-1	0.03	1	µA
SWITCH DYNAMIC CHARACTERISTICS								
Turn-On Time	t_{ON}	Figure 2	T_A = +25°C			30	150	ns
			T_A = T_{MIN} to T_{MAX}				240	
Turn-Off Time	t_{OFF}	Figure 2	T_A = +25°C			20	100	ns
			T_A = T_{MIN} to T_{MAX}				150	

ELECTRICAL CHARACTERISTICS—+5V Supply (continued)

(V+ = +4.5V to +5.5V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SWITCH DYNAMIC CHARACTERISTICS							
Charge Injection (Note 4)	Q	C_L = 1nF, V_{NO} = 0V, R_S = 0Ω, T_A = +25°C, Figure 1			2	10	pC
Off Isolation	V_{ISO}	R_L = 50Ω, C_L = 15pF, V_{NO} = 1V_{RMS}, f = 100kHz, T_A = +25°C, Figure 3			≤-90		dB
NO or NC Off Capacitance	$C_{NO(OFF)}$, $C_{NC(OFF)}$	f = 1MHz, T_A = +25°C, Figure 4			14		pF
COM Off Capacitance	$C_{COM(OFF)}$	f = 1MHz, T_A = +25°C, Figure 4			14		pF
COM On Capacitance	$C_{COM(ON)}$	f = 1MHz, T_A = +25°C, Figure 4			30		pF
POWER SUPPLY							
V+ Supply Current	I+	V_{IN} = 0V or V+	T_A = +25°C	-1		1	µA
			T_A = T_{MIN} to T_{MAX}	-10		10	

ELECTRICAL CHARACTERISTICS—+12V Supply

(V+ = +11.4V to +12.6V, V_{INH} = 5V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH								
Analog Signal Range	V_{COM}, V_{NO}, V_{NC}				0		V+	V
COM to NO or NC On-Resistance	R_{ON}	V_{COM} = 10V, I_{COM} = 1mA	T_A = +25°C			5	10	Ω
			T_A = T_{MIN} to T_{MAX}				15	
NO, NC Off-Leakage Current (Note 3)	$I_{(NO)OFF}$ $I_{(NC)OFF}$	V+ = 12.6V, V_{COM} = 1V, V_{NO} or V_{NC} = 10V	T_A = +25°C		-2		2	nA
			T_A = T_{MIN} to T_{MAX}	C, E	-50		50	
				M	-200		200	
COM Off-Leakage Current (Note 3)	$I_{COM(OFF)}$	V+ = 12.6V, V_{COM} = 10V, V_{NO} or V_{NC} = 1V	T_A = +25°C		-2		2	nA
			T_A = T_{MIN} to T_{MAX}	C, E	-50		50	
				M	-200		200	
COM On-Leakage Current (Note 3)	$I_{COM(ON)}$	V+ = 12.6V, V_{COM} = 10V, V_{NO} or V_{NC} = 10V	T_A = +25°C		-4		4	nA
			T_A = T_{MIN} to T_{MAX}	C, E	-100		100	
				M	-400		400	
DIGITAL I/O								
Input Logic High	V_{INH}				5		V+	V
Input Logic Low	V_{INL}				0		0.8	V
Input Current Logic High or Low	I_{INH}, I_{INL}	V_{IN} = V+, 0V			-1	0.03	1	µA
POWER SUPPLY								
V+ Supply Current	I+	IN = 0V or V+	T_A = +25°C		-2		2	µA
			T_A = T_{MIN} to T_{MAX}		-20		20	

Low-Voltage, Low-On-Resistance, SPST, CMOS Analog Switches

ELECTRICAL CHARACTERISTICS—+3V Supply

(V+ = +3V to +3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

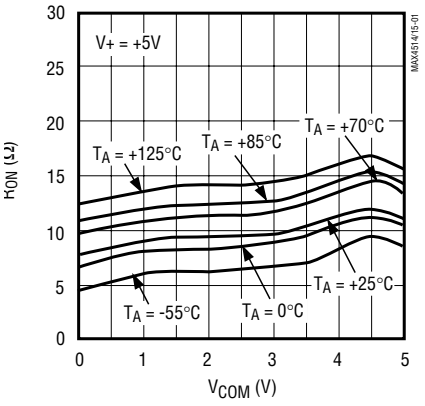
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	V_{COM}, V_{NO}, V_{NC}			0		V+	V
COM to NO or NC On-Resistance	R_{ON}	V_{COM} = 1.5V, I_{NO} = 1mA, V+ = 3V	T_A = +25°C		20	50	Ω
			T_A = T_{MIN} to T_{MAX}			75	
DIGITAL I/O							
Input Logic High	V_{INH}			2.4		V+	V
Input Logic Low	V_{INL}			0		0.80	V
Input Current Logic High or Low	I_{INH}, I_{INL}	V_{IN} = V+, 0V		-1	0.03	1	µA
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time (Note 4)	t_{ON}	Figure 2	T_A = +25°C		45	150	ns
			T_A = T_{MIN} to T_{MAX}			240	
Turn-Off Time (Note 4)	t_{OFF}	Figure 2	T_A = +25°C		30	100	ns
			T_A = T_{MIN} to T_{MAX}			150	
Charge Injection (Note 4)	Q	C_L = 1nF, Figure 1	T_A = +25°C		4	10	pC
POWER SUPPLY							
V+ Supply Current	I+	IN = 0V or V+	T_A = +25°C	-1		1	µA
			T_A = T_{MIN} to T_{MAX}	-10		10	

Note 2: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.
Note 3: Leakage parameters are 100% tested at maximum-rated hot operating temperature, and are guaranteed by correlation at +25°C.
Note 4: Guaranteed, not production tested.
Note 5: SOT packaged parts are 100% tested at +25°C. Limits at maximum and minimum rated temperature are guaranteed by design and correlation limits at +25°C.

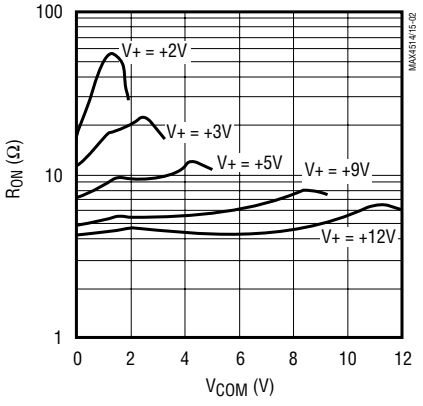
Typical Operating Characteristics

(V+ = +5V, GND = 0V, T_A = +25°C, unless otherwise noted.)

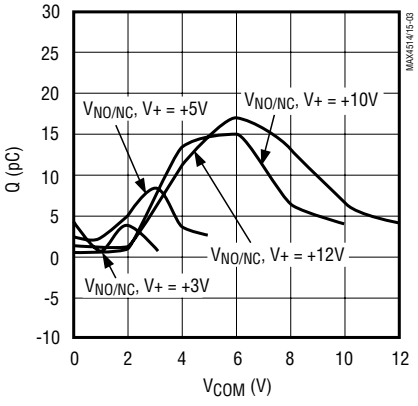
ON-RESISTANCE vs. V_{COM} OVER TEMPERATURE



ON-RESISTANCE vs. V_{COM}



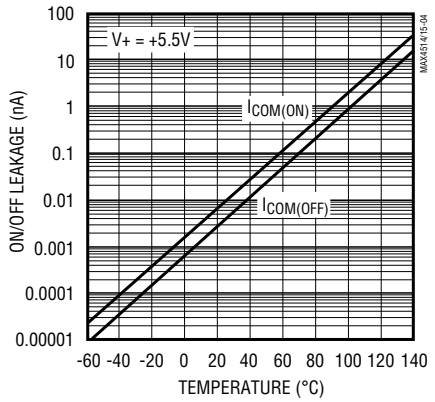
CHARGE INJECTION vs. V_{COM}



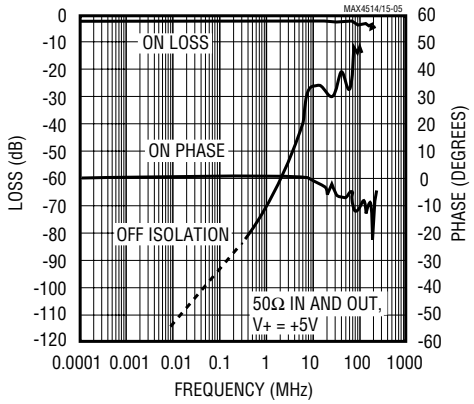
Typical Operating Characteristics (continued)

(V+ = +5V, GND = 0V, T_A = +25°C, unless otherwise noted.)

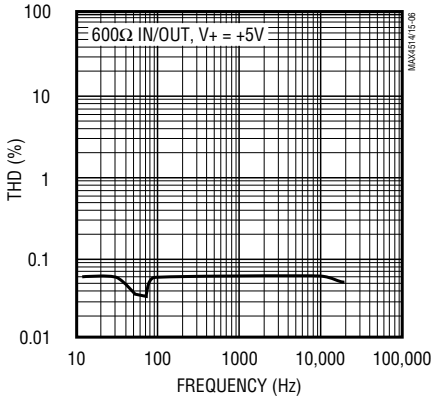
ON/OFF-LEAKAGE vs. TEMPERATURE



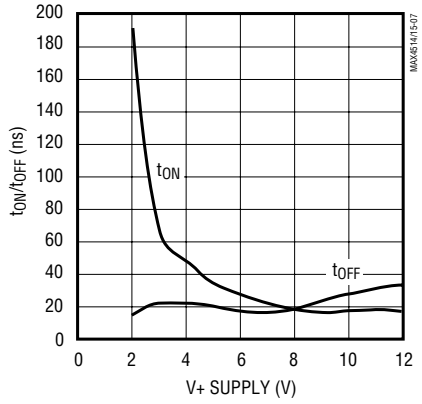
FREQUENCY RESPONSE



TOTAL HARMONIC DISTORTION vs. FREQUENCY



t_{ON}/t_{OFF} vs. V_{SUPPLY}



Pin Description

PIN				NAME	FUNCTION
MAX4514		MAX4515			
DIP/SO	SOT23-5	DIP/SO	SOT23-5		
1	1	1	1	COM	Analog Switch Common Terminal
2, 3, 5	—	2, 3, 5	—	N.C.	No Connection (Not Internally Connected)
4	5	4	5	V+	Positive Supply-Voltage Input (Analog and Digital)
6	4	6	4	IN	Digital Control Input
7	3	7	3	GND	Ground
8	2	—	—	NO	Analog Switch (Normally Open)
—	—	8	2	NC	Analog Switch (Normally Cosed)

Note: *NO, NC, and COM pins are identical and interchangeable. Any may be considered as an input or an output; signals pass equally well in both directions.*

Low-Voltage, Low-On-Resistance, SPST, CMOS Analog Switches

Applications Information

Power-Supply Considerations

The MAX4514/MAX4515 construction is typical of most CMOS analog switches, except that they have only two supply pins: V+ and GND. V+ and GND drive the internal CMOS switches and set their analog voltage limits. Reverse ESD-protection diodes are internally connected between each analog-signal pin and both V+ and GND. One of these diodes conducts if any analog signal exceeds V+ or GND.

Virtually all the analog leakage current comes from the ESD diodes to V+ or GND. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or GND and the analog signal. This means their leakages will vary as the signal varies. The *difference* in the two diode leakages to the V+ and GND pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity.

There is no connection between the analog-signal paths and V+ or GND.

V+ and GND also power the internal logic and logic-level translators. The logic-level translators convert the logic levels to switched V+ and GND signals to drive the analog signal gates.

Logic-Level Thresholds

The logic-level thresholds are CMOS/TTL compatible when V+ is +5V. As V+ is raised, the level threshold increases slightly. When V+ reaches +12V, the level threshold is about 3.0V—above the TTL guaranteed high-level minimum of 2.8V, but still compatible with CMOS outputs.

Do not connect the MAX4514/MAX4515's V+ to +3V and then connect the logic-level pins to logic-level signals that operate from +5V supply. Output levels can exceed +3V and violate the absolute maximum ratings, damaging the part and/or external circuits.

High-Frequency Performance

In 50Ω systems, signal response is reasonably flat up to 250MHz (see *Typical Operating Characteristics*). Above 20MHz, the on response has several minor peaks that are highly layout dependent. The problem is not in turning the switch on; it's in turning it off. The off-state switch acts like a capacitor and passes higher frequencies with less attenuation. At 10MHz, off isolation is about -45dB in 50Ω systems, decreasing (approximately 20dB per decade) as frequency increases. Higher circuit impedances also make off isolation decrease. Off isolation is about 3dB above that of a bare IC socket, and is due entirely to capacitive coupling.

Test Circuits/Timing Diagrams

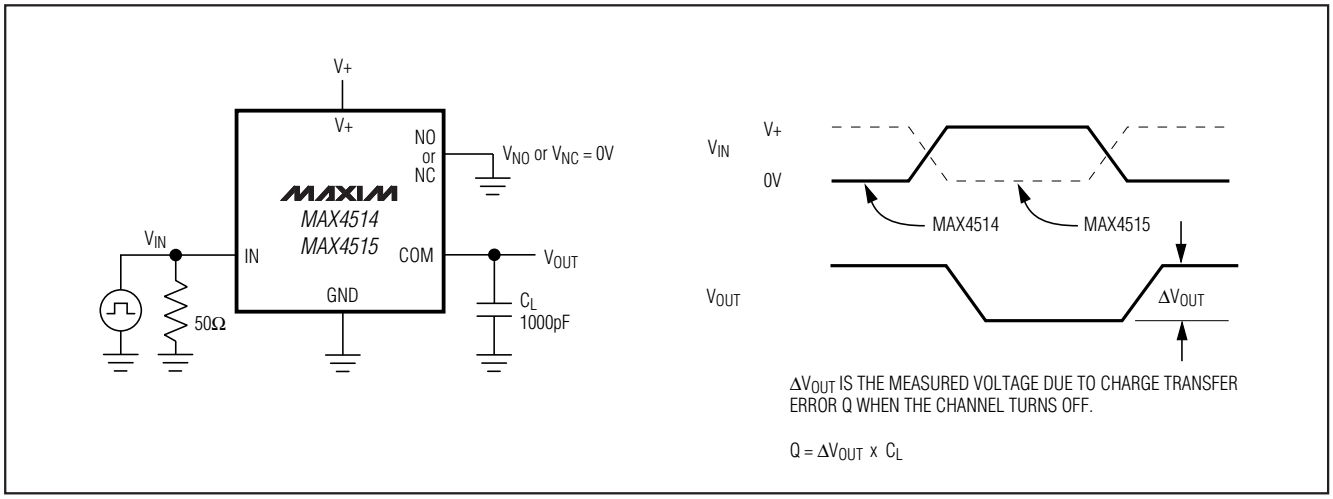


Figure 1. Charge Injection

Test Circuits/Timing Diagrams (continued)

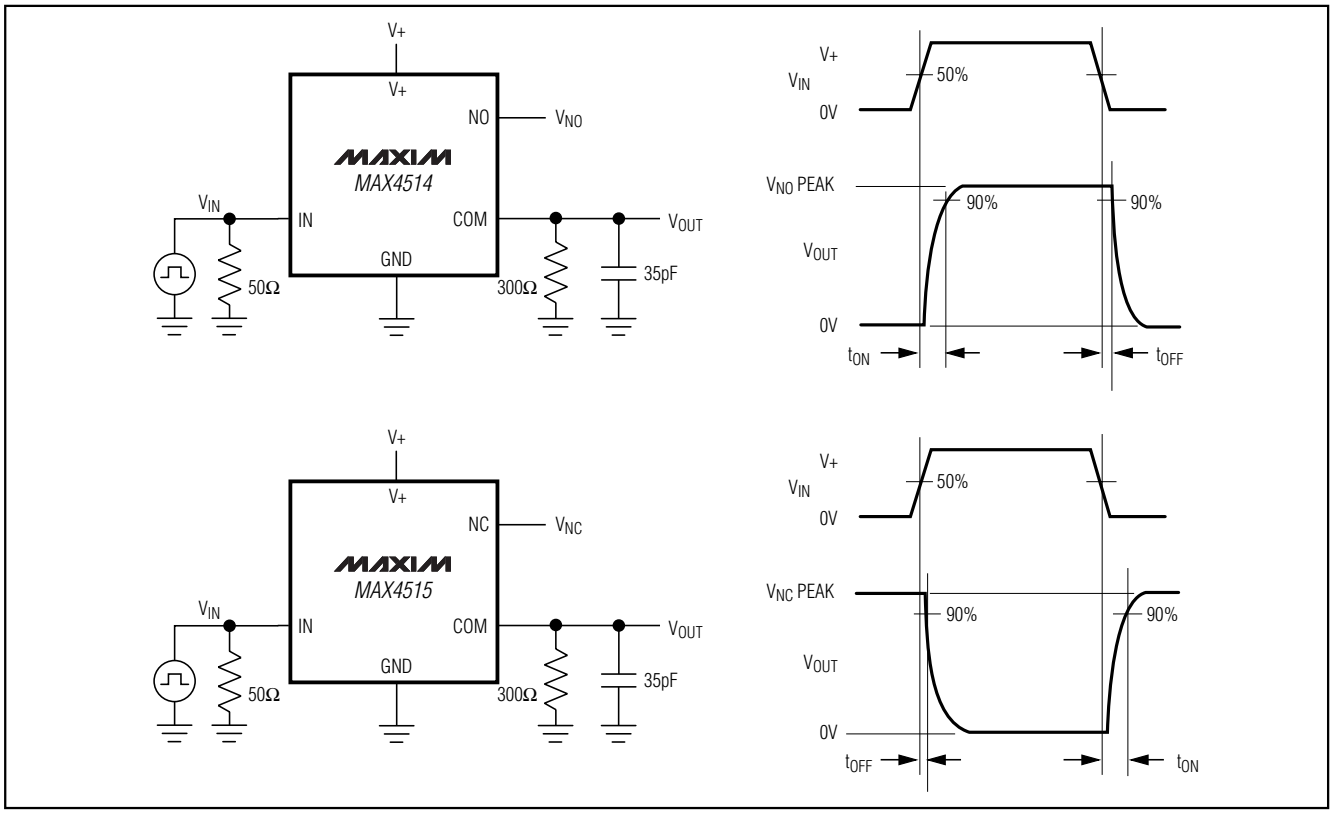


Figure 2. Switching Times

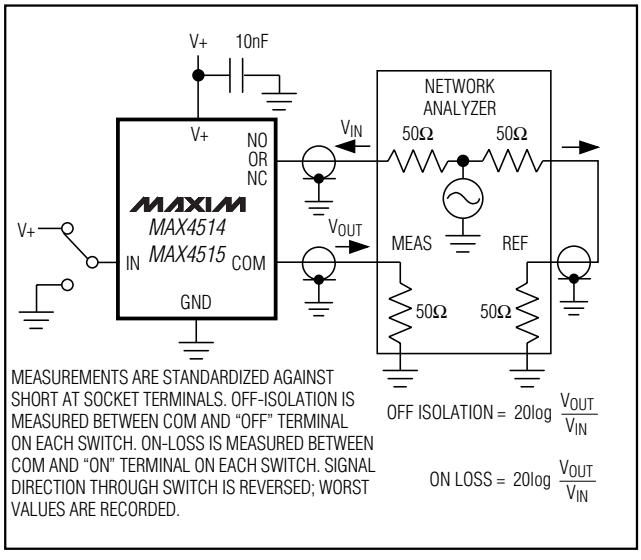


Figure 3. Off-Isolation and On-Loss

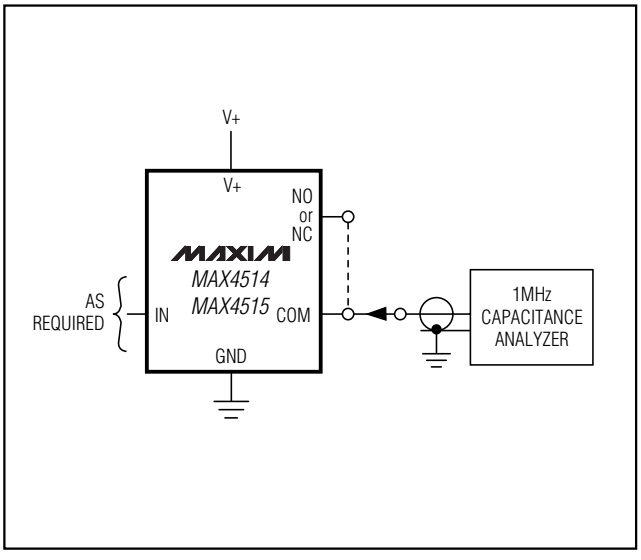


Figure 4. NO, NC, and COM Capacitance

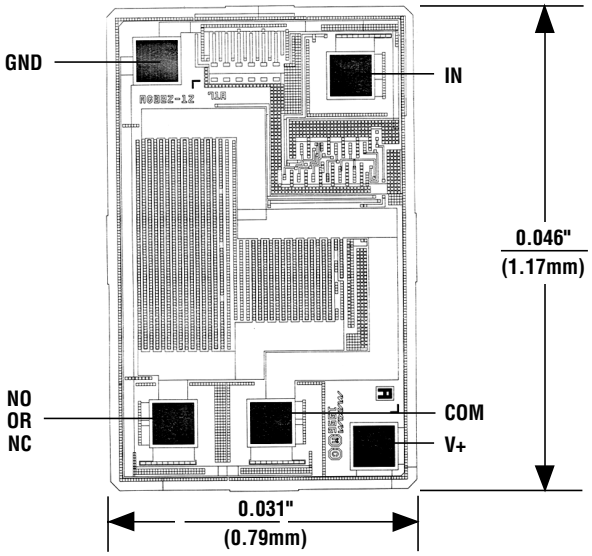
Low-Voltage, Low-On-Resistance, SPST, CMOS Analog Switches

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX4514EPA	-40°C to +85°C	8 Plastic DIP
MAX4514ESA	-40°C to +85°C	8 SO
MAX4514EUK	-40°C to +85°C	5 SOT23-5
MAX4514MJA	-55°C to +125°C	8 CERDIP**
MAX4515CPA	0°C to +70°C	8 Plastic DIP
MAX4515CSA	0°C to +70°C	8 SO
MAX4515CUK	0°C to +70°C	5 SOT23-5
MAX4515C/D	0°C to +70°C	Dice*
MAX4515EPA	-40°C to +85°C	8 Plastic DIP
MAX4515ESA	-40°C to +85°C	8 SO
MAX4515EUK	-40°C to +85°C	5 SOT23-5
MAX4515MJA	-55°C to +125°C	8 CERDIP**

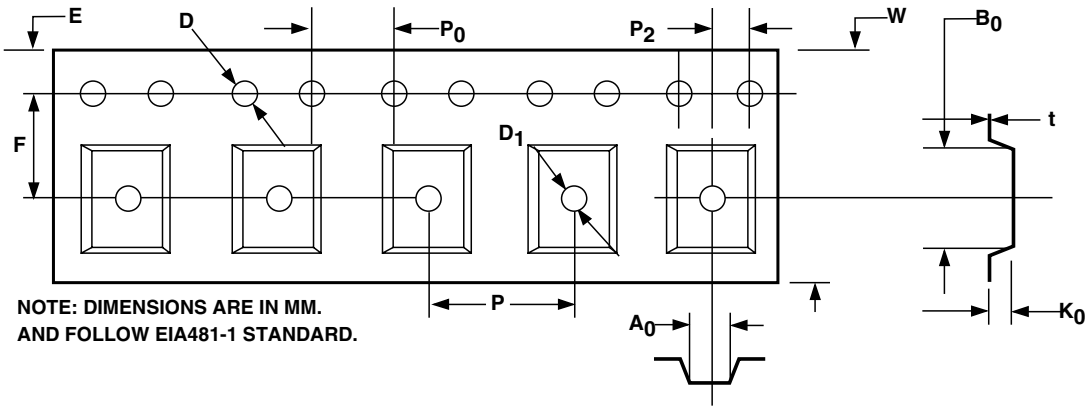
*Contact factory for dice specifications.
**Contact factory for availability.

Chip Topography



TRANSISTOR COUNT: 19
SUBSTRATE IS INTERNALLY CONNECTED TO V+

Tape-and-Reel Information



NOTE: DIMENSIONS ARE IN MM.
AND FOLLOW EIA481-1 STANDARD.

A_0	3.200	±0.102
B_0	3.099	±0.102
D	1.499	+0.102 +0.000
D_1	0.991	+0.254 +0.000

E	1.753	±0.102
F	3.505	±0.051
K_0	1.397	±0.102
P	3.988	±0.102

P_0	3.988	±0.102
$P_0$10	40.005	±0.203
P_2	2.007	±0.051
t	0.254	±0.127
W	8.001	+0.305 -0.102

5 SOT23-5