

MAX4130–MAX4134

Single/Dual/Quad, Wide-Bandwidth, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{CC} - V_{EE}$)7.5V
IN+, IN-, $\overline{SHDN}$ Voltage($V_{CC} + 0.3V$) to ($V_{EE} - 0.3V$)
Output Short-Circuit Duration (Note 1).....Continuous
(short to either supply)
Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)
5-Pin SOT23 (derate 7.1mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$).....571mW
6-Bump UCSP (derate 2.9mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$).....308mW
8-Pin SO (derate 5.88mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$).....471mW

8-Pin μMAX (derate 4.10mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$)330mW
14-Pin SO (derate 8.00mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$).....640mW
Operating Temperature Range
MAX413_E_ -40°C to $+85^\circ\text{C}$
Maximum Junction Temperature $+150^\circ\text{C}$
Storage Temperature Range -65°C to $+160^\circ\text{C}$
Lead Temperature (soldering, 10s) $+300^\circ\text{C}$
Bump Reflow Temperature $+235^\circ\text{C}$

Note 1: Provided that the maximum package power-dissipation rating is not exceeded.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

($V_{CC} = +2.7V$ to $+6.5V$, $V_{EE} = 0V$, $V_{CM} = 0V$, $V_{OUT} = V_{CC}/2$, R_L tied to $V_{CC}/2$, $\overline{SHDN} \geq 2V$ (or open), $T_A = +25^\circ\text{C}$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V _{OS}	V _{CM} = V _{EE} to V _{CC}	MAX4130EUK		±0.35	±1.50	mV
			MAX4131ESA		±0.20	±0.60	
			MAX4131EUA/ MAX4131EBT		±0.35	±1.20	
			MAX4132ESA/ MAX4133ESD		±0.25	±0.75	
			MAX4132EUA		±0.40	±1.50	
			MAX4134ESD		±0.35	±1.50	
Input Bias Current	I _B	V _{CM} = V _{EE} to V _{CC}			±50	±150	nA
Input Offset Current	I _{OS}	V _{CM} = V _{EE} to V _{CC}	MAX4131EBT			±15	nA
			All other packages			±12	
Differential Input Voltage	R _{IN}	-1.5V < V _{DIFF} < 1.5V			500		kΩ
Common-Mode Input Voltage Range	CMVR			V _{EE} - 0.25		V _{CC} + 0.25	V
Common-Mode Rejection Ratio	CMRR	V _{EE} - 0.25V < V _{CM} < V _{CC} + 0.25V	MAX4130EUK	67	90		dB
			MAX4131ESA	78	98		
			MAX4131EUA/ MAX4131EBT	68	88		
			MAX4132ESA/ MAX4133ESD	74	94		
			MAX4132EUA	66	86		
			MAX4134ESD	64	84		
Power-Supply Rejection Ratio	PSRR	V _{CC} = 2.7V to 6.5V		78	100		dB
Output Resistance	R _{OUT}	A _V = 1			0.1		Ω
Off-Leakage Current	I _{LKG}	SHDN < 0.8V, V _{OUT} = 0V to V _{CC}			±0.1	±1	μA

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DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +2.7V$ to $+6.5V$, $V_{EE} = 0V$, $V_{CM} = 0V$, $V_{OUT} = V_{CC}/2$, R_L tied to $V_{CC}/2$, $\overline{SHDN} \geq 2V$ (or open), $T_A = +25^\circ C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Large-Signal Voltage Gain	A _v	V _{CC} = 2.7V	V _{OUT} = 0.25V to 2.45V, R _L = 100kΩ		92	108	dB	
			V _{OUT} = 0.4V to 2.3V, R _L = 250Ω		72	82		
		V _{CC} = 5V	V _{OUT} = 0.25V to 4.75V, R _L = 100kΩ		94	108		
			V _{OUT} = 0.4V to 4.6V, R _L = 250Ω		75	86		
Output Voltage Swing	V _O	MAX4130/ MAX4131	R _L = 100kΩ	V _{CC} - V _{OH}	12	20	mV	
				V _{OL} - V _{EE}	20	35		
			R _L = 250Ω	V _{CC} - V _{OH}	240	290		
				V _{OL} - V _{EE}	125	170		
		MAX4132/ MAX4133/ MAX4134	R _L = 100kΩ	V _{CC} - V _{OH}	15	30		
				V _{OL} - V _{EE}	25	40		
			R _L = 250Ω	V _{CC} - V _{OH}	280	330		
				V _{OL} - V _{EE}	180	230		
Output Short-Circuit Current	I _{SC}				50		mA	
SHDN Logic Threshold	V _{IL}	MAX4131–MAX4134		Low	0.8		V	
	V _{IH}			High	2.0			
SHDN Input Current	I _{IL}	MAX4131–MAX4134			±1	±3	μA	
Operating Supply Voltage Range	V _{CC}				2.7	6.5	V	
Supply Current per Amplifier	I _{CC}	V _{CM} = V _{OUT} = V _{CC} /2		V _{CC} = 2.7V	900	1050	μA	
				V _{CC} = 5V	1000	1150		
Shutdown Supply Current per Amplifier	I _{SHDN}	SHDN > 0.8V, MAX4131–MAX4134		V _{CC} = 2.7V	25	40	μA	
				V _{CC} = 5V	40	60		

DC ELECTRICAL CHARACTERISTICS

($V_{CC} = +2.7V$ to $+6.5V$, $V_{EE} = 0V$, $V_{CM} = 0V$, $V_{OUT} = V_{CC}/2$, R_L tied to $V_{CC}/2$, $\overline{SHDN} \geq 2V$ (or open), $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$V_{CM} = V_{EE}$ to V_{CC}	MAX4130EUK			± 3.50	mV
			MAX4131ESA			± 0.75	
			MAX4131EUA/MAX4131EBT			± 4.40	
			MAX4132ESA/MAX4133ESD			± 0.95	
			MAX4132EUA			± 4.70	
			MAX4134ESD			± 4.00	
Input Offset Voltage Tempco	TCV_{OS}			± 2			$\mu V/^\circ C$
Input Bias Current	I_B	$V_{CM} = V_{EE}$ to V_{CC}				± 160	nA

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DC ELECTRICAL CHARACTERISTICS

($V_{CC} = +2.7V$ to $+6.5V$, $V_{EE} = 0V$, $V_{CM} = 0V$, $V_{OUT} = V_{CC}/2$, R_L tied to $V_{CC}/2$, $\overline{SHDN} \geq 2V$ (or open), $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Current	I_{OS}	$V_{CM} = V_{EE}$ to V_{CC}	MAX4131EBT			± 24	nA
			All other packages			± 18	
Common-Mode Input Voltage Range	CMVR			$V_{EE} - 0.20$		$V_{CC} + 0.20$	V
Common-Mode Rejection Ratio	CMRR	$V_{EE} - 0.2V < V_{CM} < V_{CC} + 0.2V$	MAX4130EUK			62	dB
			MAX4131ESA			76	
			MAX4131EUA/MAX4131EBT			60	
			MAX4132ESA/MAX4133ESD			74	
			MAX4132EUA			58	
			MAX4134ESD			60	
Power-Supply Rejection Ratio	PSRR	$V_{CC} = 2.7V$ to $6.5V$				74	dB
Off-Leakage Current	I_{LKG}	$\overline{SHDN} < 0.8V$, $V_{OUT} = 0V$ to V_{CC}				± 12	μA
Large-Signal Voltage Gain	A_v	$V_{CC} = 2.7V$	$V_{OUT} = 0.25V$ to $2.45V$, $R_L = 100k\Omega$			84	dB
			$V_{OUT} = 0.4V$ to $2.3V$, $R_L = 250\Omega$			66	
		$V_{CC} = 5V$	$V_{OUT} = 0.25V$ to $4.75V$, $R_L = 100k\Omega$			86	
			$V_{OUT} = 0.4V$ to $4.6V$, $R_L = 250\Omega$			68	
Output Voltage Swing	V_O	MAX4130/ MAX4131ESA/ MAX4131EUA	$R_L = 100k\Omega$	$V_{CC} - V_{OH}$		25	mV
				$V_{OL} - V_{EE}$		40	
			$R_L = 250\Omega$	$V_{CC} - V_{OH}$		300	
				$V_{OL} - V_{EE}$		190	
		MAX4131EBT	$R_L = 100k\Omega$	$V_{CC} - V_{OH}$		25	
				$V_{OL} - V_{EE}$		40	
			$R_L = 250\Omega$	$V_{CC} - V_{OH}$		350	
				$V_{OL} - V_{EE}$		190	
		MAX4132/ MAX4133/ MAX4134	$R_L = 100k\Omega$	$V_{CC} - V_{OH}$		35	
				$V_{OL} - V_{EE}$		50	
			$R_L = 250\Omega$	$V_{CC} - V_{OH}$		350	
				$V_{OL} - V_{EE}$		250	

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DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +2.7V$ to $+6.5V$, $V_{EE} = 0V$, $V_{CM} = 0V$, $V_{OUT} = V_{CC}/2$, R_L tied to $V_{CC}/2$, $\overline{SHDN} \geq 2V$ (or open), $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
$\overline{\text{SHDN}}$ Logic Threshold	V_{IL}	MAX4131–MAX4134		Low			0.8	V
	V_{IH}			High	2.0			
$\overline{\text{SHDN}}$ Input Current	I_{IL}	MAX4131–MAX4134					± 3	μA
Operating Supply Voltage Range	V_{CC}				2.7		6.5	V
Supply Current per Amplifier	I_{CC}	$V_{\text{CM}} = V_{\text{OUT}} = V_{\text{CC}}/2$	MAX4131EBT	$V_{\text{CC}} = 2.7\text{V}$			1200	μA
				$V_{\text{CC}} = 5\text{V}$			1350	
			All other devices	$V_{\text{CC}} = 2.7\text{V}$			1100	
				$V_{\text{CC}} = 5\text{V}$			1200	
Shutdown Supply Current per Amplifier	$I_{\overline{\text{SHDN}}}$	$\overline{\text{SHDN}} > 0.8\text{V}$, MAX4131–MAX4134		$V_{\text{CC}} = 2.7\text{V}$			50	μA
				$V_{\text{CC}} = 5\text{V}$			70	

Note 2: All devices are 100% tested at $T_A = +25^\circ C$. MAX4130EUK/MAX4131EBT temperature limits are guaranteed by design.

AC ELECTRICAL CHARACTERISTICS

($V_{CC} = +2.7V$ to $+6.5V$, $V_{EE} = 0V$, $\overline{SHDN} \geq 2V$ (or open), $T_A = +25^\circ C$, unless otherwise noted.)

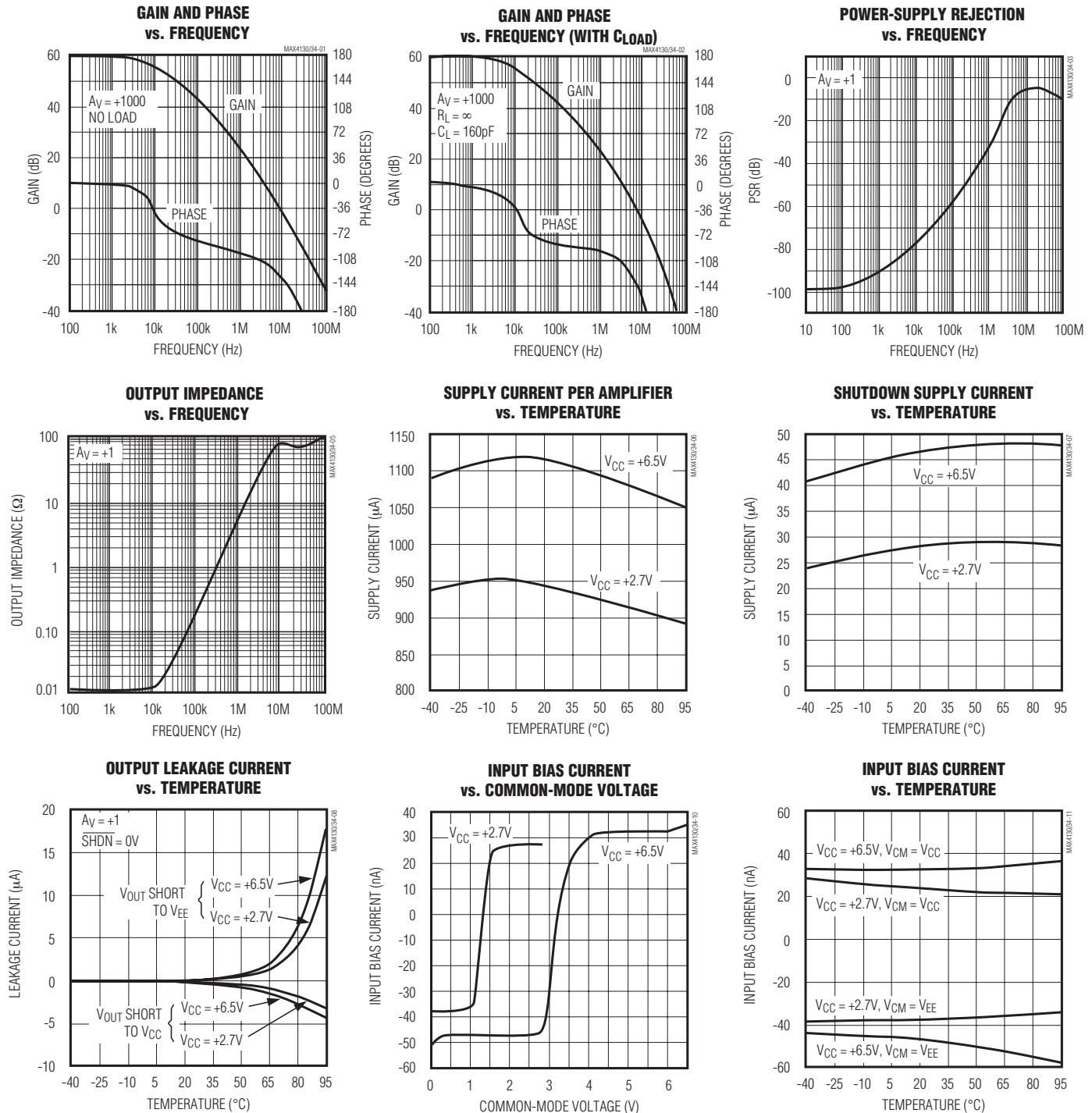
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Gain-Bandwidth Product	GBWP				10		MHz
Phase Margin	θ_M				62		Degrees
Gain Margin	G_M				12		dB
Total Harmonic Distortion	THD	$f = 10kHz$, $V_{OUT} = 2V_{P-P}$ ($A_V = 1$)			0.003		%
Slew Rate	SR				4		V/ μs
Settling Time to 0.01%	t_S	$A_V = 1$, $V_{OUT} = 2V$ step			2.0		μs
Turn-On Time	t_{ON}	$V_{CC} = 0V$ to $3V$ step, $V_{OUT} = V_{CC}/2$			1		μs
$\overline{SHDN}$ Delay		MAX4131–MAX4134, $V_{CC} = 3V$, $V_{OUT} = V_{CC}/2$	Enable		1		μs
			Disable		0.2		
Input Capacitance	C_{IN}				3		pF
Input Noise-Voltage Density	e_n	$f = 1kHz$			22		$nV/\sqrt{Hz}$
Input Noise-Current Density	i_n	$f = 1kHz$			0.4		$pA/\sqrt{Hz}$
Capacitive-Load Stability	C_L	$A_V = 1$			160		pF

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Typical Operating Characteristics

($V_{CC} = +5V$, $V_{EE} = 0V$, $V_{CM} = V_{CC} / 2$, $T_A = +25^\circ C$, unless otherwise noted.)



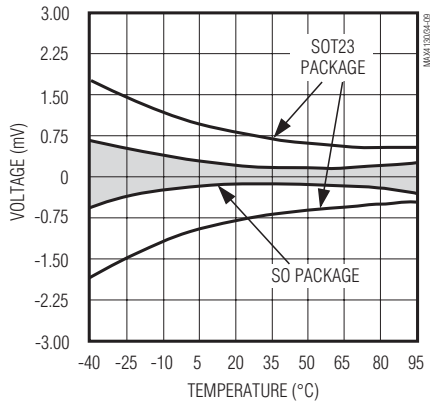
MAX4130-MAX4134

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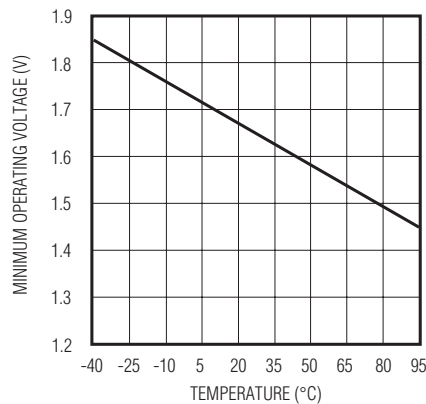
Typical Operating Characteristics (continued)

($V_{CC} = +5V$, $V_{EE} = 0V$, $V_{CM} = V_{CC} / 2$, $T_A = +25^\circ C$, unless otherwise noted.)

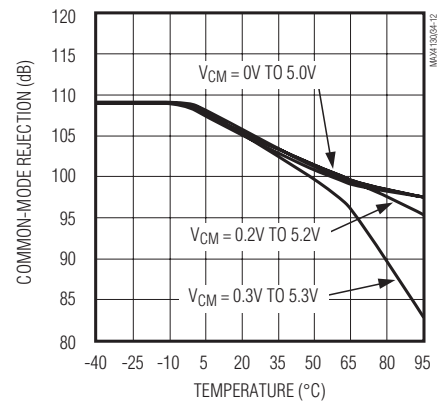
**INPUT OFFSET VOLTAGE
vs. TEMPERATURE**



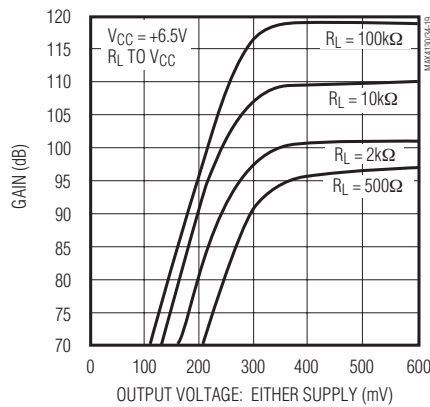
**MINIMUM OPERATING VOLTAGE
vs. TEMPERATURE**



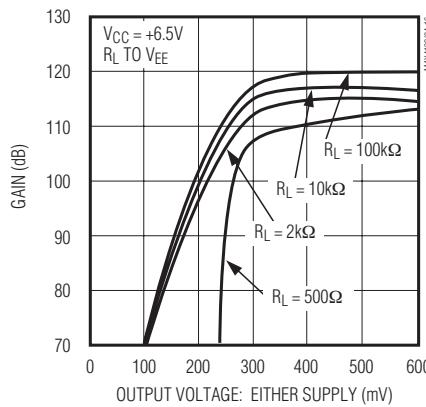
**COMMON-MODE REJECTION
vs. TEMPERATURE**



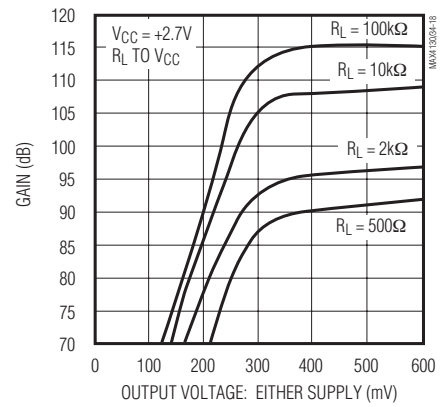
**LARGE-SIGNAL GAIN
vs. OUTPUT VOLTAGE**



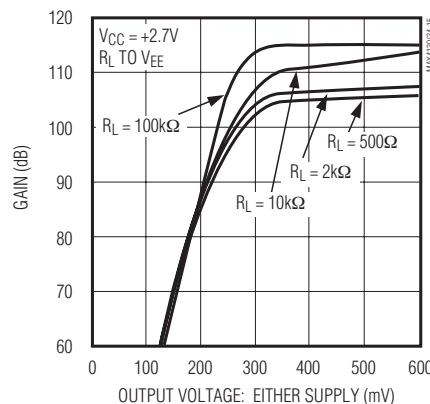
**LARGE-SIGNAL GAIN
vs. OUTPUT VOLTAGE**



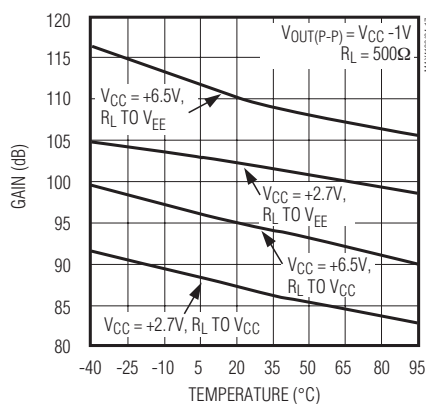
**LARGE-SIGNAL GAIN
vs. OUTPUT VOLTAGE**



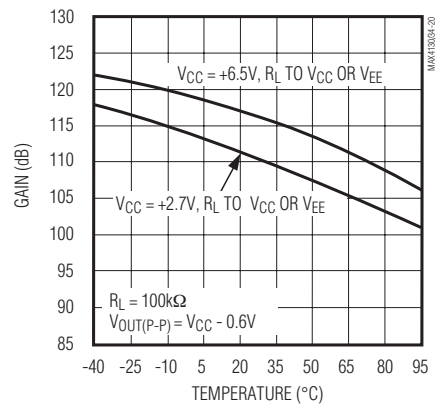
**LARGE-SIGNAL GAIN
vs. OUTPUT VOLTAGE**



**LARGE-SIGNAL GAIN
vs. TEMPERATURE**



**LARGE-SIGNAL GAIN
vs. TEMPERATURE**



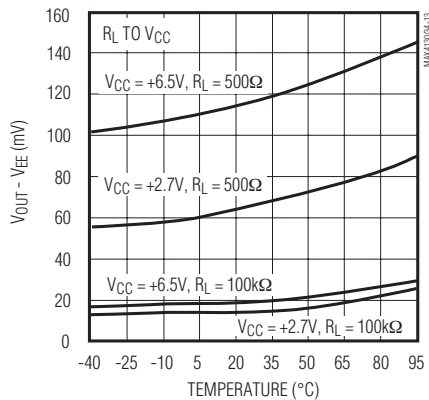
MAX4130-MAX4134

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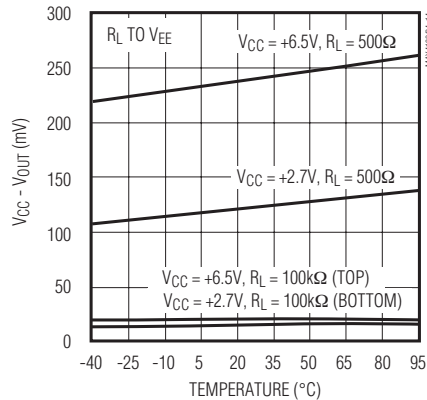
Typical Operating Characteristics (continued)

($V_{CC} = +5V$, $V_{EE} = 0V$, $V_{CM} = V_{CC} / 2$, $T_A = +25^\circ C$, unless otherwise noted.)

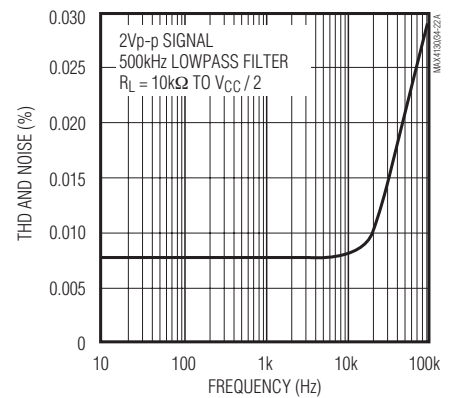
**MINIMUM OUTPUT VOLTAGE
vs. TEMPERATURE**



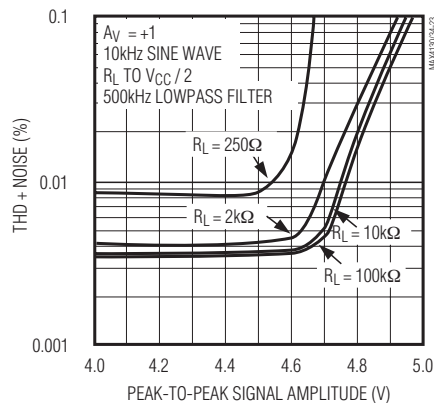
**MAXIMUM OUTPUT VOLTAGE
vs. TEMPERATURE**



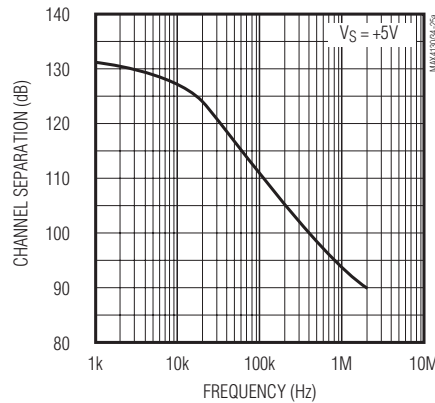
**TOTAL HARMONIC DISTORTION
AND NOISE vs. FREQUENCY**



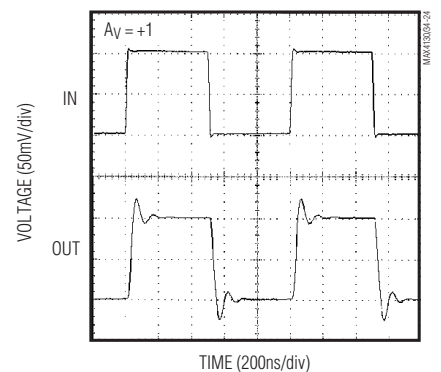
**TOTAL HARMONIC DISTORTION AND NOISE
vs. PEAK-TO-PEAK SIGNAL AMPLITUDE**



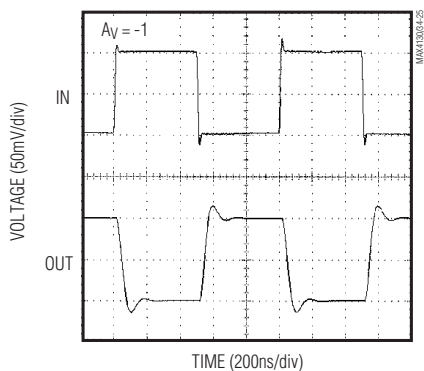
**CHANNEL SEPARATION
vs. FREQUENCY**



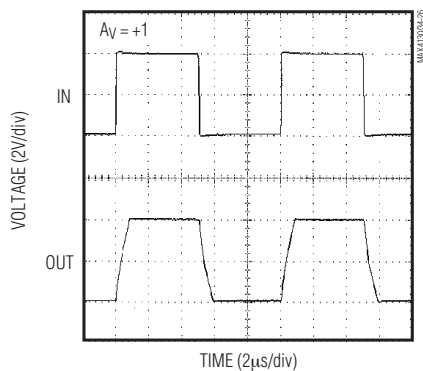
**MAX4131
SMALL-SIGNAL TRANSIENT
RESPONSE (NONINVERTING)**



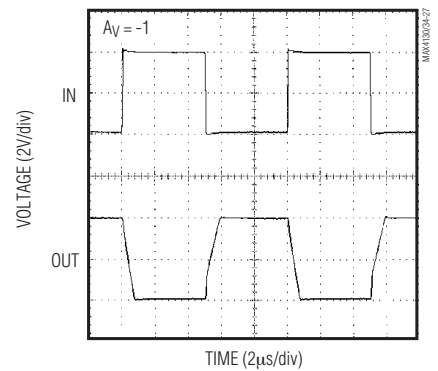
**MAX4131
SMALL-SIGNAL TRANSIENT
RESPONSE (INVERTING)**



**MAX4131
LARGE-SIGNAL TRANSIENT
RESPONSE (NONINVERTING)**



**MAX4131
LARGE-SIGNAL TRANSIENT
RESPONSE (INVERTING)**



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Pin Description

PIN						NAME	FUNCTION
MAX4130	MAX4131		MAX4132	MAX4133	MAX4134		
	SO/μMAX	UCSP					
1	6	A2	—	—	—	OUT	Output
2	4	A1	4	4	11	V _{EE}	Negative Supply. Connect to GND for single-supply operation.
3	3	B1	—	—	—	IN+	Noninverting Input
4	2	B2	—	—	—	IN-	Inverting Input
5	7	A3	8	14	4	V _{CC}	Positive Supply
—	1, 5	—	—	5, 7, 8, 10	—	N.C.	No Connection. Not internally connected.
—	8	B3	—		—	$\overline{\text{SHDN}}$	Shutdown Control. Connect to V _{CC} or leave floating to enable amplifier.
—	—	—	1, 7	1, 13	1, 7	OUT1, OUT2	Outputs for Amps 1 and 2
—	—	—	2, 6	2, 12	2, 6	IN1-, IN2-	Inverting Inputs for Amps 1 and 2
—	—	—	3, 5	3, 11	3, 5	IN1+, IN2+	Noninverting Inputs for Amps 1 and 2
—	—	—	—	6, 9	—	$\overline{\text{SHDN1}}$, SHDN2	Shutdown Control. Provides independent shutdown control for amps 1 and 2. Connect to V _{CC} or leave floating to enable amplifiers.
—	—	—	—	—	8, 14	OUT3, OUT4	Outputs for Amps 3 and 4
—	—	—	—	—	9, 13	IN3-, IN4-	Inverting Inputs for Amps 3 and 4
—	—	—	—	—	10, 12	IN3+, IN4+	Noninverting Inputs for Amps 3 and 4

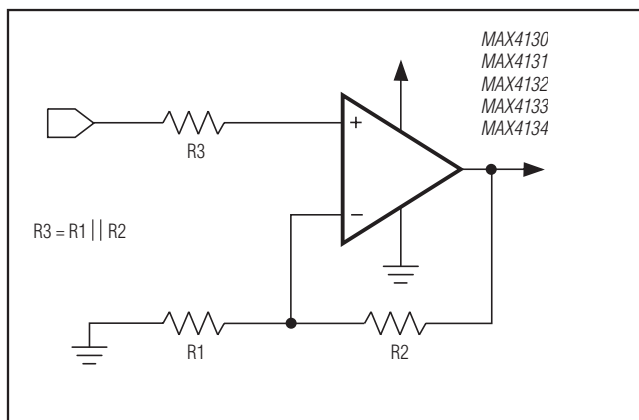


Figure 1a. Reducing Offset Error Due to Bias Current (Noninverting)

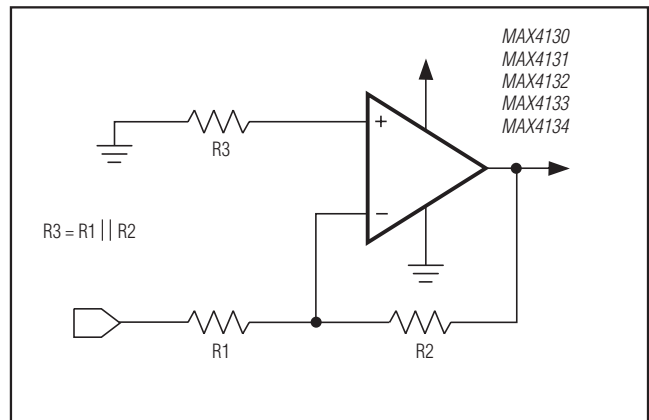


Figure 1b. Reducing Offset Error Due to Bias Current (Inverting)

MAX4130–MAX4134

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Applications Information

Rail-to-Rail Input Stage

Devices in the MAX4130–MAX4134 family of high-speed amplifiers have rail-to-rail input and output stages designed for low-voltage, single-supply operation. The input stage consists of separate NPN and PNP differential stages that combine to provide an input common-mode range that extends 0.2V beyond the supply rails. The PNP stage is active for input voltages close to the negative rail, and the NPN stage is active for input voltages near the positive rail. The input offset voltage is typically below 200μV. The switchover transition region, which occurs near $V_{CC} / 2$, has been extended to minimize the slight degradation in common-mode rejection ratio caused by the mismatch of the input pairs. Their low offset voltage, high bandwidth, and rail-to-rail common-mode range make these op amps excellent choices for precision, low-voltage data-acquisition systems.

Since the input stage switches between the NPN and PNP pairs, the input bias current changes polarity as the input voltage passes through the transition region.

Reduce the offset error caused by input bias currents flowing through external source impedances by matching the effective impedance seen by each input (Figures 1a, 1b). High source impedances, together with input capacitance, can create a parasitic pole that produces an underdamped signal response. Reducing the input impedance or placing a small (2pF to 10pF) capacitor across the feedback resistor improves response.

The MAX4130–MAX4134s' inputs are protected from large differential input voltages by 1kΩ series resistors and back-to-back triple diodes across the inputs (Figure 2). For differential input voltages less than 1.8V, input resistance is typically 500kΩ. For differential input voltages greater than 1.8V, input resistance is approximately 2kΩ. The input bias current is given by the following equation:

$$I_{BIAS} = \frac{V_{DIFF} - 1.8V}{2k\Omega}$$

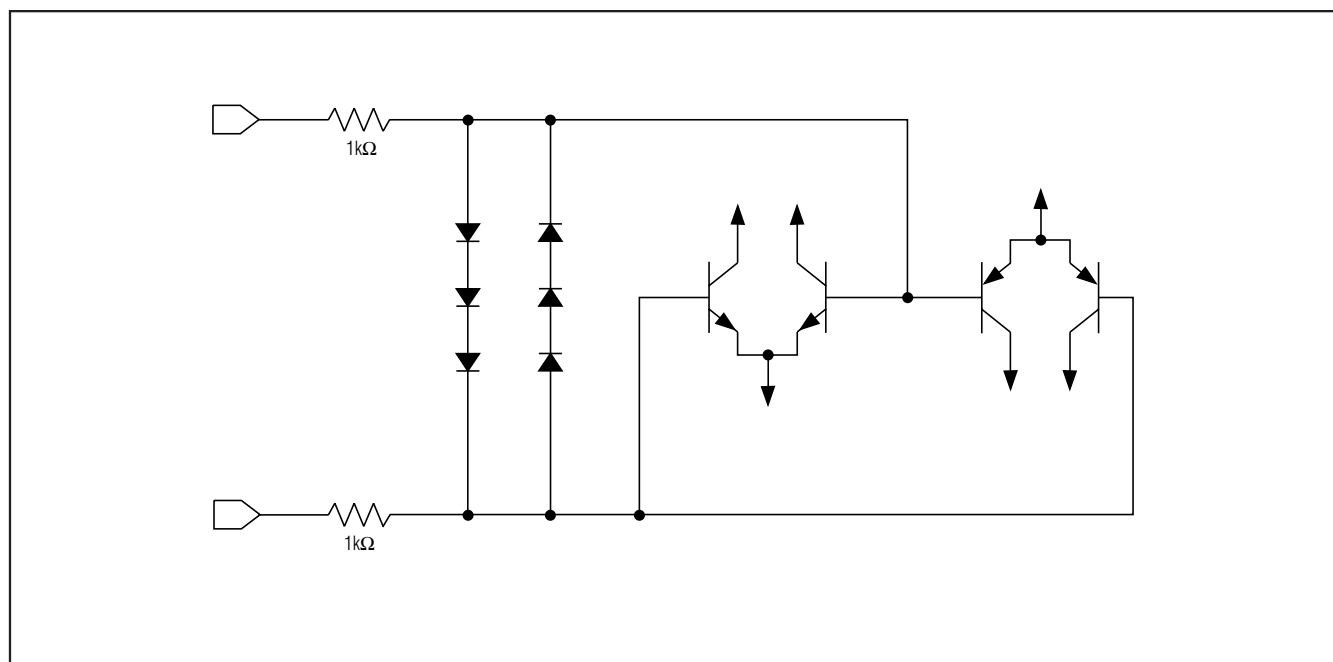


Figure 2. Input Protection Circuit

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Rail-to-Rail Output Stage

The minimum output voltage is within millivolts of ground for single-supply operation where the load is referenced to ground (V_{EE}). Figure 3 shows the input voltage range and output voltage swing of a MAX4131 connected as a voltage follower. With a +3V supply and the load tied to ground, the output swings from 0.00V to 2.90V. The maximum output voltage swing depends on the load, but will be within 150mV of a +3V supply, even with the maximum load (500 Ω to ground).

Driving a capacitive load can cause instability in most high-speed op amps, especially those with low quiescent current. The MAX4130–MAX4134 have a high tolerance for capacitive loads. They are stable with capacitive loads up to 160pF. Figure 4 gives the stable operating region for capacitive loads. Figures 5 and 6 show the response with capacitive loads and the results of adding an isolation resistor in series with the output (Figure 7). The resistor improves the circuit's phase margin by isolating the load capacitor from the op amp's output.

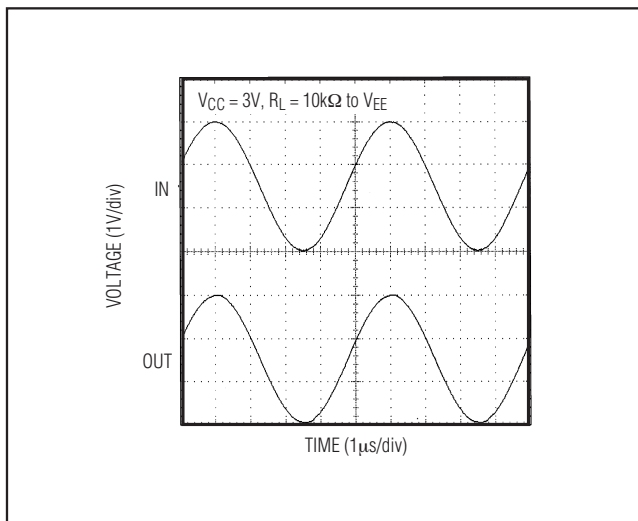


Figure 3. Rail-to-Rail Input/Output Voltage Range

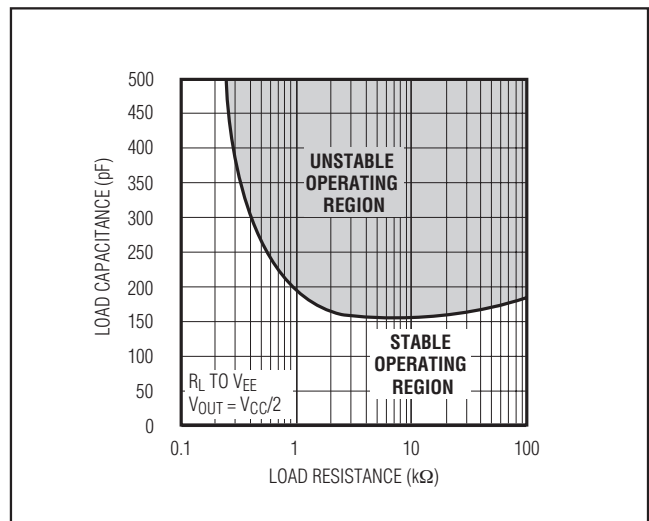


Figure 4. Capacitive-Load Stability

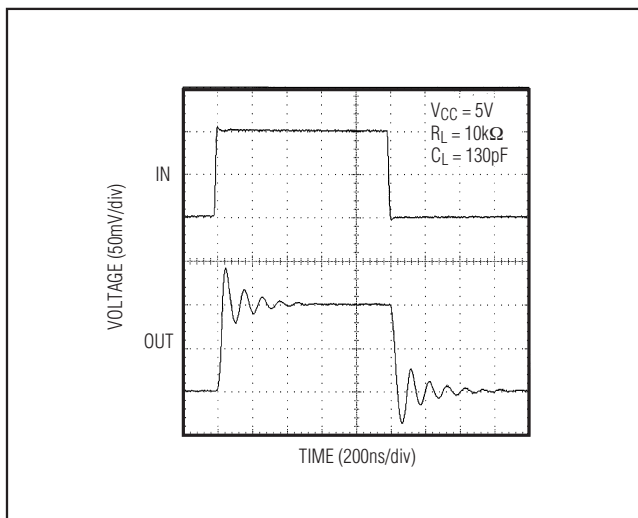


Figure 5. MAX4131 Small-Signal Transient Response with Capacitive Load

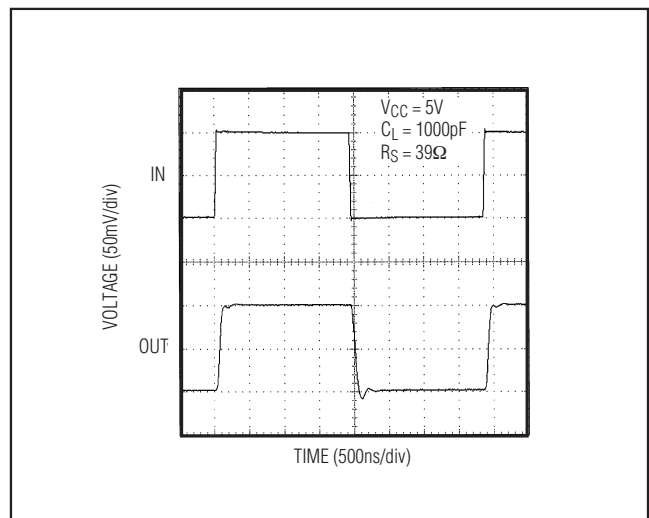


Figure 6. MAX4131 Transient Response to Capacitive Load with Isolation Resistor

MAX4130–MAX4134

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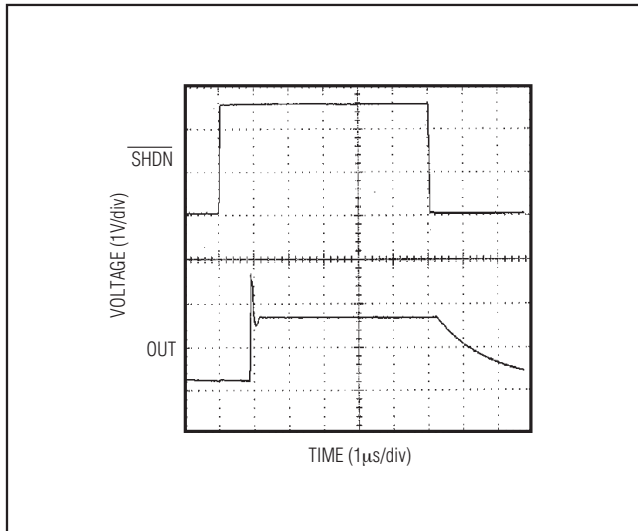


Figure 11. Shutdown Output Voltage

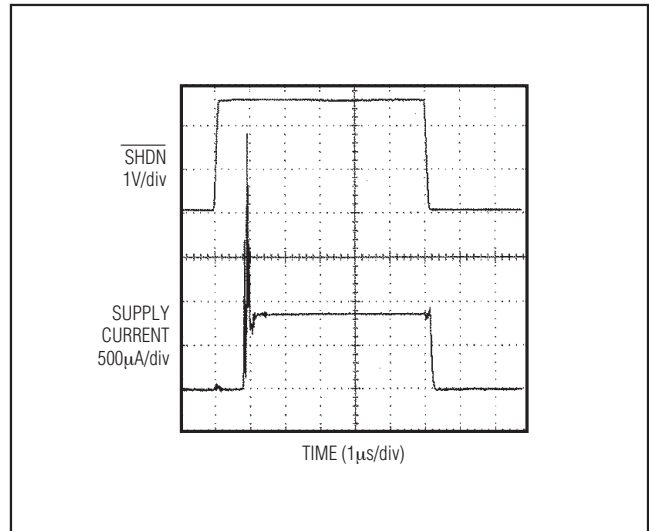


Figure 12. Shutdown Enable/Disable Supply Current

Power Supplies and Layout

The MAX4130–MAX4134 operate from a single +2.7V to +6.5V power supply, or from dual supplies of $\pm 1.35\text{V}$ to $\pm 3.25\text{V}$. For single-supply operation, bypass the power supply with a $0.1\mu\text{F}$ ceramic capacitor in parallel with at least $1\mu\text{F}$. For dual supplies, bypass each supply to ground.

Good layout improves performance by decreasing the amount of stray capacitance at the op amp's inputs and outputs. Decrease stray capacitance by placing external components close to the op amp's pins, minimizing trace lengths and resistor leads.

UCSP Applications Information

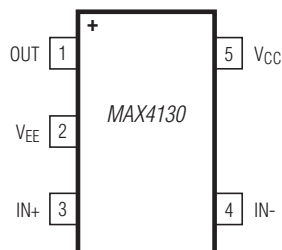
For the latest application details on UCSP construction, dimensions, tape carrier information, PC board techniques, bump-pad layout, and the recommended reflow temperature profile, as well as the latest information on reliability testing results, go to Maxim's website at www.maxim-ic.com/ucsp and search for the Application Note: *UCSP–A Wafer-Level Chip-Scale Package*.

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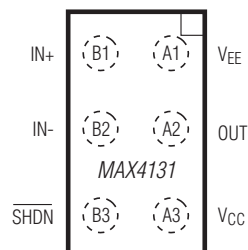
Pin Configurations

TOP VIEW

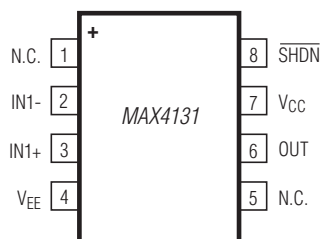


SOT23

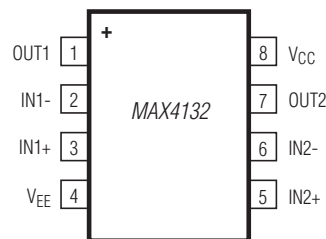
TOP VIEW
BUMPS ON BOTTOM



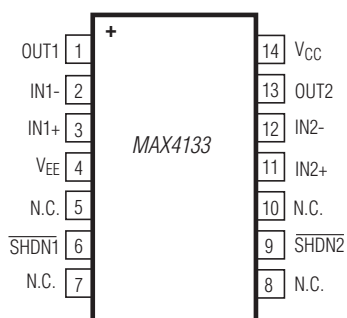
UCSP



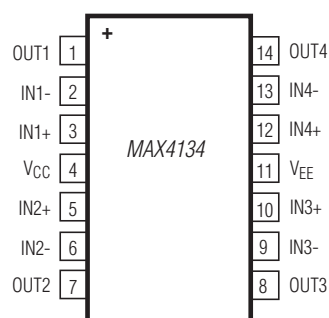
SO/μMAX



SO/μMAX



SO



SO

MAX4130–MAX4134

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Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX4132ESA	-40°C to +85°C	8 SO	—
MAX4132EUA	-40°C to +85°C	8 μ MAX	—
MAX4133C/D	0°C to +70°C	Dice*	—
MAX4133ESD	-40°C to +85°C	14 SO	—
MAX4134ESD	-40°C to +85°C	14 SO	—

*Dice are specified at $T_A = +25^\circ\text{C}$, DC parameters only.

Chip Information

MAX4130 TRANSISTOR COUNT: 170

MAX4131 TRANSISTOR COUNT: 170

MAX4132 TRANSISTOR COUNT: 340

MAX4134 TRANSISTOR COUNT: 680

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
5 SOT23	U5-1	21-0057	90-0174
6 UCSP	B6-3	21-0097	Refer to Application Note 1891
8 μ MAX	U8-1	21-0036	90-0092
8 SO	S8-2	21-0041	90-0096
14 SO	S14-1	21-0041	90-0012
14 SO	S14M-6	21-0041	90-0012

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/96	Initial release	—
1	1/14	Updated <i>Electrical Characteristics</i>	2, 4



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