TABLE OF CONTENTS

REVISION HISTORY

9/14—Rev. C to Rev. D

Changes to Figure 4 and Figure 7 ... 6

4/13—Rev. B to Rev. C

Updated Format ... Universal
Added Applications Section, Deleted Figure 2,
Renumbered Sequentially ... 1
Deleted Table 3, Renumbered Sequentially ... 4
Changes to Table 3 ... 5
Changes to Typical Performance Characteristics Section ... 6
Updated Outline Dimensions ... 11
Changes to Ordering Guide ... 11

2/02—Rev. A to Rev. B

Edits to Features ... 1
Deleted Wafer Test Limits ... 3
Deleted DICE Characteristics ... 3
Edits to Table 5 ... 7

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_{CB} = 15 V, I_C = 10 µA, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	MAT01AH Min	MAT01AH Typ	MAT01AH Max	MAT01GH Min	MAT01GH Typ	MAT01GH Min	Unit
VOLTAGE									
Breakdown Voltage	BV_{CEO}	I_C = 100 µA	45			45			V
Offset Voltage	V_{OS}			0.04	0.1		0.10	0.5	mV
Offset Voltage Stability									
First Month[1]	V_{OS}/Time			2.0			2.0		µV/Mo
Long Term[2]				0.2			0.2		µV/Mo
CURRENT									
Offset Current	I_{OS}			0.1	0.6		0.2	3.2	nA
Bias Current	I_B			13	20		18	40	nA
Current Gain	h_{FE}	I_C = 10 nA		590			430		
		I_C = 10 µA	500	770		250	560		
		I_C = 10 mA		840			610		
Current Gain Match	Δh_{FE}	I_C = 10 µA		0.7	3.0		1.0	8.0	%
		100 nA ≤ I_C ≤ 10 mA		0.8			1.2		%
NOISE									
Low Frequency Noise Voltage	e_n p-p	0.1 Hz to 10 Hz[3]		0.23	0.4		0.23	0.4	µV p-p
Broadband Noise Voltage	e_n rms	1 Hz to 10 kHz		0.60			0.60		µV rms
Noise Voltage Density	e_n	f_O = 10 Hz[3]		7.0	9.0		7.0	9.0	nV/√Hz
		f_O = 100 Hz[3]		6.1	7.6		6.1	7.6	nV/√Hz
		f_O = 1000 Hz[3]		6.0	7.5		6.0	7.5	nV/√Hz
OFFSET VOLTAGE/CURRENT									
Offset Voltage Change	$\Delta V_{OS}/\Delta V_{CB}$	0 ≤ V_{CB} ≤ 30 V		0.5	3.0		0.8	8.0	µV/V
Offset Current Change	$\Delta I_{OS}/\Delta V_{CB}$	0 ≤ V_{CB} ≤ 30 V		2	15		3	70	pA/V
LEAKAGE									
Collector to Base Leakage Current	I_{CBO}	V_{CB} = 30 V, I_E = 0[4]		15	50		25	200	pA
Collector to Emitter Leakage Current	I_{CES}	V_{CE} = 30 V, V_{BE} = 0[4, 5]		50	200		90	400	pA
Collector to Collector Leakage Current	I_{CC}	V_{CC} = 30 V[5]		20	200		30	400	pA
SATURATION									
Collector Saturation Voltage	$V_{CE(SAT)}$	I_B = 0.1 mA, I_C = 1 mA		0.12	0.20		0.12	0.25	V
		I_B = 1 mA, I_C = 10 mA		0.8			0.8		V
GAIN BANDWIDTH PRODUCT	f_T	V_{CE} = 10 V, I_C = 10 mA		450			450		MHz
CAPACITANCE									
Output Capacitance	C_{OB}	V_{CB} = 15 V, I_E = 0		2.8			2.8		pF
Collector to Collector Capacitance	C_{CC}	V_{CC} = 0		8.5			8.5		pF

[1] Exclude first hour of operation to allow for stabilization.
[2] Parameter describes long-term average drift after first month of operation.
[3] Sample tested.
[4] The collector to base (I_{CBO}) and collector to emitter (I_{CES}) leakage currents can be reduced by a factor of 2 to 10 times by connecting the substrate (package) to a potential that is lower than either collector voltage.
[5] I_{CC} and I_{CES} are guaranteed by measurement of I_{CBO}.

V_{CB} = 15 V, I_C = 10 µA, −55°C ≤ T_A ≤ +125°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	MAT01AH			MAT01GH			Unit
			Min	Typ	Max	Min	Typ	Min	
OFFSET VOLTAGE/CURRENT									
Offset Voltage	V_{OS}			0.06	0.15		0.14	0.70	mV
Average Offset Voltage Drift[1]	TCV_{OS}			0.15	0.50		0.35	1.8	µV/°C
Offset Current	I_{OS}			0.9	8.0		1.5	15.0	nA
Average Offset Current Drift[2]	TCI_{OS}			10	90		15	150	pA/°C
BIAS CURRENT	I_B			28	60		36	130	nA
CURRENT GAIN	h_{FE}		167	400		77	300		
LEAKAGE CURRENT									
Collector to Base Leakage Current	I_{CBO}	T_A = 125°C, V_{CB} = 30 V, I_E = 0[3]		15	80		25	200	nA
Collector to Emitter Leakage Current	I_{CES}	T_A = 125°C, V_{CE} = 30 V, V_{BE} = 0[1, 3]		50	300		90	400	nA
Collector to Collector Leakage Current	I_{CC}	T_A = 125°C, V_{CC} = 30 V[1]		30	200		50	400	nA

[1] Guaranteed by V_{OS} test $\left(TCV_{OS} \cong \frac{V_{OS}}{T} \text{ for } V_{OS} << V_{BE}\right)$, T = 298 K for T_A = 25°C.

[2] Guaranteed by I_{OS} test limits over temperature.

[3] The collector to base (I_{CBO}) and collector to emitter (I_{CES}) leakage currents can be reduced by a factor of 2 to 10 times by connecting the substrate (package) to a potential that is lower than either collector voltage.

ABSOLUTE MAXIMUM RATINGS

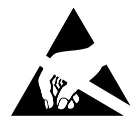
Table 3.

Parameter[1]	Rating
Breakdown Voltage of	
Collector to Base Voltage (BV_{CBO})	45 V
Collector to Emitter Voltage (BV_{CEO})	45 V
Collector to Collector Voltage (BV_{CC})	45 V
Emitter to Emitter Voltage (BV_{EE})	45 V
Emitter to Base Voltage (BV_{EBO})[2]	5 V
Current	
Collector (I_C)	25 mA
Emitter (I_E)	25 mA
Total Power Dissipation	
Case Temperature ≤ 40°C[3]	1.8 W
Ambient Temperature ≤ 70°C[4]	500 mW
Temperature Range	
Operating	−55°C to +125°C
Junction	−55°C to +150°C
Storage	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

[1] Absolute maximum ratings apply to packaged devices.
[2] Application of reverse bias voltages in excess of rating shown can result in degradation of h_{FE} and h_{FE} matching characteristics. Do not attempt to measure BV_{EBO} greater than the 5 V rating.
[3] Rating applies to applications using heat sinking to control case temperature. Derate linearity at 16.4 mW/°C for case temperatures above 40°C.
[4] Rating applies to applications not using heat sinking; device in free air only. Derate linearity at 6.3 mW/°C for ambient temperatures above 70°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

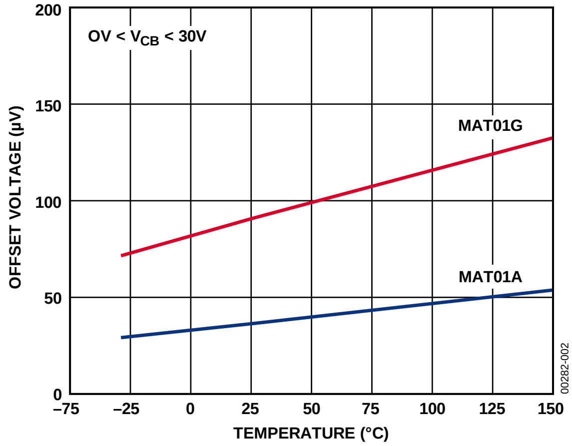


Figure 2. Offset Voltage vs. Temperature

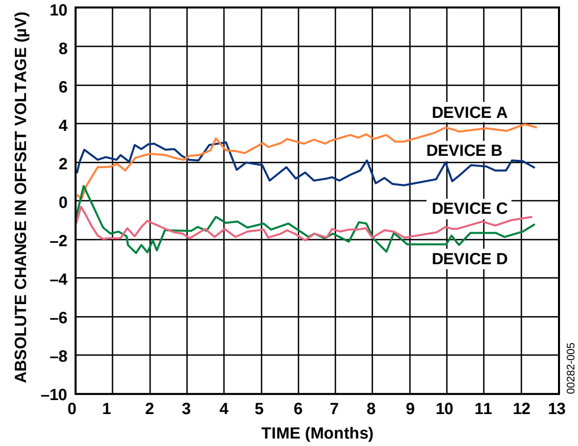


Figure 5. Offset Voltage vs. Time

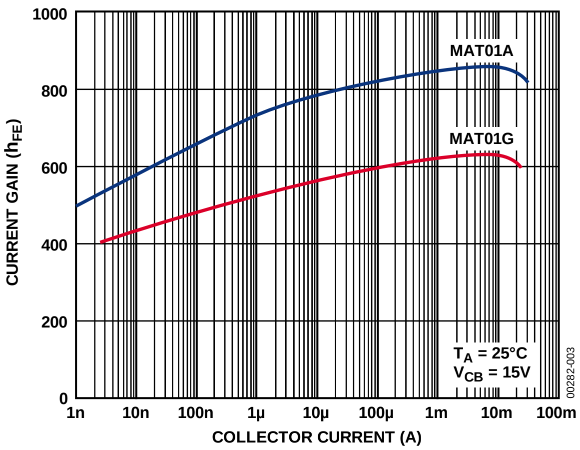


Figure 3. Current Gain vs. Collector Current

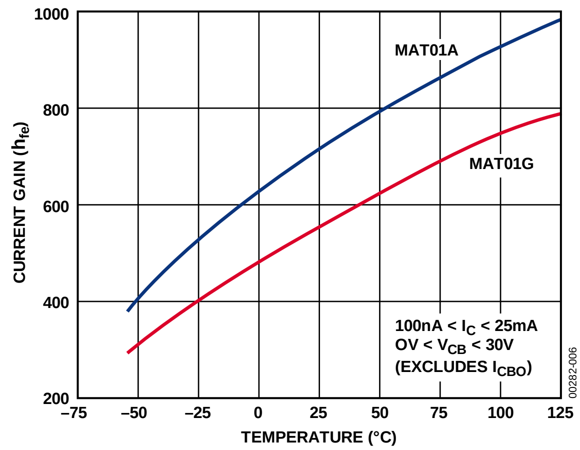


Figure 6. Current Gain vs. Temperature

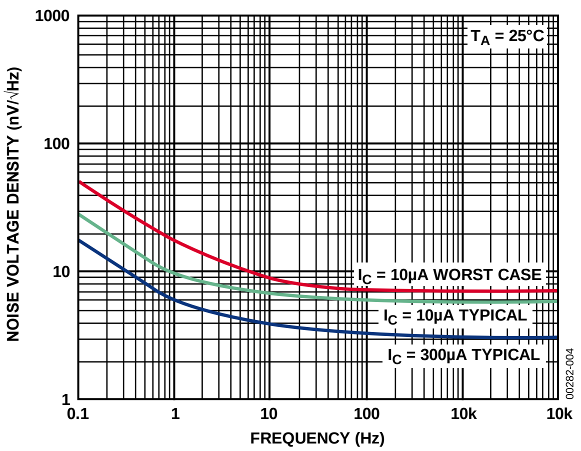


Figure 4. Noise Voltage Density vs. Frequency

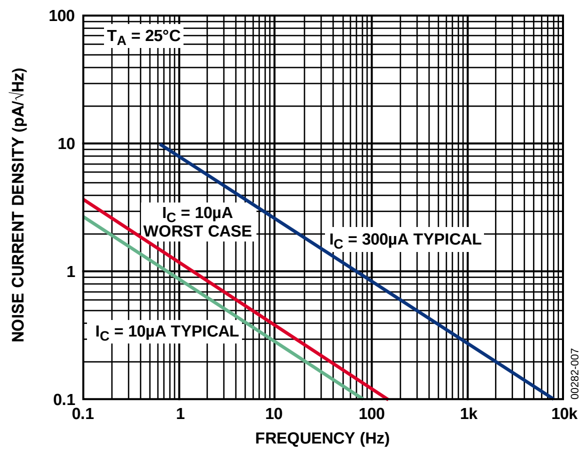


Figure 7. Noise Current Density vs. Frequency

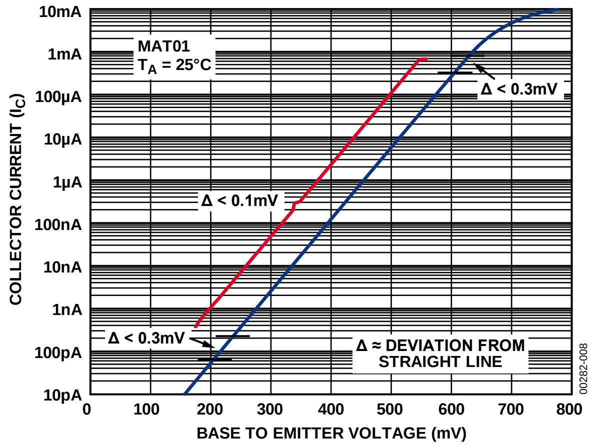


Figure 8. Collector Current vs. Base to Emitter Voltage

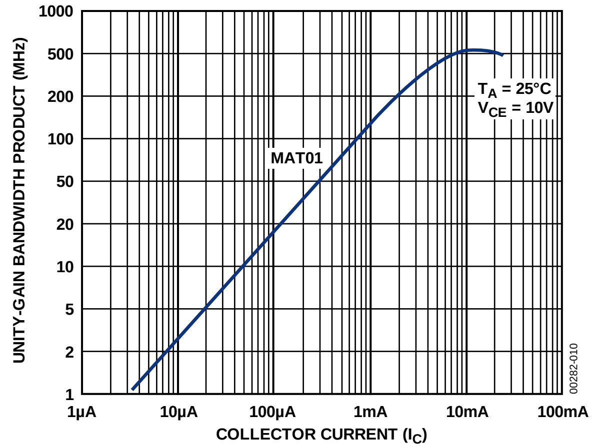


Figure 10. Unity-Gain Bandwidth vs. Collector Current

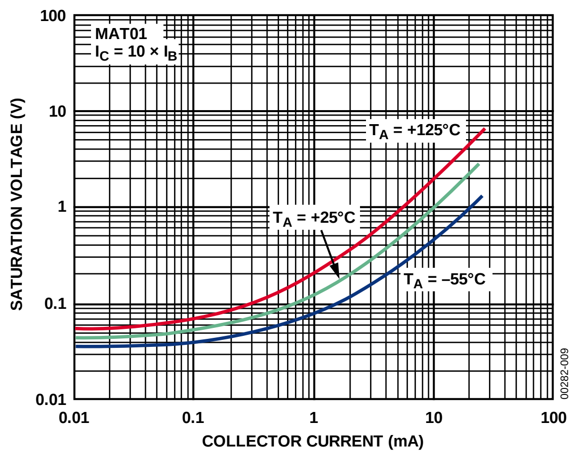
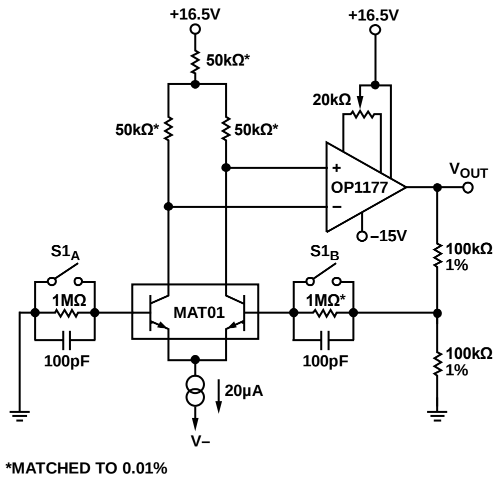


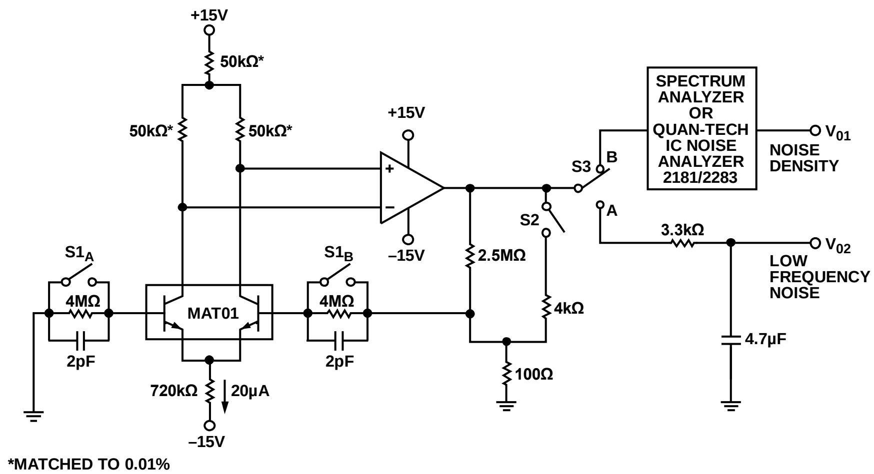
Figure 9. Saturation Voltage vs. Collector Current

TEST CIRCUITS



TEST	$S1_A$	$S1_B$	UNITS	
V_{OS}	CLOSED	CLOSED	V_{OUT1}	1V PER mV
I_{OS}	OPEN	OPEN	$V_{OUT2} - V_{OUT1}$	1V PER nA

Figure 11. Matching Measurement Circuit



TEST	$S1_A$	$S1_B$	S2	S3**	READING
NOISE VOLTAGE DENSITY (PER TRANSISTOR)	CLOSED	CLOSED	CLOSED	A	$V_{01}/\sqrt{2}$
NOISE CURRENT DENSITY (PER TRANSISTOR)	OPEN	OPEN	CLOSED	A	$V_{01}/(\sqrt{2} \times 4M\Omega)$
LOW FREQUENCY NOISE (REFERRED TO INPUT)	CLOSED	CLOSED	OPEN	B	$\frac{V_{02} \text{ PEAK-TO-PEAK}}{25{,}000}$

**A AND B REFER TO THE THROW POSITION OF THE SWITCH

00282-012

Figure 12. Noise Measurement Circuit

APPLICATIONS INFORMATION

Application of reverse bias voltages to the emitter to base junctions in excess of ratings (5 V) may result in degradation of h_{FE} and h_{FE} matching characteristics. Check circuit designs to ensure that reverse bias voltages above 5 V cannot be applied during transient conditions, such as at circuit turn-on and turn-off.

Stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can prevent realization of the predicted drift performance. Maintain both input terminals at the same temperature, preferably close to the temperature of the device package.

TYPICAL APPLICATIONS

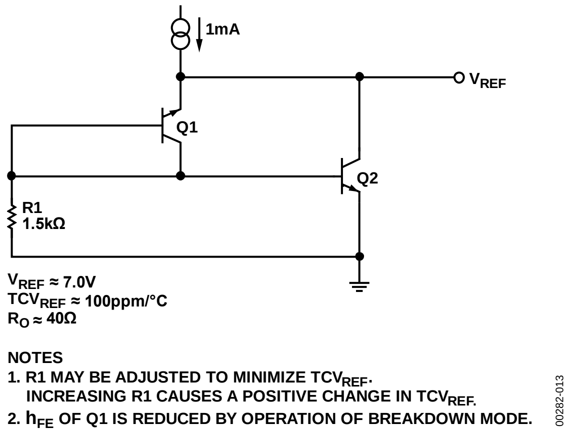


Figure 13. Precision Reference

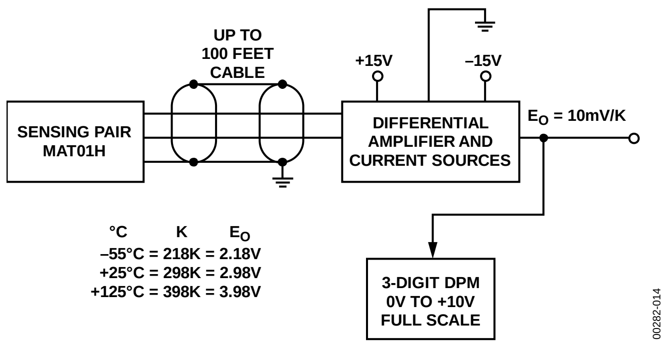


Figure 14. Basic Digital Thermometer Readout in Degrees Kelvin (K)

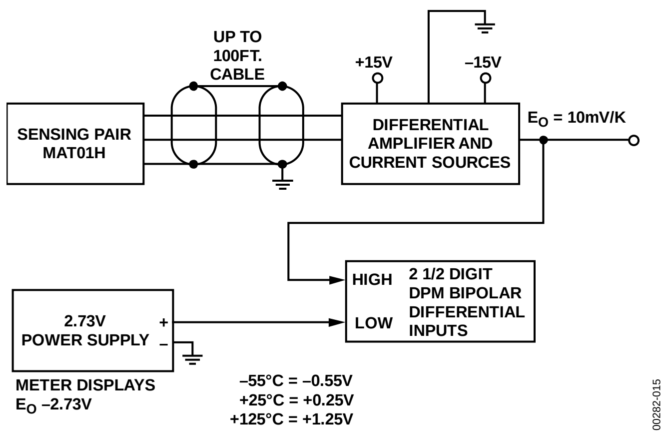


Figure 15. Digital Thermometer with Readout in °C

OUTLINE DIMENSIONS

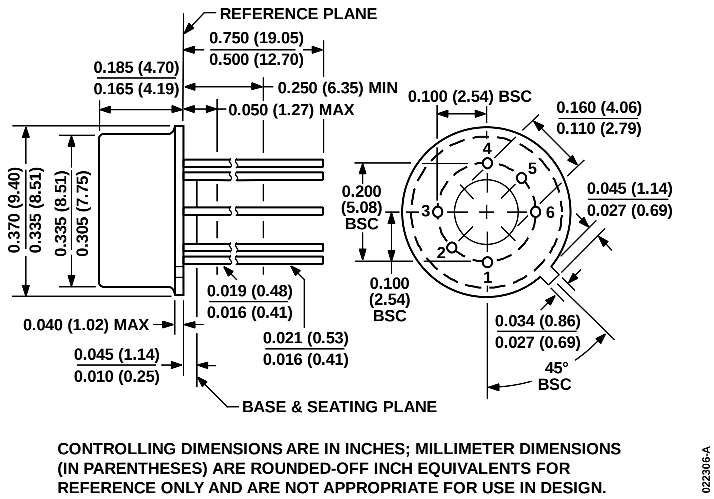


Figure 16. 6-Pin Metal Header Package [TO-78]
(H-06)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model[1]	V_{OS} Maximum (T_A = 25°C)	Temperature Range	Package Description	Package Option
MAT01AH	0.1 mV	−55°C to +125°C	6-Pin Metal Header Package [TO-78]	H-06
MAT01AHZ	0.1 mV	−55°C to +125°C	6-Pin Metal Header Package [TO-78]	H-06
MAT01GH	0.5 mV	−55°C to +125°C	6-Pin Metal Header Package [TO-78]	H-06
MAT01GHZ	0.5 mV	−55°C to +125°C	6-Pin Metal Header Package [TO-78]	H-06

[1] Z = RoHS Compliant Part.

NOTES