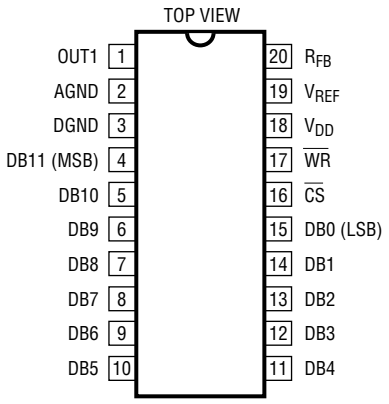
## ABSOLUTE MAXIMUM RATINGS

$V_{DD}$ to AGND ..... −0.5V to 17V
$V_{DD}$ to DGND .....−0.5V to 17V
AGND to DGND ..... −0.5V to $V_{DD}$ + 0.5V
DGND to AGND ..... −0.5V to $V_{DD}$ + 0.5V
$V_{REF}$ to AGND,DGND ..... ±25V
$R_{FB}$ to AGND,DGND ..... . ±25V
Digital Inputs to DGND ..... −0.5V to $V_{DD}$ + 0.5V
$V_{OUT1}$ to AGND, DGND ..... −0.5V to $V_{DD}$ + 0.5V
Maximum Junction Temperature ..... 150°C
Operating Temperature Range
Commercial (K, L Versions) ..... 0°C to 70°C
Industrial (B, C Versions)..... −40° C to 85°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

## PACKAGE/ORDER INFORMATION




G PACKAGE
20-LEAD PLASTIC SSOP

N PACKAGE
20-LEAD PDIP

SW PACKAGE
20-LEAD PLASTIC SO WIDE

$T_{JMAX}$ = XXX°C, $\theta_{JA}$ = XXX°C/W (G)
$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 100°C/W (N)
$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 130°C/W (SW)

| ORDER PART NUMBER |
|---|
| LTC7545ABG |
| LTC7545ABN |
| LTC7545ABSW |
| LTC7545ACG |
| LTC7545ACN |
| LTC7545ACSW |
| LTC7545AKG |
| LTC7545AKN |
| LTC7545AKSW |
| LTC7545ALG |
| LTC7545ALN |
| LTC7545ALSW |

Consult factory for Military grade parts.

## ELECTRICAL CHARACTERISTICS

**$V_{DD}$ = 5V or 15V, $V_{REF}$ = 10V, $V_{OUT1}$ = AGND = 0V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | | LTC7545AK/AB MIN | LTC7545AK/AB TYP | LTC7545AK/AB MAX | LTC7545AL/AC MIN | LTC7545AL/AC TYP | LTC7545AL/AC MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Accuracy** | | | | | | | | | | | |
| | Resolution | | | ● | 12 | | | 12 | | | Bits |
| INL | Integral Nonlinearity (Relative Accuracy) | (Note 1) | $T_A$ = 25°C | | | | ±0.5 | | | ±0.5 | LSB |
| | | | $T_{MIN}$ to $T_{MAX}$ | ● | | | ±0.5 | | | ±0.5 | LSB |
| DNL | Differential Nonlinearity | Guaranteed Monotonic | $T_A$ = 25°C | | | | ±1 | | | ±0.5 | LSB |
| | | $T_{MIN}$ to $T_{MAX}$ | $T_{MIN}$ to $T_{MAX}$ | ● | | | ±1 | | | ±0.5 | LSB |
| GE | Gain Error | (Note 2) | $T_A$ = 25°C | | | | ±2 | | | ±1 | LSB |
| | | | $T_{MIN}$ to $T_{MAX}$ | ● | | | ±3 | | | ±2 | LSB |
| | Gain Temperature Coefficient | (Note 3) ΔGain/ΔTemperature | | ● | | 1 | 5 | | 1 | 5 | ppm/°C |
| $I_{LKG}$ | OUT1 Leakage Current | (Note 4) | $T_A$ = 25°C | | | | ±10 | | | ±10 | nA |
| | | | $T_{MIN}$ to $T_{MAX}$ | ● | | | ±50 | | | ±50 | nA |
| PSRR | Power Supply Rejection | | | ● | | | ±0.002 | | | ±0.002 | %/% |
| **Reference Input** | | | | | | | | | | | |
| $R_{REF}$ | $V_{REF}$ Input Resistance | (Note 5) | | ● | 8 | 11 | 15 | 8 | 11 | 15 | kΩ |
| **AC Performance** | | | | | | | | | | | |
| | Output Current Settling Time | (Notes 3, 6, 7) | | ● | | | 1 | | | 1 | µs |
| | Propagation Delay | (Notes 3, 6, 8) | | ● | | | 150 | | | 150 | ns |
| | Digital-to-Analog Glitch Impulse | (Notes 6, 9) | | ● | | 5 | | | 5 | | nV-sec |
| | Multiplying Feedthrough Error | $V_{REF}$ = ±10V, 10kHz Sine Wave | | ● | | 5 | | | 5 | | $mV_{P-P}$ |
| **Analog Outputs** | | | | | | | | | | | |
| $C_{OUT}$ | Output Capacitance (Note 3) | DB0 to DB11 = 0V, WR, CS = 0V | $C_{OUT1}$ | ● | | 30 | 70 | | 30 | 70 | pF |
| | | DB0 to DB11 = $V_{DD}$, WR, CS = 0V | $C_{OUT1}$ | ● | | 60 | 150 | | 60 | 150 | pF |

## ELECTRICAL CHARACTERISTICS

**$V_{DD}$ = 5V, $V_{REF}$ = 10V, $V_{OUT1}$ = AGND = 0V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | ALL GRADES MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Digital Inputs** | | | | | | | |
| $V_{IH}$ | Digital Input High Voltage | | ● | 2.4 | | | V |
| $V_{IL}$ | Digital Input Low Voltage | | ● | | | 0.8 | V |
| $I_{IN}$ | Digital Input Current | | ● | | 0.001 | ±1 | µA |
| $C_{IN}$ | Digital Input Capacitance | (Note 3) $V_{IN}$ = 0V | ● | | | 8 | pF |
| **Timing Characteristics (Note 3)** | | | | | | | |
| $t_{CS}$ | $\overline{CS}$ to $\overline{WR}$ Setup Time | | ● | 100 | | | ns |
| $t_{CH}$ | $\overline{CS}$ to $\overline{WR}$ Hold Time | | ● | 0 | | | ns |
| $t_{WR}$ | Write Pulse Width | | ● | 100 | | | ns |
| $t_{DS}$ | Data Setup Time | | ● | 100 | | | ns |
| $t_{DH}$ | Data Hold Time | | ● | 5 | | | ns |
| **Power Supply** | | | | | | | |
| $V_{DD}$ | Supply Voltage | | ● | 4.75 | 5 | 5.25 | V |
| $I_{DD}$ | Supply Current | All Digital Inputs = $V_{IH}$ or $V_{IL}$ | ● | | | 2 | mA |
| | | All Digital Inputs = 0V or $V_{DD}$ | ● | | 10 | 100 | µA |

**$V_{DD}$ = 15V, $V_{REF}$ = 10V, $V_{OUT1}$ = AGND = 0V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | ALL GRADES MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Digital Inputs** | | | | | | | |
| $V_{IH}$ | Digital Input High Voltage | | ● | 13.5 | | | V |
| $V_{IL}$ | Digital Input Low Voltage | | ● | | | 1.5 | V |
| $I_{IN}$ | Digital Input Current | | ● | | | ±1 | µA |
| $C_{IN}$ | Digital Input Capacitance | (Note 3) $V_{IN}$ = 0V | ● | | | 8 | pF |
| **Timing Characteristics (Note 3)** | | | | | | | |
| $t_{CS}$ | $\overline{CS}$ to $\overline{WR}$ Setup Time | | ● | 75 | | | ns |
| $t_{CH}$ | $\overline{CS}$ to $\overline{WR}$ Hold Time | | ● | 0 | | | ns |
| $t_{WR}$ | Write Pulse Width | | ● | 75 | | | ns |
| $t_{DS}$ | Data Setup Time | | ● | 60 | | | ns |
| $t_{DH}$ | Data Hold Time | | ● | 5 | | | ns |
| **Power Supply** | | | | | | | |
| $V_{DD}$ | Supply Voltage | | ● | 14.25 | 15 | 15.75 | V |
| $I_{DD}$ | Supply Current | All Digital Inputs = $V_{IH}$ or $V_{IL}$ | ● | | | 2 | mA |
| | | All Digital Inputs = 0V or $V_{DD}$ | ● | | 10 | 100 | µA |

The ● denotes specificatons which apply over the full operating temperature range.

**Note 1:** ±0.5LSB = ±0.012% of full scale.

**Note 2:** Using internal feedback resistor.

**Note 3:** Guaranteed by design, not subject to test.

**Note 4:** $I_{OUT1}$ with DAC register loaded to all 0s.

**Note 5:** Typical temperature coefficient is 100ppm/°C.

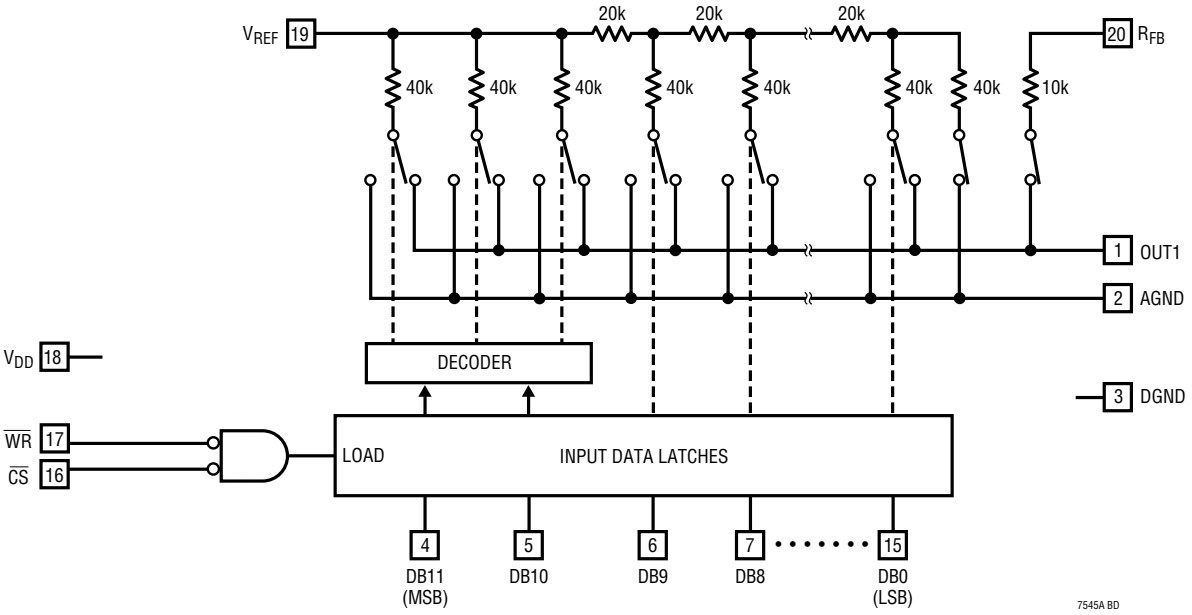
**Note 6:** OUT1 load = 100Ω in parallel with 13pF.

**Note 7:** To 0.01% for a full-scale change, measured from the falling edge of $\overline{WR}$, $\overline{CS}$ = 0V.

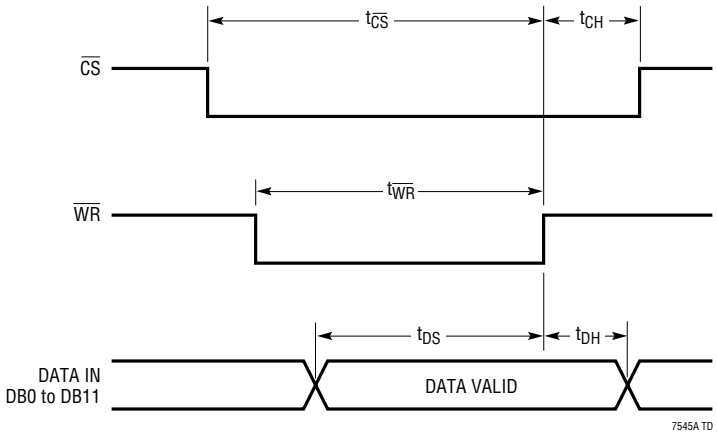
**Note 8:** From digital input change to 90% of final analog output.

**Note 9:** $V_{REF}$ = 0V. DAC register contents changed from all 0s to all 1s or all 1s to all 0s.

## BLOCK DIAGRAM




## TIMING DIAGRAM



# TYPICAL APPLICATIONS

**Unipolar Operation (2-Quadrant Multiplication)**

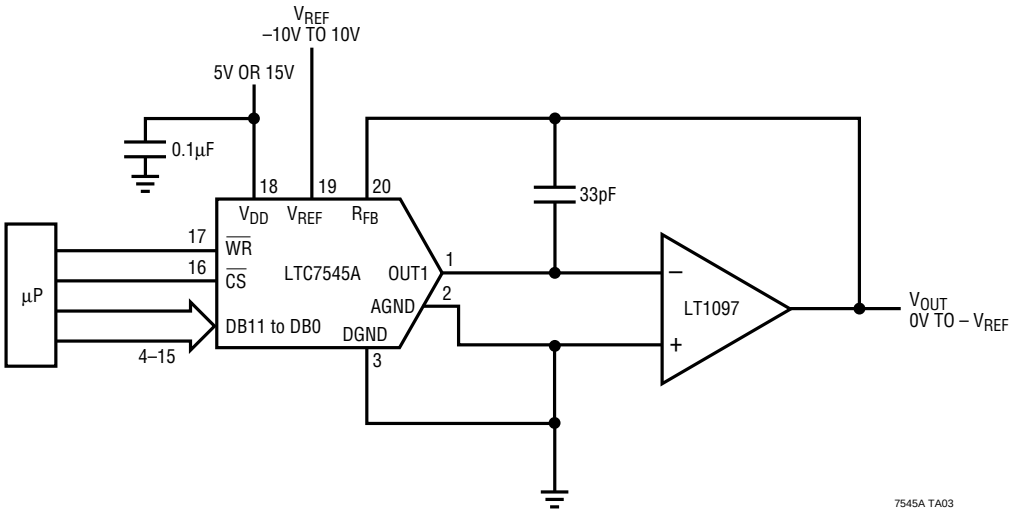



**Table 1. Unipolar Binary Code Table**

| DIGITAL INPUT BINARY NUMBER IN DAC LATCH | | | ANALOG OUTPUT $V_{OUT}$ |
|---|---|---|---|
| MSB | | LSB | |
| 1111 | 1111 | 1111 | $-V_{REF}$ (4095/4096) |
| 1000 | 0000 | 0000 | $-V_{REF}$ (2048/4096) = $-V_{REF}/2$ |
| 0000 | 0000 | 0001 | $-V_{REF}$ (1/4096) |
| 0000 | 0000 | 0000 | 0V |

## TYPICAL APPLICATIONS

**Bipolar Operation (4-Quadrant Multiplication)**

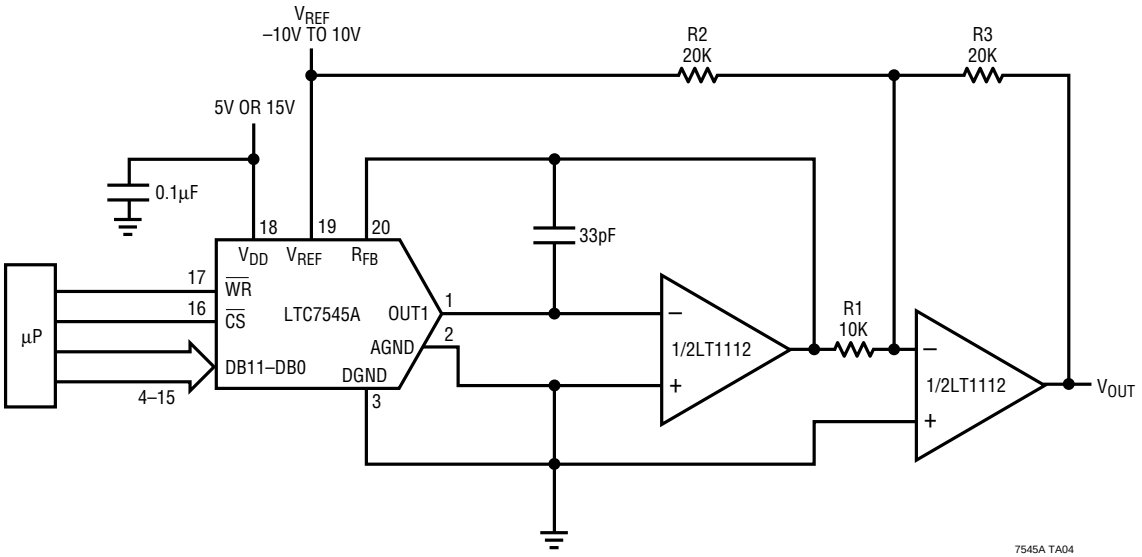
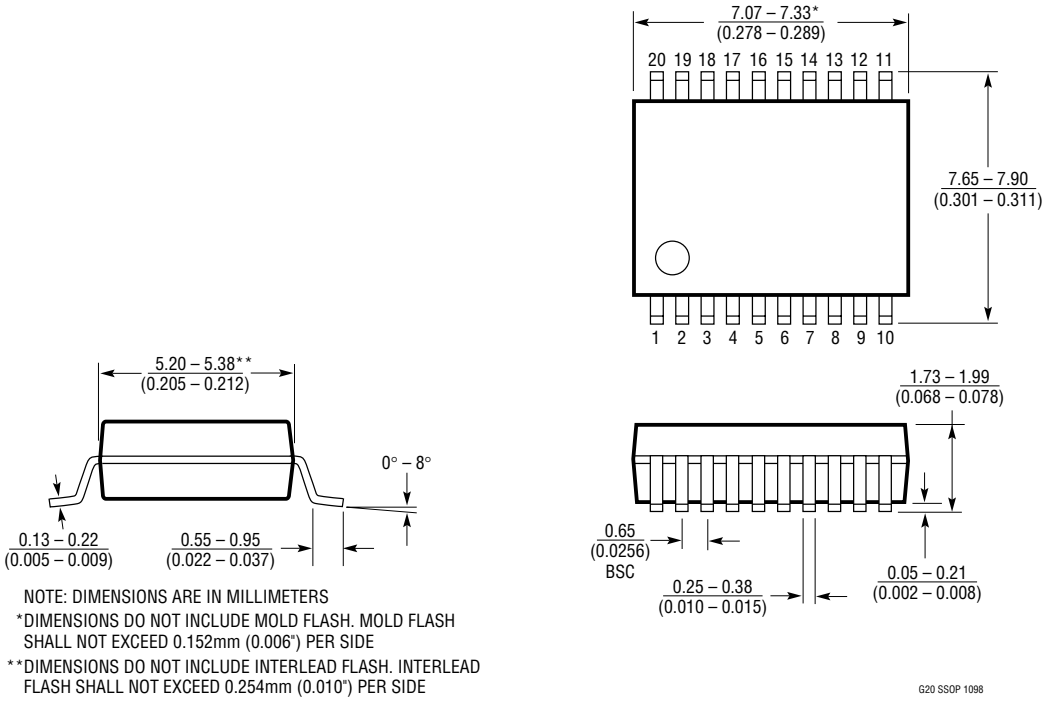



**Table 2. Bipolar Offset Binary Code Table**

| DIGITAL INPUT BINARY NUMBER IN DAC LATCH | | | ANALOG OUTPUT $V_{OUT}$ |
|---|---|---|---|
| MSB | | LSB | |
| 1111 | 1111 | 1111 | $V_{REF}$ (2047/2048) |
| 1000 | 0000 | 0001 | $V_{REF}$ (1/2048) |
| 1000 | 0000 | 0000 | 0V |
| 0111 | 1111 | 1111 | $-V_{REF}$ (1/2048) |
| 0000 | 0000 | 0000 | $-V_{REF}$ (2048/2048) = $-V_{REF}$ |

## PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

### G Package
### 20-Lead Plastic SSOP (0.209)
(LTC DWG # 05-08-1640)



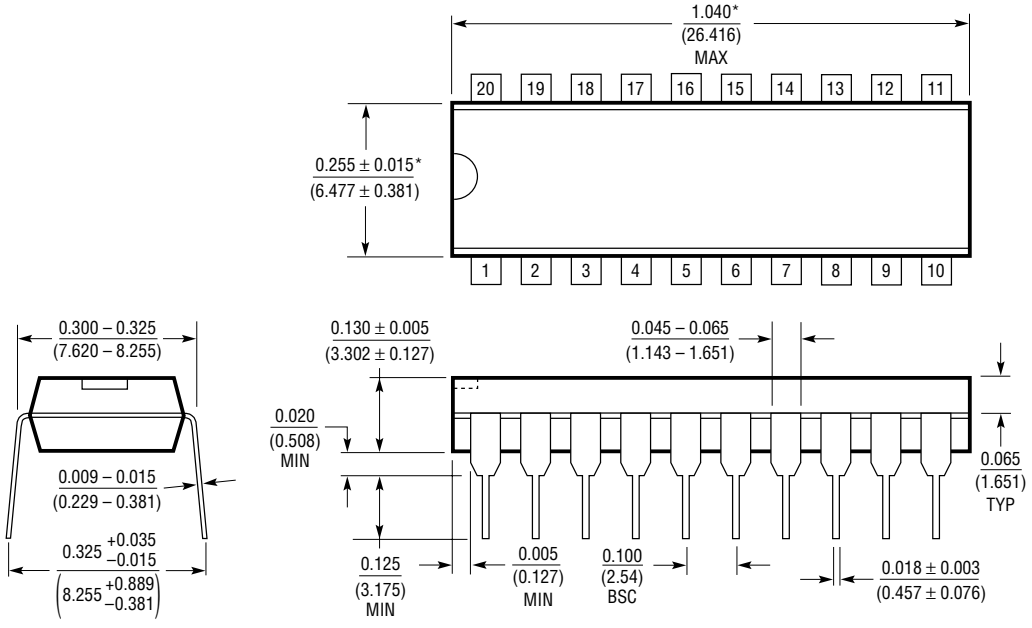

NOTE: DIMENSIONS ARE IN MILLIMETERS

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.152mm (0.006") PER SIDE

**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.254mm (0.010") PER SIDE

G20 SSOP 1098

### N Package
### 20-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)

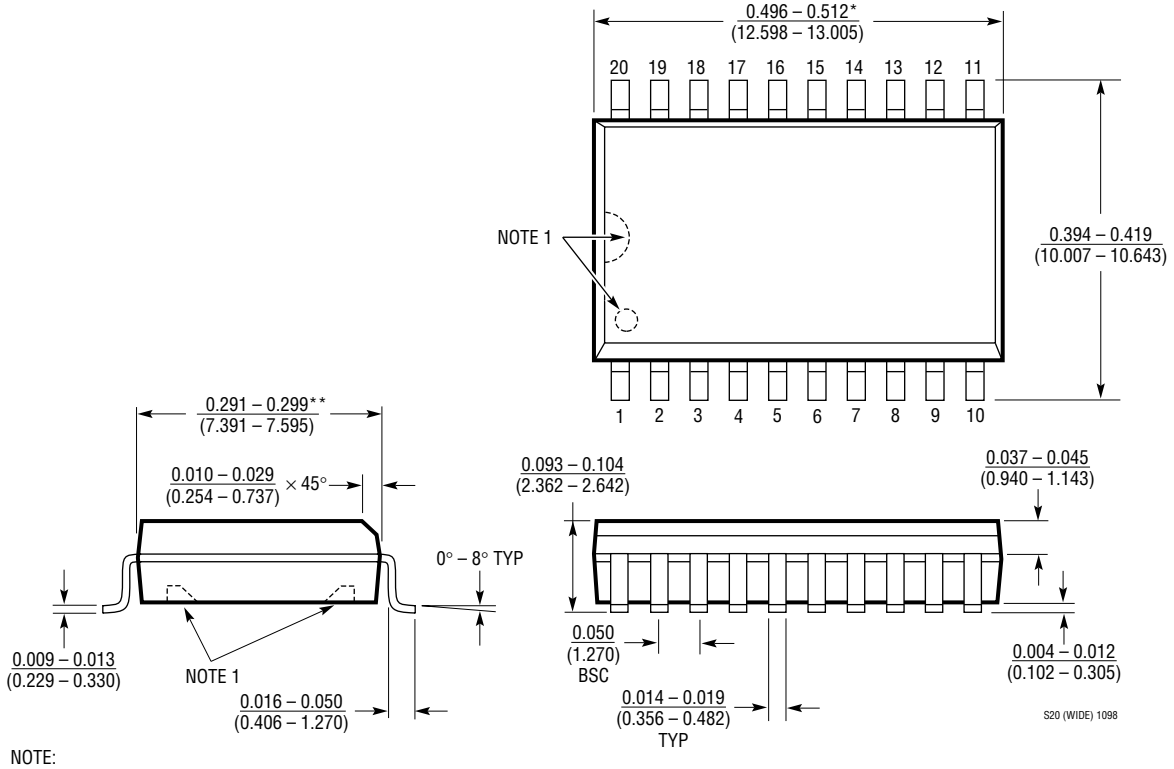



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

N20 1098

## PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

**SW Package**
**20-Lead Plastic Small Outline (Wide 0.300)**
(LTC DWG # 05-08-1620)




NOTE:
1. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS.
THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

## RELATED PARTS

| PART NUMBER | DESCRIPTON | COMMENTS |
|---|---|---|
| LTC1257 | Complete Serial I/O $V_{OUT}$ 12-Bit DAC | 5V to 15V Single Supply in 8-Pin SO and PDIP |
| LTC1450/LTC1450L | Complete Parallel Input $V_{OUT}$ 12-Bit DACs | Rail-to-Rail $V_{OUT}$, 3V/5V Single Supply, 12-Bit or (8 + 4) Bit Loading |
| LTC1451/LTC1452/LTC1453 | Complete Serial I/O $V_{OUT}$ 12-Bit DACs | Rail-to-Rail $V_{OUT}$, 3V/5V Single Supply in 8-Pin SO and PDIP |
| LTC7541A | Parallel I/O Multiplying $I_{OUT}$ 12-Bit DAC | 12-Bit Wide Parallel Input |
| LTC7543/LTC8143 | Serial I/O Multiplying $I_{OUT}$ 12-Bit DACs | Clear Pin and Serial Data Output (LTC8143) |
| LTC8043 | Serial I/O Multiplying $I_{OUT}$ 12-Bit DAC | 8-Pin SO and PDIP |


Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • TELEX: 499-3977
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