

# LTC6992-1/LTC6992-2/ LTC6992-3/LTC6992-4

## ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V <sup>+</sup> ) to GND .....	6V	Specified Temperature Range (Note 3)	
Maximum Voltage On Any Pin		LTC6992C .....	0°C to 70°C
.....(GND – 0.3V) ≤ V <sub>PIN</sub> ≤ (V <sup>+</sup> + 0.3V)		LTC6992I .....	–40°C to 85°C
Operating Temperature Range (Note 2)		LTC6992H .....	–40°C to 125°C
LTC6992C .....	–40°C to 85°C	LTC6992MP .....	–55°C to 125°C
LTC6992I .....	–40°C to 85°C	Junction Temperature .....	150°C
LTC6992H .....	–40°C to 125°C	Storage Temperature Range .....	–65°C to 150°C
LTC6992MP .....	–55°C to 125°C	Lead Temperature (Soldering, 10 sec)	
		S6 Package .....	300°C

## PIN CONFIGURATION

TOP VIEW

DCB PACKAGE  
6-LEAD (2mm × 3mm) PLASTIC DFN

T<sub>JMAX</sub> = 150°C, θ<sub>JA</sub> = 64°C/W, θ<sub>JC</sub> = 10.6°C/W  
EXPOSED PAD (PIN 7) IS GND, PCB CONNECTION IS OPTIONAL

TOP VIEW

S6 PACKAGE  
6-LEAD PLASTIC TSOT-23

T<sub>JMAX</sub> = 150°C, θ<sub>JA</sub> = 192°C/W, θ<sub>JC</sub> = 51°C/W

## ORDER INFORMATION

### Lead Free Finish

TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6992CDCB-1#TRMPBF	LTC6992CDCB-1#TRPBF	LDXC	6-Lead (2mm × 3mm) Plastic DFN	0°C to 70°C
LTC6992IDCB-1#TRMPBF	LTC6992IDCB-1#TRPBF	LDXC	6-Lead (2mm × 3mm) Plastic DFN	-40°C to 85°C
LTC6992HDCB-1#TRMPBF	LTC6992HDCB-1#TRPBF	LDXC	6-Lead (2mm × 3mm) Plastic DFN	-40°C to 125°C
LTC6992CS6-1#TRMPBF	LTC6992CS6-1#TRPBF	LTDXB	6-Lead Plastic TSOT-23	0°C to 70°C
LTC6992IS6-1#TRMPBF	LTC6992IS6-1#TRPBF	LTDXB	6-Lead Plastic TSOT-23	-40°C to 85°C
LTC6992HS6-1#TRMPBF	LTC6992HS6-1#TRPBF	LTDXB	6-Lead Plastic TSOT-23	-40°C to 125°C
LTC6992CDCB-2#TRMPBF	LTC6992CDCB-2#TRPBF	LDXF	6-Lead (2mm × 3mm) Plastic DFN	0°C to 70°C
LTC6992IDCB-2#TRMPBF	LTC6992IDCB-2#TRPBF	LDXF	6-Lead (2mm × 3mm) Plastic DFN	-40°C to 85°C
LTC6992HDCB-2#TRMPBF	LTC6992HDCB-2#TRPBF	LDXF	6-Lead (2mm × 3mm) Plastic DFN	-40°C to 125°C
LTC6992CS6-2#TRMPBF	LTC6992CS6-2#TRPBF	LTDXD	6-Lead Plastic TSOT-23	0°C to 70°C
LTC6992IS6-2#TRMPBF	LTC6992IS6-2#TRPBF	LTDXD	6-Lead Plastic TSOT-23	-40°C to 85°C
LTC6992HS6-2#TRMPBF	LTC6992HS6-2#TRPBF	LTDXD	6-Lead Plastic TSOT-23	-40°C to 125°C
LTC6992CDCB-3#TRMPBF	LTC6992CDCB-3#TRPBF	LFCP	6-Lead (2mm × 3mm) Plastic DFN	0°C to 70°C
LTC6992IDCB-3#TRMPBF	LTC6992IDCB-3#TRPBF	LFCP	6-Lead (2mm × 3mm) Plastic DFN	-40°C to 85°C
LTC6992HDCB-3#TRMPBF	LTC6992HDCB-3#TRPBF	LFCP	6-Lead (2mm × 3mm) Plastic DFN	-40°C to 125°C
LTC6992CS6-3#TRMPBF	LTC6992CS6-3#TRPBF	LTFCQ	6-Lead Plastic TSOT-23	0°C to 70°C
LTC6992IS6-3#TRMPBF	LTC6992IS6-3#TRPBF	LTFCQ	6-Lead Plastic TSOT-23	-40°C to 85°C
LTC6992HS6-3#TRMPBF	LTC6992HS6-3#TRPBF	LTFCQ	6-Lead Plastic TSOT-23	-40°C to 125°C
LTC6992CDCB-4#TRMPBF	LTC6992CDCB-4#TRPBF	LFCR	6-Lead (2mm × 3mm) Plastic DFN	0°C to 70°C
LTC6992IDCB-4#TRMPBF	LTC6992IDCB-4#TRPBF	LFCR	6-Lead (2mm × 3mm) Plastic DFN	-40°C to 85°C
LTC6992HDCB-4#TRMPBF	LTC6992HDCB-4#TRPBF	LFCR	6-Lead (2mm × 3mm) Plastic DFN	-40°C to 125°C
LTC6992CS6-4#TRMPBF	LTC6992CS6-4#TRPBF	LTFCQ	6-Lead Plastic TSOT-23	0°C to 70°C
LTC6992IS6-4#TRMPBF	LTC6992IS6-4#TRPBF	LTFCQ	6-Lead Plastic TSOT-23	-40°C to 85°C
LTC6992HS6-4#TRMPBF	LTC6992HS6-4#TRPBF	LTFCQ	6-Lead Plastic TSOT-23	-40°C to 125°C
LTC6992MPS6-1#TRMPBF	LTC6992MPS6-1#TRPBF	LTDXB	6-Lead Plastic TSOT-23	-55°C to 125°C
LTC6992MPS6-2#TRMPBF	LTC6992MPS6-2#TRPBF	LTDXD	6-Lead Plastic TSOT-23	-55°C to 125°C
LTC6992MPS6-3#TRMPBF	LTC6992MPS6-3#TRPBF	LTFCQ	6-Lead Plastic TSOT-23	-55°C to 125°C
LTC6992MPS6-4#TRMPBF	LTC6992MPS6-4#TRPBF	LTFCQ	6-Lead Plastic TSOT-23	-55°C to 125°C

### AUTOMOTIVE PRODUCTS\*\*

LTC6992IS6-1#WTRMPBF	LTC6992IS6-1#WTRPBF	LTDXB	6-Lead Plastic TSOT-23	-40°C to 85°C
LTC6992HS6-1#WTRMPBF	LTC6992HS6-1#WTRPBF	LTDXB	6-Lead Plastic TSOT-23	-40°C to 125°C
LTC6992IS6-2#WTRMPBF	LTC6992IS6-2#WTRPBF	LTDXD	6-Lead Plastic TSOT-23	-40°C to 85°C
LTC6992HS6-2#WTRMPBF	LTC6992HS6-2#WTRPBF	LTDXD	6-Lead Plastic TSOT-23	-40°C to 125°C
LTC6992IS6-3#WTRMPBF	LTC6992IS6-3#WTRPBF	LTFCQ	6-Lead Plastic TSOT-23	-40°C to 85°C
LTC6992HS6-3#WTRMPBF	LTC6992HS6-3#WTRPBF	LTFCQ	6-Lead Plastic TSOT-23	-40°C to 125°C
LTC6992IS6-4#WTRMPBF	LTC6992IS6-4#WTRPBF	LTFCQ	6-Lead Plastic TSOT-23	-40°C to 85°C
LTC6992HS6-4#WTRMPBF	LTC6992HS6-4#WTRPBF	LTFCQ	6-Lead Plastic TSOT-23	-40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. \*The temperature grade is identified by a label on the shipping container.

**Tape and reel specifications.** Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

\*\*Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

# LTC6992-1/LTC6992-2/ LTC6992-3/LTC6992-4

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . Test conditions are  $V^+ = 2.25\text{V}$  to  $5.5\text{V}$ ,  $V_{\text{MOD}} = 0\text{V}$  to  $V_{\text{SET}}$ ,  $\text{DIVCODE} = 0$  to  $15$  ( $N_{\text{DIV}} = 1$  to  $16,384$ ),  $R_{\text{SET}} = 50\text{k}$  to  $800\text{k}$ ,  $R_{\text{LOAD}} = 5\text{k}$ ,  $C_{\text{LOAD}} = 5\text{pF}$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Oscillation Frequency</b>						
$f_{\text{OUT}}$	Output Frequency		3.81		1000000	Hz
$\Delta f_{\text{OUT}}$	Frequency Accuracy (Note 4)	$3.81\text{Hz} \leq f_{\text{OUT}} \leq 1\text{MHz}$	●	$\pm 0.8$	$\pm 1.7$ $\pm 2.4$	% %
$\Delta f_{\text{OUT}}/\Delta T$	Frequency Drift Over Temperature		●	$\pm 0.005$		%/ $^\circ\text{C}$
$\Delta f_{\text{OUT}}/\Delta V^+$	Frequency Drift Over Supply	$V^+ = 4.5\text{V}$ to $5.5\text{V}$ $V^+ = 2.25\text{V}$ to $4.5\text{V}$	● ●	0.25 0.08	0.65 0.18	%/V %/V
	Long-Term Frequency Stability	(Note 10)		90		ppm/ $\sqrt{\text{kHz}}$
	Period Jitter (Note 9)	$N_{\text{DIV}} = 1$		1.2		%P-P
		$N_{\text{DIV}} = 4$		0.4 0.07		%P-P %RMS
		$N_{\text{DIV}} = 16$		0.15 0.022		%P-P %RMS
<b>Pulse Width Modulation</b>						
$\Delta D$	PWM Duty Cycle Accuracy	$V_{\text{MOD}} = 0.2 \cdot V_{\text{SET}}$ to $0.8 \cdot V_{\text{SET}}$ $V_{\text{MOD}} = 0.2 \cdot V_{\text{SET}}$ to $0.8 \cdot V_{\text{SET}}$ $V_{\text{MOD}} < 0.2 \cdot V_{\text{SET}}$ or $V_{\text{MOD}} > 0.8 \cdot V_{\text{SET}}$	● ● ●	$\pm 3.0$	$\pm 3.7$ $\pm 4.5$ $\pm 4.9$	% % %
$D_{\text{MAX}}$	Maximum Duty Cycle Limit	LTC6992-1/LTC6992-4, $\text{POL} = 0$ , $V_{\text{MOD}} = 1\text{V}$	●	100		%
		LTC6992-2/LTC6992-3, $\text{POL} = 0$ , $V_{\text{MOD}} = 1\text{V}$	●	90.5	95	99
$D_{\text{MIN}}$	Minimum Duty Cycle Limit	LTC6992-1/LTC6992-3, $\text{POL} = 0$ , $V_{\text{MOD}} = 0\text{V}$	●		0	%
		LTC6992-2/LTC6992-4, $\text{POL} = 0$ , $V_{\text{MOD}} = 0\text{V}$	●	1	5	9.5
$t_{\text{S,PWM}}$	Duty Cycle Settling Time (Note 6)	$t_{\text{MASTER}} = t_{\text{OUT}}/N_{\text{DIV}}$		$8 \cdot t_{\text{MASTER}}$		$\mu\text{s}$
<b>Power Supply</b>						
$V^+$	Operating Supply Voltage Range		●	2.25	5.5	V
	Power-On Reset Voltage		●		1.95	V
$I_{\text{S}}$	Supply Current	$R_{\text{L}} = \infty$ , $R_{\text{SET}} = 50\text{k}$ , $N_{\text{DIV}} = 1$		$V^+ = 5.5\text{V}$ ● $V^+ = 2.25\text{V}$ ●	365 225	450 285
		$R_{\text{L}} = \infty$ , $R_{\text{SET}} = 50\text{k}$ , $N_{\text{DIV}} = 4$		$V^+ = 5.5\text{V}$ ● $V^+ = 2.25\text{V}$ ●	350 225	420 280
		$R_{\text{L}} = \infty$ , $R_{\text{SET}} = 50\text{k}$ , $N_{\text{DIV}} \geq 16$		$V^+ = 5.5\text{V}$ ● $V^+ = 2.25\text{V}$ ●	325 215	390 265
		$R_{\text{L}} = \infty$ , $R_{\text{SET}} = 800\text{k}$ , $N_{\text{DIV}} = 1$ to $16,384$		$V^+ = 5.5\text{V}$ ● $V^+ = 2.25\text{V}$ ●	120 105	170 150

# LTC6992-1/LTC6992-2/ LTC6992-3/LTC6992-4

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . Test conditions are  $V^+ = 2.25\text{V}$  to  $5.5\text{V}$ ,  $V_{\text{MOD}} = 0\text{V}$  to  $V_{\text{SET}}$ ,  $\text{DIVCODE} = 0$  to  $15$  ( $N_{\text{DIV}} = 1$  to  $16,384$ ),  $R_{\text{SET}} = 50\text{k}$  to  $800\text{k}$ ,  $R_{\text{LOAD}} = 5\text{k}$ ,  $C_{\text{LOAD}} = 5\text{pF}$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Analog Inputs							
V <sub>SET</sub>	Voltage at SET Pin		●	0.97	1.00	1.03	V
ΔV <sub>SET</sub> /ΔT	V <sub>SET</sub> Drift Over Temperature		●	±75			μV/°C
R <sub>SET</sub>	Frequency-Setting Resistor		●	50		800	kΩ
	MOD Pin Input Capacitance			2.5			pF
	MOD Pin Input Current		●	±10			nA
V <sub>MOD,HI</sub>	V <sub>MOD</sub> Voltage for Maximum Duty Cycle	LTC6992-1/LTC6992-4, POL = 0, D = 100% LTC6992-2/LTC6992-3, POL = 0, D = 95%	●		0.90•V <sub>SET</sub> 0.86•V <sub>SET</sub>	0.936•V <sub>SET</sub>	V V
V <sub>MOD,LO</sub>	V <sub>MOD</sub> Voltage for Minimum Duty Cycle	LTC6992-1/LTC6992-3, POL = 0, D = 0% LTC6992-2/LTC6992-4, POL = 0, D = 5%	●	0.064•V <sub>SET</sub>	0.10•V <sub>SET</sub> 0.14•V <sub>SET</sub>		V V
V <sub>DIV</sub>	DIV Pin Voltage		●	0		V <sup>+</sup>	V
ΔV <sub>DIV</sub> /ΔV <sup>+</sup>	DIV Pin Valid Code Range (Note 5)	Deviation from Ideal V <sub>DIV</sub> /V <sup>+</sup> = (DIVCODE + 0.5)/16	●			±1.5	%
	DIV Pin Input Current		●			±10nA	
Digital Output							
I <sub>OUT(MAX)</sub>	Output Current	V <sup>+</sup> = 2.7V to 5.5V		±20			mA
V <sub>OH</sub>	High Level Output Voltage (Note 7)	V <sup>+</sup> = 5.5V I <sub>OUT</sub> = -1mA I <sub>OUT</sub> = -16mA	● ●	5.45 4.84	5.48 5.15		V V
		V <sup>+</sup> = 3.3V I <sub>OUT</sub> = -1mA I <sub>OUT</sub> = -10mA	● ●	3.24 2.75	3.27 2.99		V V
		V <sup>+</sup> = 2.25V I <sub>OUT</sub> = -1mA I <sub>OUT</sub> = -8mA	● ●	2.17 1.58	2.21 1.88		V V
V <sub>OL</sub>	Low Level Output Voltage (Note 7)	V <sup>+</sup> = 5.5V I <sub>OUT</sub> = 1mA I <sub>OUT</sub> = 16mA	● ●		0.02 0.26	0.04 0.54	V V
		V <sup>+</sup> = 3.3V I <sub>OUT</sub> = 1mA I <sub>OUT</sub> = 10mA	● ●		0.03 0.22	0.05 0.46	V V
		V <sup>+</sup> = 2.25V I <sub>OUT</sub> = 1mA I <sub>OUT</sub> = 8mA	● ●		0.03 0.26	0.07 0.54	V V
t <sub>r</sub>	Output Rise Time (Note 8)	V <sup>+</sup> = 5.5V, R <sub>LOAD</sub> = ∞ V <sup>+</sup> = 3.3V, R <sub>LOAD</sub> = ∞ V <sup>+</sup> = 2.25V, R <sub>LOAD</sub> = ∞			1.1 1.7 2.7		ns ns ns
t <sub>f</sub>	Output Fall Time (Note 8)	V <sup>+</sup> = 5.5V, R <sub>LOAD</sub> = ∞ V <sup>+</sup> = 3.3V, R <sub>LOAD</sub> = ∞ V <sup>+</sup> = 2.25V, R <sub>LOAD</sub> = ∞			1.0 1.6 2.4		ns ns ns

## ELECTRICAL CHARACTERISTICS

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTC6992C is guaranteed functional over the operating temperature range of  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

**Note 3:** The LTC6992C is guaranteed to meet specified performance from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ . The LTC6992C is designed, characterized and expected to meet specified performance from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  but it is not tested or QA sampled at these temperatures. The LTC6992I is guaranteed to meet specified performance from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ . The LTC6992H is guaranteed to meet specified performance from  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The LTC6992MP is guaranteed to meet specified performance from  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

**Note 4:** Frequency accuracy is defined as the deviation from the  $f_{\text{OUT}}$  equation, assuming  $R_{\text{SET}}$  is used to program the frequency.

**Note 5:** See Operation section, Table 1 and Figure 2 for a full explanation of how the DIV pin voltage selects the value of DIVCODE.

**Note 6:** Duty cycle settling time is the amount of time required for the output to settle within  $\pm 1\%$  of the final duty cycle after a  $\pm 10\%$  change in the setting ( $\pm 80\text{mV}$  step in  $V_{\text{MOD}}$ ).

**Note 7:** To conform to the Logic IC Standard, current out of a pin is arbitrarily given a negative value.

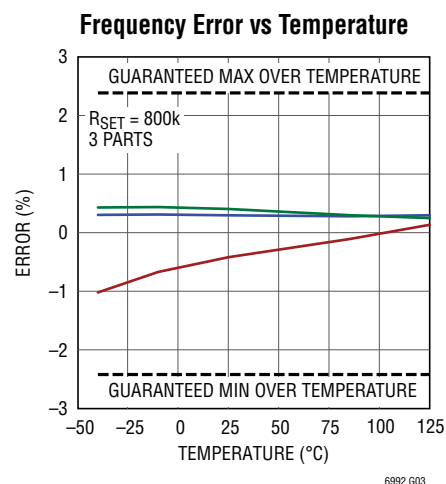
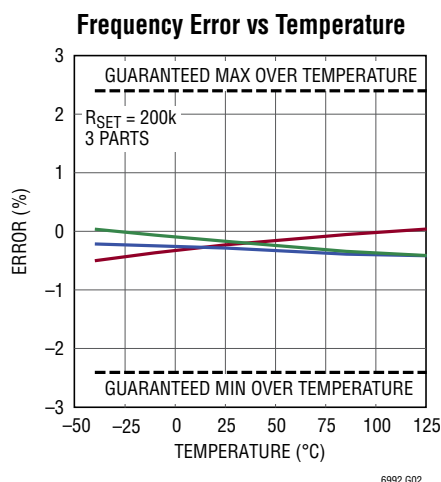
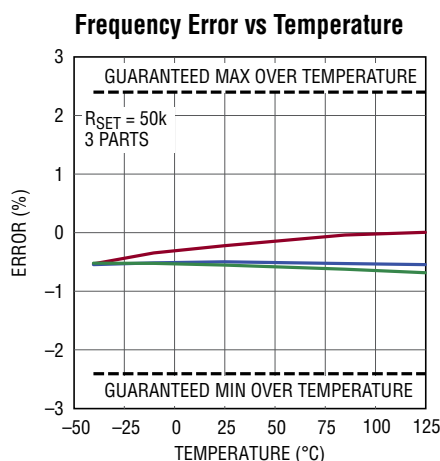
**Note 8:** Output rise and fall times are measured between the 10% and the 90% power supply levels with 5pF output load. These specifications are based on characterization.

**Note 9:** Jitter is the ratio of the peak-to-peak deviation of the period to the mean of the period. This specification is based on characterization and is not 100% tested.

**Note 10:** Long-term drift of silicon oscillators is primarily due to the movement of ions and impurities within the silicon and is tested at  $30^{\circ}\text{C}$  under otherwise nominal operating conditions. Long-term drift is specified as  $\text{ppm}/\sqrt{\text{kHr}}$  due to the typically nonlinear nature of the drift. To calculate drift for a set time period, translate that time into thousands of hours, take the square root and multiply by the typical drift number. For instance, a year is 8.77kHr and would yield a drift of 266ppm at  $90\text{ppm}/\sqrt{\text{kHr}}$ . Drift without power applied to the device may be approximated as 1/10th of the drift with power, or  $9\text{ppm}/\sqrt{\text{kHr}}$  for a  $90\text{ppm}/\sqrt{\text{kHr}}$  device.

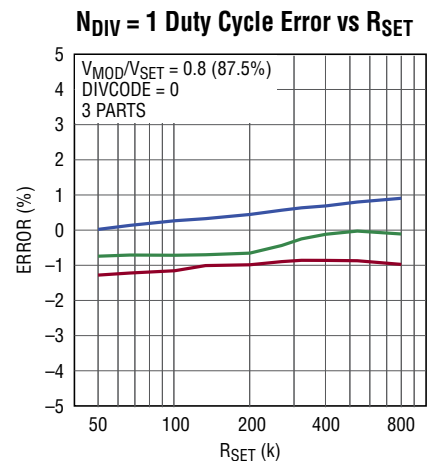
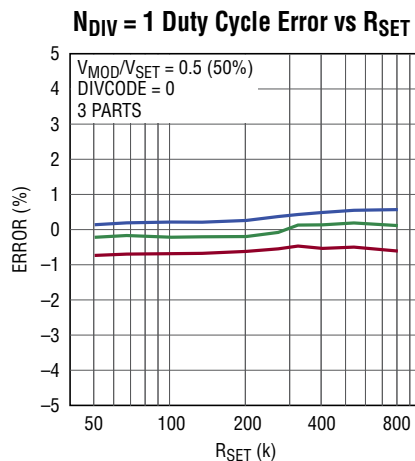
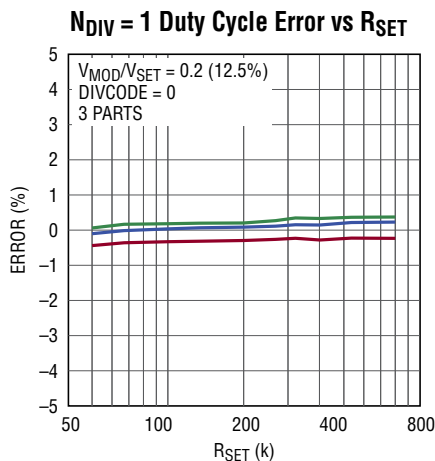
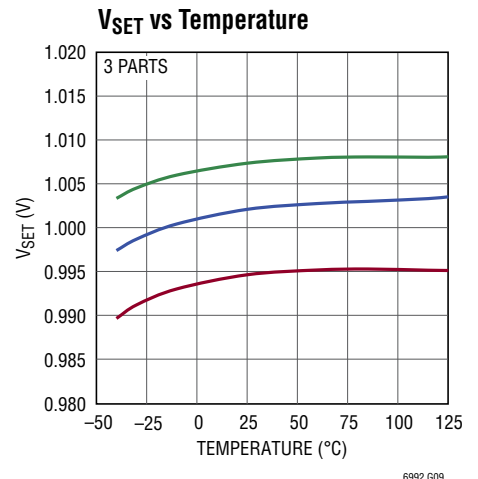
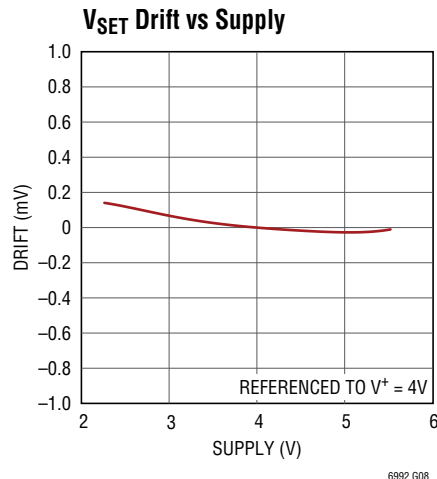
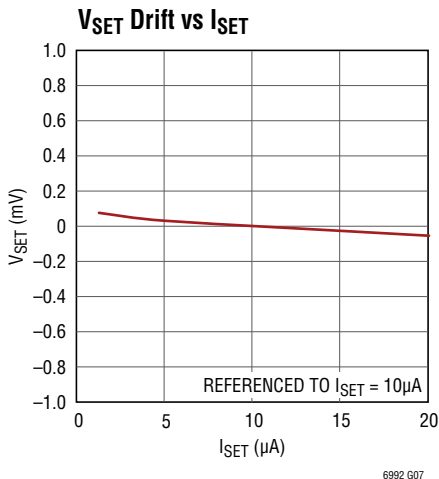
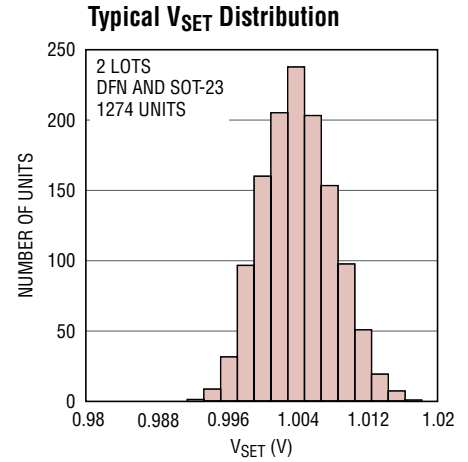
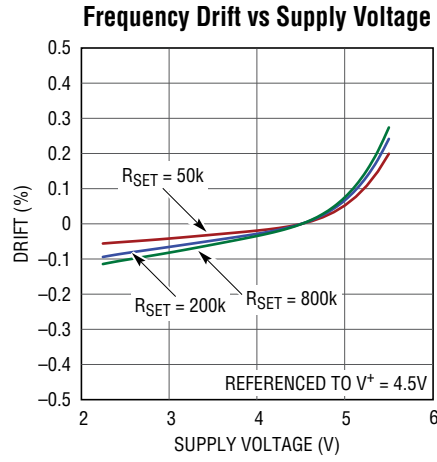
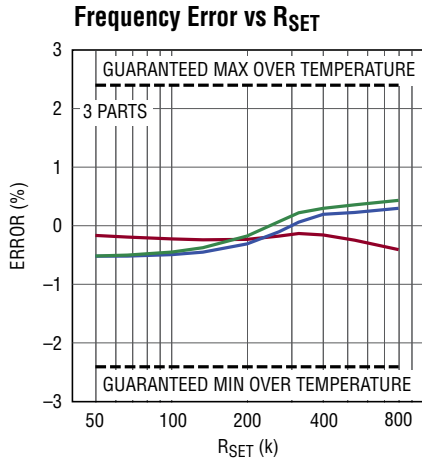
## TYPICAL PERFORMANCE CHARACTERISTICS

$V^+ = 3.3\text{V}$ ,  $R_{\text{SET}} = 200\text{k}$ , and  $T_A = 25^{\circ}\text{C}$ , unless otherwise noted.



# TYPICAL PERFORMANCE CHARACTERISTICS

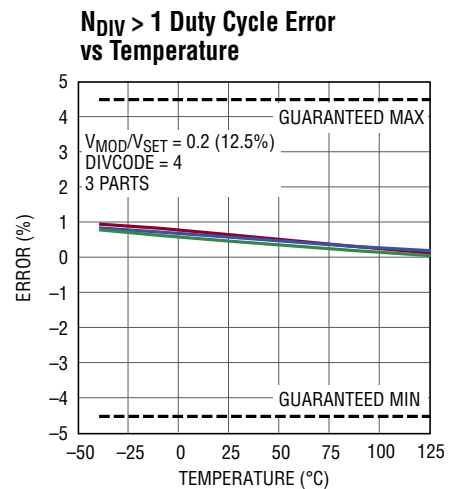
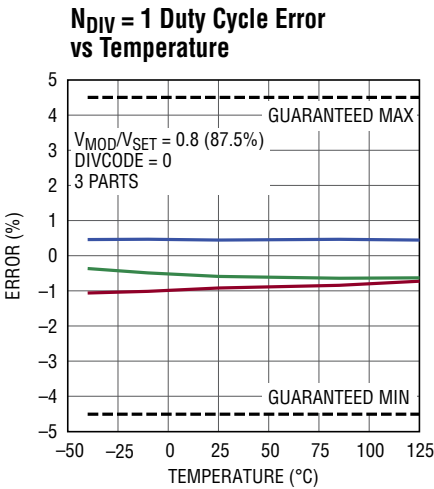
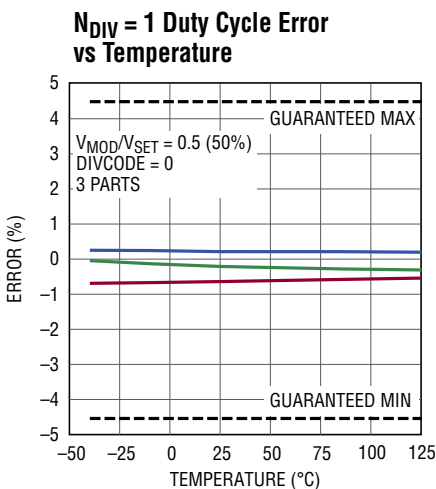
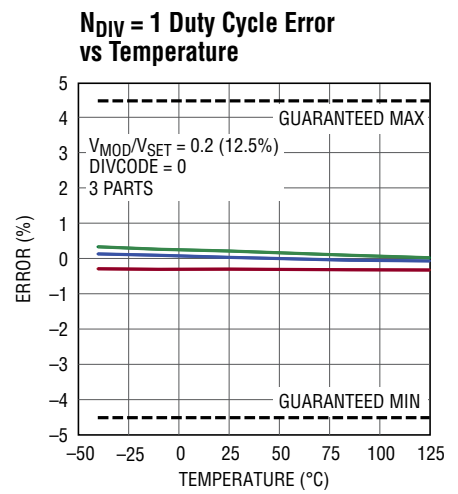
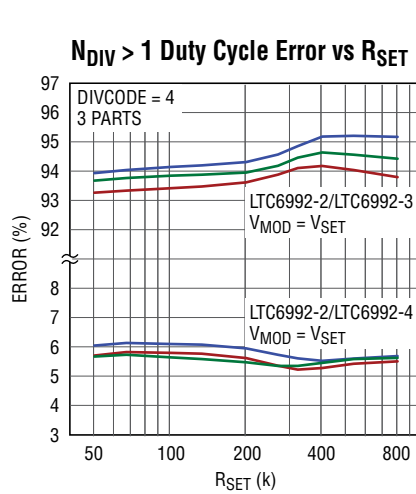
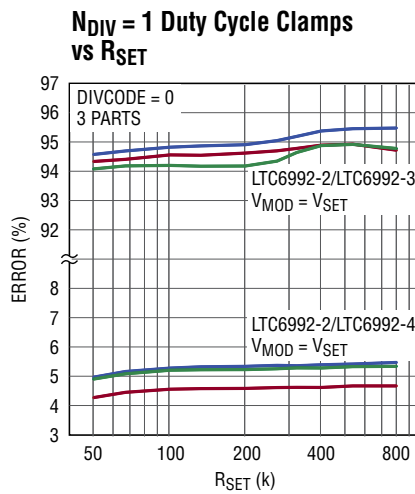
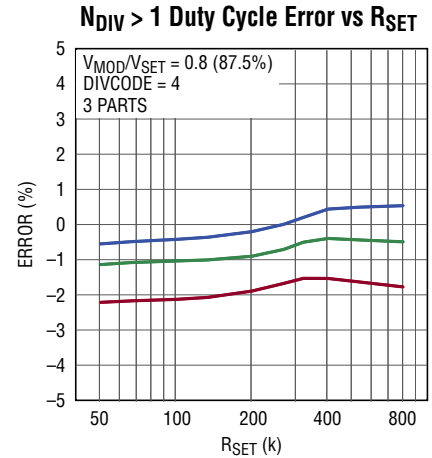
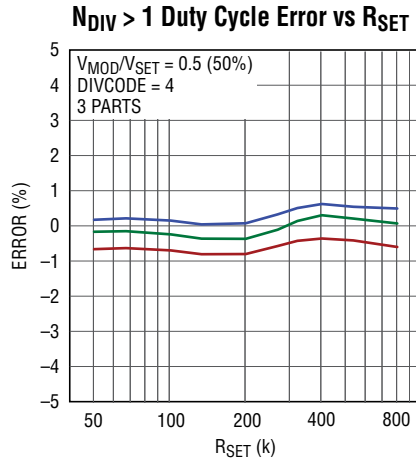
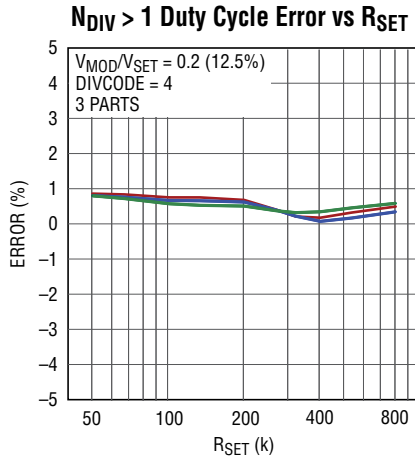
$V^+ = 3.3V$ ,  $R_{SET} = 200k$ , and  $T_A = 25^\circ C$ , unless otherwise noted.



# LTC6992-1/LTC6992-2/ LTC6992-3/LTC6992-4

## TYPICAL PERFORMANCE CHARACTERISTICS

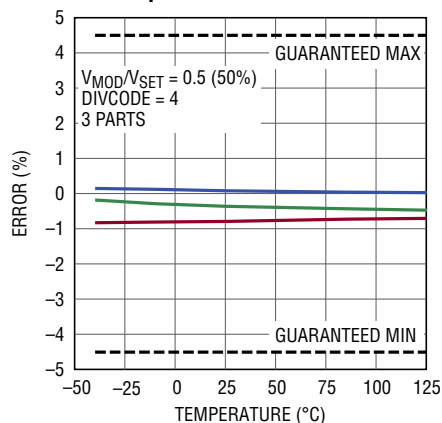
$V^+ = 3.3V$ ,  $R_{SET} = 200k$ , and  $T_A = 25^\circ C$ , unless otherwise noted.



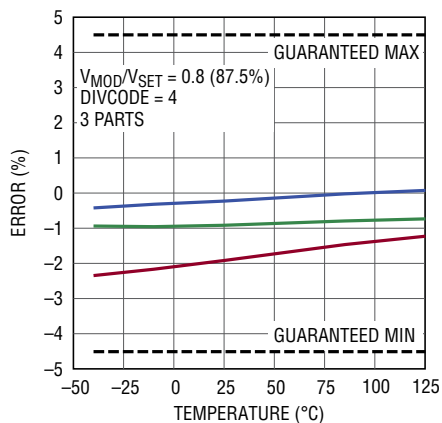
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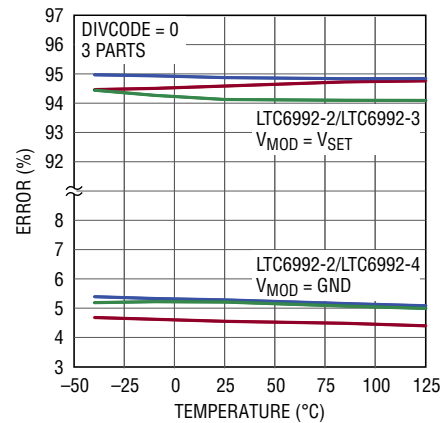
**$N_{DIV} > 1$  Duty Cycle Error vs Temperature**



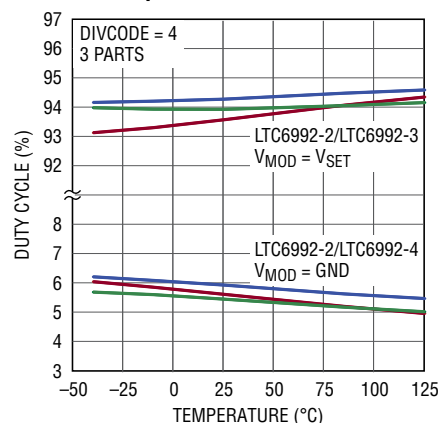
**$N_{DIV} > 1$  Duty Cycle Error vs Temperature**



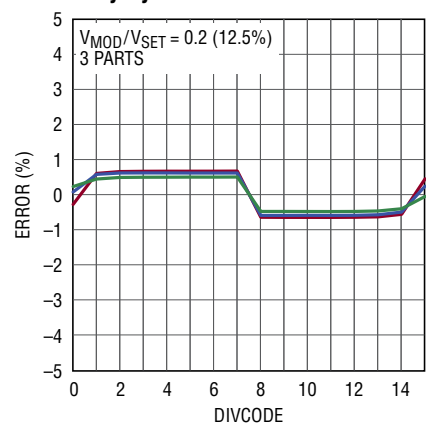
**$N_{DIV} = 1$  Duty Cycle Clamps vs Temperature**



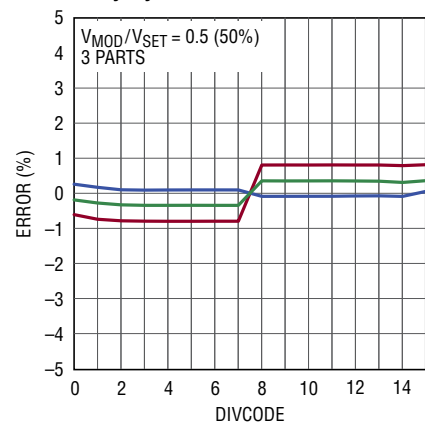
**$N_{DIV} > 1$  Duty Cycle Clamps vs Temperature**



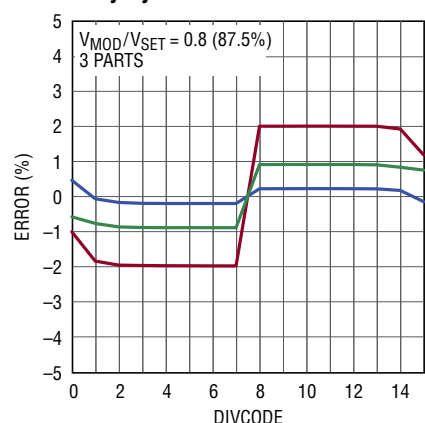
**Duty Cycle Error vs DIVCODE**



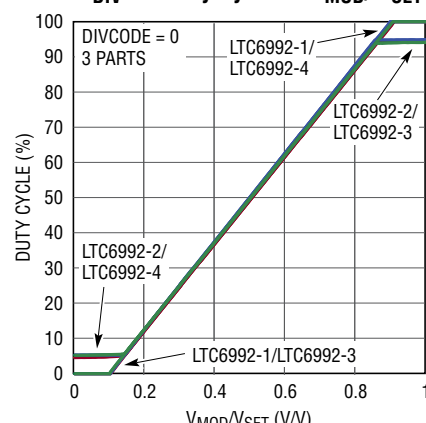
**Duty Cycle Error vs DIVCODE**



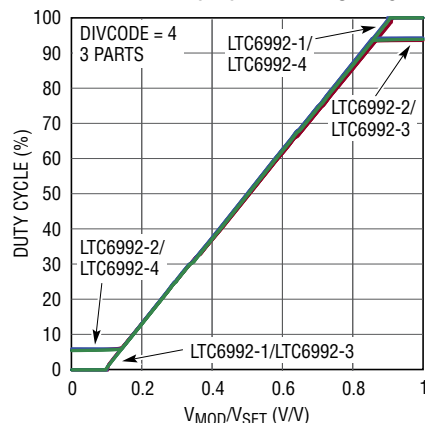
**Duty Cycle Error vs DIVCODE**



**$N_{DIV} = 1$  Duty Cycle vs  $V_{MOD}/V_{SET}$**



**$N_{DIV} > 1$  Duty Cycle vs  $V_{MOD}/V_{SET}$**



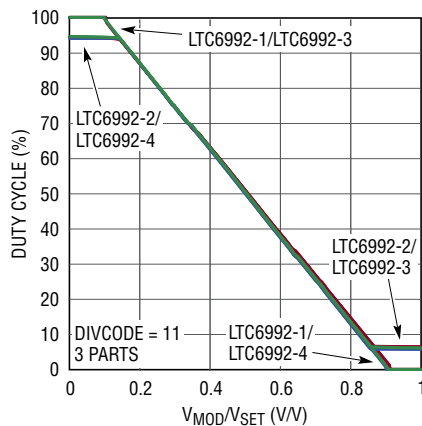


# LTC6992-1/LTC6992-2/ LTC6992-3/LTC6992-4

## TYPICAL PERFORMANCE CHARACTERISTICS

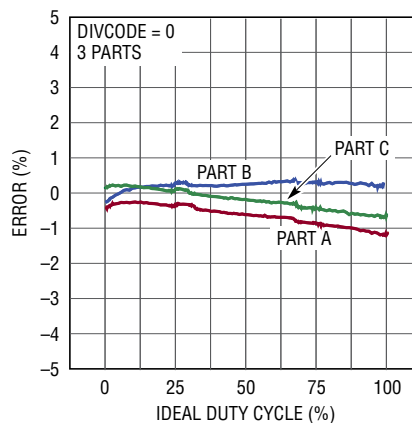
$V^+ = 3.3V$ ,  $R_{SET} = 200k$ , and  $T_A = 25^\circ C$ , unless otherwise noted.

**$N_{DIV} > 1$  Duty Cycle vs  $V_{MOD}/V_{SET}$**



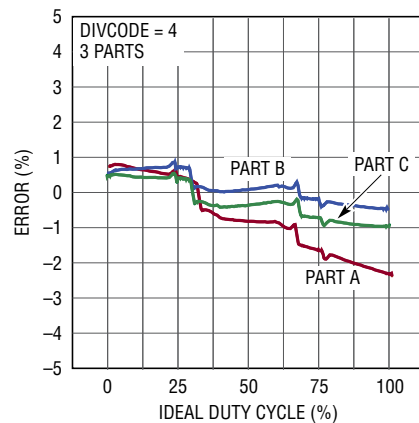
6992 G31

**$N_{DIV} = 1$  Duty Cycle Error vs Ideal**



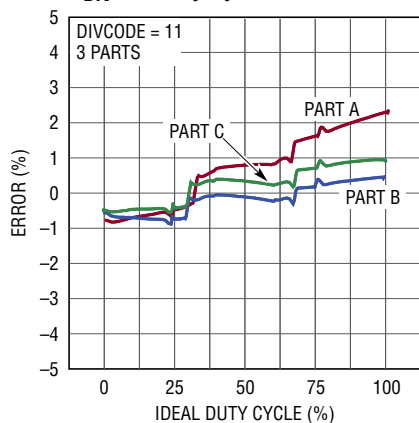
6992 G32

**$N_{DIV} > 1$  Duty Cycle Error vs Ideal**



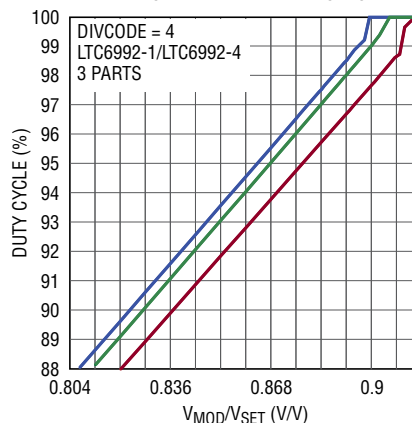
6992 G33

**$N_{DIV} > 1$  Duty Cycle Error vs Ideal**



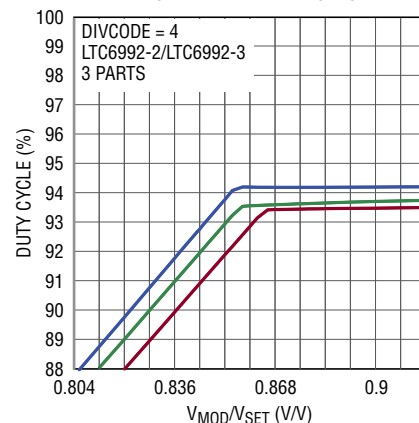
6992 G34

**Linearity Near 100% Duty Cycle**



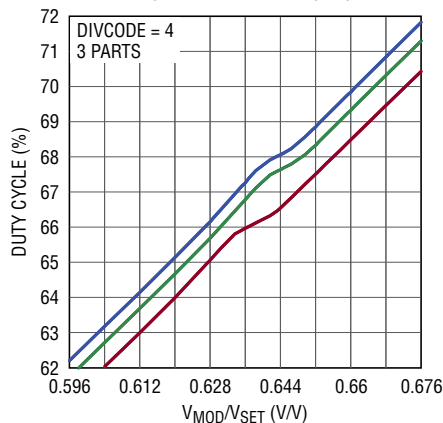
6992 G35

**Linearity Near 95% Duty Cycle**



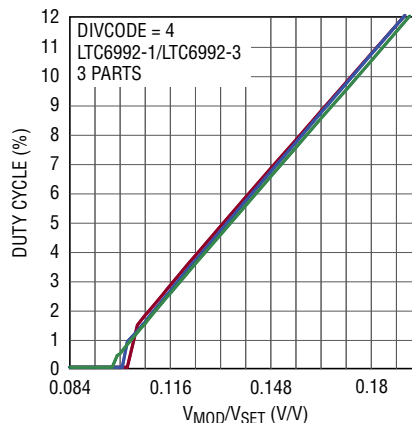
6992 G36

**Linearity Near 67% Duty Cycle**



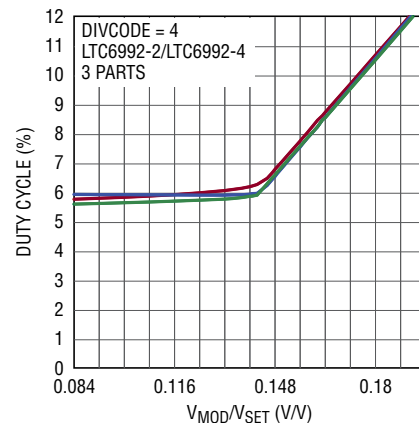
6992 G37

**Linearity Near 0% Duty Cycle**



6992 G38

**Linearity Near 5% Duty Cycle**



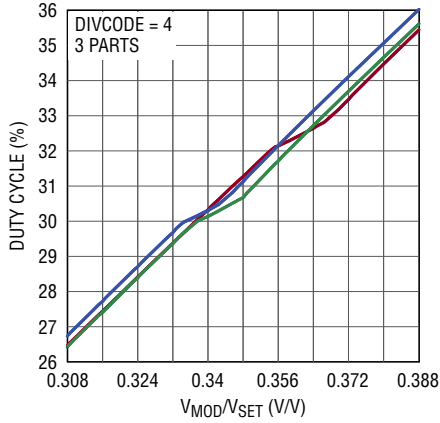
6992 G39

Rev. D

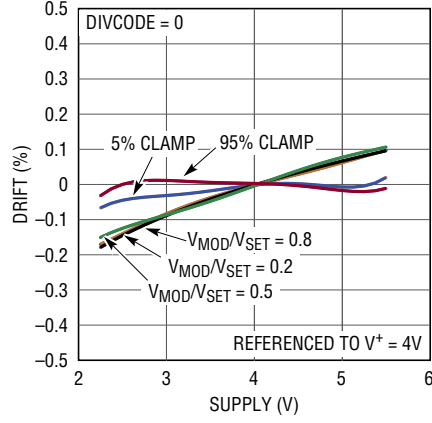
## TYPICAL PERFORMANCE CHARACTERISTICS

$V^+ = 3.3V$ ,  $R_{SET} = 200k$ , and  $T_A = 25^\circ C$ , unless otherwise noted.

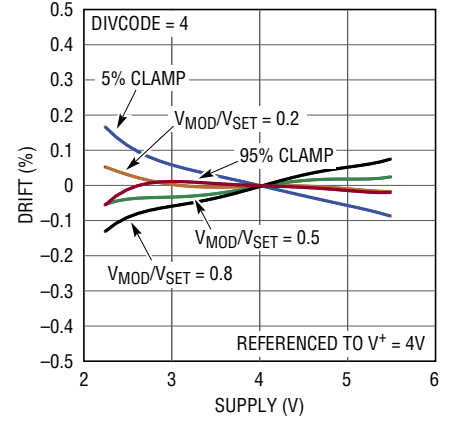
Linearity Near 31% Duty Cycle



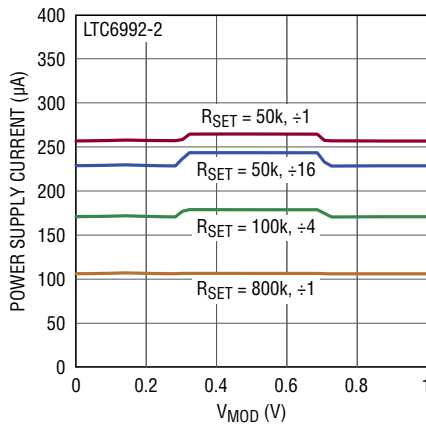
$N_{DIV} = 1$  Duty Cycle Drift vs Supply



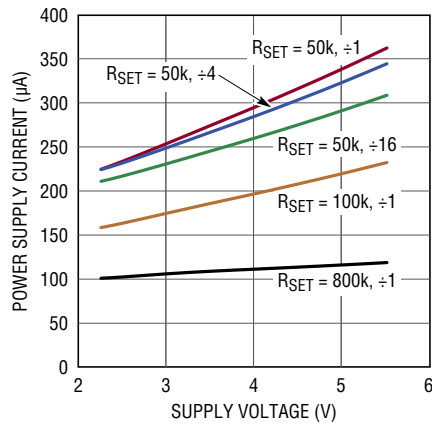
$N_{DIV} > 1$  Duty Cycle Drift vs Supply



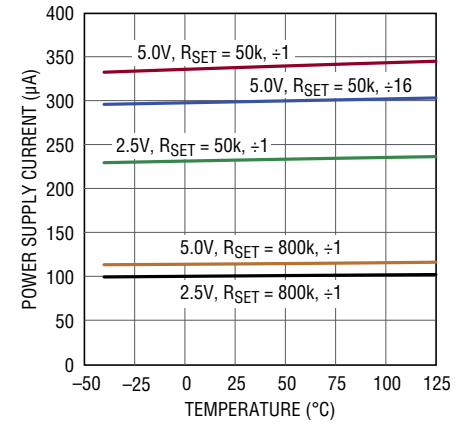
Supply Current vs  $V_{MOD}$



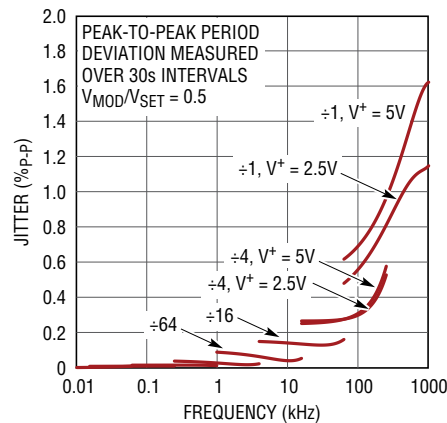
Supply Current vs Supply Voltage



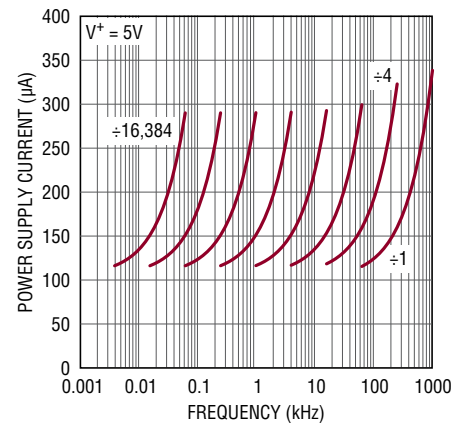
Supply Current vs Temperature



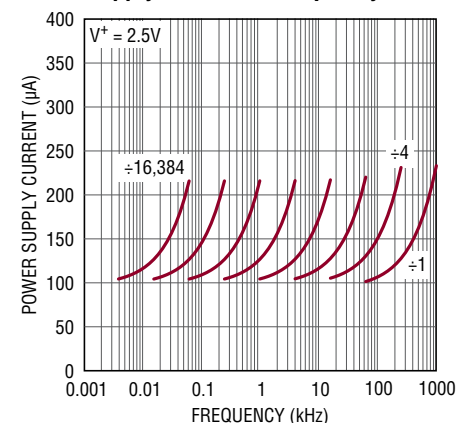
Jitter vs Frequency



Supply Current vs Frequency, 5V



Supply Current vs Frequency, 2.5V

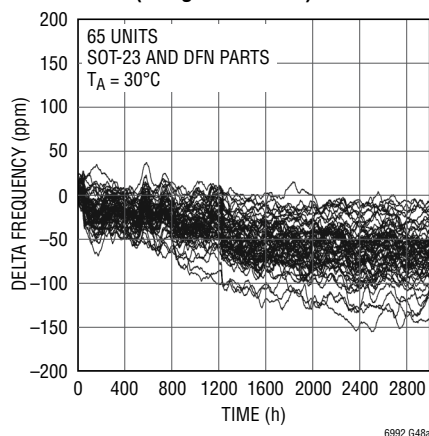


# LTC6992-1/LTC6992-2/ LTC6992-3/LTC6992-4

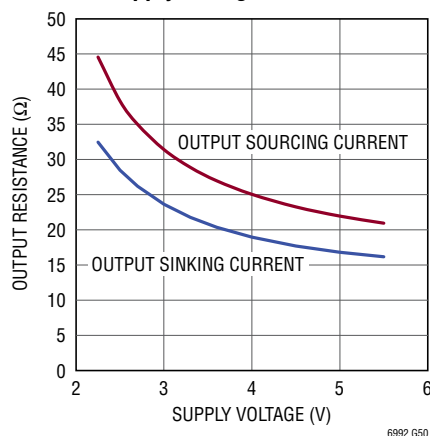
## TYPICAL PERFORMANCE CHARACTERISTICS

$V^+ = 3.3V$ ,  $R_{SET} = 200k$ , and  $T_A = 25^\circ C$ , unless otherwise noted.

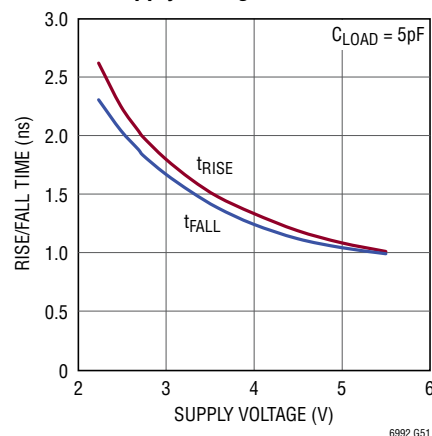
**Typical Frequency Error vs Time (Long-Term Drift)**



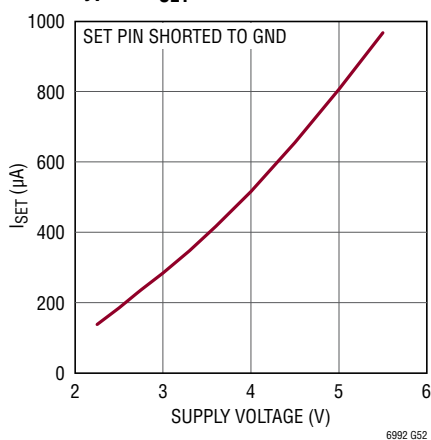
**Output Resistance vs Supply Voltage**



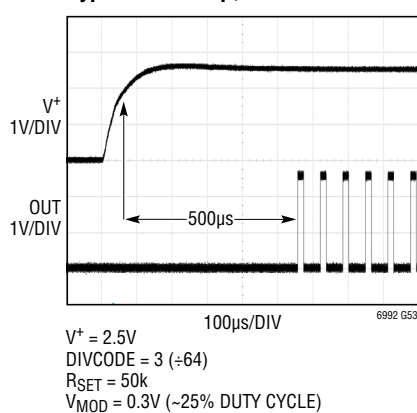
**Rise and Fall Time vs Supply Voltage**



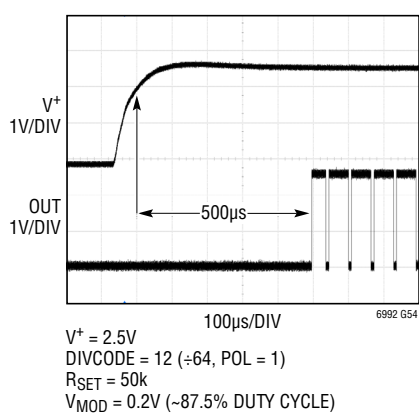
**Typical  $I_{SET}$  Current Limit vs  $V^+$**



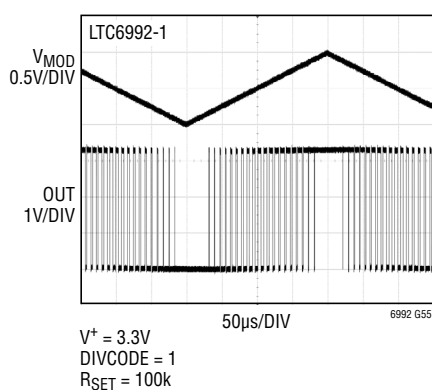
**Typical Start-Up, POL = 0**



**Typical Start-Up, POL = 1**



**125kHz Full Modulation**



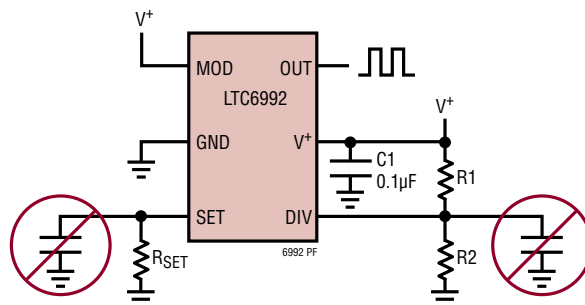
## PIN FUNCTIONS (DCB/S6)

**V<sup>+</sup> (Pin 1/Pin 5):** Supply Voltage (2.25V to 5.5V). This supply should be kept free from noise and ripple. It should be bypassed directly to the GND pin with a 0.1μF capacitor.

**DIV (Pin 2/Pin 4):** Programmable Divider and Polarity Input. The DIV pin voltage ( $V_{DIV}$ ) is internally converted into a 4-bit result (DIVCODE).  $V_{DIV}$  may be generated by a resistor divider between V<sup>+</sup> and GND. Use 1% resistors to ensure an accurate result. The DIV pin and resistors should be shielded from the OUT pin or any other traces that have fast edges. Limit the capacitance on the DIV pin to less than 100pF so that  $V_{DIV}$  settles quickly. The MSB of DIVCODE (POL) determines if the PWM signal is inverted before driving the output. When POL = 1 the transfer function is inverted (duty cycle decreasing as  $V_{MOD}$  increases).

**SET (Pin 3/Pin 3):** Frequency-Setting Input. The voltage on the SET pin ( $V_{SET}$ ) is regulated to 1V above GND. The amount of current sourced from the SET pin ( $I_{SET}$ ) programs the master oscillator frequency. The  $I_{SET}$  current range is 1.25μA to 20μA. The output oscillation will stop if  $I_{SET}$  drops below approximately 500nA. A resistor connected between SET and GND is the most accurate way to set the frequency. For best performance, use a precision metal or thin film resistor of 0.5% or better tolerance and 50ppm/°C or better temperature coefficient. For lower accuracy applications an inexpensive 1% thick film resistor may be used.

Limit the capacitance on the SET pin to less than 10pF to minimize jitter and ensure stability. Capacitance less than 100pF maintains the stability of the feedback circuit regulating the  $V_{SET}$  voltage.

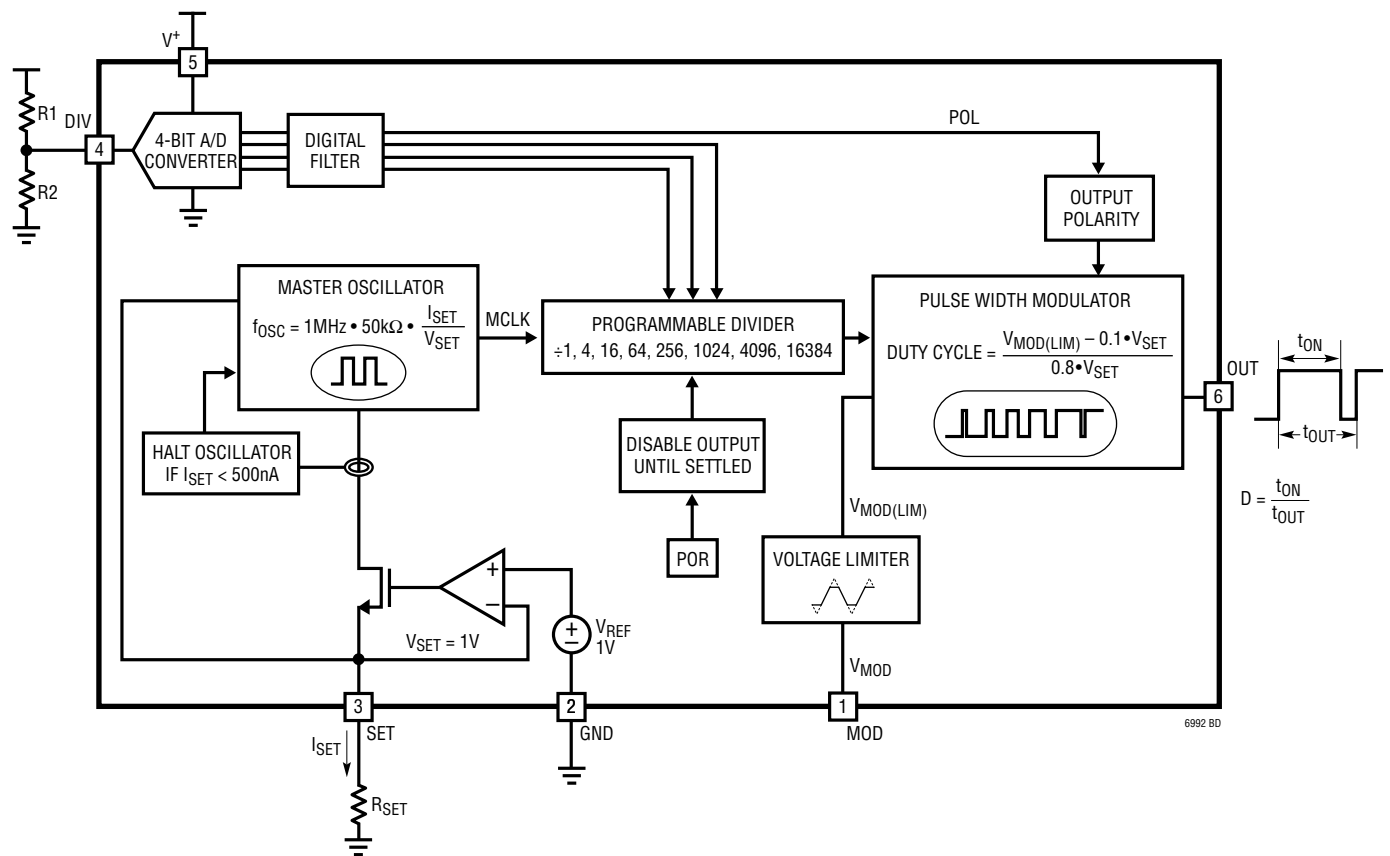


**MOD (Pin 4/Pin 1):** Pulse-Width Modulation Input. The voltage on the MOD pin controls the output duty cycle. The linear control range is between  $0.1 \cdot V_{SET}$  and  $0.9 \cdot V_{SET}$  (approximately 100mV to 900mV). Beyond those limits, the output will either clamp at 5% or 95%, or stop oscillating (0% or 100% duty cycle), depending on the version.

**GND (Pin 5/Pin 2):** Ground. Tie to a low inductance ground plane for best performance.

**OUT (Pin 6/Pin 6):** Oscillator Output. The OUT pin swings from GND to V<sup>+</sup> with an output resistance of approximately 30Ω. The duty cycle is determined by the voltage on the MOD pin. When driving an LED or other low-impedance load a series output resistor should be used to limit the source/sink current to 20mA.

**BLOCK DIAGRAM** (S6 Package Pin Numbers Shown)



## OPERATION

The LTC6992 is built around a master oscillator with a 1MHz maximum frequency. The oscillator is controlled by the SET pin current ( $I_{SET}$ ) and voltage ( $V_{SET}$ ), with a  $1\text{MHz} \cdot 50\text{k}$  conversion factor that is accurate to  $\pm 0.8\%$  under typical conditions.

$$f_{MASTER} = \frac{1}{t_{MASTER}} = 1\text{MHz} \cdot 50\text{k} \cdot \frac{I_{SET}}{V_{SET}}$$

A feedback loop maintains  $V_{SET}$  at  $1\text{V} \pm 30\text{mV}$ , leaving  $I_{SET}$  as the primary means of controlling the output frequency. The simplest way to generate  $I_{SET}$  is to connect a resistor ( $R_{SET}$ ) between SET and GND, such that  $I_{SET} = V_{SET}/R_{SET}$ . The master oscillator equation reduces to:

$$f_{MASTER} = \frac{1}{t_{MASTER}} = \frac{1\text{MHz} \cdot 50\text{k}}{R_{SET}}$$

From this equation, it is clear that  $V_{SET}$  drift will not affect the output frequency when using a single program resistor ( $R_{SET}$ ). Error sources are limited to  $R_{SET}$  tolerance and the inherent frequency accuracy  $\Delta f_{OUT}$  of the LTC6992.

$R_{SET}$  may range from 50k to 800k (equivalent to  $I_{SET}$  between  $1.25\mu\text{A}$  and  $20\mu\text{A}$ ).

The LTC6992 includes a programmable frequency divider which can further divide the frequency by 1, 4, 16, 64, 256, 1024, 4096 or 16384 before driving the OUT pin. The divider ratio  $N_{DIV}$  is set by a resistor divider attached to the DIV pin.

$$f_{OUT} = \frac{1}{t_{OUT}} = \frac{1\text{MHz} \cdot 50\text{k}}{N_{DIV}} \cdot \frac{I_{SET}}{V_{SET}}$$

With  $R_{SET}$  in place of  $V_{SET}/I_{SET}$  the equation reduces to:

$$f_{OUT} = \frac{1}{t_{OUT}} = \frac{1\text{MHz} \cdot 50\text{k}}{N_{DIV} \cdot R_{SET}}$$

## DIVCODE

The DIV pin connects to an internal,  $V^+$  referenced 4-bit A/D converter that determines the DIVCODE value. DIVCODE programs two settings on the LTC6992:

1. DIVCODE determines the output frequency divider setting,  $N_{DIV}$ .
2. DIVCODE determines the output polarity, via the POL bit.

$V_{DIV}$  may be generated by a resistor divider between  $V^+$  and GND as shown in Figure 2.

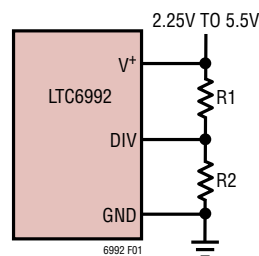


Figure 1. Simple Technique for Setting DIVCODE

## OPERATION

Table 1. DIVCODE Programming

DIVCODE	POL	N <sub>DIV</sub>	RECOMMENDED f <sub>OUT</sub>	R1 (kΩ)	R2 (kΩ)	V <sub>DIV</sub> /V <sup>+</sup>
0	0	1	62.5kHz to 1MHz	Open	Short	≤0.03125 ±0.015
1	0	4	15.63kHz to 250kHz	976	102	0.09375 ±0.015
2	0	16	3.906kHz to 62.5kHz	976	182	0.15625 ±0.015
3	0	64	976.6Hz to 15.63kHz	1000	280	0.21875 ±0.015
4	0	256	244.1Hz to 3.906kHz	1000	392	0.28125 ±0.015
5	0	1024	61.04Hz to 976.6Hz	1000	523	0.34375 ±0.015
6	0	4096	15.26Hz to 244.1Hz	1000	681	0.40625 ±0.015
7	0	16384	3.815Hz to 61.04Hz	1000	887	0.46875 ±0.015
8	1	16384	3.815Hz to 61.04Hz	887	1000	0.53125 ±0.015
9	1	4096	15.26Hz to 244.1Hz	681	1000	0.59375 ±0.015
10	1	1024	61.04Hz to 976.6Hz	523	1000	0.65625 ±0.015
11	1	256	244.1Hz to 3.906kHz	392	1000	0.71875 ±0.015
12	1	64	976.6Hz to 15.63kHz	280	1000	0.78125 ±0.015
13	1	16	3.906kHz to 62.5kHz	182	976	0.84375 ±0.015
14	1	4	15.63kHz to 250kHz	102	976	0.90625 ±0.015
15	1	1	62.5kHz to 1MHz	Short	Open	≥0.96875 ±0.015

Table 1 offers recommended 1% resistor values that accurately produce the correct voltage division as well as the corresponding N<sub>DIV</sub> and POL values for the recommended resistor pairs. Other values may be used as long as:

1. The V<sub>DIV</sub>/V<sup>+</sup> ratio is accurate to ±1.5% (including resistor tolerances and temperature effects).
2. The driving impedance (R1||R2) does not exceed 500kΩ.

If the voltage is generated by other means (i.e. the output of a DAC) it must track the V<sup>+</sup> supply voltage. The last

column in Table 1 shows the ideal ratio of V<sub>DIV</sub> to the supply voltage, which can also be calculated as:

$$\frac{V_{DIV}}{V^+} = \frac{DIVCODE + 0.5}{16} \pm 1.5\%$$

For example, if the supply is 3.3V and the desired DIVCODE is 4, V<sub>DIV</sub> = 0.281 • 3.3V = 928mV ± 50mV.

Figure 2 illustrates the information in Table 1, showing that N<sub>DIV</sub> is symmetric around the DIVCODE midpoint.

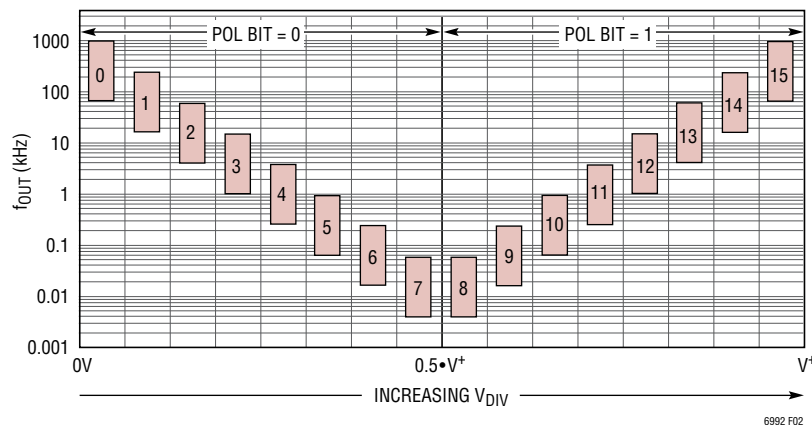


Figure 2. Frequency Range and POL Bit vs DIVCODE

## OPERATION

### Pulse Width (Duty Cycle) Modulation

The MOD pin is a high impedance analog input providing direct control of the output duty cycle. The duty cycle is proportional to the voltage applied to the MOD pin,  $V_{MOD}$ .

$$\text{Duty Cycle} = D = \frac{V_{MOD}}{0.8 \cdot V_{SET}} - \frac{1}{8}$$

The PWM duty cycle accuracy  $\Delta D$  specifies that the above equation is valid to within  $\pm 4.5\%$  for  $V_{MOD}$  between  $0.2 \cdot V_{SET}$  and  $0.8 \cdot V_{SET}$  (12.5% to 87.5% duty cycle).

Since  $V_{SET} = 1V \pm 30mV$ , the duty cycle equation may be approximated by the following equation.

$$\text{Duty Cycle} = D \approx \frac{V_{MOD} - 100mV}{800mV}$$

The  $V_{MOD}$  control range is approximately 0.1V to 0.9V. Driving  $V_{MOD}$  beyond that range (towards GND or  $V^+$ ) will have no further effect on the duty cycle.

### Duty Cycle Limits

The only difference between the four versions of the LTC6992 is the limits, or clamps, placed on the output duty cycle. The LTC6992-1 generates output duty cycles ranging from 0% to 100%. At 0% or 100% the output will stop oscillating and rest at GND or  $V^+$ , respectively.

The LTC6992-2 will never stop oscillating, regardless of the  $V_{MOD}$  level. Internal clamping circuits limit its duty cycle to a 5% to 95% range (1% to 99% guaranteed). Therefore, its  $V_{MOD}$  control range is  $0.14 \cdot V_{SET}$  to  $0.86 \cdot V_{SET}$  (approximately 0.14V to 0.86V).

The LTC6992-3 and LTC6992-4 complete the family by providing one-sided clamping. The LTC6992-3 allows 0% to 95% duty cycle, and the LTC6992-4 allows 5% to 100% duty cycle.

### Output Polarity (POL Bit)

The duty cycle equation describes a proportional transfer function, where duty cycle increases as  $V_{MOD}$  increases. The LTC6992 includes a POL bit (determined by the DIVCODE as described earlier) that inverts the output signal. This makes the duty cycle gain negative, reducing duty cycle as  $V_{MOD}$  increases.

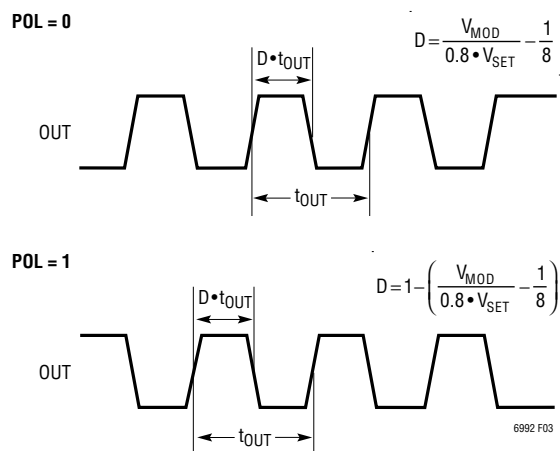


Figure 3. POL Bit Functionality



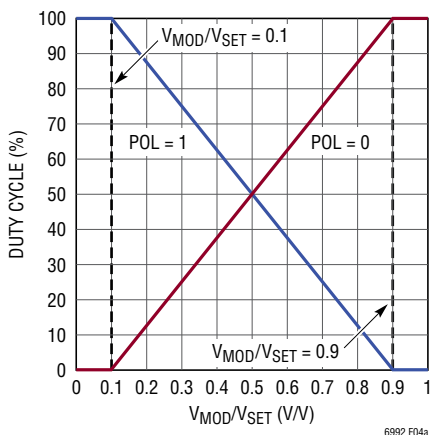
# LTC6992-1/LTC6992-2/ LTC6992-3/LTC6992-4

## OPERATION

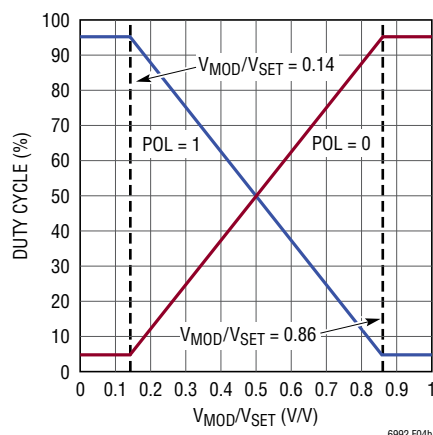
POL = 1 forces a simple logic inversion, so it changes the duty cycle range of the LTC6992-3 (making it 100% to 5%) and LTC6992-4 (making it 95% to 0%). These transfer functions are detailed in Figure 4.

Table 2. Duty Cycle Ranges

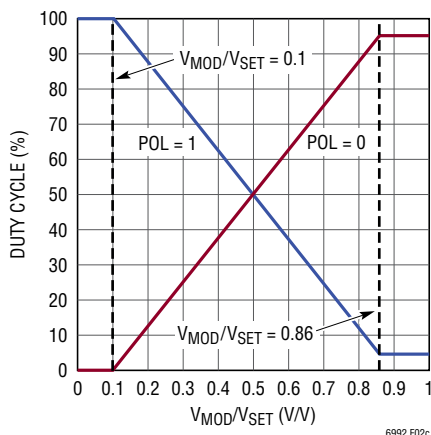
PART NUMBER	DUTY CYCLE RANGE vs $V_{MOD} = 0V \rightarrow 1V$	
	POL = 0	POL = 1
LTC6992-1	0% to 100%	100% to 0%
LTC6992-2	5% to 95%	95% to 5%
LTC6992-3	0% to 95%	100% to 5%
LTC6992-4	5% to 100%	95% to 0%



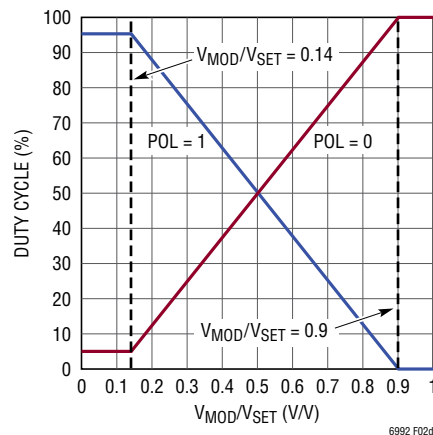
LTC6992-1



LTC6992-2



LTC6992-3



LTC6992-4

Figure 4. PWM Transfer Functions for All LTC6992 Family Parts

## OPERATION

### Changing DIVCODE After Start-Up

Following start-up, the A/D converter will continue monitoring  $V_{DIV}$  for changes. Changes to DIVCODE will be recognized slowly, as the LTC6992 places a priority on eliminating any “wandering” in the DIVCODE. The typical delay depends on the difference between the old and new DIVCODE settings and is proportional to the master oscillator period.

$$t_{DIVCODE} = 16 \cdot (\Delta DIVCODE + 6) \cdot t_{MASTER}$$

A change in DIVCODE will not be recognized until it is stable, and will not pass through intermediate codes. A digital filter is used to guarantee the DIVCODE has settled to a new value before making changes to the output. Then the output will make a clean (glitchless) transition to the new divider setting.

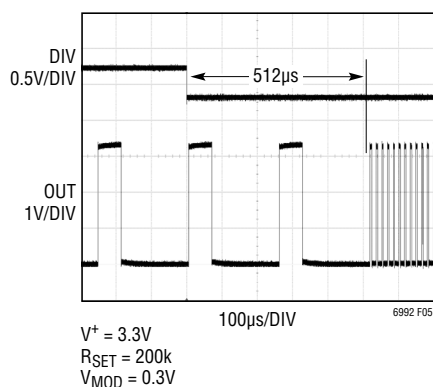


Figure 5. DIVCODE Change from 3 to 1

### Start-Up Time

When power is first applied, the power-on reset (POR) circuit will initiate the start-up time,  $t_{START}$ . The OUT pin is held low during this time. The typical value for  $t_{START}$  ranges from 0.5ms to 8ms depending on the master oscillator frequency (independent of  $N_{DIV}$ ):

$$t_{START(TYP)} = 500 \cdot t_{MASTER}$$

The output will begin oscillating after  $t_{START}$ . If  $POL = 0$  the first pulse has the correct width. If  $POL = 1$  ( $DIVCODE \geq 8$ ), the first pulse width can be shorter or longer than expected, depending on the duty cycle setting, and will never be less than 25% of  $t_{OUT}$ .

During start-up, the DIV pin A/D converter must determine the correct DIVCODE before the output is enabled. The start-up time may increase if the supply or DIV pin voltages are not stable. For this reason, it is recommended to minimize the capacitance on the DIV pin so it will properly track  $V^+$ . Less than 100pF will not affect performance.

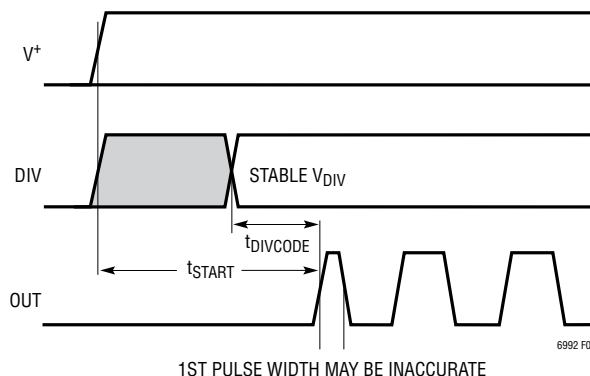


Figure 6. Start-Up Timing Diagram

## APPLICATIONS INFORMATION

### Basic Operation

The simplest and most accurate method to program the LTC6992 is to use a single resistor,  $R_{SET}$ , between the SET and GND pins. The design procedure is a four step process. After choosing the proper LTC6992 version and POL bit setting, select the  $N_{DIV}$  value and then calculate the value for the  $R_{SET}$  resistor.

Alternatively, Analog Devices offers the easy to use TimerBlox Designer tool to quickly design any LTC6992 based circuit. Use the free [TimerBlox LTC6992: PWM Web-Based Design Tool](#).

### Step 1: Selecting the POL Bit Setting

Most applications will use  $POL = 0$ , resulting in a positive transfer function. However, some applications may require a negative transfer function, where increasing  $V_{MOD}$  reduces the output duty cycle. For example, if the LTC6992 is used in a feedback loop,  $POL = 1$  may be required to achieve negative feedback.

### Step 2: Selecting the LTC6992 Version

The difference between the LTC6992 versions is observed at the endpoints of the duty cycle control range. Applications that require the output to never stop oscillating should use the LTC6992-2. On the other hand, if the output should be allowed to rest at GND or  $V^+$  (0% or 100% duty cycle), select the LTC6992-1.

The LTC6992-3 and LTC6992-4 clamp the duty cycle at only one end of the control range, allowing the output to stop oscillating at the other extreme. If  $POL = 1$  the clamp will swap from low duty cycle to high, or vice-versa. Refer to Table 2 and Figure 4 for assistance in selecting the proper version.

### Step 3: Selecting the $N_{DIV}$ Frequency Divider Value

As explained earlier, the voltage on the DIV pin sets the DIVCODE which determines both the POL bit and the  $N_{DIV}$  value. For a given output frequency,  $N_{DIV}$  should be selected to be within the following range.

$$\frac{62.5\text{kHz}}{f_{OUT}} \leq N_{DIV} \leq \frac{1\text{MHz}}{f_{OUT}} \quad (1a)$$

To minimize supply current, choose the lowest  $N_{DIV}$  value (generally recommended). For faster start-up or decreased jitter, choose a higher  $N_{DIV}$  setting. Alternatively, use Table 1 as a guide to select the best  $N_{DIV}$  value for the given application.

With POL already chosen, this completes the selection of DIVCODE. Use Table 1 to select the proper resistor divider or  $V_{DIV}/V^+$  ratio to apply to the DIV pin.

### Step 4: Calculate and Select $R_{SET}$

The final step is to calculate the correct value for  $R_{SET}$  using the following equation.

$$R_{SET} = \frac{1\text{MHz} \cdot 50\text{k}}{N_{DIV} \cdot f_{OUT}} \quad (1b)$$

Select the standard resistor value closest to the calculated value.

*Example:* Design a PWM circuit that satisfies the following requirements:

- $f_{OUT} = 20\text{kHz}$
- Positive  $V_{MOD}$  to duty cycle response
- Output can reach 100% duty cycle, but not 0%
- Minimum power consumption

### Step 1: Selecting the POL Bit Setting

For positive transfer function (duty cycle increases with  $V_{MOD}$ ), choose  $POL = 0$ .

### Step 2: Selecting the LTC6992 Version

To limit the minimum duty cycle, but allow the maximum duty cycle to reach 100%, choose LTC6992-4. (Note that if  $POL = 1$  the LTC6992-3 would be the correct choice.)

### Step 3: Selecting the $N_{DIV}$ Frequency Divider Value

Choose an  $N_{DIV}$  value that meets the requirements of Equation (1a).

$$3.125 \leq N_{DIV} \leq 50$$

Potential settings for  $N_{DIV}$  include 4 and 16.  $N_{DIV} = 4$  is the best choice, as it minimizes supply current by using

## APPLICATIONS INFORMATION

a large  $R_{SET}$  resistor.  $POL = 0$  and  $N_{DIV} = 4$  requires  $DIVCODE = 1$ . Using Table 1, choose the  $R1$  and  $R2$  values to program  $DIVCODE = 1$ .

### Step 4: Select $R_{SET}$

Calculate the correct value for  $R_{SET}$  using Equation (1b).

$$R_{SET} = \frac{1\text{MHz} \cdot 50\text{k}}{4 \cdot 20\text{kHz}} = 625\text{k}$$

Since 625k is not available as a standard 1% resistor, substitute 619k if a 0.97% frequency shift is acceptable. Otherwise, select a parallel or series pair of resistors such as 309k and 316k to attain a more precise resistance.

The completed design is shown in Figure 7.

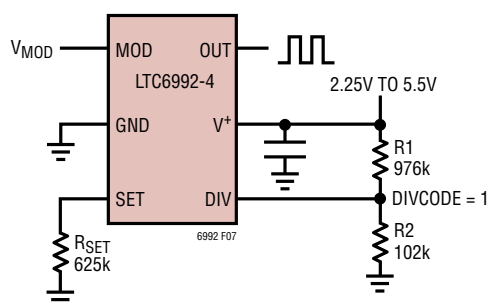


Figure 7. 20kHz PWM Oscillator

### Duty Cycle Sensitivity to $\Delta V_{SET}$

The output duty cycle is proportional to the ratio of  $V_{MOD}/V_{SET}$ . Since  $V_{SET}$  can vary up to  $\pm 30\text{mV}$  from 1V it can effectively gain or attenuate  $V_{MOD}$ , as shown below when  $\Delta V_{SET}$  is added to the equation.

$$D = \frac{V_{MOD}}{0.8 \cdot (V_{SET} + \Delta V_{SET})} - \frac{1}{8}$$

For many designs, the absolute  $V_{MOD}$  to duty cycle accuracy is not critical. For others, making the simplifying assumption of  $\Delta V_{SET} = 0\text{V}$  creates the potential for additional duty cycle error, which increases with  $V_{MOD}$ , reaching a maximum of 3.4% if  $\Delta V_{SET} = -30\text{mV}$ .

$$\Delta D \approx -\frac{V_{MOD}}{800\text{mV}} \cdot \frac{\Delta V_{SET}}{V_{SET}} \approx -\left(D_{IDEAL} + \frac{1}{8}\right) \cdot \frac{\Delta V_{SET}}{V_{SET}}$$

Figure 8 demonstrates the worst-case impact of this variation (if  $V_{SET}$  is at its 0.97V or 1.03V limits).

This error is in addition to the inherent PWM duty cycle accuracy spec  $\Delta D$  ( $\pm 4.5\%$ ), so care should be taken if accuracy at high duty cycles ( $V_{MOD}$  near 0.9V) is critical.

Sensitivity to  $\Delta V_{SET}$  can be eliminated by making  $V_{MOD}$  proportional to  $V_{SET}$ . For example, Figure 9 shows a simple circuit for generating an arbitrary duty cycle. The equation for duty cycle does not depend on  $V_{SET}$  at all.

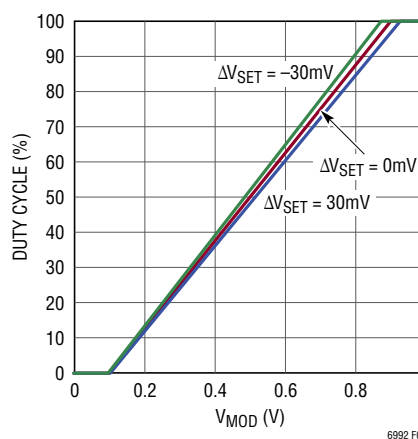


Figure 8. Duty Cycle Variation Due to  $\Delta V_{SET}$

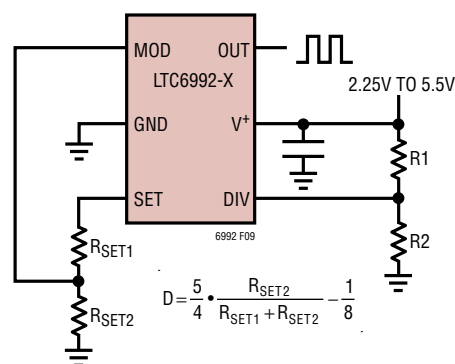


Figure 9. Fixed-Frequency, Arbitrary Duty Cycle Oscillator

## APPLICATIONS INFORMATION

### $I_{SET}$ Extremes (Master Oscillator Frequency Extremes)

When operating with  $I_{SET}$  outside of the recommended  $1.25\mu A$  to  $20\mu A$  range, the master oscillator operates outside of the  $62.5kHz$  to  $1MHz$  range in which it is most accurate.

The oscillator will still function with reduced accuracy for  $I_{SET} < 1.25\mu A$ . At approximately  $500nA$ , the oscillator output will be frozen in its current state. The output could halt in a high or low state. This avoids introducing short pulses while frequency modulating a very low frequency output.

At the other extreme, it is not recommended to operate the master oscillator beyond  $2MHz$  because the accuracy of the DIV pin ADC will suffer.

### Pulse Width Modulation Bandwidth and Settling Time

The LTC6992 has a wide PWM bandwidth, making it suitable for a variety of feedback applications. Figure 10 shows that the frequency response is flat for modulation frequencies up to nearly  $1/10$  of the output frequency. Beyond that point, some peaking may occur (depending on  $N_{DIV}$  and average duty cycle setting).

Duty cycle settling time depends on the master oscillator frequency. Following a  $\pm 80mV$  step change in  $V_{MOD}$ , the duty cycle takes approximately eight master clock cycles ( $8 \cdot t_{MASTER}$ ) to settle to within 1% of the final value. Examples are shown in Figure 11a and Figure 11b.

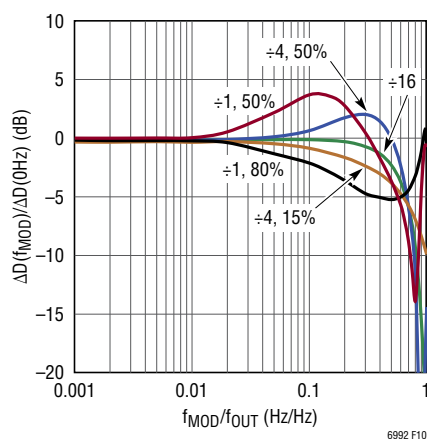
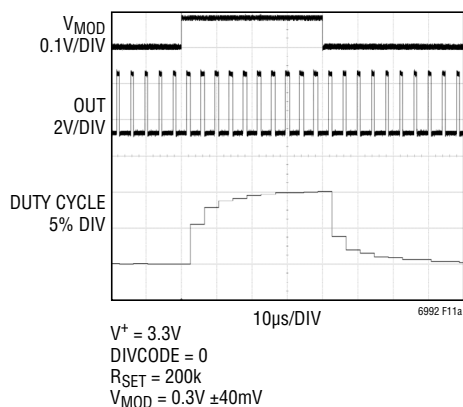
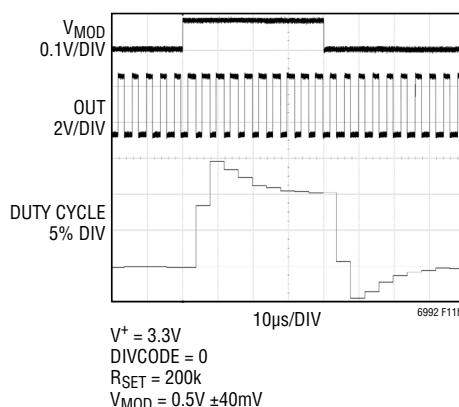


Figure 10. PWM Frequency Response



(a) 25% Duty Cycle



(b) 50% Duty Cycle

Figure 11. PWM Settling Time

## APPLICATIONS INFORMATION

### Power Supply Current

The power supply current varies with frequency, supply voltage and output loading. It can be estimated under any condition using the following equation:

If  $N_{DIV} = 1$  (DIVCODE = 0 or 15):

$$I_{S(TYP)} \approx V^+ \cdot f_{OUT} \cdot (39pF + C_{LOAD}) \\ \dots + \frac{V^+}{320k\Omega} + \frac{V^+ \cdot \text{Duty Cycle}}{R_{LOAD}} + 2.2 \cdot I_{SET} + 85\mu A$$

If  $N_{DIV} > 1$  (DIVCODE = 1 or 14):

$$I_{S(TYP)} \approx V^+ \cdot N_{DIV} \cdot f_{OUT} \cdot 27pF \\ \dots + V^+ \cdot f_{OUT} \cdot (28pF + C_{LOAD})$$

### SUPPLY BYPASSING AND PCB LAYOUT GUIDELINES

The LTC6992 is a 2.4% accurate silicon oscillator when used in the appropriate manner. The part is simple to use and by following a few rules, the expected performance is easily achieved. Adequate supply bypassing and proper PCB layout are important to ensure this.

Figure 12 shows example PCB layouts for both the TSOT-23 and DFN packages using 0603 sized passive components. The layouts assume a two layer board with a ground plane layer beneath and around the LTC6992. These layouts are a guide and need not be followed exactly.

1. Connect the bypass capacitor, C1, directly to the V<sup>+</sup> and GND pins using a low inductance path. The connection from C1 to the V<sup>+</sup> pin is easily done directly on the top layer. For the DFN package, C1's connection to GND is also simply done on the top layer. For the TSOT-23, OUT can be routed through the C1 pads to allow a good C1 GND connection. If the PCB design rules do not allow that, C1's GND connection can be accomplished through multiple vias to the ground plane. Multiple vias for both the GND pin connection to the ground plane and the C1 connection to the ground plane are recommended to minimize the inductance. Capacitor C1 should be a 0.1μF ceramic capacitor.
2. Place all passive components on the top side of the board. This minimizes trace inductance.
3. Place R<sub>SET</sub> as close as possible to the SET pin and make a direct, short connection. The SET pin is a current summing node and currents injected into this pin directly modulate the operating frequency. Having a short connection minimizes the exposure to signal pickup.
4. Connect R<sub>SET</sub> directly to the GND pin. Using a long path or vias to the ground plane will not have a significant affect on accuracy, but a direct, short connection is recommended and easy to apply.
5. Use a ground trace to shield the SET pin. This provides another layer of protection from radiated signals.
6. Place R1 and R2 close to the DIV pin. A direct, short connection to the DIV pin minimizes the external signal coupling.

## APPLICATIONS INFORMATION

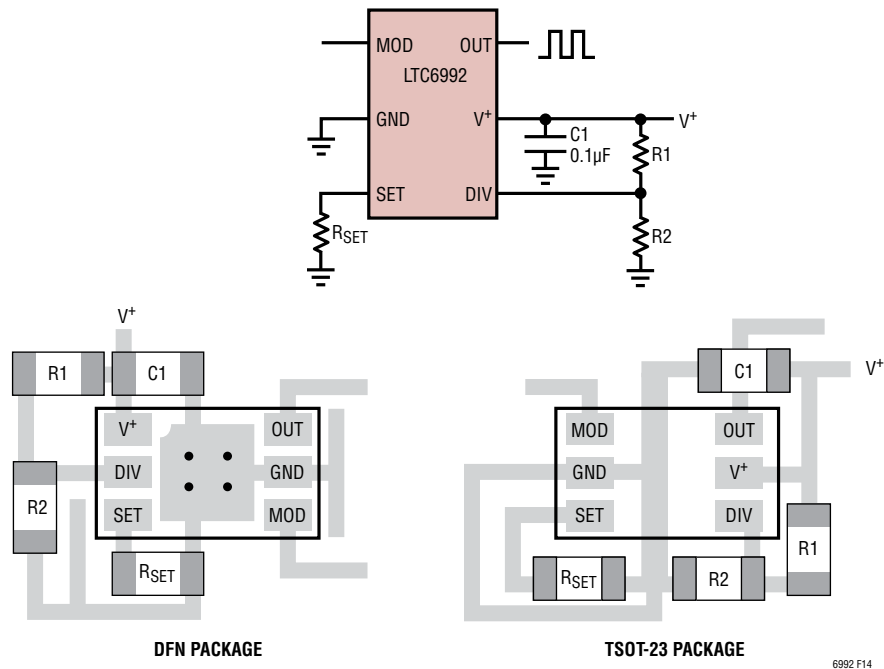
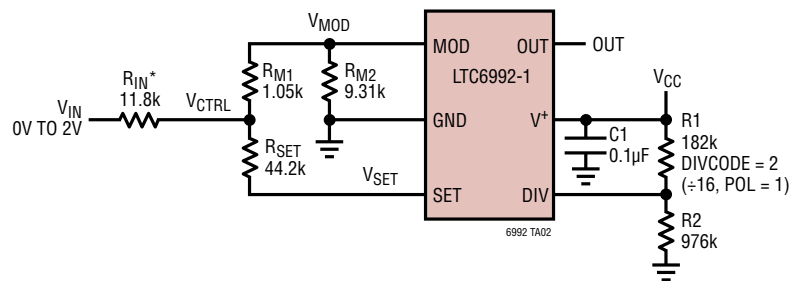


Figure 12. Supply Bypassing and PCB Layout

## TYPICAL APPLICATIONS

### Constant On-Time Modulator



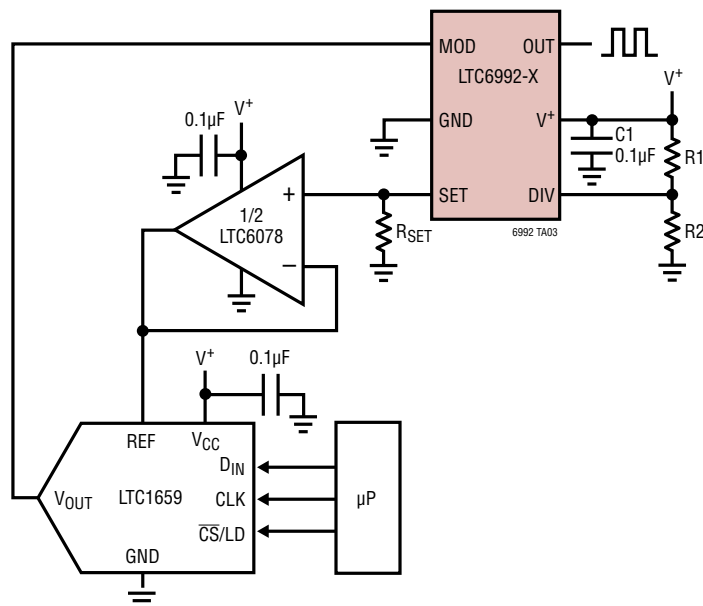
\*OPTIONAL RESISTOR ADJUSTS FOR DESIRED  $V_{IN}$  RANGE.

$$\text{IF } \frac{R_{M2}}{R_{M1} + R_{M2}} = 0.9 \text{ THEN } t_{ON} = N_{DIV} \cdot 1.125\mu s \cdot \frac{R_{SET}}{50k}$$

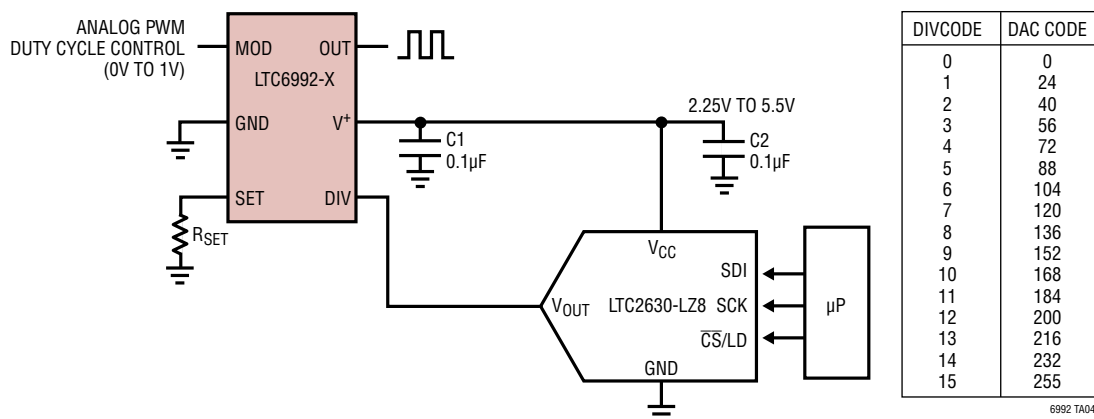
AS  $V_{IN}$  INCREASES,  $t_{OUT}$  INCREASES AND DUTY CYCLE DECREASES (BECAUSE  $POL = 1$ ) TO MAINTAIN A CONSTANT  $t_{ON}$ . FOR CONSTANT OFF-TIME, JUST CHANGE  $DIVCODE$  SO  $POL = 0$ .

## TYPICAL APPLICATIONS

### Digitally Controlled Duty Cycle with Internal $V_{REF}$ Reference Variation Eliminated



### Programming $N_{DIV}$ Using an 8-Bit DAC





## TYPICAL APPLICATIONS

The diagram shows an LTC6992-X IC configured as a PWM oscillator. The MOD pin is connected to an 'ANALOG PWM DUTY CYCLE CONTROL' input ranging from 0V to 1V. The OUT pin produces a square wave output. The GND pin is connected to ground. The V+ pin is connected to a positive supply voltage V, with a 0.1μF capacitor connected between V+ and GND. The SET pin is connected to ground. The DIV pin is connected to a voltage divider consisting of resistors R1 and R2, with the junction connected to ground. The oscillator's timing network consists of two resistors, RSET1 and RSET2, connected between the V+ pin and the SET pin. A 2N7002 N-channel MOSFET is connected with its gate to the SET pin, its source to ground, and its drain to the V+ pin. The MOSFET's switching action is controlled by an inverter (labeled 'HC04') whose input is a square wave between f<sub>MIN</sub> and f<sub>MAX</sub>.

6992 T405

5V

R6 45.3k

R7 16.9k

D1 1N458

R8 84.5k

5V

0.1μF

+10mV/C

LT6003

MOD

OUT

LTC6992-2

GND

V+

SET

DIV

6992 TA06

R9 365Ω

5V

0.1μF

MOC207M

D3

Q1

5V

0.1μF

R11 422Ω

C1 1μF

OUTPUT

R1 130k

R2 50k

R3 130k

ADJUST FOR 50% DUTY CYCLE AT 25°C

$N_{DIV} = 16$

$f = 10\text{kHz}$

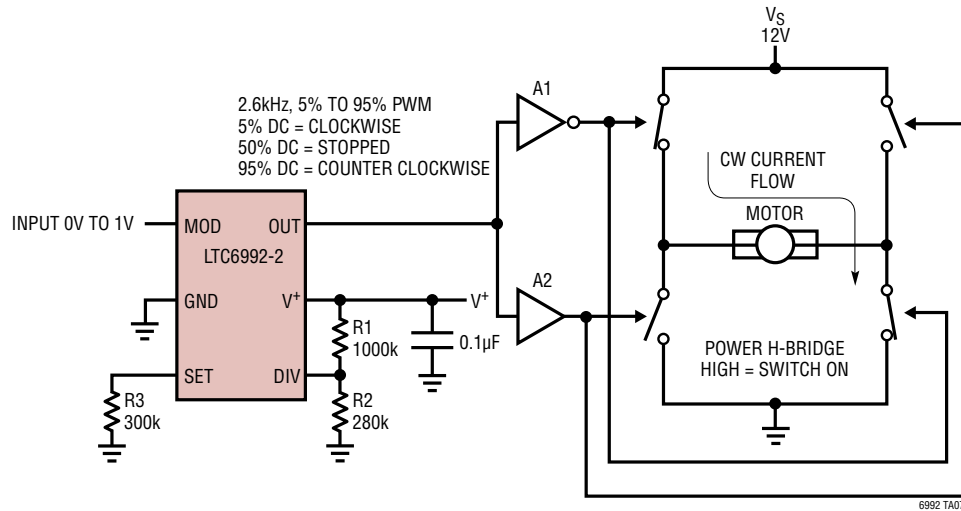
PWM OUTPUT FOR ISOLATED MEASUREMENT

+1% DUTY CYCLE CHANGE PER DEGREE C

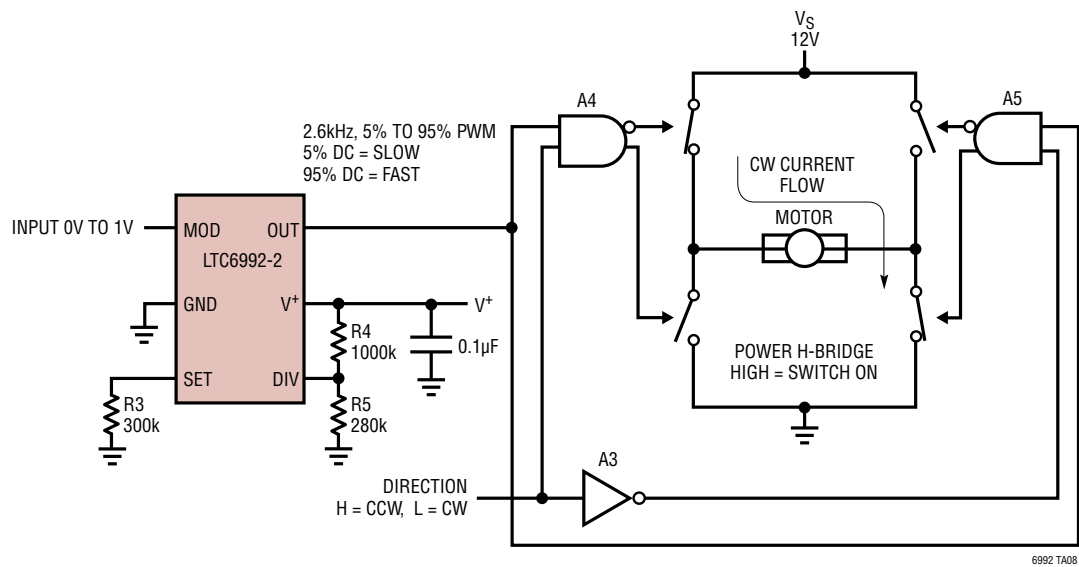
-10°C TO 65°C RANGE WITH OPTO-ISOLATOR (DC: 15% TO 95%)

## TYPICAL APPLICATIONS

### Motor Speed/Direction Control for Full H-Bridge (Locked Anti-Phase Drive)

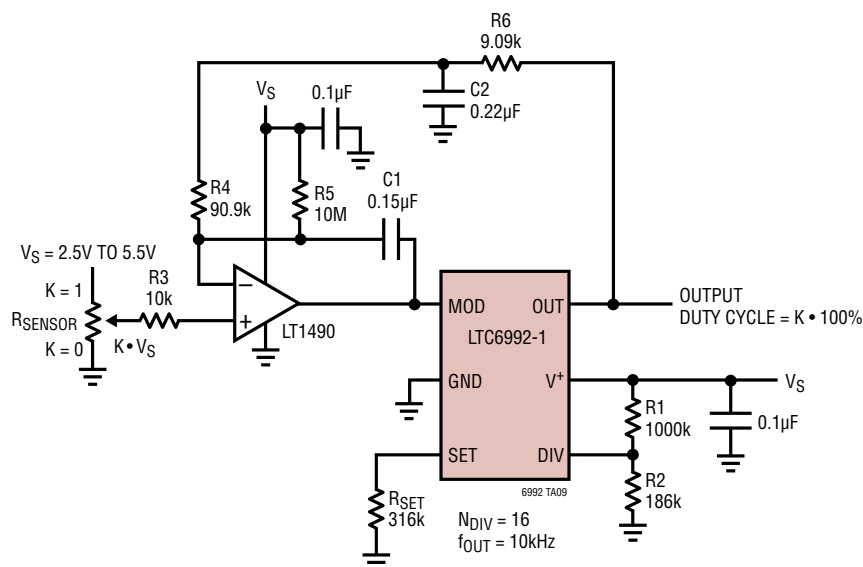


### Motor Speed/Direction Control for Full H-Bridge (Sign/Magnitude Drive)

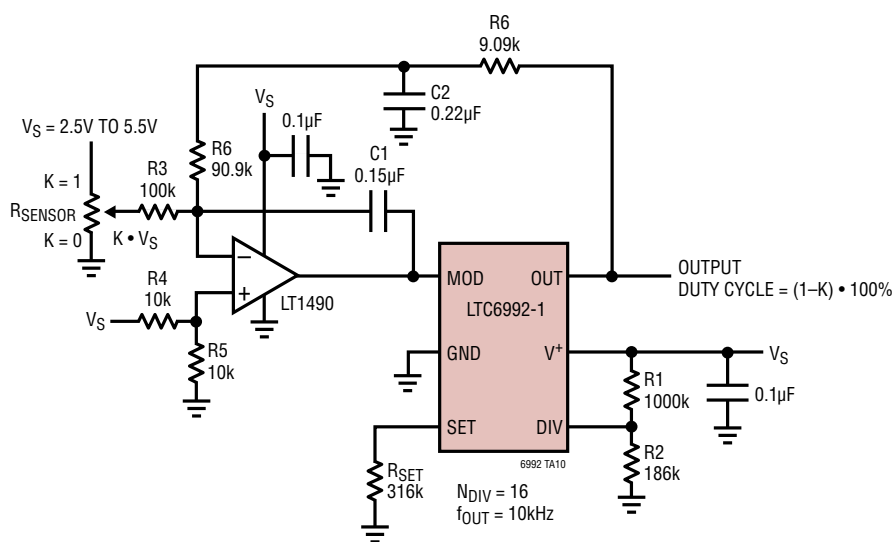


## TYPICAL APPLICATIONS

### Ratiometric Sensor to Pulse Width, Non-Inverting Response

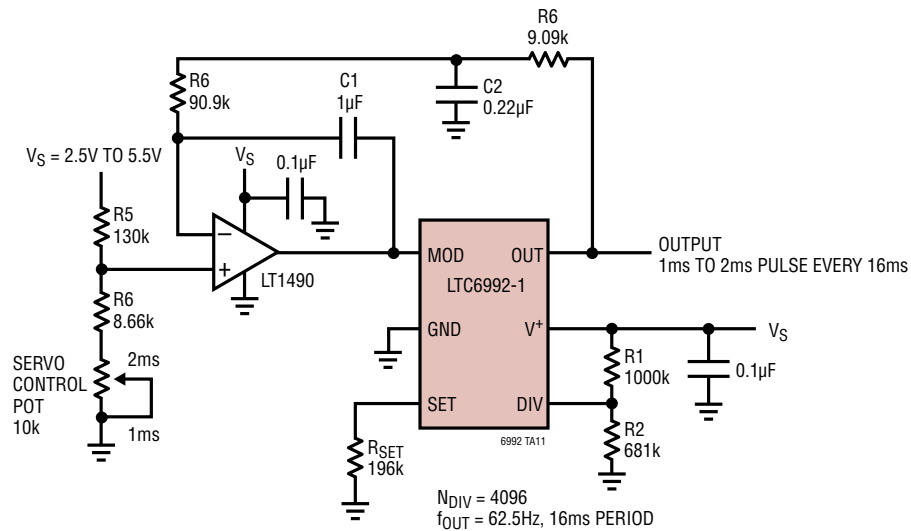


### Ratiometric Sensor to Pulse Width, Inverting Response

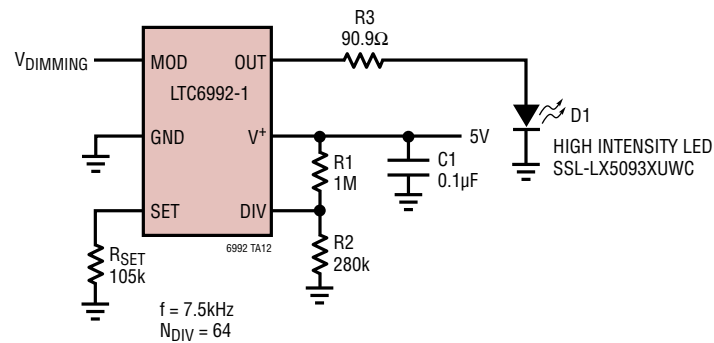


## TYPICAL APPLICATIONS

### Radio Control Servo Pulse Generator

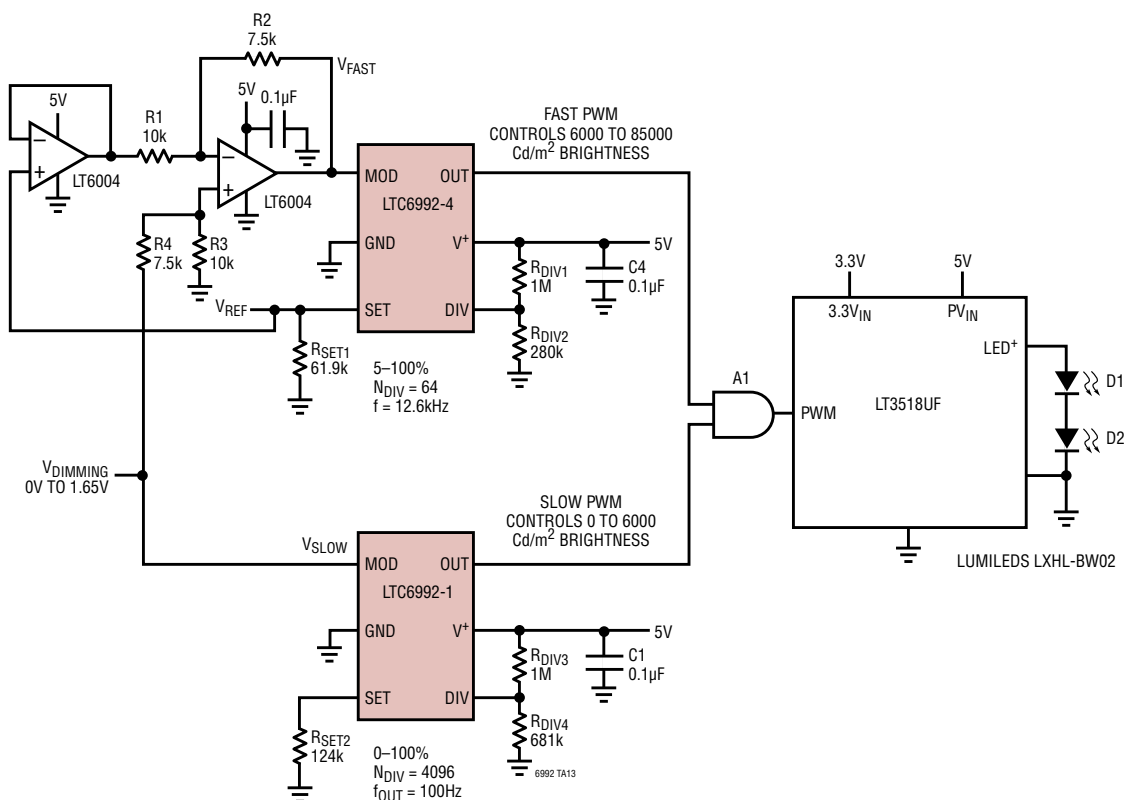


### Direct Voltage Controlled PWM Dimming (0 to 15000 Cd/m<sup>2</sup> Intensity)

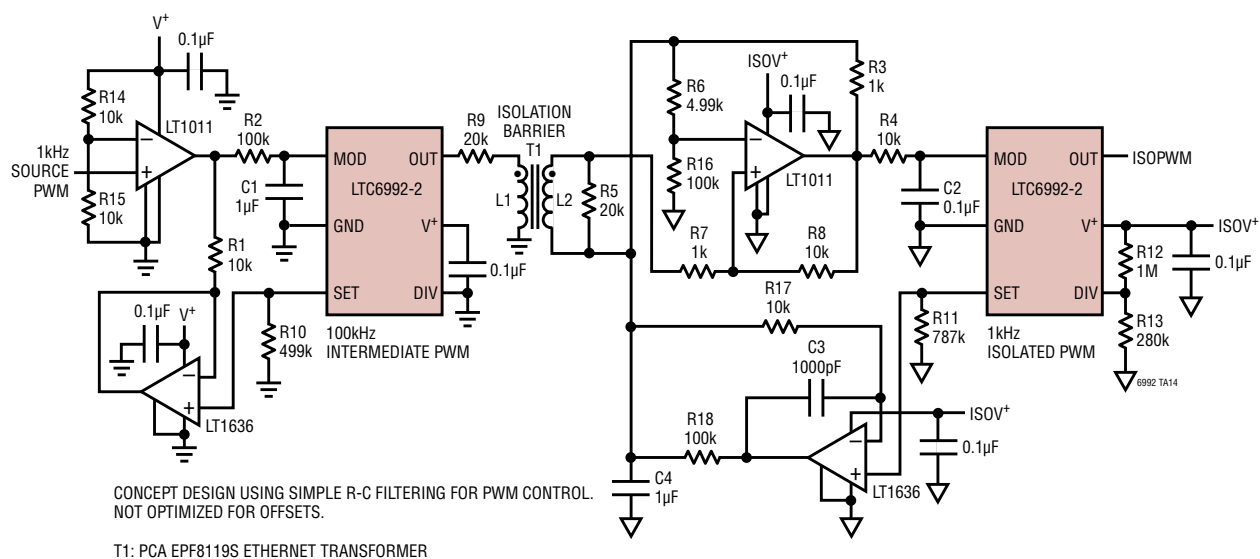


## TYPICAL APPLICATIONS

### Wide Range LED Dimming (0 to 85000 Cd/m<sup>2</sup> Brightness)

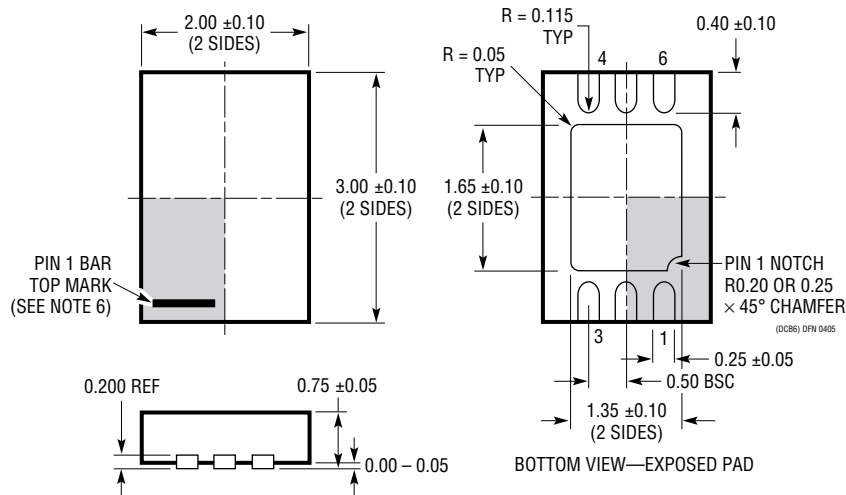
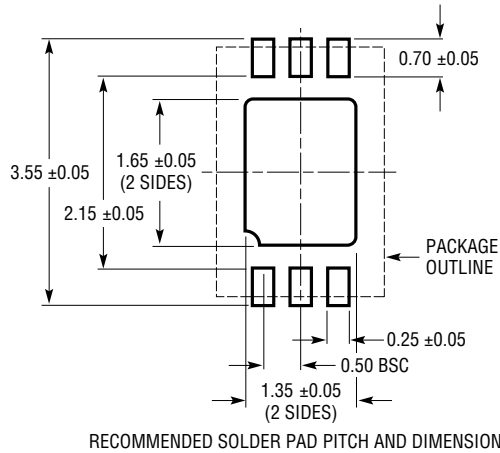


### Isolated PWM (5% to 95%) Controller



## PACKAGE DESCRIPTION

**DCB Package**  
**6-Lead Plastic DFN (2mm × 3mm)**  
(Reference LTC DWG # 05-08-1715 Rev A)

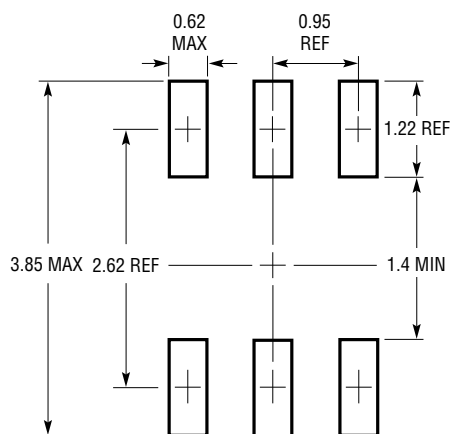


**NOTE:**

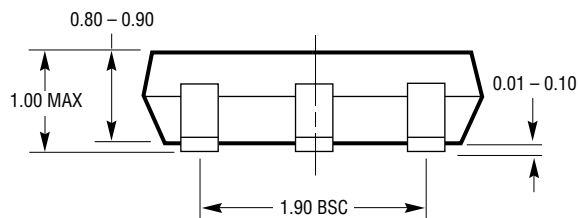
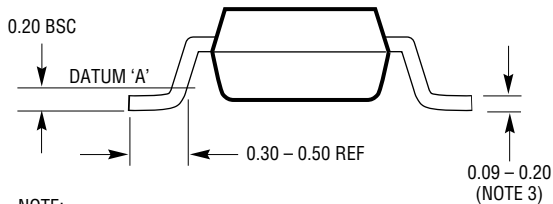
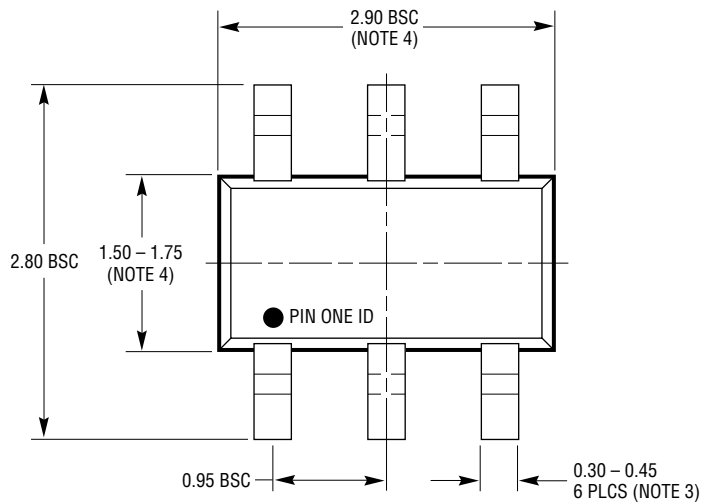
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (TBD)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

## PACKAGE DESCRIPTION

**S6 Package**  
**6-Lead Plastic TSOT-23**  
(Reference LTC DWG # 05-08-1636)



RECOMMENDED SOLDER PAD LAYOUT  
PER IPC CALCULATOR



S6 TSOT-23 0302

**NOTE:**

1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

## REVISION HISTORY

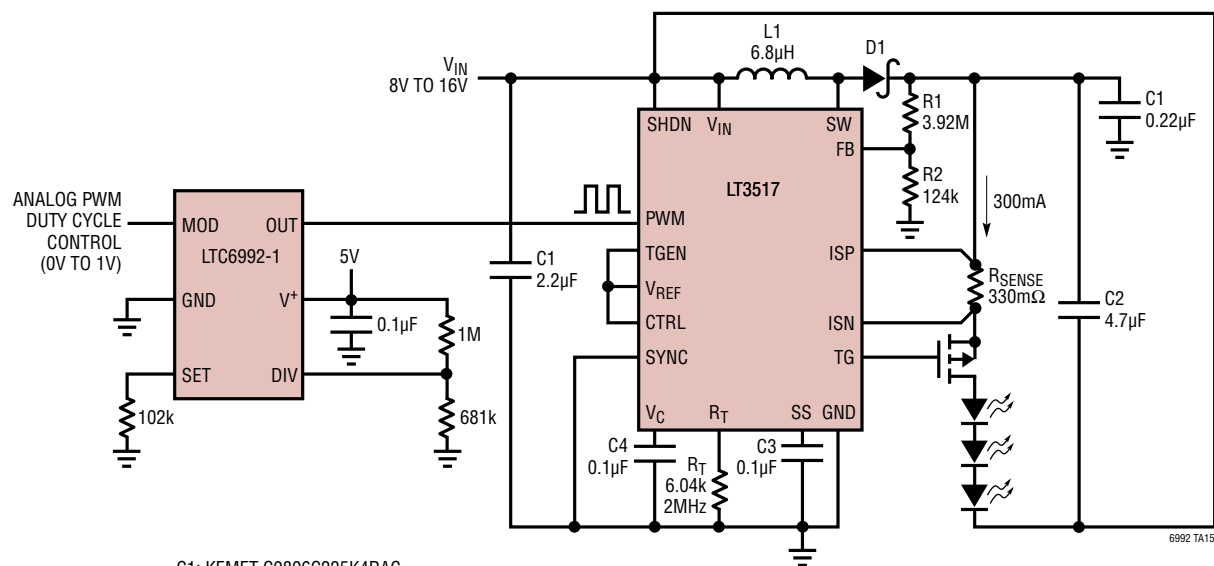
REV	DATE	DESCRIPTION	PAGE NUMBER
A	01/11	Revised $\theta_{JA}$ value for TSOT package in the Pin Configuration.	2
		Added Note 7 for $V_{OH}$ and $V_{OL}$ in the Electrical Characteristics table.	4
		Minor edit to the Block Diagram.	12
		Minor edit to the equation in the "Duty Cycle Sensitivity to $\Delta V_{SET}$ " section.	19
		Revised Typical Application drawings.	25
B	07/11	Revised Description and Order Information sections	1 to 3
		Added additional information to $\Delta f_{OUT}/\Delta V^+$ and included Note 11 in Electrical Characteristics section	3, 4
		Added Typical Frequency Error vs Time curve to Typical Performance Characteristics section	11
		Added text to Basic Operation paragraph in Applications Information section	19
		Corrected $f_{OUT}$ value in Typical Application drawing 6692 TA13	29
C	01/12	Added MP-Grade	1, 2, 3, 5
D	11/19	Added AEC-Q100 Qualified Note to Front Page	1
		Added W-Grade Order Information	3



LTC6992-1/LTC6992-2/  
LTC6992-3/LTC6992-4

TYPICAL APPLICATION

PWM Controller for LED Driver



C1: KEMET C0806C225K4RAC  
C2: KEMET C1206C475K3RAC  
C3, C4: MURATA GRM21BR71H104KA01B  
C5: MURATA GRM21BR71H224KA01B  
D1: DIODE DFSL160  
L1: TOKO B992AS-6R8N  
LEDs: LUXEON I (WHITE)  
M1: ZETEX ZXMP6A13FTA

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
<a href="#">LTC1799</a>	1MHz to 33MHz ThinSOT Silicon Oscillator	Wide Frequency Range
<a href="#">LTC6900</a>	1MHz to 20MHz ThinSOT Silicon Oscillator	Low Power, Wide Frequency Range
<a href="#">LTC6906/LTC6907</a>	10kHz to 1MHz or 40kHz ThinSOT Silicon Oscillator	Micropower, ISUPPLY = 35μA at 400kHz
<a href="#">LTC6930</a>	Fixed Frequency Oscillator, 32.768kHz to 8.192MHz	0.09% Accuracy, 110μs Start-Up Time, 105μA at 32kHz
<a href="#">LTC6990</a>	TimerBlox, Voltage Controlled Oscillator	Frequency from 488Hz to 1MHz, No Caps, 2.2% Accurate
<a href="#">LTC6991</a>	TimerBlox, Very Low Frequency Clock with Reset	Cycle Time from 2ms to 9.5 Hours, No Caps, 2.2% Accurate
<a href="#">LTC6993</a>	TimerBlox, Monostable Pulse Generator	Resistor Set Pulse Width from 1μs to 34sec, No Caps, 3% Accurate
<a href="#">LTC6994</a>	TimerBlox, Delay Block/Debouncer	Resistor Set Delay from 1μs to 34sec, No Caps Required, 3% Accurate