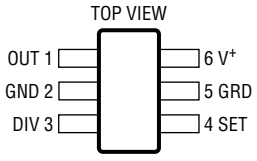
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V^+ ..... –0.3V to 6V
DIV to GND ..... –0.3V to (V^+ + 0.3V)
SET to GND ..... –0.3V to (V^+ + 0.3V)
GRD to GND ..... –0.3V to (V^+ + 0.3V)
Operating Temperature Range (Note 7)
LTC6907C ..... –40°C to 85°C
LTC6907I ..... –40°C to 85°C
LTC6907H ..... –40°C to 125°C
Specified Temperature Range (Note 7)
LTC6907C ..... 0°C to 70°C
LTC6907I ..... –40°C to 85°C
LTC6907H ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



S6 PACKAGE
6-LEAD PLASTIC TSOT-23

T_{JMAX} = 150°C, θ_{JA} = 200°C/W

ORDER PART NUMBER
LTC6907CS6 LTC6907IS6 LTC6907HS6
S6 PART MARKING*
LTBTX

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.
*The temperature grade is indicated by a label on the shipping container.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full specified temperature range, otherwise specifications are at T_A = 25°C. V^+ = 3V to 3.6V, C_L = 5pF, Pin 3 = V^+ unless otherwise noted. All voltages are with respect to GND.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Δf	Frequency Accuracy (Notes 2, 3)	V^+ = 3V to 3.6V	400kHz ≤ f ≤ 4MHz			±0.25	±0.65	%
			400kHz ≤ f ≤ 4MHz, LTC6907C	●			±1	%
			400kHz ≤ f ≤ 4MHz, LTC6907I, H	●			±1.3	%
R_{SET}	Frequency-Setting Resistor Range			●	50		500	kΩ
Δf/ΔT	Frequency Drift Over Temp (Note 3)	R_{SET} = 158k		●		±0.005		%/°C
Δf/ΔV	Frequency Drift Over Supply (Note 3)	V^+ = 3V to 3.6V, 50k ≤ R_{SET} ≤ 500k				0.06		%/V
	Timing Jitter (Peak-to-Peak) (Note 4)	Pin 3 = V^+, 50k ≤ R_{SET} ≤ 500k				0.12		%
		Pin 3 = Open, 50k ≤ R_{SET} ≤ 500k				0.28		%
		Pin 3 = 0V, 50k ≤ R_{SET} ≤ 500k				0.60		%
S_f	Long-Term Stability of Output Frequency (Note 9)	Pin 3 = V^+				300		ppm/√kHr
		Stability Over 1 Year				888		ppm
		Stability Over 10 Years				2809		ppm
DC	Duty Cycle			●	43	50	57	%
V^+	Operating Supply Range (Note 8)			●	3		3.6	V
I_S	Power Supply Current	R_{SET} = 500k, Pin 3 = 0V, R_L = 10M (DIV = 1, f_{OUT} = 400kHz)	V^+ = 3.6V	●		40	55	μA
			V^+ = 3V	●		36	48	μA
		R_{SET} = 50k, Pin 3 = 0V, R_L = 10M (DIV = 1, f_{OUT} = 4MHz)	V^+ = 3.6V	●		305	406	μA
			V^+ = 3V	●		275	366	μA
V_{IH}	High Level DIV Input Voltage		V^+ = 3.6V	●	3.1			V
			V^+ = 3V	●	2.6			V
V_{IL}	Low Level DIV Input Voltage		V^+ = 3.6V	●			0.5	V
			V^+ = 3V	●			0.2	V
I_{DIV}	DIV Input Current (Note 5)	Pin 3 = V^+	V^+ = 3.6V	●		1	2	μA
		Pin 3 = 0V		●	–2	–1		μA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full specified temperature range, otherwise specifications are at T_A = 25°C. V^+ = 3V to 3.6V, C_L = 5pF, Pin 3 = V^+ unless otherwise noted. All voltages are with respect to GND.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
V_{OH}	High Level Output Voltage (Note 5)	V^+ = 3.6V	I_{OH} = –100µA I_{OH} = –1mA	● ●	3.40 3.10	3.57 3.45		V V
		V^+ = 3V	I_{OH} = –100µA I_{OH} = –1mA	● ●	2.8 2.5	2.97 2.80		V V
V_{OL}	Low Level Output Voltage (Note 5)	V^+ = 3.6V	I_{OL} = 100µA I_{OL} = 1mA	● ●		0.08 0.25	0.2 0.8	V V
		V^+ = 3V	I_{OL} = 100µA I_{OL} = 1mA	● ●		0.07 0.25	0.2 0.8	V V
t_r	OUT Rise Time (Note 6)	V^+ = 3.6V V^+ = 3V				10 25		ns ns
t_f	OUT Fall Time (Note 6)	V^+ = 3.6V V^+ = 3V				10 25		ns ns
VGS	GRD Pin Voltage Relative to SET Pin Voltage	–10µA ≤ I_{GRD} ≤ 0.3µA		●	–10		10	mV

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Some frequencies may be generated using two different values of R_{SET}. For these frequencies, the error is specified assuming that the larger value of R_{SET} is used.

Note 3: Frequency accuracy is defined as the deviation from the f_{OUT} equation.

Note 4: Jitter is the ratio of the peak-to-peak deviation of the period to the mean of the period. This specification is based on characterization and is not 100% tested.

Note 5: Current into a pin is given as a positive value. Current out of a pin is given as a negative value.

Note 6: Output rise and fall times are measured between the 10% and 90% power supply levels.

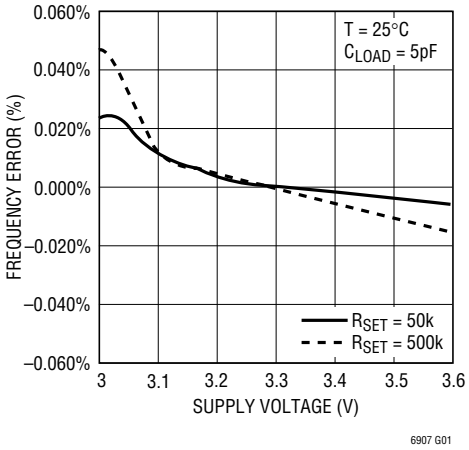
Note 7: The LTC6907C is guaranteed to meet specified performance from 0°C to 70°C. The LTC6907C is designed, characterized and expected to meet specified performance from –40°C to 85°C but is not tested or QA sampled at these temperatures. The LTC6907I is guaranteed to meet specified performance from –40°C to 85°C.

Note 8: Consult the Applications Information section for operation with supplies higher than 3.6V.

Note 9: Long term drift on silicon oscillators is primarily due to the movement of ions and impurities within the silicon and is tested at 30°C under otherwise nominal operating conditions. Long term drift is specified as ppm/$\sqrt{kHr}$ due to the typically non-linear nature of the drift. To calculate drift for a set time period, translate that time into thousands of hours, take the square root and multiply by the typical drift number. For instance, a year is 8.77kHr and would yield a drift of 888ppm at 300ppm/$\sqrt{kHr}$. Ten years is 87.7kHr and would yield a drift of 2,809 ppm at 300 ppm/$\sqrt{kHr}$. Drift without power applied to the device may be approximated as 1/10^{th} of the drift with power, or 30ppm/$\sqrt{kHr}$ for a 300ppm/$\sqrt{kHr}$ device.

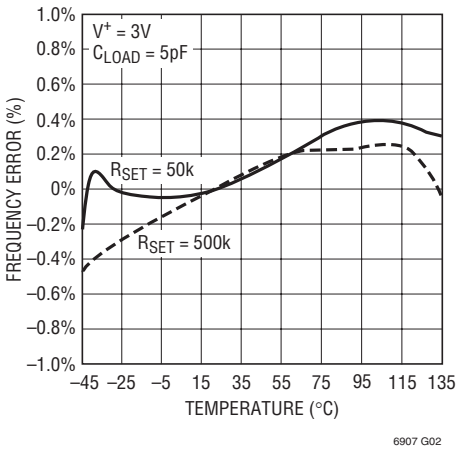
TYPICAL PERFORMANCE CHARACTERISTICS

Typical Frequency Error vs Power Supply Voltage



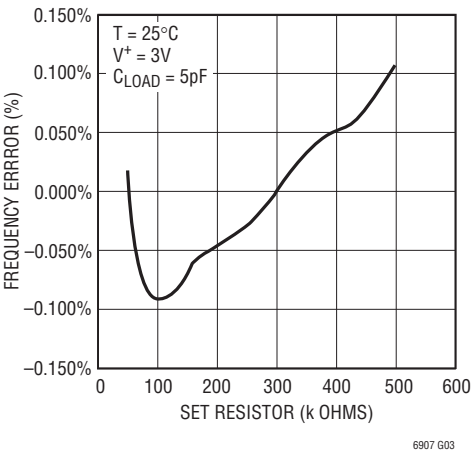
6907 G01

Typical Frequency Error vs Temperature



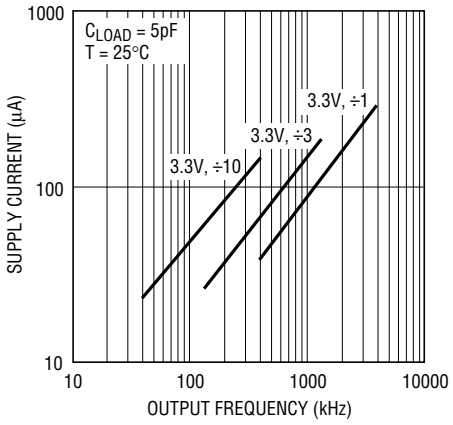
6907 G02

Typical Frequency Error vs R_{SET}



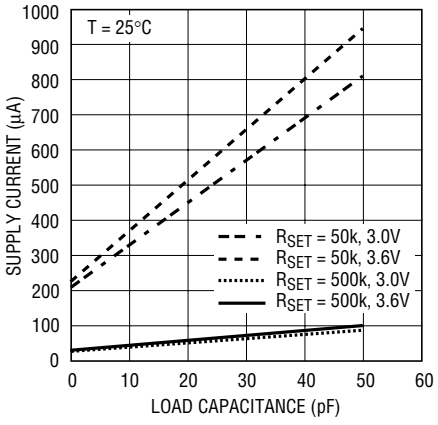
6907 G03

Typical Supply Current vs Frequency



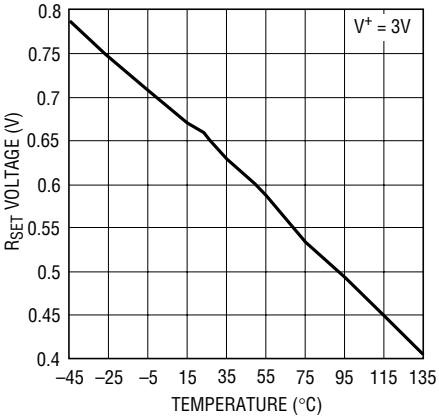
6907 G04

Typical Supply Current vs Load Capacitance



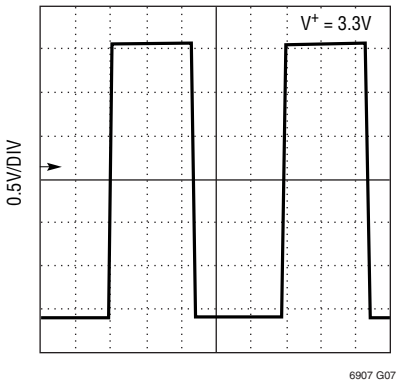
6907 G05

V_{SET} vs Temperature (V_{SET} is the Voltage Measured at the SET Pin)



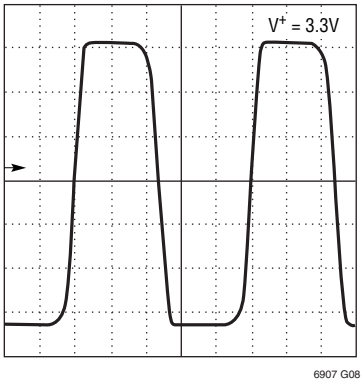
6907 G06

Output Waveform, 400kHz



6907 G07

Output Waveform, 4MHz



6907 G08

PIN FUNCTIONS

OUT (Pin 1): Oscillator Output. The OUT pin swings from GND to V^+ with an output resistance of approximately 150Ω. For micropower operation, the load resistance must be kept as high as possible and the load capacitance as low as possible.

GND (Pin 2): Ground.

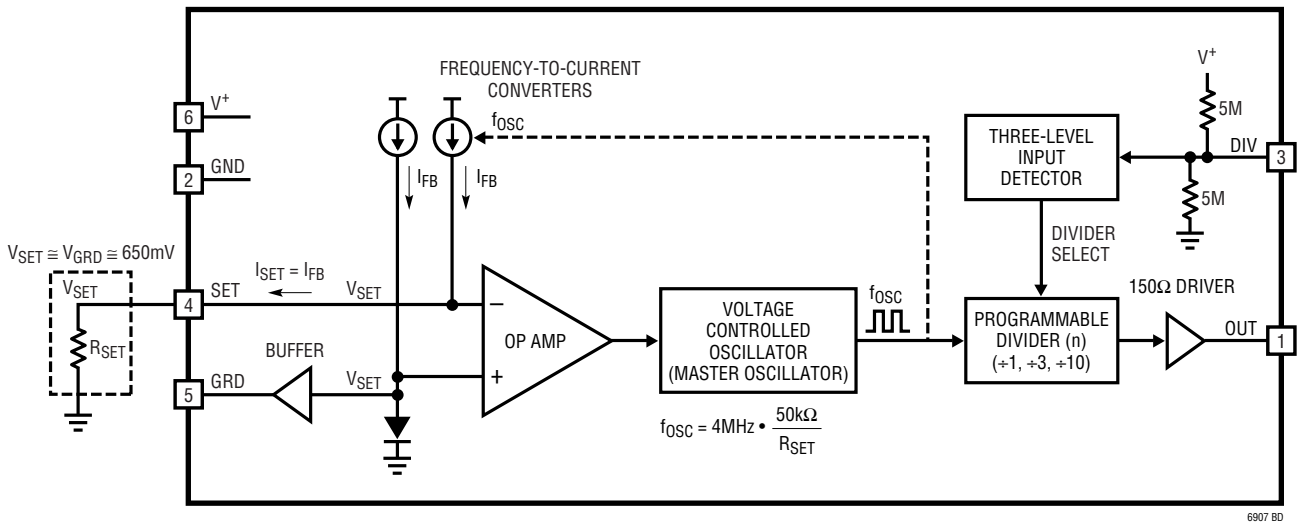
DIV (Pin 3): Divider Setting Input. This three-level input selects one of three internal digital divider settings, determining the value of N in the frequency equation. Tie to GND for ÷1, leave floating for ÷3 and tie to V^+ for ÷10. When left floating, the LTC6907 pulls Pin 3 to mid-supply with a 2.5M resistor. When Pin 3 is floating, care should be taken to reduce coupling from the OUT pin and its trace to Pin 3. Coupling can be reduced by increasing the physical space between traces or by shielding the DIV pin with grounded metal.

SET (Pin 4): Frequency Setting Resistor Input. Connect a resistor, R_{SET}, from this pin to GND to set the oscillator frequency. For best performance use a precision metal or thin-film resistor of 0.1% or better tolerance and 50ppm/°C or better temperature coefficient. For lower accuracy applications, an inexpensive 1% thick-film resistor may be used. Limit the capacitance in parallel with R_{SET} to less than 10pF to reduce jitter and to ensure stability. The voltage on the SET pin is approximately 650mV at 25°C and decreases with temperature by about –2.3mV/°C.

GRD (Pin 5): Guard Signal. This pin can be used to reduce PC board leakage across the frequency setting resistor, R_{SET}. The GRD pin is held within a few millivolts of the SET pin and shunts leakage current away from the SET pin. To control leakage, connect a bare copper trace (a trace with no solder mask) to GRD and loop it around the SET pin and all PC board metal connected to SET. Careful attention to board layout and assembly can prevent leakage currents. The use of a guard ring provides additional shielding of leakage currents from the SET pin and is optional. If unused, the GRD pin should be left unconnected.

V^+ (Pin 6): Voltage Supply (3V to 3.6V). A 0.1µF decoupling capacitor should be placed as close as possible to this pin for best performance.

BLOCK DIAGRAM



TEST CIRCUIT

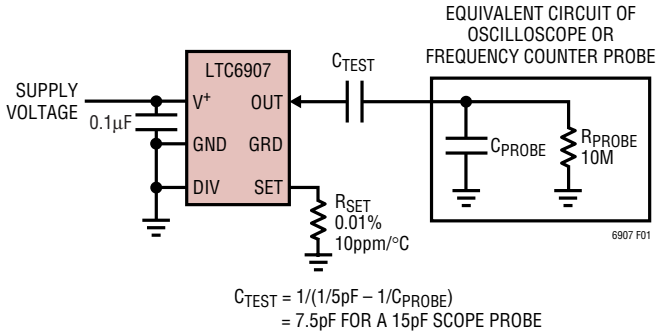


Figure 1. Test Circuit with 5pF Effective Load

EQUIVALENT INPUT AND OUTPUT CIRCUITS

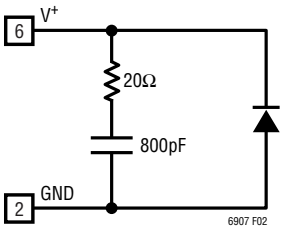


Figure 2. V+ Pin

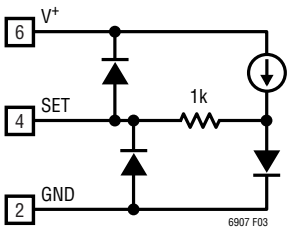


Figure 3. SET Pin

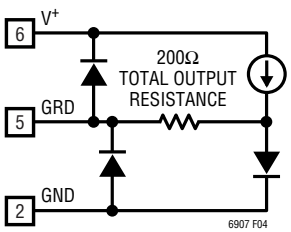


Figure 4. GRD Pin

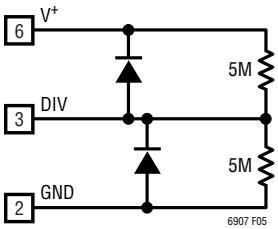


Figure 5. DIV Pin

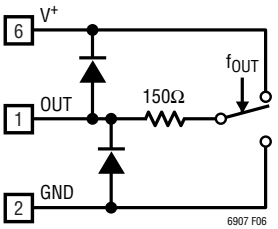


Figure 6. OUT Pin

THEORY OF OPERATION

The LTC6907 is a precision, resistor programmable oscillator (see Block Diagram). It generates a square wave at the OUT pin with a period directly proportional to the value of an external resistor, R_{SET}. A feedback circuit measures and controls the oscillator frequency to achieve the highest possible accuracy. In equilibrum, this circuit ensures that the current in the SET pin, I_{SET}, is balanced by I_{FB}. I_{FB} is proportional to the master oscillator frequency, so we have the relationship:

$$I_{SET} = I_{FB} = V_{SET} \bullet f_{OSC} \bullet C_{OSC} \quad (1)$$

Where C_{OSC} is a precision internal capacitor:

C_{OSC} = 5pF for the LTC6907

Solving for the oscillator period:

$$t_{OSC} = \frac{1}{f_{OSC}} = \frac{V_{SET}}{I_{SET}} \bullet C_{OSC} \quad (2)$$

This is the fundamental equation for the LTC6907. It holds regardless of how the SET pin is driven. When a resistor, R_{SET}, is connected from the SET pin to ground, we have the relationship:

$$\frac{V_{SET}}{I_{SET}} = R_{SET} \quad (3)$$

so

$$t_{OSC} = \frac{1}{f_{OSC}} = R_{SET} \bullet C_{OSC} \quad (4)$$

The period and frequency are determined exclusively by R_{SET} and the precision internal capacitor. Importantly, the value of V_{SET} is immaterial, and the LTC6907 maintains its accuracy even though V_{SET} is not a precision reference voltage.

The digital dividers shown in the Block Diagram further divide the master oscillator frequency by 1, 3 or 10 producing:

$$f_{OUT} = \frac{f_{OSC}}{N} \quad (5)$$

and

$$t_{OUT} = N \bullet t_{OSC} \quad (6)$$

Table 1 gives specific frequency and period equations for the LTC6907. The Applications Information section gives further detail and discusses alternative ways of setting the LTC6907 output frequency.

Table 1. Output Frequency Equations

PART NUMBER	FREQUENCY	PERIOD	DIVIDER RATIOS
LTC6907	$f_{OUT} = \frac{4MHz}{N} \bullet \left(\frac{50k}{R_{SET}}\right)$	$t_{OUT} = N \bullet 250ns \bullet \left(\frac{R_{SET}}{50k}\right)$	$N = \begin{cases} 10, & DIV\ Pin = V^+ \\ 3, & DIV\ Pin = Open \\ 1, & DIV\ Pin = GND \end{cases}$

APPLICATIONS INFORMATION

Selecting R_{SET} and the Divider Ratio

The LTC6907 contains a master oscillator followed by a digital divider (see Block Diagram). R_{SET} determines the master oscillator frequency and the three level DIV pin sets the divider ratio, N. The range of frequencies accessible in each divider ratio overlap, as shown in Figure 7. This figure is derived from the equations in Table 1. ***For any given frequency, power can be minimized by minimizing the master oscillator frequency. This implies maximizing R_{SET} and using the lowest possible divider ratio, N***. The relationship between R_{SET}, N and the unloaded power consumption is shown in Figure 8. The supply current decreases for large values of R_{SET}. Refer to the section titled "Jitter and Divide Ratio."

Minimizing Power Consumption

The supply current of the LTC6907 has four current components:

- Constant (Independent V^+, f_{OUT} and C_{LOAD})
- Proportional to I_{SET} (which is the current in R_{SET})
- Proportional to V^+, f_{OUT} and C_{LOAD}
- Proportional to V^+ and R_{LOAD}

An approximate expression for the total supply current is:

$$I^+ \cong 7\mu A + 6 \bullet I_{SET} + V^+ \bullet f_{OUT} \bullet (C_{LOAD} + 5pF) + \frac{V^+}{2 \bullet R_{LOAD}}$$

or, in terms of V_{SET},

$$I^+ \cong 7\mu A + 6 \bullet \frac{V_{SET}}{R_{SET}} + V^+ \bullet f_{OUT} \bullet (C_{LOAD} + 5pF) + \frac{V^+}{2 \bullet R_{LOAD}}$$

V_{SET} is approximately 650mV at 25°C, but varies with temperature. This behavior is shown in the Typical Performance Characteristics.

Power can be minimized by maximizing R_{SET}, minimizing the load on the OUT pin and operating at lower frequencies. Figure 9 shows total supply current vs frequency under typical conditions. Below 100kHz the load current is negligible for the 5pF load shown.

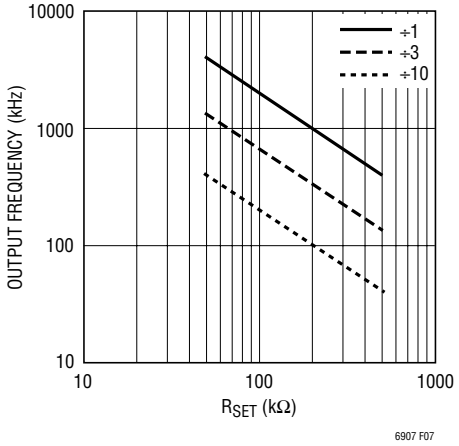


Figure 7. R_{SET} vs Desired Output Frequency

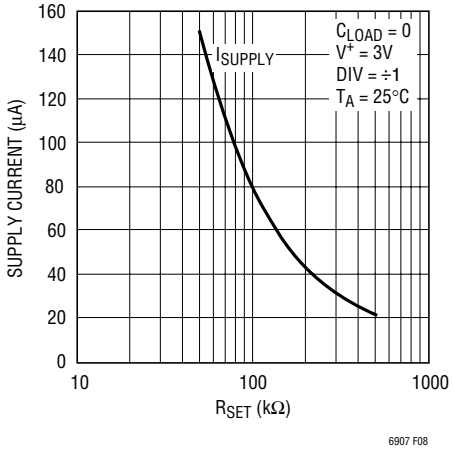


Figure 8. Unloaded Supply Current vs R_{SET}

Guarding Against PC Board Leakage

The LTC6907 uses relatively large resistance values for R_{SET} to minimize power consumption. For R_{SET} = 500k, the SET pin current is typically only 13µA. Thus, only 13nA leaking into the SET pin causes a 0.1% frequency error. Similarly, 500M of leakage resistance across R_{SET} (1000 • R_{SET}) causes the same 0.1% error.

Achieving the highest accuracy requires controlling potential leakage paths. PC board leakage is aggravated by both dirt and moisture. Effective cleaning is a good first step to minimizing leakage.

Another effective method for controlling leakage is to shunt the leakage current away from the sensitive node through a low impedance path. The LTC6907 provides a signal on the GRD pin for this purpose. Figure 10 shows a PC board

APPLICATIONS INFORMATION

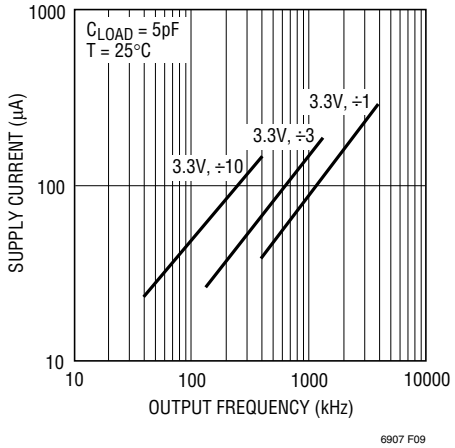


Figure 9. Supply Current vs Frequency over DIV Settings

layout that uses the GRD pin and a "guard ring" to absorb leakage currents. The guard ring surrounds the SET pin and the end of R_{SET} to which it is connected. The guard ring must have no solder mask covering it to be effective. The GRD pin voltage is held within a few millivolts of the SET pin voltage, so any leakage path between the SET pin and the guard ring generates no leakage current.

Start-Up Time

When the LTC6907 is powered up, it holds the OUT pin low. After the master oscillator has settled, the OUT pin is enabled and the first output cycle is accurate. The time from power-up to the first output transition is given approximately by:

$$t_{START} \cong 64 \bullet t_{OSC} + 100\mu s$$

The digital divider ratio, N, does not affect the start-up time.

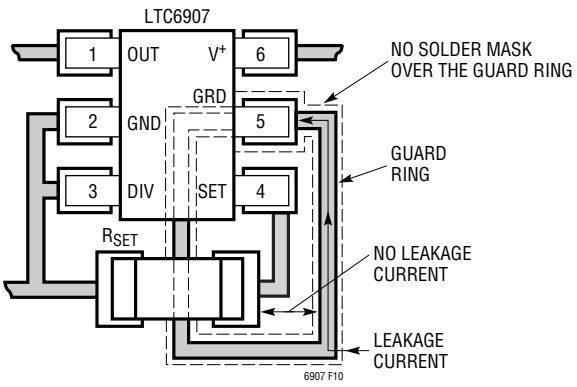


Figure 10. PC Board Layout with Guard Ring

Power Supply Rejection

The LTC6907 has a very low supply voltage coefficient, meaning that the output frequency is nearly insensitive to the DC power supply voltage. In most cases, this error term can be neglected.

High frequency noise on the power supply (V^+) pin has the potential to interfere with the LTC6907's master oscillator. Periodic noise, such as that generated by a switching power supply, can shift the output frequency or increase jitter. The risk increases when the fundamental frequency or harmonics of the noise fall near the master oscillator frequency. It is relatively easy to filter the LTC6907 power supply because of the very low supply current. For example, an RC filter with R = 160Ω and C = 10µF provides a 100Hz lowpass filter while dropping the supply voltage only about 10mV.

Operating the LTC6907 with Supplies Higher Than 3.6V

The LTC6907 may also be used with supply voltages between 3.6V and 5.5V under very specific conditions. To ensure proper functioning above 3.6V, a filter circuit must be attached to the power supply and located within 1cm of the device. A simple RC filter consisting of a 100Ω resistor and 1µF capacitor (Figure 11) will ensure that supply resonance at higher supply voltages does not induce unpredictable oscillator behavior. Accuracy under higher supplies may be estimated from the typical Frequency vs Supply Voltage curves in the Typical Performance Characteristics section of this data sheet.

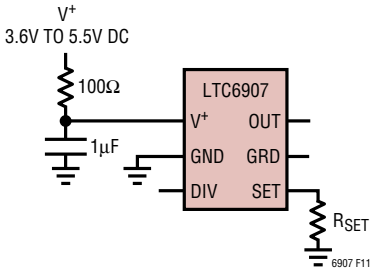


Figure 11. Using the LTC6907 at Higher Supply Voltages

APPLICATIONS INFORMATION

Alternative Methods for Setting the Output Frequency

Any means of sinking current from the SET pin will control the output frequency of the LTC6907. Equation 2 (repeated below) gives the fundamental relationship between frequency and the SET pin voltage and current:

$$t_{OSC} = \frac{1}{f_{OSC}} = \frac{V_{SET}}{I_{SET}} \bullet 5pF \quad (2)$$

This equation shows that the LTC6907 converts conductance (I_{SET}/V_{SET}) to frequency or, equivalently, converts resistance ($R_{SET} = V_{SET}/I_{SET}$) to period.

V_{SET} is the voltage across an internal diode, and as such it is given approximately by:

$$V_{SET} \cong V_T \bullet Log_e \frac{I_{SET}}{I_S}$$

$$\cong 25.9mV \bullet Log_e \left(\frac{I_{SET}}{82 \bullet 10^{-18} A} \right) - 2.3mV/°C$$

where

$V_T = kT/q = 25.9mV$ at $T = 300°K$ (27°C)

$I_S \cong 82 \bullet 10^{-18}$ Amps

(I_S is also temperature dependent)

V_{SET} varies with temperature and the SET pin current. The response of V_{SET} to temperature is shown in the Typical Performance graphs. V_{SET} changes approximately –2.3mV/°C. At room temperature V_{SET} increases 18mV/octave or 60mV/decade of increase in I_{SET}.

If the SET pin is driven with a current source generating I_{SET}, the oscillator output frequency will be:

$$f_{OSC} \cong \frac{\frac{I_{SET}}{5pF}}{25.9mV \bullet Log_e \left(\frac{I_{SET}}{82 \bullet 10^{-18} A} \right) - 2.3mV/°C}$$

Figure 12 and Figure 13 show a current controlled oscillator and a voltage controlled oscillator. These circuits are not highly accurate if used alone, but can be very useful if they are enclosed in an overall feedback circuit such as a phase-locked loop.

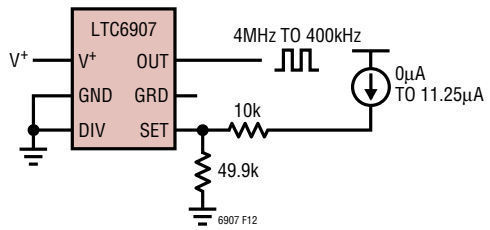


Figure 12. Current Controlled Oscillator

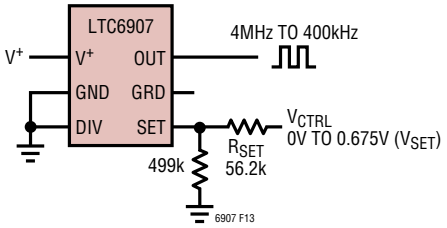


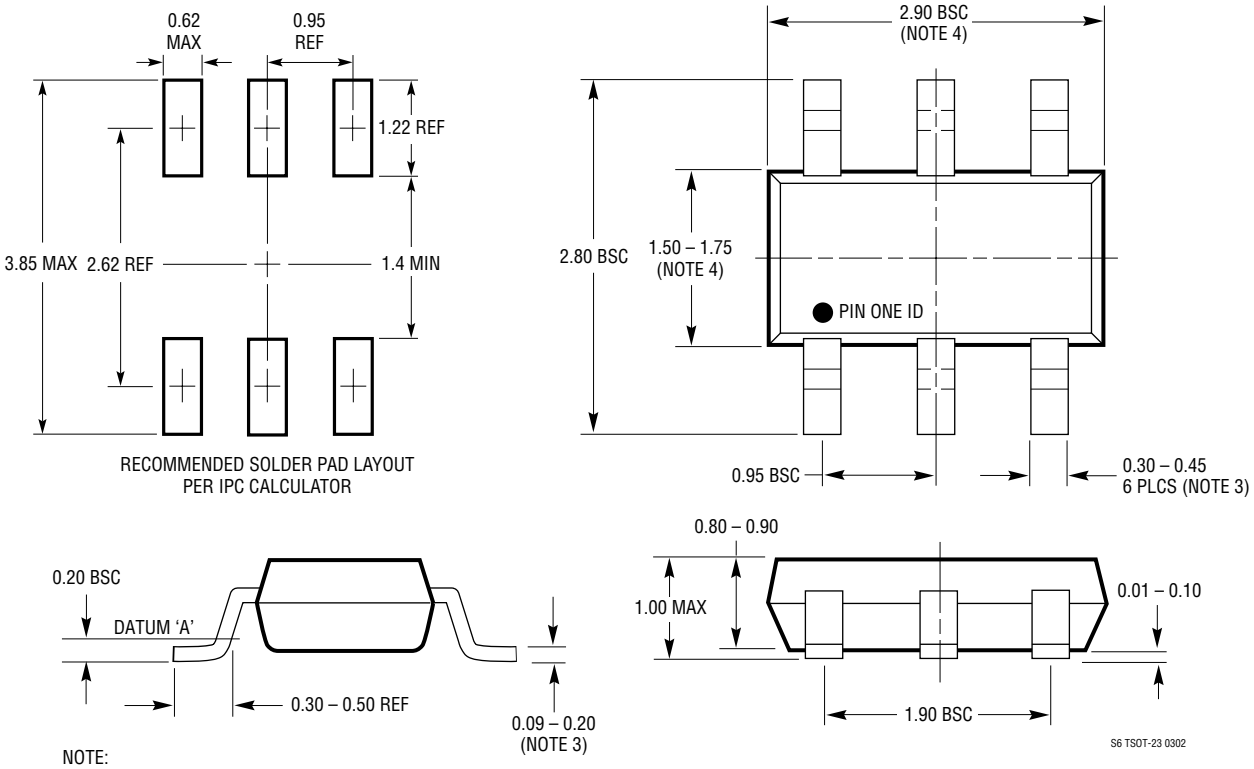
Figure 13. Voltage Controlled Oscillator

Jitter and Divide Ratio

At a given output frequency, a higher master oscillator frequency and a higher divide ratio will result in lower jitter and higher power supply dissipation. Indeterminate jitter percentage will decrease by a factor of slightly less than the square root of the divider ratio, while determinate jitter will not be similarly attenuated. Please consult the specification tables for typical jitter at various divider ratios.

PACKAGE DESCRIPTION

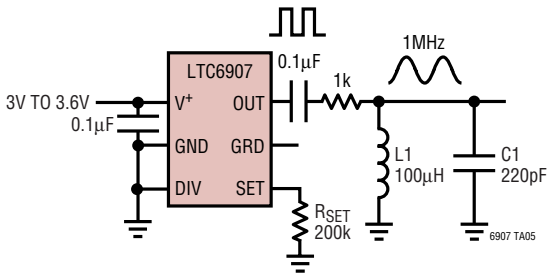
S6 Package
6-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1636)



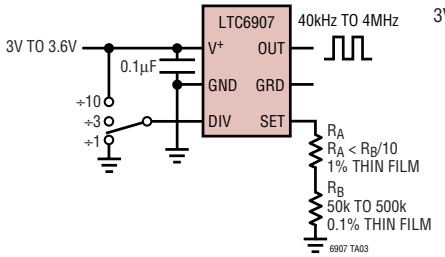
NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

TYPICAL APPLICATIONS

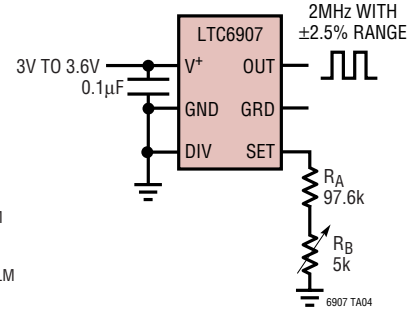
Sine Wave Oscillator



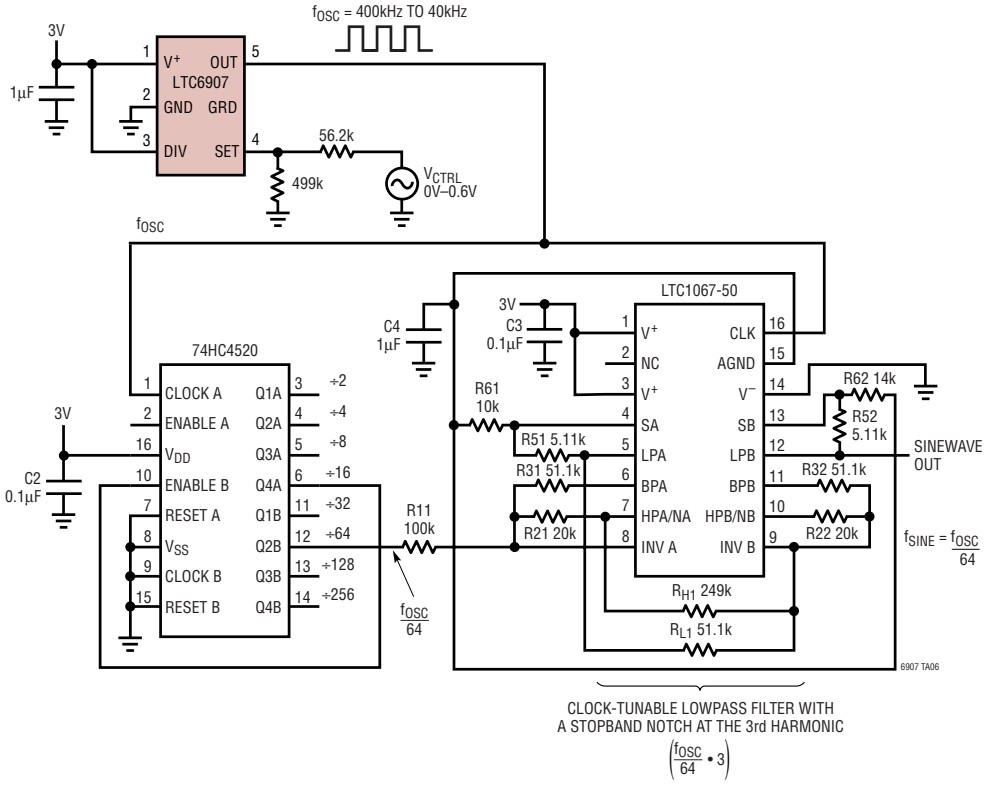
Setting Frequency to 0.1% Resolution with Standard Resistors



Trimming the Frequency



Low Power 62.5Hz to 6.25kHz Sine Wave Generator (I_Q < 1.5mA)



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1799	1kHz to 33MHz ThinSOT Oscillator, Resistor Set	Wide Frequency Range
LTC6900	1kHz to 20MHz ThinSOT Oscillator, Resistor Set	Low Power, Wide Frequency Range
LTC6902	Multiphase Oscillator with Spread Spectrum Modulation	2-, 3- or 4-Phase Outputs
LTC6903/LTC6904	1kHz to 68MHz Serial Port Programmable Oscillator	0.1% Frequency Resolution, I²C or SPI Interface
LTC6905	17MHz to 170MHz ThinSOT Oscillator, Resistor Set	High Frequency, 100µsec Startup, 7ps RMS Jitter
LTC6905-XXX	Fixed Frequency ThinSOT Oscillator Family, up to 133MHz	No Trim Components Required
LTC6906	Micropower 10kHz to 1MHz ThinSOT Oscillator, Resistor Set	12µA Supply Current of 100kHz, 0.65% Frequency Accuracy

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