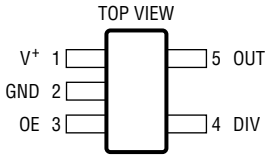
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V^+) to GND ..... –0.3V to 6V
DIV to GND ..... –0.3V to (V^+ + 0.3V)
OE to GND ..... –0.3V to (V^+ + 0.3V)
Output Short-Circuit Duration (Note 6) ..... Indefinite
Operating Temperature Range (Note 8)
LTC6905C ..... –40°C to 85°C
LTC6905I ..... –40°C to 85°C
LTC6905H ..... –40°C to 125°C
Specified Temperature Range (Note 8)
LTC6905C ..... 0°C to 70°C
LTC6905I ..... –40°C to 85°C
LTC6905H ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



S5 PACKAGE
5-LEAD PLASTIC SOT-23

T_{JMAX} = 125°C, θ_{JA} = 150°C/W

ORDER PART NUMBER	S5 PART MARKING*
LTC6905CS5-133 LTC6905IS5-133 LTC6905HS5-133	LTBPM LTBPM LTBPM
LTC6905CS5-100 LTC6905IS5-100 LTC6905HS5-100	LTBPK LTBPK LTBPK
LTC6905CS5-96 LTC6905IS5-96 LTC6905HS5-96	LTBPJ LTBPJ LTBPJ
LTC6905CS5-80 LTC6905IS5-80 LTC6905HS5-80	LTBPH LTBPH LTBPH

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

*The temperature grade is identified by a label on the shipping container.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full specified temperature range, otherwise specifications are at T_A = 25°C or as noted. OE = DIV = V^+, V^+ = 2.7V to 3.6V, R_L = 15k, C_L = 5pF, unless otherwise noted. All voltages are with respect to GND.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Δf	Frequency Accuracy (Notes 2, 7)	LTC6905C-XXX					
		T_A = 25°C, V^+ = 3V			±0.5	±1.0	%
		0°C < T_A < 70°C	●			±1.5	%
		LTC6905I-XXX					
		25°C < T_A < 85°C				±1.8	%
		–40°C < T_A < 85°C	●			±2.9	%
		LTC6905H-XXX					
		25°C < T_A < 125°C				±2.3	%
		–40°C < T_A < 125°C	●			±2.9	%
		V^+ = 5V			±1.5		%
Δf/ΔT	Freq Drift Over Temp (Note 2)		●		±20		ppm/°C
Δf/ΔV	Freq Drift Over Supply (Notes 2, 7)	V^+ = 2.7V to 3.6V			0.5		%/V
	Timing Jitter (Note 3)				0.8		%
	Long-Term Stability of Output Frequency				300		ppm/√kHr

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full specified temperature range, otherwise specifications are at T_A = 25°C or as noted. OE = DIV = V+, V+ = 2.7V to 3.6V, R_L = 15k, C_L = 5pF, unless otherwise noted. All voltages are with respect to GND.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Duty Cycle	DIV = 0V	●	47.5	50	52.5	%
V^+	Operating Supply Range		●	2.7		5.5	V
I_S	Power Supply Current	DIV = V^+ (÷ 1), V^+ = 3.6V					
		LTC6905-133	●		10	15	mA
		LTC6905-100	●		8	12	mA
		LTC6905-96	●		8	12	mA
		LTC6905-80	●		7	11	mA
		DIV = 0 (÷ 4), V^+ = 3.6V					
		LTC6905-133	●		5	8	mA
		LTC6905-100	●		4	7	mA
		LTC6905-96	●		4	7	mA
		LTC6905-80	●		3.5	6	mA
V_{IH}	High Level DIV or OE Pins Input Voltage		●	V^+ – 0.15			V
V_{IL}	Low Level DIV or OE Pins Input Voltage		●			0.2	V
I_{DIV}	DIV Input Current (Note 4)	DIV = V^+ V^+ = 5.5V	●		15	40	µA
		DIV = 0V V^+ = 5.5V	●	–40	–11		µA
I_{OE}	OE Input Current (Note 4)	OE = V^+ V^+ = 5.5V			15		µA
		OE = 0V V^+ = 5.5V			–11		µA
V_{OH}	High Level Output Voltage (Note 4)	V^+ = 5.5V I_{OH} = –1mA	●	5.25	5.45		V
		I_{OH} = –4mA	●	5.20	5.30		V
		V^+ = 2.7V I_{OH} = –1mA	●	2.5	2.6		V
		I_{OH} = –4mA	●	2.3	2.5		V
V_{OL}	Low Level Output Voltage (Note 4)	V^+ = 5.5V I_{OL} = 1mA	●		0.05	0.25	V
		I_{OL} = 4mA	●		0.2	0.3	V
		V^+ = 2.7V I_{OL} = 1mA	●		0.1	0.3	V
		I_{OL} = 4mA	●		0.4	0.5	V
t_r, t_f	OUT Rise/Fall Time (Note 5)				0.5		ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: Frequency accuracy is tested with DIV = V^+ (÷1). Other divide ratios are guaranteed by design.

Note 3: Jitter is the ratio of the peak-to-peak distribution of the period to the mean of the period. This specification is based on characterization and is not 100% tested.

Note 4: To conform with the Logic IC Standard convention, current out of a pin is arbitrarily given as a negative value.

Note 5: Output rise and fall times are measured between the 10% and 90% power supply levels.

Note 6: A heat sink may be required to keep the junction temperature below the absolute maximum when the output is shorted indefinitely.

Note 7: The LTC6905 is optimized for the performance with a 3V power supply voltage. Refer to Typical Performance Characteristics curves in this data sheet for additional information regarding the LTC6905 voltage coefficient, especially between 4.5V and 5.5V. Please consult LTC Marketing for parts optimized for 5V operation.

Note 8: The LTC6905C-XXX is guaranteed functional over the operating temperature range and is guaranteed to meet specified performance from 0°C to 70°C. The LTC6905C-XXX is designed, characterized and expected to meet specified performance from –40°C to 85°C but is not tested or QA sampled at these temperatures. The LTC6905I-XXX is guaranteed to meet specified performance from –40°C to 85°C.

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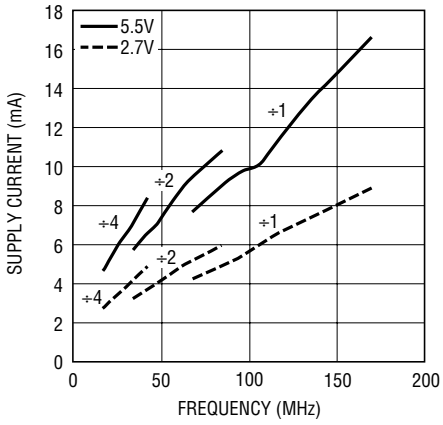
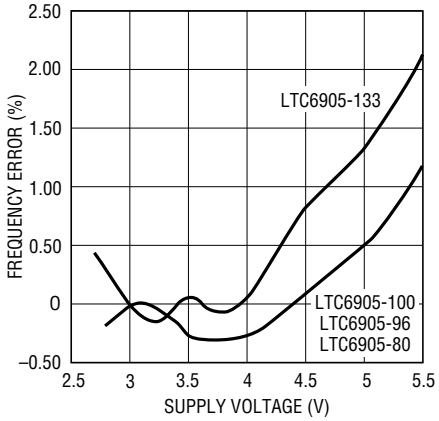
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Frequency



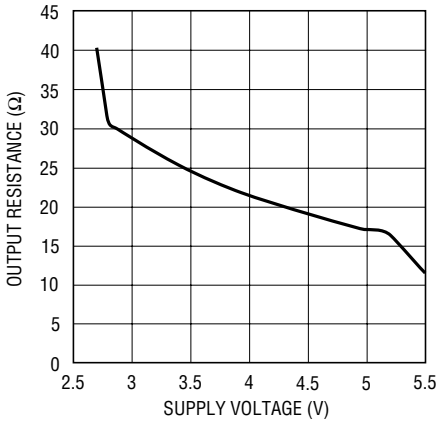
6905x G01

Frequency Error vs Supply Voltage



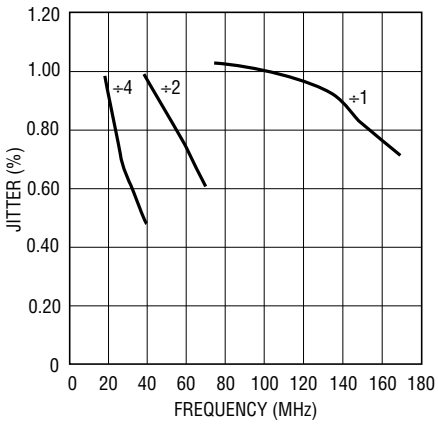
6905x G09

R_{OUT} vs V^+



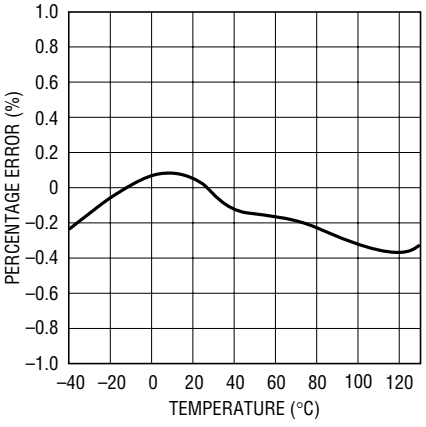
6905x G04

Jitter vs Frequency



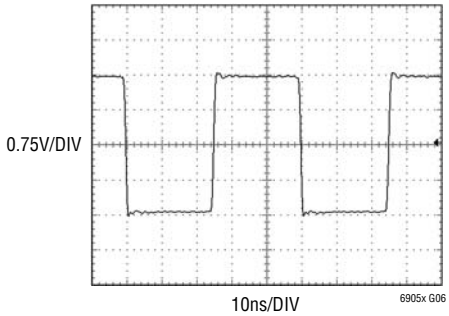
6905x G05

Frequency vs Temperature



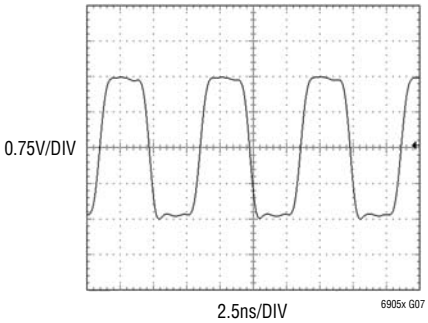
6905x G08

LTC6905-80 Output Operating at 20MHz, V_S = 3V



6905x G06

LTC6905-133 Output Operating at 133MHz, V_S = 3V



6905x G07

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PIN FUNCTIONS

V+ (Pin 1): Voltage Supply (2.7V ≤ V+ ≤ 5.5V). This supply must be kept free from noise and ripple. It should be bypassed directly to the GND (Pin 2) with a 0.1µF capacitor or higher.

GND (Pin 2): Ground. Should be tied to a ground plane for best performance.

OE (Pin 3): Output Enable. Pull to V+ or leave floating to enable the output driver (Pin 5). Pull low to disable the output. The output is disabled asynchronously. Pulling OE pin low will immediately disable the output. Pulling the OE pin high will bring the output high on the next low to high transition of the clock. This eliminates pulse slivers.

DIV (Pin 4): Divider-Setting Input. This three-state input selects among three divider settings. Pin 4 should be tied to V+ for the ÷1 setting, the highest frequency range. Floating Pin 4 divides the master oscillator by 2. Pin 4 should be tied to GND for the ÷4 setting, the lowest frequency range. To detect a floating DIV pin, the LTC6905 attempts to pull the pin toward midsupply. This is realized with two internal current sources, one tied to V+ and Pin 4 and the other one tied to ground and Pin 4. Therefore, driving the DIV pin high requires sourcing approximately 15µA. Likewise, driving DIV low requires sinking 15µA. When Pin 4 is floated, it should be bypassed by a 1nF capacitor to ground or it should be surrounded by a ground shield to prevent excessive coupling from other PCB traces.

OUT (Pin 5): Oscillator Output. This pin can drive 5kΩ and/or 5pF loads. For heavier loads, refer to the Applications Information section.

BLOCK DIAGRAM

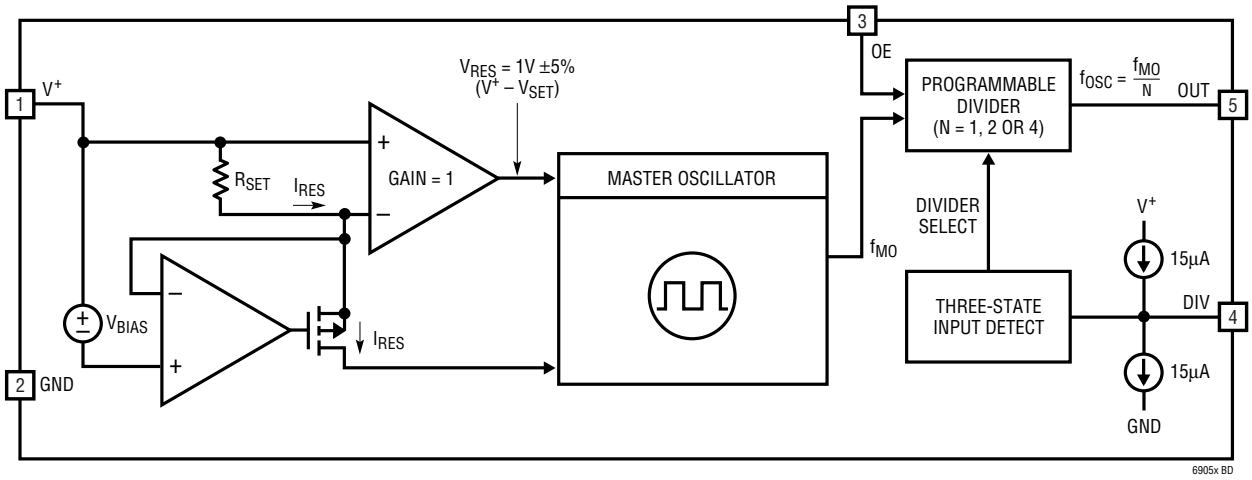

Table 1. LTC6905-XXX Frequency Settings

DIV SETTING	LTC6905-133	LTC6905-100	LTC6905-96	LTC6905-80
V+	133.33MHz	100MHz	96MHz	80MHz
OPEN	66.66MHz	50MHz	48MHz	40MHz
GND	33.33MHz	25MHz	24MHz	20MHz

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APPLICATIONS INFORMATION

START-UP TIME

The start-up and settling time to within 1% of the final frequency is typically 100µs.

MAXIMUM OUTPUT LOAD

The LTC6905 output (Pin 5) can drive a capacitive load (C_{LOAD}) of 5pF or more. Performance driving a C_{LOAD} greater than 5pF depends on the oscillator's frequency (f_{OSC}) and output resistance (R_{OUT}). The output rise time or fall time due to R_{OUT} and C_{LOAD} is equal to $2.2 \bullet R_{OUT} \bullet C_{LOAD}$ (from 10% to 90% of the rise or fall transition). If the total output rise time plus fall time is arbitrarily specified to be equal to or less than 20% of the oscillator's period ($1/f_{OSC}$), then the maximum output C_{LOAD} in picofarads (pF) should be equal to or less than $[45454/(R_{OUT} \bullet f_{OSC})]$ (R_{OUT} in ohms and f_{OSC} in MHz).

Example: An LTC6905-100 is operating with a 3V power supply and is set for a f_{OSC} = 50MHz.

R_{OUT} with V^+ = 3V is 27Ω (using the R_{OUT} vs V^+ graph in the Typical Performance Characteristics).

The maximum output C_{LOAD} should be equal to or less than $[45454/(27 \bullet 50)]$ = 33.6pF.

The lowest resistive load Pin 5 can drive can be calculated using the minimum high level output voltage in the Electrical Characteristics. With a V^+ equal to 5.5V and 4mA output current, the minimum high level output voltage is 5.2V and the lowest resistive load Pin 5 can drive is 1.30k (5.2V/4mA). With a V^+ equal to 2.7V and 4mA output current, the minimum high level output voltage is 2.4V and the lowest resistive load Pin 5 can drive is 600Ω (2.4V/4mA).

FREQUENCY ACCURACY AND POWER SUPPLY NOISE

The frequency accuracy of the LTC6905 may be affected when its power supply generates noise with frequency contents equal to $f_{MO}/64$ or its multiples. f_{MO} is the highest frequency for an LTC6905-XXX which is with DIV = V^+ (÷1). This is also the frequency indicated in the part number (i.e., LTC6905-100, f_{MO} = 100MHz). $f_{MO}/64$ is the master oscillator control loop frequency. For example, if the LTC6905-80 with a master oscillator frequency of 80MHz is powered by a switching regulator, then the oscillator frequency may show an additional error if the switching frequency is 1.4MHz (80MHz/64). The magnitude of this effect is heavily dependent on supply bypass and routing.

JITTER AND POWER SUPPLY NOISE

If the LTC6905 is powered by a supply that has frequency content equal to the output frequency then the output jitter may increase. In addition, power supply ripple in excess of 20mV at any frequency may increase jitter.

Higher divide ratios will result in lower percentage jitter. For example, jitter percentage of the LTC6905-80 operating at 20MHz is lower than for the same part operating at 80MHz. Please consult the Jitter vs Frequency graph showing jitter at various divider ratios.

LTC6905 SUGGESTED CRITICAL COMPONENT LAYOUT

In order to provide the specified performance, it is required that the supply bypass capacitor be placed as close as possible to the LTC6905. The following additional rules should be followed for best performance:

1) The bypass capacitor must be placed as close as possible to the LTC6905, and no vias should be placed between the capacitor and the LTC6905. The bypass capacitor must be on the same side of the circuit board as the LTC6905.

2) If a ground plane is used, the connection of the LTC6905 to the ground plane should be as close as possible to the LTC6905 GND pin and should be composed of multiple, high current capacity vias.

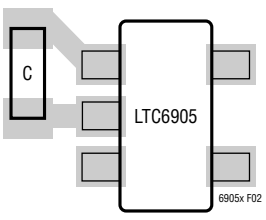

Figure 2. LTC6905 Suggested Critical Component Layout

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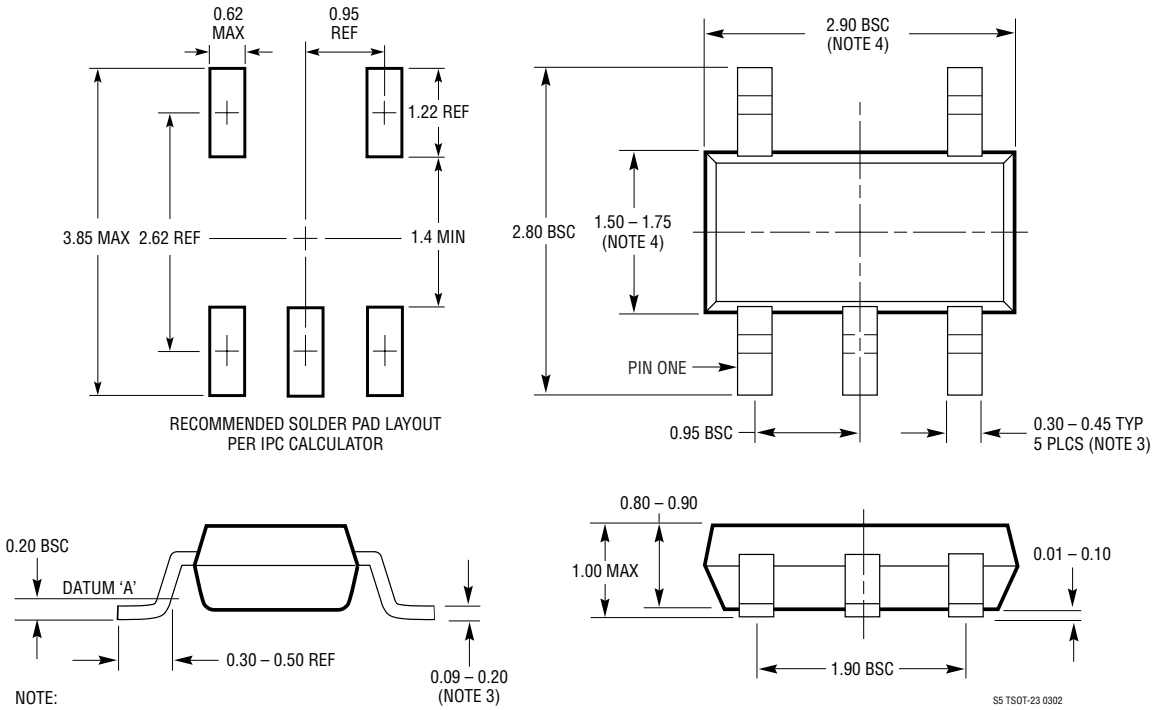
PACKAGE DESCRIPTION

S5 Package
5-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1635)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

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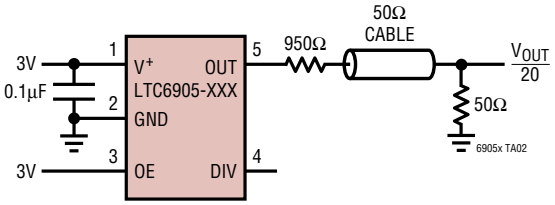
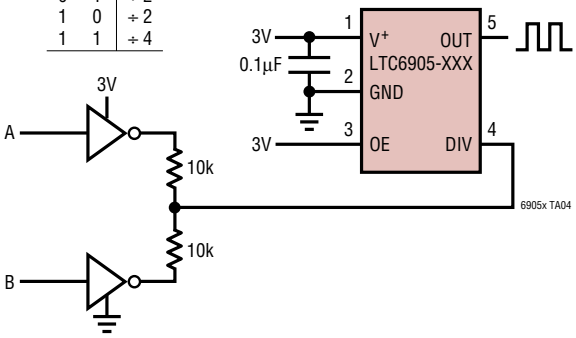
TYPICAL APPLICATIONS

Driving a 50Ω Cable with the LTC6905



Driving the DIV Pin Without Three-State Buffers

A	B	DIV
0	0	÷1
0	1	÷2
1	0	÷2
1	1	÷4



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1799	1kHz to 33MHz ThinSOT Oscillator	Single Output, High Frequency Operation
LTC6900	1kHz to 20MHz ThinSOT Oscillator	Single Output Lower Power
LTC6902	Multiphase Oscillator with Spread Spectrum Modulation	2-, 3- or 4-Phase Outputs
LTC6903/LTC6904	1kHz to 68MHz Serial Port Programmable Oscillator	3-Wire or I²C™ Programmable
LTC6905	17MHz to 170MHz Resistor Set ThinSOT Oscillator	Single Resistor Sets Frequency
LTC6906	Micropower, 10kHz to 1MHz Resistor Set ThinSOT Oscillator	Ultralow Power, Resistor Sets Frequency

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