ABSOLUTE MAXIMUM RATINGS

(Notes 1, 4)

LTC4292

Supply Voltages

AGNDP – V_{EE} ..... –0.3V to 80V

VSSK12, VSSK34 (Note 7)... V_{EE} – 0.3V to V_{EE} + 0.3V

Digital Pins

PWRMD0, PWRMD1 ..... V_{EE} – 0.3V to CAP2 + 0.3V

Analog Pins

SENSEnM, GATEnM, OUTnM V_{EE} – 0.3V to V_{EE} + 80V

CAP2 (Note 13) ..... V_{EE} – 0.3V to V_{EE} + 5V

CPA, CNA, DPA, DNA.....V_{EE} – 0.3V to V_{EE} + 0.3

Operating Ambient Temperature Range

LTC4292I .....–40°C to 85°C

Junction Temperature (Note 2) ..... 125°C

Storage Temperature Range .....–65°C to 150°C

(Note 1)

LTC4291-1

Supply Voltages

V_{DD} – DGND ..... –0.3V to 3.6V

Digital Pins

SCL, SDAIN, SDAOUT, $\overline{INT}$, $\overline{RESET}$, $\overline{MSD}$, ADn, AUTO, $\overline{4PVALID}$, GPn .....DGND – 0.3V to V_{DD} + 0.3V

Analog Pins

CAP1 (Note 13).....–0.3V to DGND + 2V

CPD, CND, DPD, DND .....DGND – 0.3V to V_{DD} + 0.3V

Operating Ambient Temperature Range

LTC4291I-1 .....–40°C to 85°C

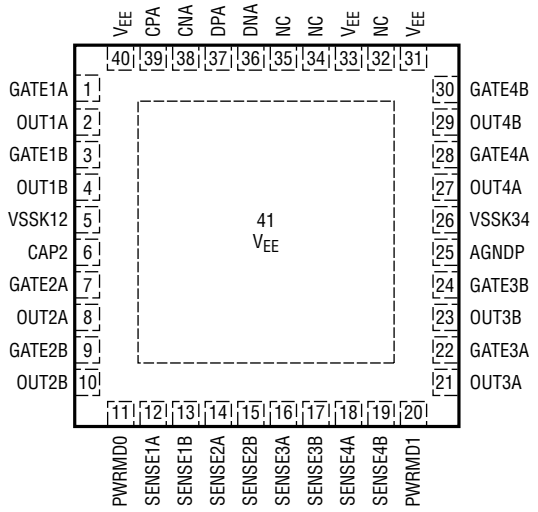
Junction Temperature (Note 2) ..... 125°C

Storage Temperature Range .....–65°C to 150°C

PIN CONFIGURATION

LTC4292

TOP VIEW



UJ PACKAGE

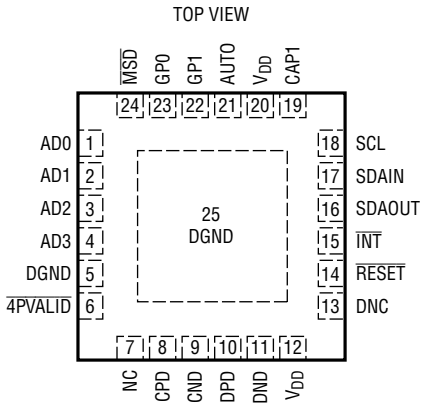
40-LEAD (6mm × 6mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JC} = 2°C/W, θ_{JA} = 33°C/W

EXPOSED PAD (PIN 41) IS V_{EE}, MUST BE SOLDERED TO PCB

LTC4291-1

TOP VIEW



UF PACKAGE

24-LEAD (4mm × 4mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JC} = 4°C/W, θ_{JA} = 47°C/W

EXPOSED PAD (PIN 25) IS DGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4291IUF-1#PBF	LTC4291IUF-1#TRPBF	42911	24-Lead (4mm × 4mm) Plastic QFN	–40°C to 85°C
LTC4292IUJ#PBF	LTC4292IUJ#TRPBF	LTC4292UJ	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 85°C

Contact the factory for parts specified with wider operating temperature ranges.
Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. AGNDP – V_{EE} = 54V and V_{DD} – DGND = 3.3V unless otherwise noted. (Notes 3 and 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Main PoE Supply Voltage	AGNDP – V_{EE} For IEEE Type 3 Compliant Output For IEEE Type 4 Compliant Output	 ● ●	 51 53		 57 57	 V V
	Undervoltage Lock-Out	AGNDP – V_{EE}	●	20	25	30	V
V_{DD}	V_{DD} Supply Voltage	V_{DD} – DGND	●	3.0	3.3	3.6	V
	Undervoltage Lock-Out	V_{DD} – DGND			2.7		V
V_{CAP1}	Internal Regulator Supply Voltage	V_{CAP1} – DGND			1.84		V
V_{CAP2}	Internal Regulator Supply Voltage	V_{CAP2} – V_{EE}			4.3		V
I_{EE}	V_{EE} Supply Current	(AGNDP – V_{EE}) = 55V	●		9	15	mA
R_{EE}	V_{EE} Supply Resistance	(AGNDP – V_{EE}) < 15V	●			12	kΩ
I_{DD}	V_{DD} Supply Current	(V_{DD} – DGND) = 3.3V	●		10	15	mA
Detection/Connection Check							
	Forced Current	First Point, AGNDP – V_{OUTnM} = 9V Second Point, AGNDP – V_{OUTnM} = 3.5V	● ●	220 143	240 160	260 180	µA µA
	Forced Voltage	AGNDP – V_{OUTnM}, 5µA ≤ I_{OUTnM} ≤ 500µA First Point Second Point	 ● ●	 7 3	 8 4	 9 5	 V V
	Detection/Connection Check Current Compliance	AGNDP – V_{OUTnM} = 0V	●		0.8	0.9	mA
V_{OC}	Detection/Connection Check Voltage Compliance	AGNDP – V_{OUTnM}, Open Port	●		10.4	12	V
	Detection/Connection Check Voltage Slew Rate	AGNDP – V_{OUTnM}, C_{PORT} = 0.15µF (Note 7)	●			0.01	V/µs
	Min. Valid Signature Resistance		●	15.5	17	18.5	kΩ
	Max. Valid Signature Resistance		●	27.5	29.7	32	kΩ

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. AGNDP – V_{EE} = 54V and V_{DD} – DGND = 3.3V unless otherwise noted. (Notes 3 and 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Classification							
V_{CLASS}	Classification Voltage	AGNDP – V_{OUTnM}, 0mA ≤ I_{OUTnM} ≤ 50mA	●	16.0		20.5	V
	Classification Current Compliance	V_{OUTnM} = AGNDP	●	53	61	67	mA
	Classification Threshold Current	Class Signature 0 – 1	●	5.5	6.5	7.5	mA
		Class Signature 1 – 2	●	13.5	14.5	15.5	mA
		Class Signature 2 – 3	●	21.5	23	24.5	mA
		Class Signature 3 – 4	●	31.5	33	34.9	mA
		Class Signature 4 – Overcurrent	●	45.2	48	50.8	mA
V_{MARK}	Classification Mark State Voltage	AGNDP – V_{OUTnM}, 0.1mA ≤ I_{CLASS} ≤ 5mA	●	7.5	9	10	V
	Mark State Current Compliance	V_{OUTnM} = AGNDP	●	53	61	67	mA
Gate Driver							
	GATE Pin Pull-Down Current	Port Off, V_{GATEnM} = V_{EE} + 5V	●	0.4			mA
		Port Off, V_{GATEnM} = V_{EE} + 1V	●	0.08	0.12		mA
	GATE Pin Fast Pull-Down Current	V_{GATEnM} = V_{EE} + 5V			30		mA
	GATE Pin On Voltage	V_{GATEnM} – V_{EE}, I_{GATEnM} = 1µA	●	8	12	14	V
Output Voltage Sense							
V_{PG}	Power Good Threshold Voltage	V_{OUTnM} – V_{EE}	●	2	2.4	2.8	V
	OUT Pin Pull-Up Resistance to AGNDP	0V ≤ (AGNDP – V_{OUTnM}) ≤ 5V	●	300	500	700	kΩ
Current Sense							
V_{CUT-2P}	Overcurrent Sense Voltage, Single-Signature PD	$V_{SENSEnM}$ – VSSKn					
		Class 1, CUT*n*[6:0] = 45h	●	13.5	14.1	14.6	mV
		Class 2, CUT*n*[6:0] = 48h	●	21.6	22.5	23.4	mV
		Class 3, CUT*n*[6:0] = 52h	●	47.5	50.5	53.5	mV
		Class 4, CUT*n*[6:0] = 62h	●	92.0	96.0	100.0	mV
		Class 5, CUT*n*[6:0] = 5Fh	●	84.0	87.0	91.0	mV
		Class 6, CUT*n*[6:0] = 67h	●	105	110	114	mV
		Class 7, CUT*n*[6:0] = 6Ch	●	119	124	129	mV
		Class 8, CUT*n*[6:0] = 74h (Note 12)	●	140	146	152	mV
	Overcurrent Sense Voltage, Dual-Signature PD	$V_{SENSEnM}$ – VSSKn					
		Class 1, CUT*n*[6:0] = 45h	●	13.5	14.1	14.6	mV
		Class 2, CUT*n*[6:0] = 48h	●	21.6	22.5	23.4	mV
		Class 3, CUT*n*[6:0] = 52h	●	47.5	50.5	53.5	mV
		Class 4, CUT*n*[6:0] = 62h	●	92.0	96.0	100.0	mV
		Class 5, CUT*n*[6:0] = 74h (Note 12)	●	140	146	152	mV
V_{LIM-2P}	Active Current Limit, Single-Signature PD	V_{OUTnM} – V_{EE} < 10V					
		Class 1 – Class 3, LIM*n* = 80h	●	61.2	63.6	67.3	mV
		Class 4 – Class 6, LIM*n* = C0h	●	122	128	135	mV
		Class 7, LIM*n* = D0h	●	153	159	169	mV
		Class 8, LIM*n* = E9h (Note 12)	●	168	175	185	mV
	Active Current Limit, Dual-Signature PD	V_{OUTnM} – V_{EE} < 10V					
		Class 1 – Class 3, LIM*n* = 80h	●	61.2	63.6	67.3	mV
		Class 4, LIM*n* = C0h	●	122	128	135	mV
		Class 5, LIM*n* = E9h (Note 12)	●	168	175	185	mV
$V_{INRUSH-2P}$	Active Current Limit, Inrush	AGNDP – V_{OUTnM} > 30V (Note 17)					
		LIMn = 80h	●	61.2	63.6	67.3	mV
		LIMn = 08h	●	30.6	31.8	33.7	mV
$V_{HOLD-2P}$	DC Disconnect Sense Voltage	$V_{SENSEnM}$ – VSSKn					
		CUT*n*[7] (Dis) Bit = 0	●	0.31	0.53	0.74	mV
		CUT*n*[7] (Dis) Bit = 1 (Note 12)	●	0.76	1.13	1.49	mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. AGNDP – V_{EE} = 54V and V_{DD} – DGND = 3.3V unless otherwise noted. (Notes 3 and 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{SC}	Short-Circuit Sense	$V_{SENSEnM} – V_{EE} – V_{LIM}$	●	20	50	80	mV
Port Current Readback							
	Full-Scale Range	(Notes 7, 15, 16)			1.018		V
	LSB Weight	$V_{SENSEnM}$ – VSSKn, VSSKn = V_{EE} (Note 15)	●	61.0	62.1	63.5	µV/LSB
	Averaging Period	FILTER_TYPE Bit = 1 FILTER_TYPE Bit = 0 (Note 7)			100 1000		ms ms
	Update Interval	(Note 7)			100		ms
Port Power Readback							
	Full-Scale Range	(Notes 7, 15, 16)			83.8		V^2
	LSB Weight	($V_{SENSEnM}$ – VSSKn) × (AGNDP – V_{EE}) VSSKn = V_{EE} (Note 15)	●	4.992	5.115	5.235	mV^2/LSB
	Averaging Period	FILTER_TYPE Bit = 1 FILTER_TYPE Bit = 0 (Note 7)			100 1000		ms ms
	Update Interval	(Note 7)			100		ms
System Voltage Readback							
	Full-Scale Range	(Note 7)			82		V
	LSB Weight	AGNDP – V_{EE}	●	9.8	10.1	10.3	mV/LSB
	Averaging Period	FILTER_TYPE Bit = 1 FILTER_TYPE Bit = 0 (Note 7)			100 1000		ms ms
	Update Interval	(Note 7)			100		ms
Digital Interface							
V_{ILD}	Digital Input Low Voltage	ADn, $\overline{RESET}$, $\overline{MSD}$, GPn, AUTO, $\overline{4PVALID}$ (Note 6)	●			0.8	V
	I^2C Input Low Voltage	SCL, SDAIN (Note 6)	●			1.0	V
V_{IHD}	Digital Input High Voltage	(Note 6)	●	2.2			V
	Digital Output Voltage Low	I_{SDAOUT} = 3mA, $I_{\overline{INT}}$ = 3mA I_{SDAOUT} = 5mA, $I_{\overline{INT}}$ = 5mA	● ●			0.4 0.7	V V
	Internal Pull-Up to V_{DD}	AD*n*, $\overline{RESET}$, $\overline{MSD}$, GP*n*			50		kΩ
	Internal Pull-Down to DGND	AUTO, $\overline{4PVALID}$			50		kΩ
PWRMD							
	PWRMD Digital Input Low Voltage	V_{PWRMDn} – V_{EE}	●			0.8	V
	PWRMD Digital Input High Voltage	V_{PWRMDn} – V_{EE}	●	3.4			V
	Internal Pull Up to CAP2	PWRMD0, PWRMD1			50		kΩ
PSE Timing Characteristics (Note 7)							
t_{DET}	Detection Time	Beginning to End of Detection	●		320	500	ms
t_{CLASS_RESET}	Classification Reset Duration		●	15			ms
t_{CEV}	Class Event Duration		●	6	12	20	ms
t_{CEVON}	Class Event Turn On Duration	C_{PORT} = 0.6µF	●			0.1	ms
t_{LCE}	Long Class Event Duration		●	88		105	ms
t_{CLASS}	Class Event I_{CLASS} Measurement Timing		●	6			ms
t_{CLASS_LCE}	Long Class Event I_{CLASS} Measurement Timing		●	6		75	ms
t_{CLASS_ACS}	Autoclass I_{CLASS} Measurement Timing		●	88			ms

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. AGNDP – V_{EE} = 54V and V_{DD} – DGND = 3.3V unless otherwise noted. (Notes 3 and 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{ME1}	Mark Event Duration (Except Last Mark Event)	(Note 11)	●	6	8.6	12	ms
t_{ME2}	Last Mark Event Duration	(Note 11)	●	6	20		ms
t_{PON}	Power On Delay, Auto Mode	From End of Valid Detect to End of Valid Inrush (Note 14)	●			400	ms
t_{AUTO_PSE1}	Autoclass Power Measurement Start	From End of Inrush to Beginning of Autoclass Power Measurement	●	1.4		1.6	s
t_{AUTO_PSE2}	Autoclass Power Measurement End	From End of Inrush to End of Autoclass Power Measurement	●	3.1		3.5	s
t_{AUTO_WINDOW}	Autoclass Average Power Sliding Window		●	0.15	0.2	0.3	s
t_{ED}	Fault Delay	From Power On Fault to Next Detect	●	1.0	1.3	1.5	s
t_{START}	Maximum Current Limit Duration During Inrush		●	52	59	66	ms
t_{CUT}	Maximum Overcurrent Duration After Inrush		●	52	59	66	ms
	Maximum Overcurrent Duty Cycle		●	5.8	6.3	6.7	%
t_{LIM}	Maximum Current Limit Duration After Inrush	(Note 12) Type 3, t_{LIMn} = 8h Type 4, t_{LIMn} = 5h	 ● ●	 10 6	 12 8	 14 10	 ms ms
t_{MPS}	Maintain Power Signature (MPS) Pulse Width Sensitivity	Current Pulse Width to Reset Disconnect Timer (Note 8)	●	1.6		3.6	ms
t_{DIS}	Maintain Power Signature (MPS) Dropout Time	(Note 5)	●	320	350	380	ms
$t_{\overline{MSD}}$	Masked Shut Down Delay					6.5	µs
	I^2C Watchdog Timer Duration		●	1.5	2	3	s
	Minimum Pulse Width for Masked Shut Down		●	3			µs
	Minimum Pulse Width for $\overline{RESET}$		●	4.5			µs
I^2C Timing (Note 7)							
f_{SCLK}	Clock Frequency		●			1	MHz
t_1	Bus Free Time	Figure 5 (Note 9)	●	480			ns
t_2	Start Hold Time	Figure 5 (Note 9)	●	240			ns
t_3	SCL Low Time	Figure 5 (Note 9)	●	480			ns
t_4	SCL High Time	Figure 5 (Note 9)	●	240			ns
t_5	SDAIN Data Hold Time	Figure 5 (Note 9)	●	60			ns
t_5	Data Clock to SDAOUT Valid	Figure 5 (Note 9)	●			130	ns
t_6	Data Set-Up Time	Figure 5 (Note 9)	●	80			ns
t_7	Start Set-Up Time	Figure 5 (Note 9)	●	240			ns
t_8	Stop Set-Up Time	Figure 5 (Note 9)	●	240			ns
t_r	SCL, SDAIN Rise Time	Figure 5 (Note 9)	●			120	ns
t_f	SCL, SDAIN Fall Time	Figure 5 (Note 9)	●			60	ns
	Fault Present to $\overline{INT}$ Pin Low	(Notes 9, 10)	●			150	ns
	Stop Condition to $\overline{INT}$ Pin Low	(Notes 9, 10)	●			1.5	µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. AGNDP – V_{EE} = 54V and V_{DD} – DGND = 3.3V unless otherwise noted. (Notes 3 and 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	ARA to $\overline{INT}$ Pin High Time	(Note 9)	●			1.5	µs
	SCL Fall to ACK Low	(Note 9)	●			130	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. With the exception of (V_{DD} – DGND), exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 140ºC when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 3: All currents into device pins are positive; all currents out of device pins are negative.

Note 4: The LTC4292 operates with a negative supply voltage (with respect to AGNDP). To avoid confusion, voltages in this data sheet are referred to in terms of absolute magnitude.

Note 5: t_{DIS} is the same as t_{MPDO} defined by IEEE 802.3.

Note 6: The LTC4291-1 digital interface operates with respect to DGND. All logic levels are measured with respect to DGND.

Note 7: Guaranteed by design, not subject to test.

Note 8: The IEEE 802.3 specification allows a PD to present its Maintain Power Signature (MPS) on an intermittent basis without being disconnected. In order to stay powered, the PD must present the MPS for t_{MPS} within any t_{MPDO} time window.

Note 9: Values Measured at V_{ILD} and V_{IHD}.

Note 10: If a fault condition occurs during an I^2C transaction, the $\overline{INT}$ pin will not be pulled down until a stop condition is present on the I^2C bus.

Note 11: Load characteristics of the LTC4292 during Mark: 7V < (AGNDP – V_{OUTnM}) < 10V or I_{OUTnM} < 50µA.

Note 12: See the LTC4291 Software Programming documentation for information on serial bus usage and device configuration and status registers.

Note 13: Do not source or sink current from CAP1 and CAP2.

Note 14: For single-signature PDs, t_{PON} is measured from end of valid detect on either power channel. For dual-signature PDs, t_{PON} is measured from the end of valid detect on the same power channel.

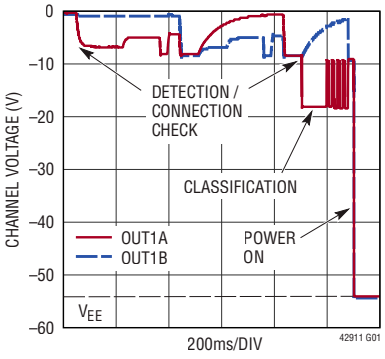
Note 15: Port current and port power measurements depend on sense resistor value (0.15Ω typical). See External Component Selection for details.

Note 16: The full-scale range for each power channel is half of the port full-scale range.

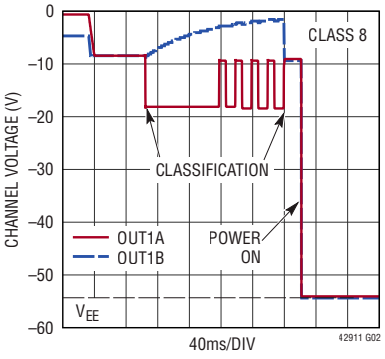
Note 17: See Inrush Control for details on inrush threshold selection.

TYPICAL PERFORMANCE CHARACTERISTICS

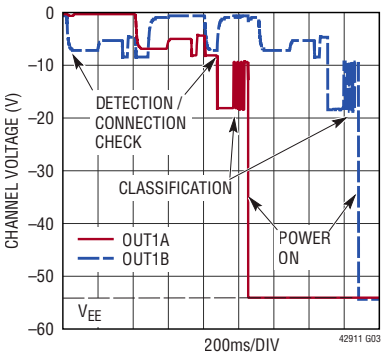
802.3bt Single–Signature Power On Sequence



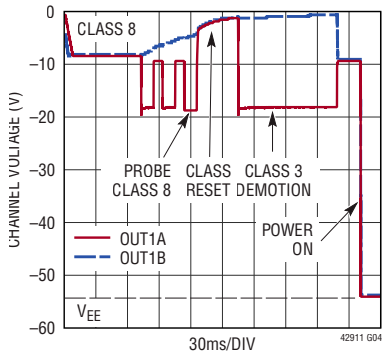
802.3bt Single–Signature Classification and Power On



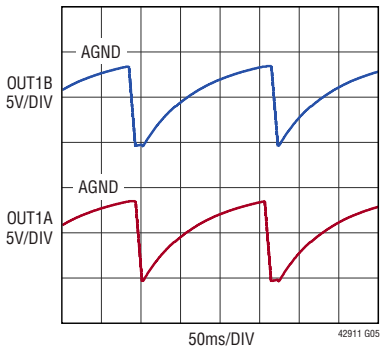
802.3bt Dual–Signature Power On Sequence



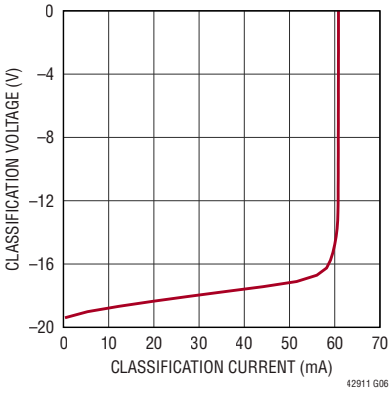
802.3bt Single–Signature Class Probe and Demotion



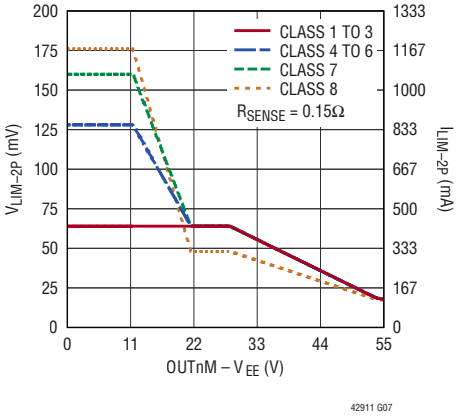
Open Circuit Detection



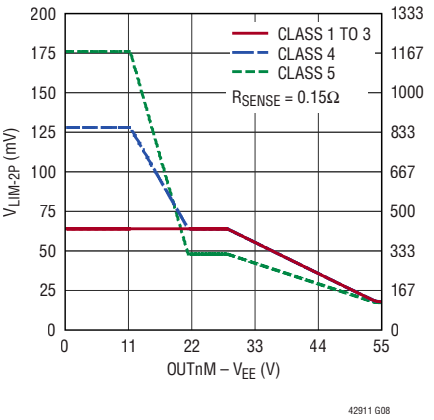
Classification Current Compliance



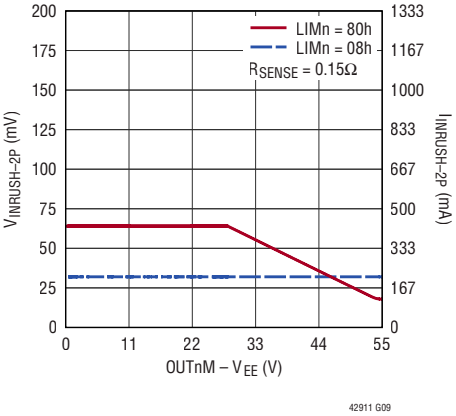
Power On Current Limits Single–Signature



Power On Current Limits Dual–Signature

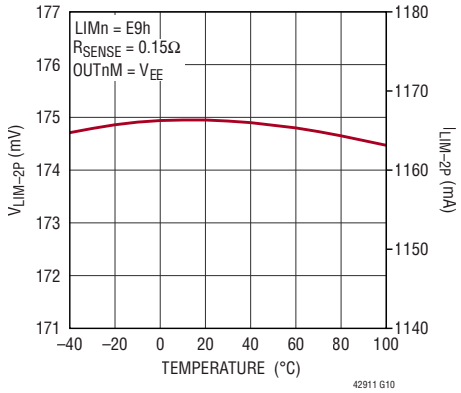


Inrush Current Limits (Note 17)

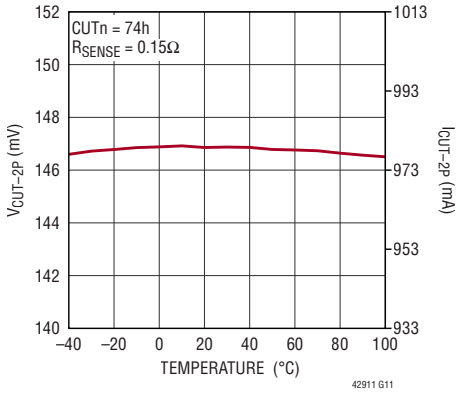


TYPICAL PERFORMANCE CHARACTERISTICS

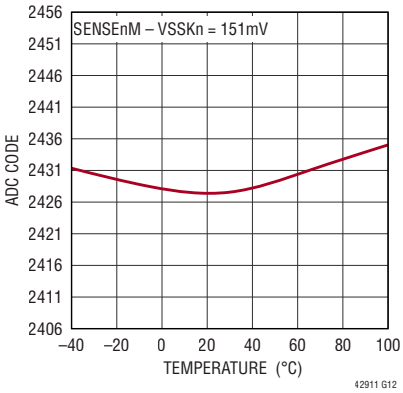
I_{LIM-2P} vs Temperature



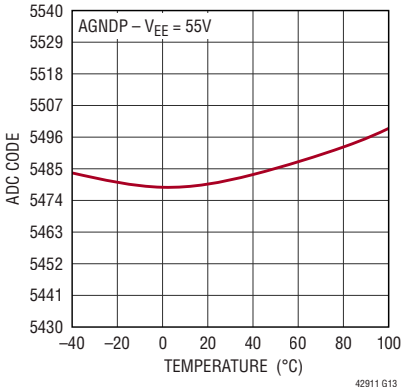
I_{CUT-2P} vs Temperature



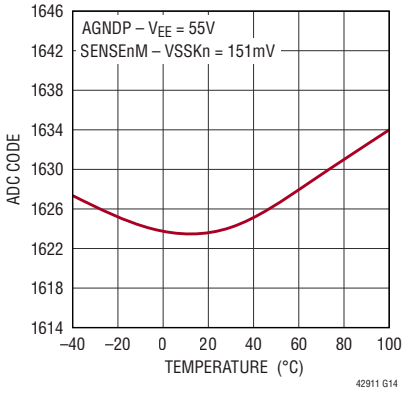
Current Readback ADC vs Temperature



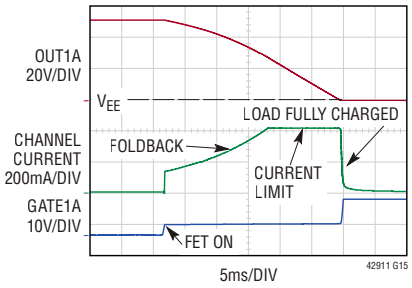
Voltage Readback ADC vs Temperature



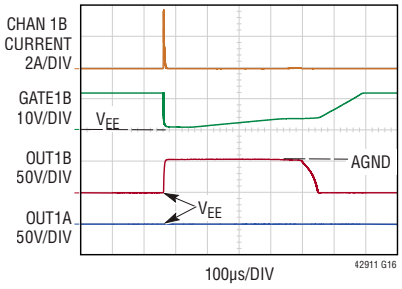
Power Readback ADC vs Temperature



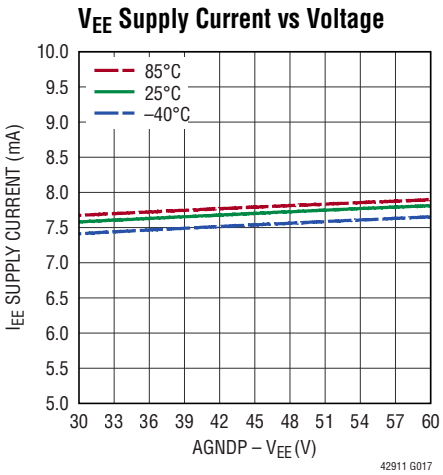
Powering Up into 180µF Load

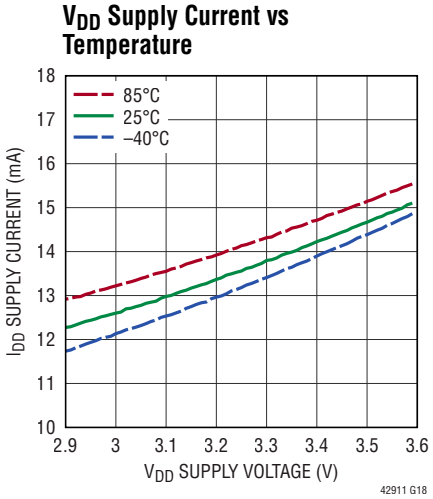


Temporary Short Circuit on Channel 1B



TYPICAL PERFORMANCE CHARACTERISTICS





TEST TIMING DIAGRAMS

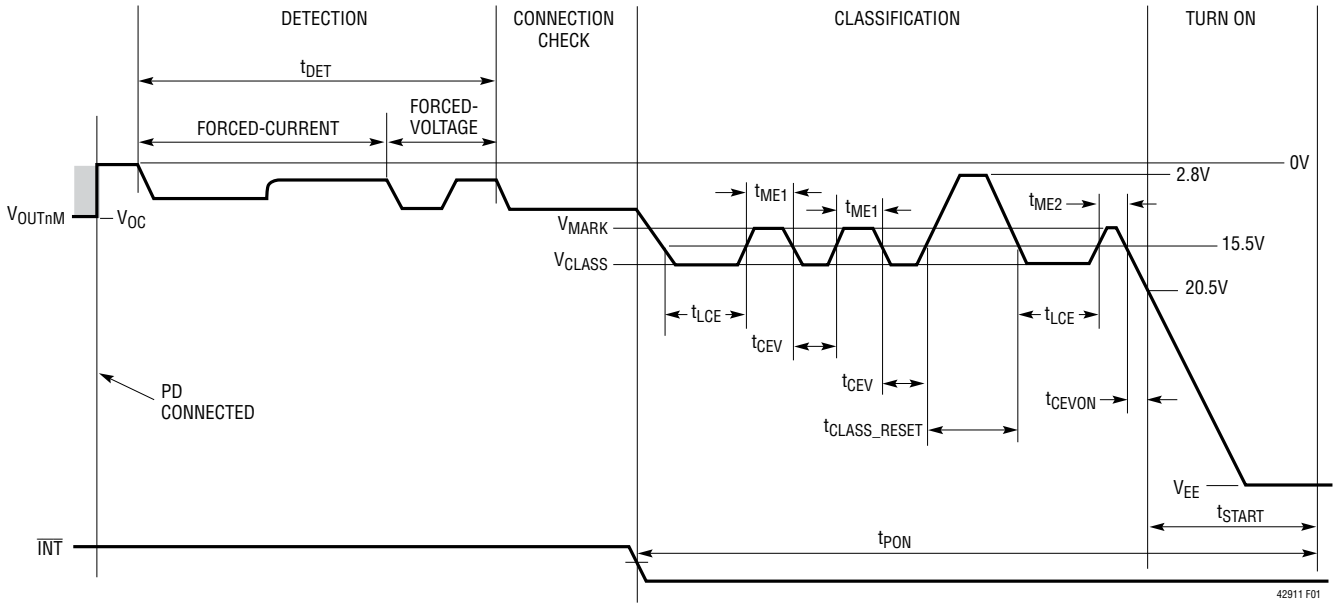


Figure 1. Detect, Class and Turn-On Timing in Auto or Semi-Auto Modes

TEST TIMING DIAGRAMS

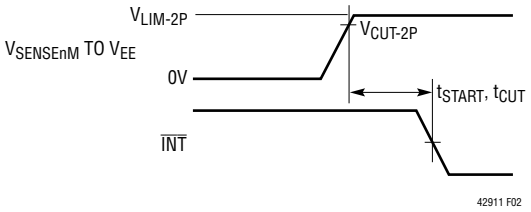


Figure 2. Current Limit Timing

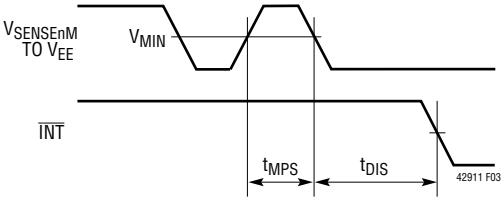


Figure 3. DC Disconnect Timing

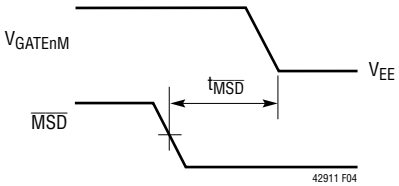


Figure 4. Shut Down Delay Timing

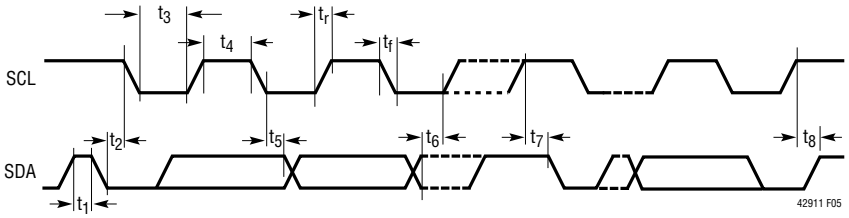


Figure 5. I²C Interface Timing

I²C TIMING DIAGRAMS

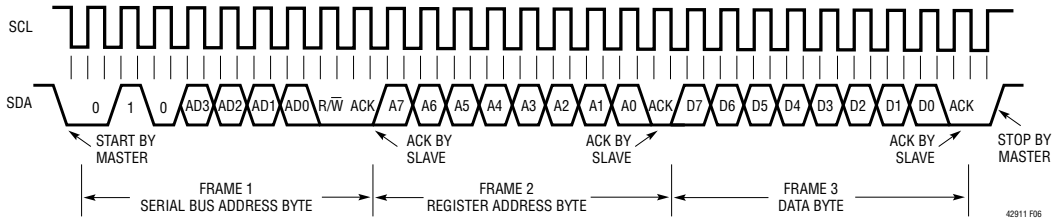


Figure 6. Writing to a Register

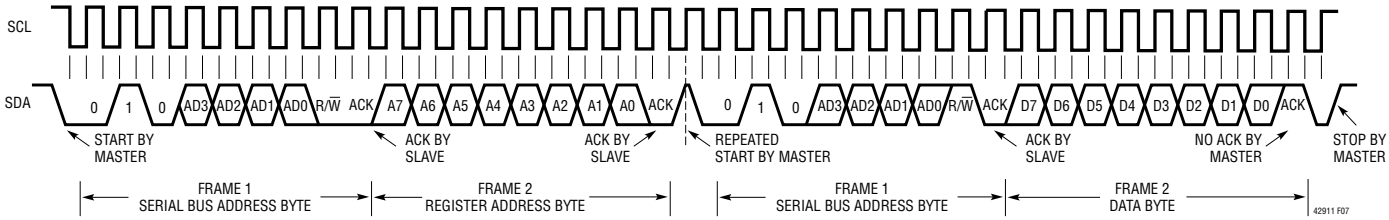


Figure 7. Reading from a Register

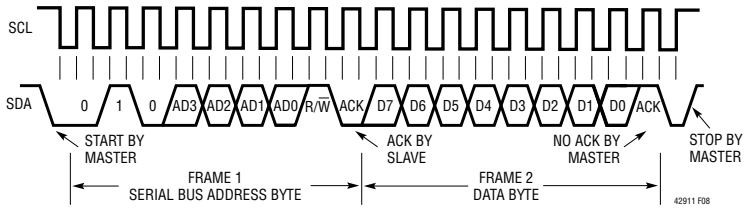


Figure 8. Reading the Interrupt Register (Short Form)

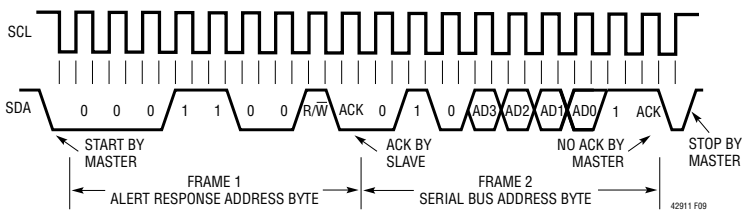


Figure 9. Reading from Alert Response Address

PIN FUNCTIONS

LTC4292

V_{EE} (Pins 31, 33, 40, Exposed Pad Pin 41): Main PoE Supply Input. Connect to a –51V to –57V supply, relative to AGNDP. Voltage depends on PSE Type (Type 3 or 4).

GATEnM (Pins 1, 3, 7, 9, 22, 24, 28, 30): Gate Drive, Port n, Channel M. Connect GATEnM to the gate of the external MOSFET for port n, channel M. When the MOSFET is turned on, the gate voltage is driven to 12V (typ) above V_{EE}. During a current limit condition, the voltage at GATEnM will be reduced to maintain constant current through the external MOSFET. If the fault timer expires, GATEnM is pulled down, turning the MOSFET off and raising a port n fault event. If the channel is unused, the GATEnM pin must be floated.

OUTnM (Pins 2, 4, 8, 10, 21, 23, 27, 29): Output Voltage Monitor, Port n, Channel M. Connect OUTnM to the output channel. A current limit foldback circuit limits the power dissipation in the external MOSFET by reducing the current limit threshold when the drain-to-source voltage exceeds 10V. The port n power good event is raised when the voltage from OUTnM to V_{EE} drops below 2.4V (typ). A 500k resistor is connected internally from OUTnM to AGNDP when the channel is idle. If the channel is unused, the OUTnM pin must be floated.

CAP2 (Pin 6): Analog Internal 4.3V Power Supply Bypass Capacitor. Connect a 0.22µF ceramic cap to V_{EE}.

PWRMDn (Pins 11, 20): Maximum Power Mode Input. Logic input signals between V_{EE} and V_{EE} + 4.3V for configuration of maximum output power per-port in auto mode. See Auto Mode Maximum PSE Power section. Internally pulled up to CAP2.

SENSEnM (Pins 12, 13, 14, 15, 16, 17, 18, 19): Current Sense Input, Port n, Channel M. SENSEnM monitors the external MOSFET current via a 0.15Ω sense resistor between SENSEnM and VSSKn. Whenever the voltage across the sense resistor exceeds the overcurrent detection threshold V_{CUT-2P}, the current limit fault timer counts up. If the voltage across the sense resistor reaches the current limit threshold V_{LIM-2P}, the GATEnM pin voltage is lowered to maintain constant current in the external MOSFET. See Applications Information for further details. If the channel is unused, the SENSEnM pin must be tied to V_{EE}.

AGNDP (Pin 25): Analog Ground. Connect AGNDP to the return for the V_{EE} supply through a 10Ω resistor.

DNA (Pin 36): Data Transceiver Negative Input Output (Analog). Connect to DND through a data transformer.

DPA (Pin 37): Data Transceiver Positive Input Output (Analog). Connect to DPD through a data transformer.

CNA (Pin 38): Clock Transceiver Negative Input Output (Analog). Connect to CND through a data transformer.

CPA (Pin 39): Clock Transceiver Positive Input Output (Analog). Connect to CPD through a data transformer.

VSSK12 (Pin 5): Kelvin Sense to V_{EE}. Connect to sense resistor common node for ports 1 and 2 through a 0.15Ω resistor. Connect to AGNDP through a 0.22µF, 100V capacitor. Do not connect directly to V_{EE} plane. See Layout Requirements.

VSSK34 (Pin 26): Kelvin Sense to V_{EE}. Connect to sense resistor common node for ports 3 and 4 through a 0.15Ω resistor. Connect to AGNDP through a 0.22µF, 100V capacitor. Do not connect directly to V_{EE} plane. See Layout Requirements.

Common Pins

NC, DNC (LTC4291-1 Pins 7, 13; LTC4292 Pins 32, 34, 35): All pins identified with "NC" or "DNC" must be left unconnected.

LTC4291-1

AD0 (Pin 1): Address Bit 0. Tie the address pins high or low to set the I^2C serial address to which the LTC4291-1 responds. The address will be $(010A_3A_2A_1A_0)b$. Internally pulled up to V_{DD}.

AD1 (Pin 2): Address Bit 1. See AD0.

AD2 (Pin 3): Address Bit 2. See AD0.

AD3 (Pin 4): Address Bit 3. See AD0.

$\overline{\text{4PVALID}}$ (Pin 6): 4-Pair Valid Input, Active Low. When low, the LTC4291-1/LTC4292 will not apply power to a port unless both pairsets present a valid signature. When high, the LTC4291-1/LTC4292 will power any pairset presenting a valid signature, regardless of the other pairset. Internally pulled down to DGND.

PIN FUNCTIONS

CPD (Pin 8): Clock Transceiver Positive Input Output (Digital). Connect to CPA through a data transformer.

CND (Pin 9): Clock Transceiver Negative Input Output (Digital). Connect to CNA through a data transformer.

DPD (Pin 10): Data Transceiver Positive Input Output (Digital). Connect to DPA through a data transformer.

DND (Pin 11): Data Transceiver Negative Input Output (Digital). Connect to DNA through a data transformer.

V_{DD} (Pins 12, 20): V_{DD} IO Power Supply. Connect to a 3.3V power supply relative to DGND. V_{DD} must be bypassed to DGND near the LTC4291-1 with at least a 0.1µF capacitor.

$\overline{\text{RESET}}$ (Pin 14): Reset Input, Active Low. When $\overline{\text{RESET}}$ is low, the LTC4291-1/LTC4292 is held inactive with all ports off and all internal registers reset. When $\overline{\text{RESET}}$ is pulled high, the LTC4291-1/LTC4292 begins normal operation. $\overline{\text{RESET}}$ can be connected to an external capacitor or RC network to provide a power turn-on delay. Internal filtering of $\overline{\text{RESET}}$ prevents glitches less than 1µs wide from resetting the LTC4291-1/LTC4292. Internally pulled up to V_{DD}.

$\overline{\text{INT}}$ (Pin 15): Interrupt Output, Open Drain. $\overline{\text{INT}}$ will pull low when any one of several events occur in the LTC4291-1. It will return to a high impedance state when bits 6 or 7 are set in the Reset PB register (1Ah). The $\overline{\text{INT}}$ signal can be used to generate an interrupt to the host processor, eliminating the need for continuous software polling. Individual $\overline{\text{INT}}$ events can be disabled using the $\overline{\text{INT}}$ Mask register (01h). See LTC4291 Software Programming documentation for more information. $\overline{\text{INT}}$ is only updated between I^2C transactions.

SDAOUT (Pin 16): Serial Data Output, Open Drain Data Output for the I^2C Serial Interface Bus. The LTC4291-1 uses two pins to implement the bidirectional SDA function to simplify opto isolation of the I^2C bus. To implement a standard bidirectional SDA pin, tie SDAOUT and SDAIN together. See Applications Information for more information.

SDAIN (Pin 17): Serial Data Input. High impedance data input for the I^2C serial interface bus. The LTC4291-1 uses two pins to implement the bidirectional SDA function to simplify opto isolation of the I^2C bus. To implement a standard bidirectional SDA pin, tie SDAOUT and SDAIN together. See Applications Information for more information.

SCL (Pin 18): Serial Clock Input. High impedance clock input for the I^2C serial interface bus. The SCL pin should be connected directly to the I^2C SCL bus line. SCL must be tied high if the I^2C serial interface bus is not used.

CAP1 (Pin 19): Core Power Supply Bypass Capacitor. Connect a 1µF capacitance to DGND for the internal 1.8V regulator bypass. Do not use other capacitor values.

AUTO (Pin 21): Auto Mode Input, Active High. When high, the LTC4291-1 detects, classifies and powers up valid PDs without host interaction. AUTO determines the state of the internal registers when the LTC4291-1 is reset or comes out of UVLO (see LTC4291 Software Programming documentation). The state of these register bits can subsequently be changed via the I^2C interface. Internally pulled down to DGND.

GP1 (Pin 22): General Purpose Digital Input Output for customer applications. Referenced to DGND.

GP0 (Pin 23): General Purpose Digital Input Output for customer applications. Referenced to DGND.

$\overline{\text{MSD}}$ (Pin 24): Maskable Shutdown Input, Active Low. When pulled low, all ports that have their corresponding mask bit set in the mconf register (17h) will be reset. Internal filtering of the $\overline{\text{MSD}}$ pin prevents glitches less than 1µs wide from resetting ports. The MSD Pin Mode register can configure the $\overline{\text{MSD}}$ pin polarity. Internally pulled up to V_{DD}.

DGND (Pin 5, Exposed Pad Pin 25): Digital Ground. DGND should be connected to the return from the V_{DD} supply.

APPLICATIONS INFORMATION

OVERVIEW

Power over Ethernet, or PoE, is a standard protocol for sending DC power over copper Ethernet data wiring. The IEEE group that administers the 802.3 Ethernet data standards added PoE powering capability in 2003. This original PoE standard, known as 802.3af, allowed for 48V DC power at up to 13W. 802.3af was widely popular, but 13W was not adequate for some applications. In 2009, the IEEE released a new standard, known as 802.3at or PoE+, increasing the voltage and current requirements to provide 25.5W of delivered power.

The IEEE standard also defines PoE terminology. A device that provides power to the network is known as a PSE, or power sourcing equipment, while a device that draws power from the network is known as a PD, or powered device. PSEs come in two types: Endpoints (typically network switches or routers), which provide data and power; and Midspans, which provide power but pass through data. Midspans are typically used to add PoE capability to existing non-PoE networks. PDs are typically IP phones, wireless access points, security cameras, and similar devices.

PoE++ Evolution

Even during the development of the IEEE 802.3at (PoE+) 25.5W standard, it became clear there was a significant and increasing need for more than 25.5W of delivered power. In 2013, the 802.3bt task force was formed to develop a standard capable of increasing delivered PD power.

The primary objective of the task force is to use all four pairs of the Ethernet cable as opposed to the two pair power utilized by 802.3at. Using all four pairs allows for at least twice the delivered power over existing Ethernet cables. Further, the amount of current per two pairs (known as a pairset) has been increased while maintaining the Ethernet data signal integrity. 802.3bt increases PD delivered power from 25.5W to 71.3W, enabling IEEE-compliant high power PD applications.

The LTC4291-1/LTC4292 delivers power over two power channels. Each pairset is driven by a dedicated power channel. In this data sheet, the term “channel” refers to the PSE circuitry assigned to a corresponding pairset. For the purposes of this document, the terms channel and pairset may be considered interchangeable.

In addition, IEEE 802.3bt enables substantially lower Maintain Power Signature (MPS) currents, resulting in significantly lower standby power consumption. This allows new and emerging government or industry standby regulations to be met using standard PoE components.

LTC4291-1/LTC4292 Product Overview

The LTC4291-1/LTC4292 is a fifth generation PSE controller that implements four PSE ports in either an Endpoint or Midspan application. Virtually all necessary circuitry is included to implement an IEEE 802.3bt compliant PSE design, requiring a pair of external power MOSFETs and sense resistors per port; these minimize power loss compared to alternative designs with onboard MOSFETs, and increase system reliability.

The LTC4291-1/LTC4292 chipset implements a proprietary isolation scheme for inter-chip communication. This architecture substantially reduces BOM cost by replacing expensive opto-isolators and isolated power supplies with a single low-cost transformer.

The LTC4291-1/LTC4292 offers advanced fifth generation PSE features including a configurable interrupt signal triggered by per-port events, per-channel power on control and fault telemetry, per-port current monitoring, V_{EE} monitoring, one second rolling current, voltage, and port power averaging, and two general purpose input/output pins.

APPLICATIONS INFORMATION

V_{EE} and port current measurements are performed simultaneously, providing fully coherent port power calculations. The reported port power calculations enable coherent and precise per-port power monitoring.

PoE BASICS

Common Ethernet data connections consist of two or four twisted pairs of copper wire (commonly known as Ethernet cable), transformer-coupled at each end to avoid ground loops. PoE systems take advantage of this coupling arrangement by applying voltage between the center-taps of the data transformers to transmit power from the PSE to the PD without affecting data transmission. Figures 10 and 11 show high level PoE system schematics.

To avoid damaging legacy data equipment that does not expect to see DC voltage, the PoE standard defines a protocol that determines when the PSE may apply and remove power. Valid PDs are required to have a specific 25k common-mode resistance at their input. When such a PD is connected to the cable, the PSE detects this signature resistance and applies power. When the PD is later disconnected, the PSE senses the open circuit and removes power. The PSE also removes power in the event of a current fault or short circuit.

When a PD is detected, the PSE looks for a classification signature that tells the PSE the maximum power the PD will draw. The PSE can use this information to allocate power among several ports, to police the current consumption of the PD, or to reject a PD that will draw more power than the PSE has available.

New in 802.3bt

The 802.3bt draft introduces several new features:

- Type 3 and Type 4 PSEs may provide power over all four pairs (both pairsets), depending on connected PD characteristics.
- Type 3 and Type 4 PDs are required to be capable of receiving power over all four pairs (both pairsets).
- Type 3 and 4 PDs can be formed as either a single-signature PD or dual-signature PD. A single-signature PD presents the same valid signature resistor to both pairsets simultaneously. A dual-signature PD presents two fully independent valid detection signatures, one to each pairset.
- Type 3 single-signature PDs request exactly one of six possible power levels: 3.84W, 6.49W, 13W, 25.5W, 40W, or 51W.
- Type 3 dual-signature PDs request exactly one of four possible power levels on each pairset: 3.84W, 6.49W, 13W, or 25.5W. The total PD requested power is the sum of the requested power on both pairsets.
- Type 3 PD Classes overlap with Type 1 and 2 Classes in order to provide additional Type 3 feature sets at lower power levels.
- Type 4 single-signature PDs request exactly one of two possible power levels: 62W or 71.3W.
- Type 4 dual-signature PDs request exactly 35.6W on at least one pairset and one of five possible power levels on the other pairset: 3.84W, 6.49W, 13W, 25.5W, or 35.6W. The total PD requested power is the sum of the requested power on both pairsets.
- Classification is extended to a possible maximum of five class events. The additional events allow for unique identification of existing and new PD Classes.
- Type 3 and 4 PSEs issue a long first class event to advertise Type 3 and 4 feature support to attached PDs.
- Lower standby power is enabled by shortening the length of the maintain power signature pulse (short MPS). The PD duty cycle drops from ~23% to ~2%. A PD is allowed to present short MPS if the PSE issues a long first class event.
- Power management is augmented by Autoclass, an optional feature for 802.3bt PSEs and PDs. In an Autoclass system the maximum PD power is measured and reported to the PSE host, enabling the PSE to reclaim output power not used by the PD application and losses in the Ethernet cabling (Table 1). See Autoclass section and LTC4291 Software Programming documentation for details.

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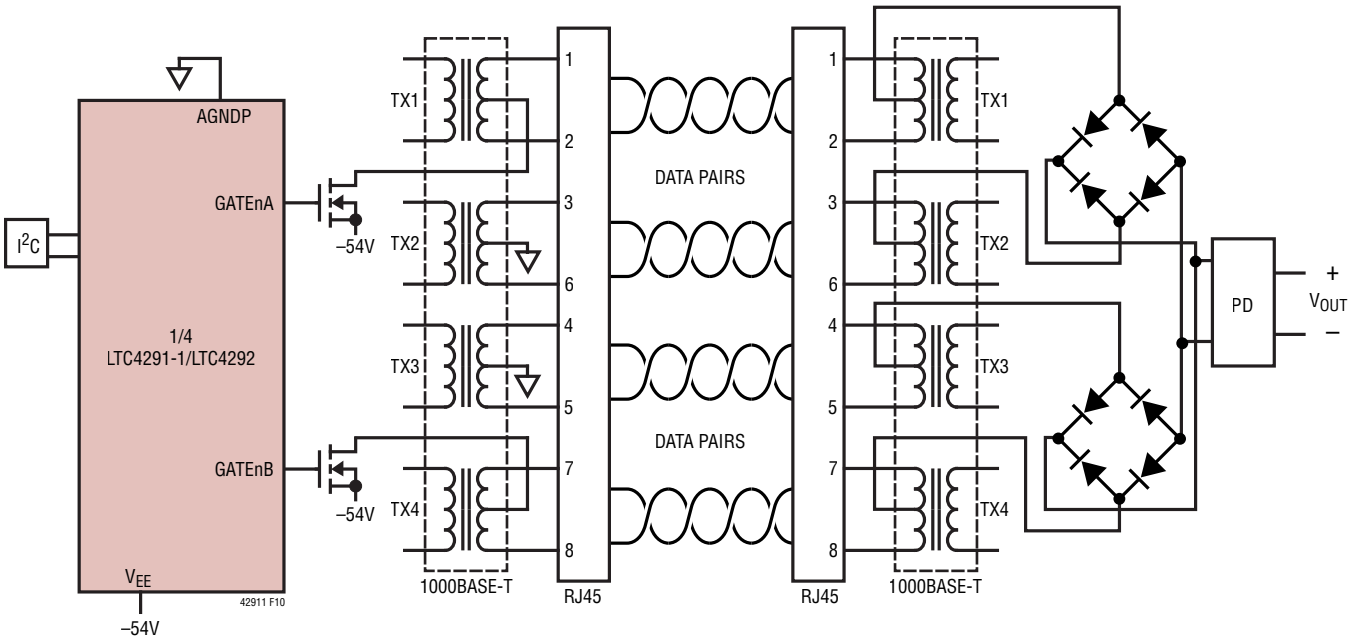

Figure 10. Power over Ethernet Single-Signature PD System Diagram

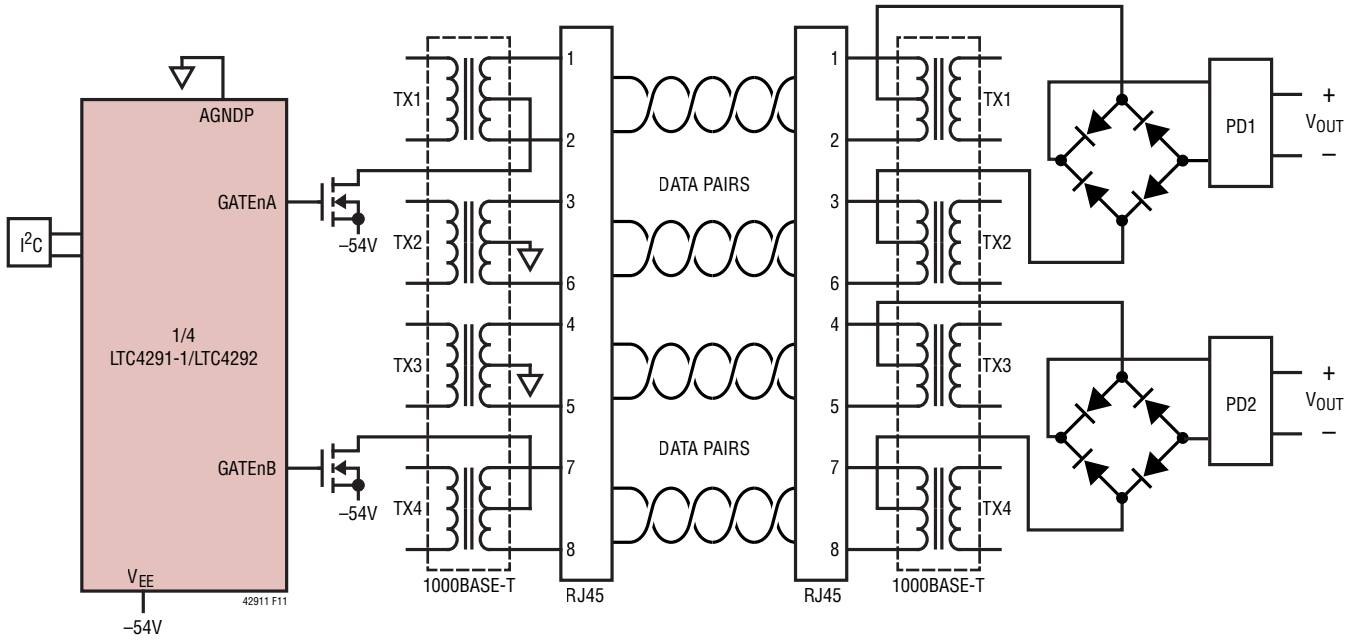

Figure 11. Power over Ethernet Dual-Signature PD System Diagram

APPLICATIONS INFORMATION

Table 1. IEEE-Specified Power Allocations, Single-Signature PD

PD CLASS	PSE OUTPUT POWER	ALLOCATED CABLING LOSS	PD INPUT POWER
1	4W	0.16W	3.84W
2	6.7W	0.21W	6.49W
3	14W	1W	13W
4	30W	4.5W	25.5W
5	45W	5W	40W
6	60W	9W	51W
7	75W	13W	62W
8	90W	18.7W	71.3W

BACKWARD COMPATIBILITY

The LTC4291-1/LTC4292 may be configured as an 802.3bt-compliant PSE, either Type 3 or Type 4. While 802.3bt PSEs cannot identify as an 802.3at Type 1 or Type 2 PSE, there is no loss in PSE functionality; all 802.3bt-compliant PSEs are fully backwards compatible with existing 802.3at Type 1 and Type 2 PDs as shown in Table 2. In addition to full compatibility, 802.3bt PSEs extend support for lower standby power, enhanced current limit timing, and dynamic power management to all PD Types (as supported by the PD application).

Table 2. PSE Maximum Delivered Power, Per-Port

DEVICE			PSE			
	STANDARD		802.3at		802.3bt	
		TYPE	1	2	3	4
PD	802.3at	1	13W	13W	13W	13W
		2	13W*	25.5W	25.5W	25.5W
	802.3bt	3	13W*	25.5W*	51W	51W
		4	13W*	25.5W*	51W*	71.3W

*Indicates PD allocated less power than requested.

Software register map compatibility with LTC4266 and LTC4271-based PSEs has been maintained to the extent possible. LTC4291-based PSEs utilize two channels to control a single PSE port. This multiplicity of channel status and control requires extensions to the existing register map.

For register map details please contact Analog Devices to request the LTC4291 Software Programming documentation.

Special Compatibility Mode Notes

- As with prior generations, each I^2C address provides status and control for four PoE ports. Each port register slice provides port control and status as well as channel A vs B control and status.
- Certain status registers, e.g. Port Status and Power Status, relate to a channel state, as opposed to port state and are split into three copies; a generalized port state, channel A state and channel B state.
- Certain command registers, e.g., Power-on pushbutton, likewise are bifurcated to allow per-channel control.

OPERATING MODES

The LTC4291-1/LTC4292 includes four independent ports, each of which can operate in one of three modes: manual, semi-auto, or auto. A fourth mode, shutdown, disables the port (see Table 3).

Table 3. Operating Modes

MODE	AUTO PIN	OPMD	DETECT/ CLASS	POWER-UP	AUTOMATIC THRESHOLD ASSIGNMENT
Auto	1	11b	Enabled at Reset	Automatically	Yes
	0	11b	Host Enabled	Automatically	Yes
Semi-auto	0	10b	Host Enabled	Upon Request	No
Manual	0	01b	Once Upon Request	Upon Request	No
Shutdown	0	00b	Disabled	Disabled	No

In manual mode, the port waits for instructions from the host system before taking any action. It runs a single detection, or detection and classification cycle when commanded to by the host, and reports the result in its Port Status register. The host system can command the port to apply or remove power at any time.

In semi-auto mode, the port repeatedly attempts to detect and classify any PD attached to it. It reports the status of these attempts back to the host, and waits for a command from the host before applying power to the port. The host must enable detection and classification.

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Auto mode operates the same as semi-auto mode except it will automatically apply power to the port if detection and classification are successful. Auto mode will autonomously set the I_{CUT-2P}, I_{LIM-2P}, and P_{CUT-4P} values based on the Class result. This operational mode may be entered by setting AUTO high at reset or by changing the OPMD state to Auto. See Auto Mode Maximum PSE Power section.

In shutdown mode the port is disabled and will not detect or power a PD.

Regardless of which mode it is in, the LTC4291-1/LTC4292 will remove power automatically from any port and/or channel, as appropriate, that generates a fault. It will also automatically remove power from any port/channel that generates a disconnect event if disconnect detection is enabled. The host controller may also command the port to remove power at any time.

Reset and the AUTO Pin

The initial LTC4291-1/LTC4292 configuration depends on the state of AUTO during reset. Reset occurs at power-up, whenever $\overline{RESET}$ is pulled low, or when the global Reset All bit is set. Changing the state of AUTO after power-up will not change the port behavior of the LTC4291-1/LTC4292 until a reset occurs.

Although typically actively managed by a host controller, the LTC4291-1/LTC4292 may alternatively be configured for autonomous operation by setting AUTO high. With AUTO high, each port will detect and classify repeatedly until a PD is discovered, set I_{CUT-2P}, I_{LIM-2P}, and P_{CUT-4P} according to the PSE assigned Class, apply power to valid PDs, and remove power when a PD is disconnected.

Tables 4 and 5 show the I_{CUT-2P}, I_{LIM-2P}, and P_{CUT-4P} values that will be automatically set in auto mode, based on the PD requested Class.

Table 4. Typical Auto Mode Power On Thresholds, Single-Signature PD

	PER-CHANNEL		PER-PORT
CLASS	I_{CUT-2P}	I_{LIM-2P}	P_{CUT-4P}
1	94mA	425mA	5.43W
2	150mA	425mA	8.69W
3	338mA	425mA	19.5W
4	638mA	850mA	36.4W
5	581mA	850mA	52.7W
6	731mA	850mA	70.0W
7	825mA	1063mA	87.4W
8	975mA	1167mA	96.6W

Table 5. Typical Auto Mode Power On Thresholds, Dual-Signature PD

	PER-CHANNEL		
CLASS	I_{CUT-2P}	I_{LIM-2P}	P_{CUT-2P}*
1	94mA	425mA	5.43W
2	150mA	425mA	8.69W
3	338mA	425mA	19.5W
4	638mA	850mA	36.4W
5	975mA	1167mA	48.3W

*A per-port P_{CUT-4P} threshold holds the sum of P_{CUT-2P} for each powered channel.

CONNECTION CHECK

Connection Check Overview

IEEE 802.3bt introduces a new detection subroutine known as connection check. A connection check is required to determine whether the attached PD is a single-signature PD, a dual-signature PD or an invalid result.

In 802.3at, only one PD configuration was described; this is known as a single-signature PD and is shown in Figure 10. A single-signature PD presents the same 25k detection resistor to both the pairsets in parallel.

New in 802.3bt is the dual-signature PD as shown in Figure 11. A dual-signature PD presents two fully independent 25k detection signature resistors, one to each pairset.

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The PD configuration (single or dual) determines how the PD is managed during subsequent detection, classification and power on procedures. Throughout the remainder of this data sheet attention will be called to the different treatment of single-signature and dual-signature PDs.

Connection check is performed with two current measurements, at the same forced voltage, on the first channel. The second channel is tested for aggressor behavior by introducing a forced current on the second channel during the second measurement. Comparison of the two resulting current measurements on the first channel allows for the connected device to be categorized as a single-signature PD, a dual-signature PD, or an invalid result.

An invalid connection check result is reported when a device is added or removed during connection check.

DETECTION

Detection Overview

To avoid damaging network devices that were not designed to tolerate DC voltage, a PSE must determine whether the connected device is a valid PD before applying power. The IEEE specification requires that a valid PD have a common-mode resistance of 25k ±5% at any channel voltage below 10V. The PSE must accept resistances that fall between 19k and 26.5k, and it must reject resistances above 33k or below 15k (shaded regions in Figure 12). The PSE may choose to accept or reject resistances in the undefined areas between the must-accept and must-reject ranges. In particular, the PSE must reject standard computer Network Interface Cards (NICs), many of which have 150Ω common-mode termination resistors that will be damaged if power is applied to them (the black region at the left of Figure 12).

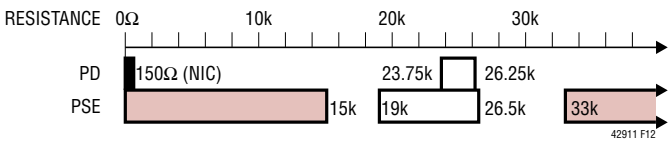

Figure 12. IEEE 802.3 Signature Resistance Ranges

Multipoint Detection

The LTC4291-1/LTC4292 uses a multipoint method to detect PDs. False-positive detections are minimized by checking for signature resistance with both forced current and forced voltage measurements.

Initially, two test currents are forced onto the channel (via the OUTnM pin) and the resulting voltages are measured. The detection circuitry subtracts the two V-I points to determine the resistive slope while removing offset caused by series diodes or leakage at the port (see Figure 13). If the forced current detection yields a valid signature resistance, two test voltages are then forced onto the channel and the resulting currents are measured and subtracted. Both methods must report valid resistances to report a valid detection. PD signature resistances between 17k and 29k (typically) are detected as valid and reported as Detect Good in the corresponding Port Status register or Channel Status register, as appropriate. Values outside this range, including open and short circuits, are also reported. If the channel measures less than 1V during any forced current test, the detection cycle will abort and Short Circuit will be reported. Tables 6 and 7 show the possible detection results.

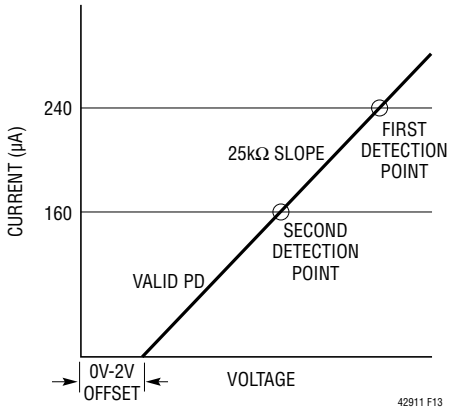

Figure 13. PD Detection

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Table 6. Port Detection Status

MEASURED PD SIGNATURE (TYPICAL)	PORT DETECTION RESULT
Incomplete or Not Yet Tested	Detect Status Unknown
V_{PD} < 1V	Short Circuit
R_{PD} < 17k	R_{SIG} Too Low
17k < R_{PD} < 29k	Detect Good, Single-Signature PD
R_{PD} > 29k	R_{SIG} Too High
R_{PD} > 50k	Open Circuit
V_{PD} > 10V	Port Voltage Outside Detect Range
Connection Check = INVALID	Connection Check Invalid
Connection Check = DUAL or Channel Detection Results Differ	Refer to Channel Detect Results

Table 7. Channel Detection Status

MEASURED PD SIGNATURE (TYPICAL)	CHANNEL DETECTION RESULT
Incomplete or Not Yet Tested	Detect Status Unknown
V_{PD} < 1V	Short Circuit
C_{PD} > 2.7µF	C_{PD} Too High
R_{PD} < 17k	R_{SIG} Too Low
17k < R_{PD} < 29k	Detect Good, Dual-Signature PD
R_{PD} > 29k	R_{SIG} Too High
R_{PD} > 50k	Open Circuit
V_{PD} > 10V	Channel Voltage Outside Detect Range
Connection Check = INVALID	Connection Check Invalid
Connection Check = SINGLE or Channel Detection Results Match	Refer to Port Detect Result

More on Operating Modes

The port's operating mode determines when the LTC4291-1/LTC4292 runs a detection cycle. In manual mode, the port will idle until the host orders a detect cycle. It will then run detection, report the result, and return to idle to wait for another command.

In semi-auto mode the LTC4291-1/LTC4292 autonomously polls a port for PDs, but it will not apply power until commanded to do so by the host. The Port Status and Channel Status registers are updated at the end of each detection/classification cycle.

In semi-auto mode, if a valid signature resistance is detected and classification is enabled, the port will classify the PD and report that result as well. The port will then wait for at least 100ms, and will repeat the detection cycle to refresh the data in the Port Status registers.

The port will not turn on in response to a power-on command unless the current detect result is Detect Good. Any other detect result will generate a t_{START} fault if a power-on command is received.

Behavior in auto mode is similar to semi-auto; however, after Detect Good is reported and the port is classified, it is automatically powered on without host intervention. In auto mode the I_{CUT-2P}, I_{LIM-2P}, and P_{CUT-4P} thresholds are automatically set; see the Reset and the AUTO Pin section for more information.

Detection is disabled for a port when the LTC4291-1/LTC4292 is initially powered up with AUTO low, when the port is in shutdown mode, or when the corresponding Detect Enable bit is cleared.

Detection of Legacy PDs

Proprietary PDs that predate the original IEEE 802.3af standard are commonly referred to today as legacy PDs. One type of legacy PD uses a large common-mode capacitance (>10µF) as the detection signature. Note that PDs in this range of capacitance are defined as invalid, so a PSE that powers legacy PDs is noncompliant with the IEEE standard. The LTC4291-1/LTC4292 can be configured to detect this type of legacy PD. Legacy detection is disabled by default, but can be manually enabled on a per-port basis. When enabled, the port will report Detect Good when it sees either a valid IEEE PD or a high-capacitance legacy PD. With legacy mode disabled, only valid IEEE PDs will be recognized.

If a nonstandard PD presents an invalid detection signature not included by legacy detection, the LTC4291-1/LTC4292 may be configured to perform classification and/or apply power regardless of detection result. To accomplish this, the LTC4291-1/LTC4292 introduces per-port Force Power and Class Event overrides. These overrides intentionally defeat compliance checks. See the LTC4291 Software Programming documentation for details.

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Classification

802.3af Classification

A PD may optionally present a classification signature to the PSE to indicate the maximum power it will draw while operating. The IEEE specification defines this signature as a constant current draw when the PSE port voltage is in the V_{CLASS} range (between 15.5V and 20.5V) as shown in Figure 15, with the current level indicating one of five possible PD signatures. Figure 14 shows a typical PD load line, starting with the slope of the 25k signature resistor below 10V, then transitioning to the classification signature current (in this case, Class 3) in the V_{CLASS} range. Table 8 shows the possible classification values.

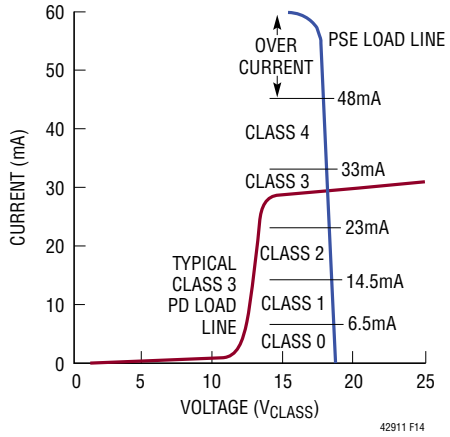

Figure 14. PD Classification

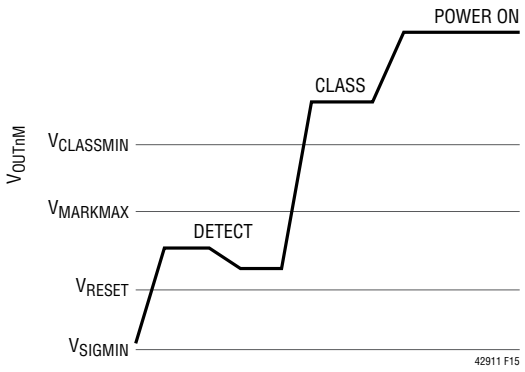

Figure 15. Type 1 PSE, 1-Event Class Sequence

Table 8. Type 1 and Type 2 PD Classification Values

CLASS	RESULT
Class 0	No Class Signature Present; Treat Like Class 3
Class 1	3.84W
Class 2	6.49W
Class 3	13W
Class 4	25.5W (Type 2)

If classification is enabled, the PSE will classify the PD immediately after a successful detection cycle. The PSE measures the PD classification signature by applying V_{CLASS} to the port via OUTnM and measuring the resulting current; it then reports the discovered class in the Port Status or Channel Status register, as appropriate. If the LTC4291-1/LTC4292 is in auto mode, it will additionally use the classification result to set the I_{CUT-2P}, I_{LIM-2P}, and P_{CUT-4P} thresholds.

Classification is disabled for a port when the LTC4291-1/LTC4292 is initially powered up with the AUTO pin low, when the port is in shutdown mode, or when the corresponding Class Enable bit is cleared.

LLDP Classification

Introduced in 802.3at and extended by 802.3bt, the PoE specification defines a Link Layer Discovery Protocol (LLDP) method of classification. The LLDP method adds extra fields to the Ethernet LLDP data protocol.

Although the LTC4291-1/LTC4292 is compatible with this classification method, it cannot perform LLDP classification directly since it does not have access to the data path. LLDP classification allows the host to perform LLDP communication with the PD and update the PD's power allocation. The LTC4291-1/LTC4292 supports changing the I_{LIM-2P}, I_{CUT-2P}, and P_{CUT-4P} levels dynamically, enabling system-level LLDP support.

802.3at 2-Event Classification

In 802.3at, 802.3af classification is named Type 1 classification. The 802.3at standard introduces an extension of Type 1 classification: Type 2 (2-event) classification. Type 2 PSEs are required to perform classification.

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A Type 2 PD requesting 25.5W presents class signature 4 during all class events. If a Type 2 PSE with 25.5W of available power sees class signature 4 during the first class event, it forces the PD to V_{MARK} (9V typical), pauses briefly, and issues a second class event as shown in Figure 16. The second class event informs the PD that the PSE has allocated 25.5W.

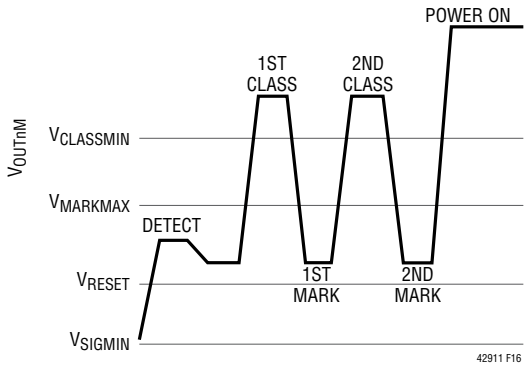

Figure 16. Type 2 PSE, 2-Event Class Sequence

Note that the second classification event only runs if required by the IEEE classification procedure. For example, a single-signature Class 0 to 3 PD will only be issued a single class event in all situations.

The concept of demotion is introduced in 802.3at. A Type 2 PD may be connected to a PSE only capable of delivering 13W, perhaps due to power management limitations. In this case, the PSE will perform a single classification event as shown in Figure 15, and note that 25.5W is requested. Due to the limited power availability, the PSE will not issue a second event and proceeds directly to power on the PD. The presence of a single class event informs the Type 2 PD it has been demoted to 13W. If demoted, the PD is subject to power limitations and may operate in a reduced power mode.

802.3bt Multi-Event Classification

The LTC4291-1/LTC4292 implements Type 3 and Type 4 classification, as required by 802.3bt. Type 3 and Type 4 classification are backwards-compatible with Type 1 and Type 2 PDs.

While Type 2 (802.3at) classification extends Type 1 (802.3af) classification, Type 3 and Type 4 (802.3bt) classification supersede Type 1 and Type 2 classification. Type 1 and Type 2 classification are described in the preceding sections as a historical reference and to define common terminology such as power demotion, class events, mark events, and electrical parameters.

IEEE 802.3bt defines eight PD Classes for single-signature PDs and five PD Classes for dual-signature PDs, as shown in Table 9.

Classification treatment of single-signature and dual-signature PDs differs. The following sections explain the Physical Layer classification of each PD configuration separately.

Table 9. Type 3 and Type 4 PD Classifications by PD Configuration

SINGLE-SIGNATURE PDs		DUAL-SIGNATURE PDs	
CLASS	PD AVAILABLE POWER	CLASS	CHANNEL AVAILABLE POWER*
Class 1	3.84W	Class 1	3.84W
Class 2	6.49W	Class 2	6.49W
Class 3	13W	Class 3	13W
Class 4	25.5W	Class 4	25.5W
Class 5	40W	Class 5	35.6W
Class 6	51W		
Class 7	62W		
Class 8	71.3W		

*Dual-signature PD total available power is the sum of both channels available power. Class signatures may differ between channels of a port, e.g., Class 3 + Class 4 = 13W + 25.5W = 38.5W.

802.3bt Classification of Single-Signature PDs

Type 3 and Type 4 PSEs issue a single classification event (see Figure 17) to Class 0 through 3 single-signature (SS) PDs. A Class 0 through 3 SS PD presents its class signature to the PSE and is then powered on if sufficient power is available. Power limited 802.3bt PSEs may also issue a single classification event to Class 4 and higher SS PDs in order to demote those PDs to 13W. See Figure 17.

Type 3 and 4 PSEs present three classification events to Class 4 SS PDs (see Figure 18) if sufficient power is available. Class 4 SS PDs present class signature 4 on all events. The third event differentiates a Class 4 SS PD from a higher Class SS PD. Power limited IEEE 802.3bt

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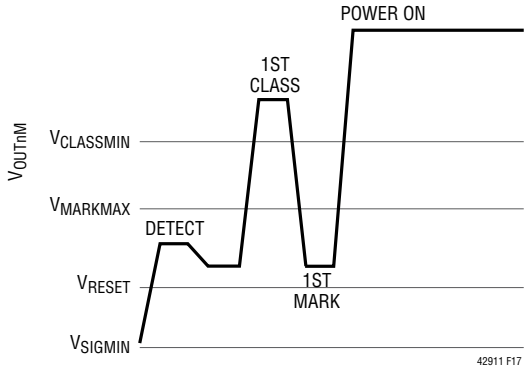

Figure 17. Type 3 or 4 PSE, 1-Event Class Sequence

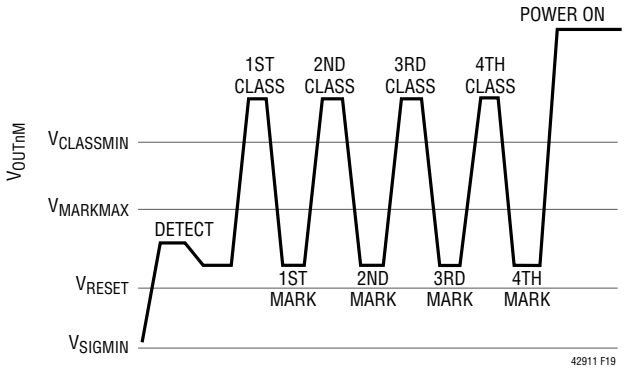

Figure 19. Type 3 or 4 PSE, 4-Event Class Sequence

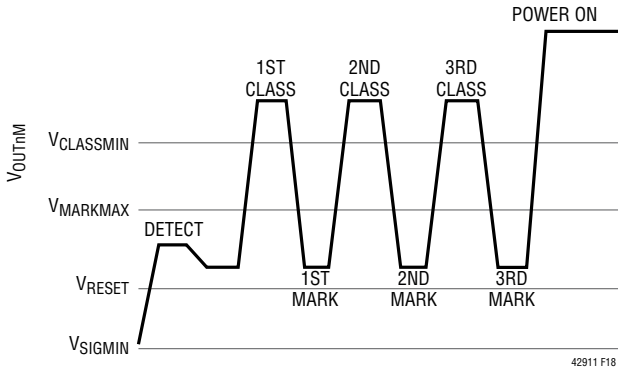

Figure 18. Type 3 or 4 PSE, 3-Event Class Sequence

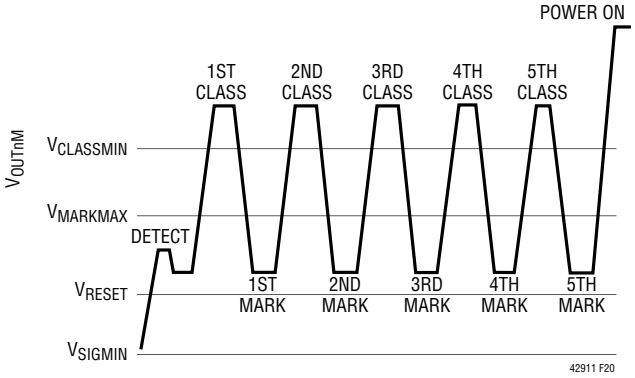

Figure 20. Type 4 PSE, 5-Event Class Sequence

PSEs may issue three classification events to Class 5 and higher SS PDs in order to demote those PDs to 25.5W.

Type 3 and 4 PSEs present four classification events (see Figure 19) to Class 5 and 6 SS PDs if sufficient power is available. Class 5 and 6 SS PDs present class signature 4 on the first two events. Class 5 and 6 SS PDs present class signature 0 or 1, respectively, on the subsequent events. Power limited PSEs may issue four events to Class 7 and 8 SS PDs in order to demote those PDs to 51W.

Type 4 PSEs present five classification events (see Figure 20) to Class 7 and 8 SS PDs if sufficient power is available. Class 7 and 8 PDs present class signature 4 on the first two events. Class 7 and 8 SS PDs present class signature 2 or 3, respectively, on the subsequent events.

802.3bt Classification of Dual-Signature PDs

Classification and power allocations to each pairset of a dual-signature (DS) PD are fully independent. For example, a DS PD may request Class 1 (3.84W) on one pairset and a Class 4 (25.5W) on the second pairset for a total PD requested power of 29.3W. As such, all classification is performed to the pairset entity as opposed to the PD. The terms should be considered interchangeable for the remainder of this section.

Type 3 and Type 4 PSEs issue three classification events (see Figure 18) to all Class 1 through 4 DS PDs.

Power limited Type 3 and Type 4 PSEs may issue a class reset to Class 4 and 5 DS PDs in order to demote those PDs to 13W (see Understanding 4PID section).

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Power limited Type 3 and Type 4 PSEs may issue only three events to Class 5 DS PDs in order to demote those PDs to 25.5W.

Type 4 PSEs present four classification events (see Figure 19) to Class 5 DS PDs if sufficient power is available. Class 5 DS PDs present class signature 4 on the first two events and class signature 3 on subsequent events.

Understanding 4PID

4-pair identification (4PID) refers to a set of conditions for determining whether a PD is capable of receiving power over both pairsets simultaneously.

The PSE may apply 4-pair power if the PD presents a valid detection signature on both pairsets and one or more of the following conditions are met:

- The PD is single-signature configuration.
- The PD is Type 3 or Type 4.
- The PD presents a valid detection signature on an unpowered pairset when power is applied over the other pairset.

Although PD signature configuration is not defined for Type 1 and Type 2 PDs, a Type 3 or Type 4 PSE may identify such a PD as single-signature or dual-signature. Single-signature PDs may receive 4-pair power regardless of PD Type. Certain pre-802.3bt “dual-signature” PDs may be damaged by 4-pair power.

Type 3 and Type 4 dual-signature PDs are required to present a unique classification response from pre-802.3bt dual-signature PDs of the same Class. For dual-signature PDs, the LTC4291-1/LTC4292 determines and reports both PD Class and PD Type during classification.

Type 3, Type 4, and pre-802.3bt Class 1 through Class 4 dual-signature PDs present class signature 1 through 4, respectively, during the first and second class events. Type 3 and Type 4 dual-signature PDs present class signature 0 for all subsequent class events. Thus, a PSE can conclusively determine PD Type by the third class event for all dual-signature PDs.

An issue arises when a Class 4 or Class 5 dual-signature PD is connected. In order to determine PD Type, three class events are issued. Based on the class event count, the PD has been allocated 25.5W. If the PSE desires to both determine PD Type (3 events) and demote to 13W (1 event), a class reset event must be issued as shown in Figure 21.

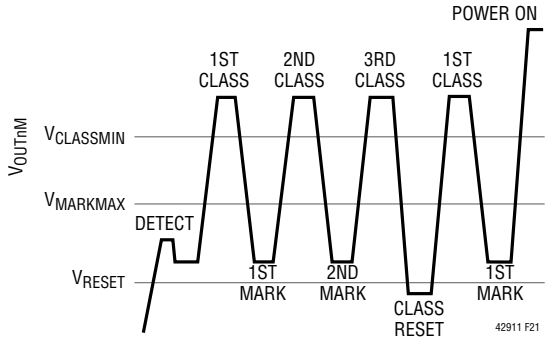

Figure 21. Class Reset Event Between Class Sequences

A class reset event is issued by maintaining the channel voltage below 2.8V for at least t_{CLASS_RESET}. The subsequent single event classification is used to demote the PD to 13W.

In auto mode the 4PID information and the state of $\overline{4PVALID}$ are used to automatically determine the number of powered channels.

LLDP signaling may, at some time later, determine the pre-bt PD is actually four pair capable and the LTC4291-1/LTC4292 may be instructed to deliver 4-pair power.

Invalid Multi-Event Classification Combinations

The 802.3bt specification defines a set of valid class signature combinations. All PDs return the same classification signature on the first two class events. Type 3 and 4 PDs modify the classification signature on all subsequent class events. For example, a single-signature Class 5 PD will respond to the class events 1, 2, 3, and 4 with a class signature of 4, 4, 0, and 0, respectively.

Any individual class signature that exceeds the class current limit is flagged as an invalid classification result. Any sequence of class signatures that does not represent a legal sequence based on PD configuration will likewise be flagged as an invalid classification result.

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Auto Mode Maximum PSE Power

In auto mode the LTC4291-1/LTC4292 automatically detects, classifies and powers all connected valid PDs. In order to do this, the PSE must be configured for its maximum power allocation. The maximum power allocation is a reflection of the power supply and power path capability. The PWRMD pins must be set appropriately to reflect the PSE system's power delivery capabilities. These pins are sampled at reset.

Table 10. Auto Mode Maximum Delivered Power Capabilities

PWRMD1	PWRMD0	MAX PORT POWER (SINGLE-SIGNATURE)	MAX PAIRSET POWER (DUAL-SIGNATURE)
0	0	40W	13W
0	1	51W	25.5W
1	0	62W	25.5W
1	1	71.3W	35.6W

POWER CONTROL

The primary function of the LTC4291-1/LTC4292 is to control power delivery to the PSE port. With the LTC4291-1/LTC4292, a PSE port is composed of two power channels; each power channel controls power delivery over a pairset. Within this section, power delivery and control are defined per-channel.

The LTC4291-1/LTC4292 delivers power by controlling the gate drive voltage of an external power MOSFET while monitoring the current (through an external sense resistor) and the output voltage (across the OUT pin).

The LTC4291-1/LTC4292 connects the V_{EE} power supply to the PSE port in a controlled manner, meeting the power demands of the PD while minimizing power dissipation in the external MOSFET and disturbances to the V_{EE} backplane.

Inrush Control

When commanded to apply power to a port, the LTC4291-1/LTC4292 ramps up the GATE pin of one or both channels (as commanded), raising the external MOSFET gate voltage in a controlled manner.

During a typical inrush, the MOSFET gate voltage will rise until the external MOSFET is fully enhanced or the channel reaches the inrush current limit ($I_{INRUSH-2P}$). $I_{INRUSH-2P}$ is set automatically by the PSE. When the PSE is applying 4-pair power to a single-signature PD assigned Class 0 to Class 4, $I_{INRUSH-2P}$ is 212.5mA (typical) per channel (LIMn = 08h). Otherwise, $I_{INRUSH-2P}$ is 425mA (typical) per channel (LIMn = 80h).

The GATE pin will be servoed if channel current exceeds $I_{INRUSH-2P}$, actively limiting current to $I_{INRUSH-2P}$. When the GATE pin is not being servoed, the final VGS is 12V (typical).

During inrush, each powered channel runs a timer (t_{START}). Each powered channel stays in inrush until t_{START} expires. When t_{START} expires, the PSE inspects channel voltage and current. When the PSE is applying power to a PD, inrush is successful if the channel(s) are drawing current below $I_{INRUSH-2P}$, as appropriate per the PD configuration and Class.

If inrush is not successful, power is removed and the corresponding t_{START} faults are set. Otherwise, the port or channel, as appropriate, advances to power on and the programmed current limiting thresholds are used as described in the Current Limit section.

Port Power Policing

The power policing threshold (P_{CUT-4P}) is monitored on a per-port basis, up to 128W in 0.5W increments (typical). When the total output power over a one second moving average exceeds the specified threshold, power will be removed from the port and the corresponding t_{CUT} faults are set.

In particular, the port policing feature may be used to ensure delivery of PD Class power while staying below 100W Limited Power Source (LPS) requirements.

Current Cutoff and Limit

Each LTC4291-1/LTC4292 port includes two current limiting thresholds (I_{CUT-2P} and I_{LIM-2P}), each with a corresponding timer (t_{CUT} and t_{LIM}). Setting the I_{CUT-2P} and I_{LIM-2P} thresholds depends on several factors: the PD

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assigned Class, the main supply voltage (V_{EE}), the PSE Type (Type 3 or 4), and the MOSFET SOA.

A single set of programmable port I_{CUT-2P} and I_{LIM-2P} thresholds is shared by both channels. The thresholds should be set based on the classification result as shown in Table 4 and Table 5. For a dual-signature PD assigned unequal Classes, the highest Class is used to set the thresholds. For example, a dual-signature PD assigned Class 1 and Class 5 would enforce I_{CUT-2P} and I_{LIM-2P} based on Class 5.

Per the IEEE specification, the LTC4291-1/LTC4292 will allow the channel current to exceed I_{CUT-2P} for a limited period of time before removing power from the port, or channel, as appropriate whereas it will actively control the MOSFET gate drive to keep the channel current below I_{LIM-2P}. The channel does not take any action to limit the current when only the I_{CUT-2P} threshold is exceeded, but does start the t_{CUT} timer. If the current drops below the I_{CUT-2P} threshold before its timer expires, the t_{CUT} timer counts back down, but at 1/16 the rate that it counts up. If the t_{CUT} timer reaches 59ms (typical), the port or channel, as appropriate, is turned off and the corresponding t_{CUT} faults are set. This allows the channel to tolerate intermittent overload signals with duty cycles below about 6%; longer duty cycle overloads will remove power from the port or channel, as appropriate.

The I_{LIM-2P} current limiting circuit is always enabled and actively limiting channel current. The t_{LIM} timer is enabled only when the t_{LIM} Timer Configuration field is set to a non-zero value. This allows t_{LIM} to be set to a shorter value than t_{CUT} to provide more aggressive MOSFET protection and turn off a port before MOSFET damage can occur. The t_{LIM} timer starts when the I_{LIM-2P} threshold is exceeded. When the t_{LIM} timer reaches 1.7ms (typical) times the value in the t_{LIM} Timer Configuration field, the port or channel, as appropriate, is turned off and the appropriate t_{LIM} faults are set. When the t_{LIM} Timer Configuration field is set to 0, t_{LIM} behaviors are tracked by the t_{CUT} timer, which counts up during both I_{LIM-2P} and I_{CUT-2P} events. To maintain IEEE compliance, the programmed t_{LIM} Timer Configuration field should be set as shown in the LTC4291 Software Programming documentation.

I_{CUT-2P} is typically set to a lower value than I_{LIM-2P}, allowing the port to tolerate minor faults without current limiting.

To maintain IEEE compliance, the programmed I_{LIM-2P} should be set as shown in Tables 4 and 5. The programmed I_{LIM-2P} setting is automatically applied following the completion of inrush.

The t_{CUT} and t_{LIM} timers are maintained on a per channel basis. When a t_{CUT} or t_{LIM} fault occurs a determination is made to turn off one or both channels. See the Port Fault vs Channel Fault section for details.

I_{LIM-2P} Foldback

The LTC4291-1/LTC4292 I_{LIM-2P} threshold is implemented as a two-stage foldback circuit that reduces the channel current if the channel voltage falls below the normal operating voltage. This keeps MOSFET power dissipation at safe levels. Current limit and foldback behavior are programmable on a per-port basis.

The LTC4291-1/LTC4292 supports current levels well beyond the maximum values in the 802.3bt specification. Large values of I_{LIM-2P} may require larger external MOSFETs, additional heat sinking, and setting the t_{LIM} Timer Configuration field to a lower value.

MOSFET Fault Detection

LTC4291-1/LTC4292 PSE ports are designed to tolerate significant levels of abuse, but in extreme cases it is possible for an external MOSFET to be damaged. A failed MOSFET may short source to drain, which will make the port appear to be on when it should be off; this condition may also cause the sense resistor to fuse open, turning off the port but causing SENSE to rise to an abnormally high voltage. A failed MOSFET may also short from gate to drain, causing GATE to rise to an abnormally high voltage. OUT, SENSE and GATE are designed to tolerate up to 80V faults without damage.

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If the LTC4291-1/LTC4292 sees a power good condition on either channel of an unpowered port (neither channel powered), it disables all port functionality, reduces the gate drive pull-down current for the port and reports a FET Bad fault. This is typically a permanent fault, but the host can attempt to recover by resetting the port, or by resetting the entire chip if a port reset fails to clear the fault. If the MOSFET is in fact bad, the fault will quickly return, and the port will disable itself again. The remaining ports of the LTC4291-1/LTC4292 are unaffected.

An open or missing MOSFET will not trigger a FET Bad fault, but will cause a t_{START} fault if the LTC4291-1/LTC4292 attempts to turn on the port.

Disconnect

The LTC4291-1/LTC4292 monitors powered channels to ensure the PD continues to draw the minimum specified current. The $I_{HOLD-2P}$ threshold, monitored as the $V_{HOLD-2P}$ threshold across the 0.15Ω sense resistor, is used to determine if a PD has been disconnected.

The $I_{HOLD-2P}$ threshold is set automatically in auto mode and is set by the user in semi-auto and manual modes. When powering a single-signature PD assigned Class 0 to Class 4 over a single channel, set the $I_{HOLD-2P}$ threshold to 7.5mA (typ) via the Disconnect Configuration bit. In all other cases, set the $I_{HOLD-2P}$ threshold to 3.5mA (typ).

A disconnect timer (t_{DIS}) counts up whenever channel current is below the $I_{HOLD-2P}$ threshold, indicating that the PD has been disconnected. If the appropriate t_{DIS} timer(s) expire, the port or channel (Table 11) will be turned off and the corresponding t_{DIS} faults are set. If the current increases above $I_{HOLD-2P}$ before the t_{DIS} timer expires, the timer(s) reset. As long as the PD exceeds the minimum current level before t_{DIS} expires, it will remain powered.

Although not recommended, the DC disconnect feature can be disabled by clearing the corresponding DC Disconnect Enable bits. Disabling the DC disconnect feature forces the LTC4291-1/LTC4292 out of compliance with the IEEE standard. A powered port will stay powered after the PD is removed; the still-powered port may be subsequently connected to a non-PoE data device, potentially causing damage.

The LTC4291-1/LTC4292 does not include AC disconnect circuitry. AC disconnect is not a supported feature of 802.3bt.

Port Fault vs Channel Fault

The t_{CUT}, t_{LIM} and t_{DIS} timers are maintained on a per-channel basis. When any channel timer expires, a determination is made to remove power from both, one, or neither channel of the port.

Optional behavior is allowed by the 802.3bt standard when faults occur on single-signature PDs. This option allows a single-signature PD to remain powered on pairset X, even if a fault occurs on pairset Y. The FAULT2Pn bit, when set, enables this optional behavior. This behavior is not recommended for normal operation, as a fault in the PD or cabling is indicative of imminent PD or cable failure.

Table 11. Channel Fault Effect on Port/Channel State

PD CONFIGURATION	FAULT2Pn	FAULT RESULT: TURN OFF PORT OR CHANNEL		
		t_{CUT}**	t_{LIM}	t_{DIS}
Single	0	Port	Port	Port*
	1	Channel	Channel	
Dual	x	Channel	Channel	Channel

*If t_{DIS} Expires on Both Channels

**Port power policing (P_{CUT-4P}) raises a t_{CUT} event. When enabled, port power policing removes power from the port regardless of FAULT2Pn configuration.

Fault Telemetry

As discussed in the preceding sections, faults may occur on one or both channels, resulting in power removal on one or both channels. The fault event registers have traditionally been implemented at the port level. In order to trace faults to the offending channel, a second layer of fault registers have been added to the LTC4291-1/LTC4292: the Fault Telemetry registers. See the LTC4291 Software Programming documentation for additional information.

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Autoclass

IEEE 802.3bt introduces a new optional feature, Autoclass. Autoclass enables the PSE to reclaim power budget from single-signature PDs requesting more power than needed under worst-case operating conditions. 802.3bt does not specify Autoclass for dual-signature PDs. The LTC4291-1/LTC4292 fully supports Autoclass.

Prior versions of the 802.3 PoE standard specify minimum PSE output power for worst-case IR drop across the Ethernet cable and minimum PSE output voltage. However, a method for the PSE to reclaim over-allocated power is not specified. When a shorter Ethernet cable is used, or when the guaranteed PSE output voltage is above the specified minimum, the specified minimum PSE output power substantially over-allocates power to the PD.

An example PoE system is shown in two versions. Figure 22 shows a 100W four port PSE servicing three 25.5W PDs over 100m cables. Such a system requires the PSE to allocate 25.5W per PD and a further 4.5W for each 100m cable's IR drop.

The total power allocation is:

3 Ports • (4.5W + 25.5W) = 90W

If an additional 13W PD is plugged into the fourth PSE port, only 10W is available and the PD cannot be powered.

Figure 23 shows a 100W four port PSE servicing three 25.5W PDs over 10m cables. Such a system requires the PSE to allocate 25.5W per PD and a further ~0.5W for each 10m cable's IR drop.

Without Autoclass, the total power allocation is:

3 ports • (4.5W + 25.5W) = 90W

If an additional 13W PD is plugged into the fourth PSE port, only 10W is available and the PD cannot be powered even though the IR drop is much less than in the prior example.

Assuming the system in Figure 23 is Autoclass-enabled, the recovered power budget can be used to power additional ports. During classification, the PSE observes the PD's Autoclass request. After power on is completed, the PD draws its maximum power while the PSE performs an Autoclass measurement, as specified by 802.3bt. The PSE in Figure 23 will measure and report 26W of power consumption for each of the three 25.5W PDs. This result allows the host to revise the PSE available power budget.

With Autoclass, the total power allocation for Figure 23 is:

3 Ports • 26W (Measured) = 78W

If an additional 13W PD is plugged into the fourth PSE port, a full 22W is now available and the PD can be successfully powered.

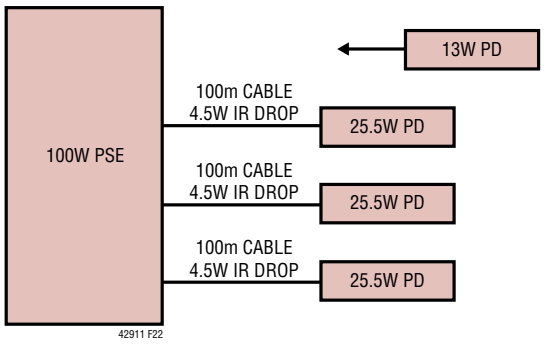

Figure 22. 100W PoE System with 100m Cables

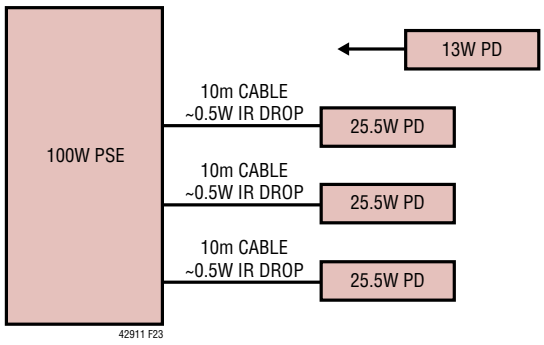

Figure 23. 100W PoE System with 10m Cables

APPLICATIONS INFORMATION

Autoclass Negotiation Procedure

A PSE may receive an Autoclass request from the PD by Physical Layer classification or LLDP (by way of the PSE host). For Physical Layer requests, the Autoclass negotiation procedure listed below is shown in Figure 24.

1. PSE begins issuing the long first class event. The PD class signature is allowed to settle during this time.
2. The PD responds with a class signature corresponding to its Class. The class signature during this time period is unrelated to the Autoclass negotiation.
3. The PSE measures the PD class signature during this time and uses the result for the normal Multi-event Classification.
4. The PD continues presenting its class signature.
5. The PSE continues the long class event and does not measure the class signature current at this time.
6. The PD, if requesting Autoclass, transitions to class signature 0. If the PD is not requesting Autoclass it continues presenting its class signature.

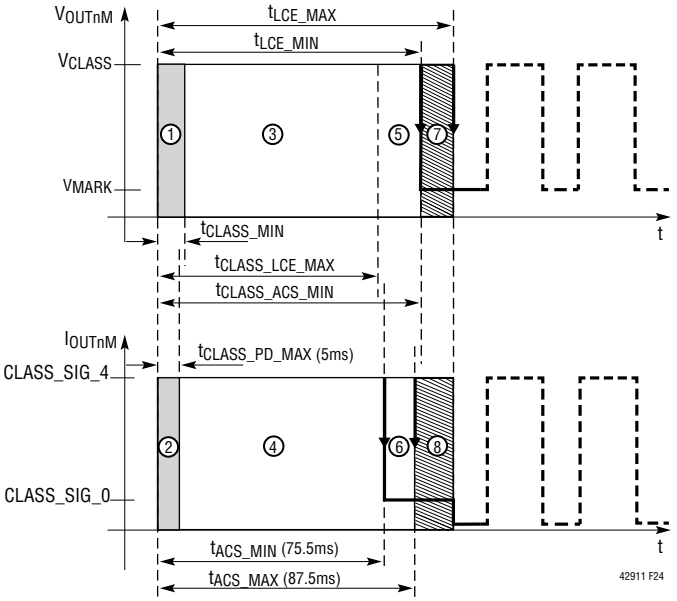

Figure 24. Autoclass Negotiation, Voltage and Current

7. The PSE measures the Autoclass response of the PD. If class signature 0 is measured, the PD is requesting Autoclass. When the measurement is complete the first class event is ended.
8. The PD continues holding the class signature selected in step 6 until the end of the first class event.

Following the Autoclass negotiation procedure, PSE and PD continue Physical Layer classification and power up as normal. Regardless of Autoclass, the PD is required to operate below the negotiated power allocation corresponding to PD assigned Class.

Autoclass Measurement Procedure

Autoclass measurements may be requested by the PD through Physical Layer classification or, following power on, through LLDP. Although the LTC4291-1/LTC4292 is compatible with LLDP-based Autoclass requests, it cannot receive LLDP Autoclass requests directly since it does not have access to the data path.

If the PSE is commanded to perform an Autoclass measurement following a Physical Layer request, the measurement typically begins t_{AUTO_PSE1} (1.5s typical) after port inrush is successfully completed. For LLDP-based Autoclass requests, the measurement begins immediately.

The Autoclass measurement period is $t_{AUTO\_PSE2} - t_{AUTO\_PSE1}$ (1.8s typical) using a sliding window of t_{AUTO_WINDOW} (0.2s typical). During the Autoclass measurement period, the PSE continuously monitors I_{PORT} and V_{EE}, calculating maximum average power. Following the Autoclass measurement period, the Autoclass measurements are reported in the Port Parametric registers.

See the LTC4291 Software Programming documentation for details on enabling Autoclass, the status of the Autoclass negotiation, reading Autoclass measurement results and dynamically requesting an Autoclass measurement.

Port Current Readback

The LTC4291-1/LTC4292 measures the current at each power channel with per-channel A/D converters. The total port current (sum of both channels) is reported. Port

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current is only valid when at least one power channel of a port is on and reads zero at all other times. The converter has two modes:

- 100ms mode: Samples are taken continuously and the measured value is updated every 100ms
- 1s mode: Samples are taken continuously; a moving 1 second average is updated every 100ms

V_{EE} Readback

The LTC4291-1/LTC4292 continuously measures the V_{EE} voltage with a dedicated A/D converter. This global V_{EE} measurement is fully synchronized to all port current measurements.

Port Power Readback

The LTC4291-1/LTC4292 provides fully continuous and synchronized port power measurements. The LTC4291-1/LTC4292 calculates the port power by multiplying the port current and V_{EE} measurements.

$$P_{PORT} = I_{PORT} \times V_{EE}$$

The Port Power measurements replace the Port Voltage measurements provided in prior ADI PSEs. Port voltage may be characterized and extrapolated from the V_{EE} measurement in a user-defined manner.

Masked Shutdown

The LTC4291-1/LTC4292 provides a low latency port shedding feature to quickly reduce the system load when required. By allowing a pre-determined set of ports to be turned off, the current on an overloaded main power supply can be reduced rapidly while keeping high priority devices powered. Each port can be configured to high or low priority; all low-priority ports will shut down within 6.5µs after $\overline{MSD}$ is pulled low, high priority ports will remain powered. If a port is turned off via $\overline{MSD}$, the corresponding Detection and Classification Enable bits are cleared, so the port will remain off until the host explicitly re-enables detection.

In the LTC4291-1/LTC4292 chipset, the active level of $\overline{MSD}$ is register configurable as active high or low. The default behavior is active low.

General Purpose IO

Two general purpose IO pins, GP0 and GP1 are available on the LTC4291-1. These fully bidirectional IO pins use 3.3V CMOS logic.

Code Download

The LTC4291-1 includes a default firmware image, enabling 802.3bt-compliant operation with no user intervention required. In addition, the LTC4291-1 firmware is field-upgradable by downloading and executing firmware images. Firmware images are volatile and must be re-downloaded after each V_{DD} power cycle, but will remain valid during reset and V_{EE} power events.

The LTC4291-1 is intended for use with Analog Devices firmware images only. Contact Analog Devices for code download procedures and firmware images.

SERIAL DIGITAL INTERFACE

Overview

The LTC4291-1 communicates with the host using a standard SMBus/I^2C 2-wire interface. The LTC4291-1 is a slave-only device, and communicates with the host master using standard SMBus protocols. Interrupts are signaled to the host via $\overline{INT}$. The Timing Diagrams (Figure 5 through Figure 9) show typical communication waveforms and their timing relationships. More information about the SMBus data protocols can be found at www.smbus.org.

The LTC4291-1 requires both the V_{DD} and V_{EE} supply rails to be present for the serial interface to function.

Bus Addressing

The LTC4291-1's primary 7-bit serial bus address is $010A_3A_2A_1A_0b$, with the lower four bits set by AD3 – AD0; this allows up to 16 LTC4291-1s on a single bus. Sixteen LTC4291-1s are equivalent to 64 ports. All LTC4291-1s also respond to the broadcast address 0110000b, allowing the host to write the same command (typically configuration commands) to multiple LTC4291-1s in a single transaction.

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If the LTC4291-1 is asserting $\overline{INT}$, it will also respond to the alert response address (0001100b) per the SMBus specification.

Each LTC4291-1/LTC4292 is logically composed of a single four port quad, packed into a single I^2C address.

Interrupts and SMBAlert

Most port events can be configured to trigger an interrupt, asserting $\overline{INT}$ and alerting the host to the event. This removes the need for the host to poll the LTC4291-1, minimizing serial bus traffic and conserving host CPU cycles. Multiple LTC4291-1s can share a common $\overline{INT}$ line, with the host using the SMBAlert protocol (ARA) to determine which LTC4291-1 caused an interrupt.

Register Description

For information on serial bus usage and device configuration and status, refer to the LTC4291 Software Programming documentation. Contact Analog Devices to request this document.

ISOLATION REQUIREMENTS

IEEE 802.3 Ethernet specifications require that network segments (including PoE circuitry) be electrically isolated from the chassis ground of each network interface device. However, network segments are not required to be isolated from each other, provided that the segments are connected to devices residing within a single building on a single power distribution system.

For simple devices, such as small PoE switches, the isolation requirement can be met by using an isolated main power supply for the entire device. This strategy can be used if the device has no electrically conducting ports other than twisted-pair Ethernet. In this case, the SDAIN and SDAOUT pins can be tied together and will act as a standard I^2C/SMBus SDA pin.

If the device is part of a larger system, contains additional external non-Ethernet ports, or must be referenced to protective ground for some other reason, the PoE subsystem must be electrically isolated from the rest of the system.

The LTC4291-1/LTC4292 chipset simplifies PSE isolation by allowing the LTC4291-1 chip to reside on the non-isolated side. There it can receive power from the main logic supply and connect directly to the I^2C/SMBus bus. Isolation between the LTC4291-1 and LTC4292 is implemented using a proprietary transformer-based communication protocol. Additional details are provided in the Serial Bus Isolation section of this data sheet.

EXTERNAL COMPONENT SELECTION

Power Supplies

The LTC4291-1/LTC4292 requires two supply voltages to operate. V_{DD} requires 3.3V (nominally) relative to DGND. V_{EE} requires a negative voltage of between –51V to –57V for Type 3 PSEs, or –53V to –57V for Type 4 PSEs, relative to AGNDP.

Digital Power Supply

V_{DD} provides digital power for the LTC4291-1 processor. A ceramic decoupling cap of at least 0.1µF should be placed from V_{DD} to DGND, as close as practical to each LTC4291-1. A 1.8V core voltage supply is generated internally and requires a 1µF ceramic decoupling cap between the CAP1 pin and DGND.

In the LTC4291-1, V_{DD} should be delivered by the host controller's non-isolated 3.3V supply. To maintain required isolation, LTC4292 AGNDP and LTC4291-1 DGND must not be connected in any way.

Main PoE Power Supply

V_{EE} is the main isolated PoE supply that provides power to the PDs. Because it supplies a relatively large amount of power and is subject to significant current transients, it requires more design care than a simple logic supply. For minimum IR loss and best system efficiency, set V_{EE} near maximum amplitude (57V), leaving enough margin to account for transient over or undershoot, temperature drift, and the line regulation specifications of the particular power supply used.

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Bypass capacitance between AGNDP and V_{EE} is very important for reliable operation. If a short circuit occurs at one of the output ports it can take as long as 1µs for the LTC4292 to begin regulating the current. During this time the current is limited only by the small impedances in the circuit; a high current spike typically occurs, causing a voltage transient on the V_{EE} supply and possibly causing the LTC4291-1/LTC4292 to reset due to a UVLO fault. A 1µF, 100V X7R capacitor placed near the V_{EE} and AGNDP pins along with an electrolytic bulk capacitor of at least 47µF across the supply is recommended to minimize spurious resets.

Serial Bus Isolation

The LTC4291-1/LTC4292 chipset uses transformers to isolate the LTC4291-1 from the LTC4292 (see Figure 25). In this case, the SDAIN and SDAOUT pins can be shorted to each other and tied directly to the I^2C/SMBus bus. The transformers should be 10BASE-T or 10/100BASE-T with a 1:1 turns ratio. It is optimal that the selected transformers do not have common-mode chokes. These transformers typically provide 1500V of isolation between the LTC4291-1 and the LTC4292. For proper operation, strict layout guidelines must be met.

External MOSFET

Careful selection of the power MOSFET is critical to system reliability. Choosing a MOSFET requires extensive analysis and testing of the MOSFET SOA curve against the various PSE current limit conditions. ADI recommends the PSMN075-100MSE for PSEs configured to deliver up to 51W maximum port power (single-signature) or 25.5W maximum pairset power (dual-signature). For PSEs configured to power up to 71.3W maximum port power (single-signature) or 35.6W maximum pairset power (dual-signature), ADI recommends the PSMN040-100MSE. These MOSFETs are selected for their proven reliability in PoE applications. Contact ADI Applications before using a MOSFET other than one of these recommended parts.

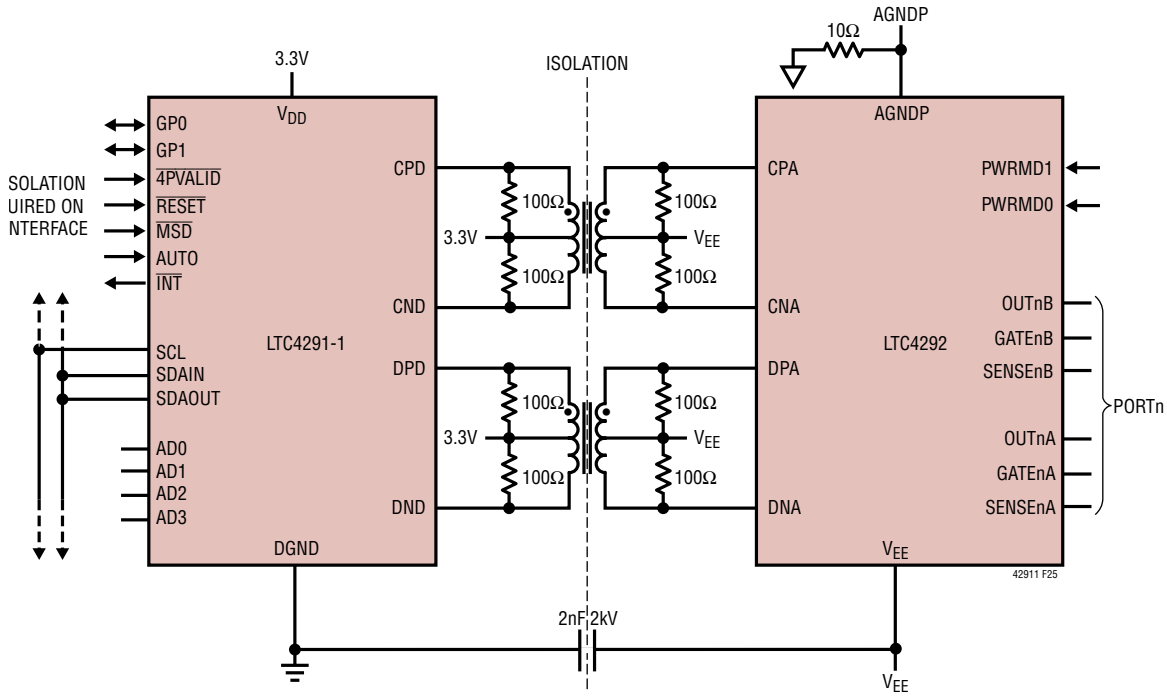

Figure 25. LTC4291-1/LTC4292 Proprietary Isolation

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Sense Resistors

The LTC4291-1/LTC4292 is designed for a low 0.15Ω current sense resistance per channel. Two parallel 0.3Ω resistors must be laid out as shown in the Layout Requirements section. In order to meet the $I_{HOLD-2P}$, I_{CUT-2P}, and I_{LIM-2P} accuracy required by the IEEE specification, the sense resistors should have ±1% tolerance or better, and no more than ±200ppm/°C temperature coefficient.

Port Output Cap

Each port requires a 0.22µF cap across OUTnM to AGNDP (see Figure 25) to keep the LTC4292 stable while in current limit during startup or overload. Common ceramic capacitors often have significant voltage coefficients; this means the capacitance is reduced as the applied voltage increases. To minimize this problem, X7R ceramic capacitors rated for at least 100V are recommended and must be located close to the LTC4292.

Surge Protection

Ethernet ports can be subject to significant cable surge events. To keep PoE voltages below a safe level and protect the application against damage, protection components, as shown in Figure 26, are required at the main supply, at the LTC4292 supply pins, and at each port.

Bulk transient voltage suppression (TVS_{BULK}) and bulk capacitance (C_{BULK}) are required across the main PoE supply and should be sized to accommodate system level surge requirements.

Each LTC4292 requires a 10Ω, 0805 resistor (R1) in series from supply AGND to the LTC4292 AGNDP pin. Across the LTC4292 AGNDP pin and V_{EE} pin is a SMAJ58A 58V TVS (D1) and a 1µF, 100V bypass capacitor (C1). These components must be placed close to the LTC4292 pins.

Finally, each port requires a pair of S1B clamp diodes: one from OUTnM to supply AGND and one from OUTnM to supply V_{EE}. The diodes at the ports steer harmful surges into the supply rails where they are absorbed by the surge suppressors and the V_{EE} bypass capacitance. The layout of these paths must be low impedance.

LAYOUT REQUIREMENTS

Strict adherence to board layout, parts placement and routing requirements is critical for IEEE compliance, parametric measurement accuracy, system robustness and thermal dissipation. Refer to the DC2685A demo kit for example layout references.

Sense Resistor Block Layout Requirements

A channel sense resistor may be affected by currents flowing in other channels. To ensure IEEE parametric compliance, the sense resistor layout is strictly defined and must be adhered to. In addition, the sense resistor block's common V_{EE} plane connections and layout are specified.

Figure 33 shows the component names for ports 1 and 2 as referenced in the remainder of this section. The sense resistors (RST1 to RST4 and RSU1 to RSU4) for channels 1A, 1B, 2A, and 2B must be grouped together in a sense resistor block. The same requirements apply to channel 3A, 3B, 4A, and 4B sense resistors and VSSK34.

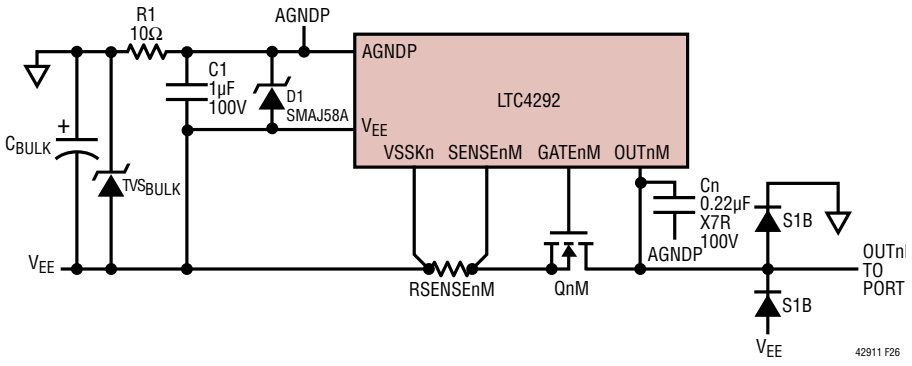


Figure 26. LTC4292 Surge Protection

APPLICATIONS INFORMATION

Figure 27 shows the top layer PCB placement of sense resistors RST1 to RST4. Each bottom layer sense resistor, RSU1 to RSU4, is placed directly underneath its paired top layer sense resistor. The V_{EE}–facing side of the sense resistors connect to a common V_{EE} copper area on the solder pad top edge with a 5mil to 10mil overlap.

Figure 28 shows the top component layer common V_{EE} area copper requirements. On the top layer, the common V_{EE} area copper is extended at the bottom center down to the length of the sense resistor pads to allow copper to flow between the two center sense resistors and bottom center power via. A 10mil keepout is placed around the common V_{EE} copper area and V_{EE} pads of the sense resistors. These instructions for the top component layer are repeated for the bottom component layer.

Figure 29 shows the inner layer 2 (V_{EE} plane) common V_{EE} copper area requirements. A 10mil keepout is placed around the common V_{EE} copper area; the exception is the bottom center where the common V_{EE} area copper opens up to the V_{EE} plane. The common V_{EE} copper area only connects to V_{EE} on layer 2.

Figure 30 shows the inner layer 3 (AGND plane and routing) common V_{EE} area copper requirements. A 10mil keepout is placed around the common V_{EE} copper area to separate it from the surrounding AGND plane.

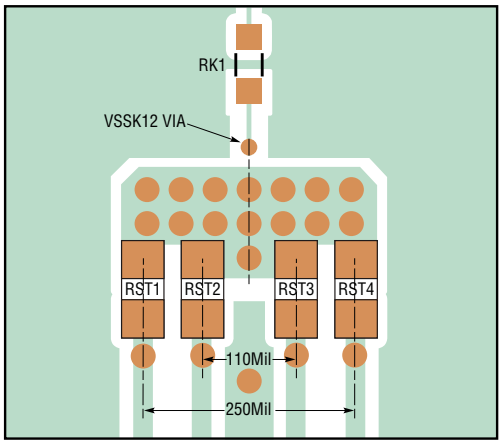
Figure 31 shows the common V_{EE} copper area power via placement. There are 15 power vias in the common V_{EE} copper area and connect the common copper in this area on all four layers. The power vias must be sized to a 17mil drill and 30mil diameter annular ring.

Figure 32 is the PCB layer structure defining the copper thickness requirements for each layer.

Kelvin Sense

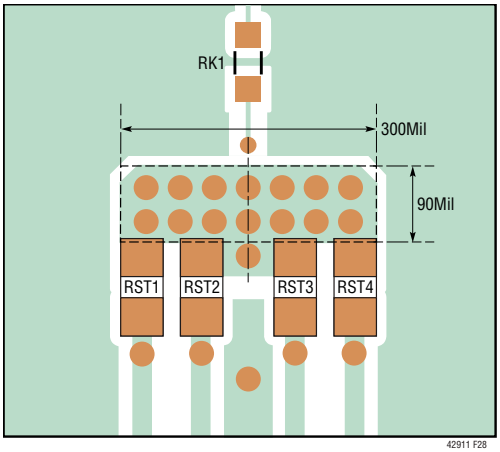
Proper Kelvin sensing must be implemented in the layout. VSSK12 connects to a series resistor RK1 in Figure 33. From RK1 (Figure 28), a Kelvin sense small signal trace connects to V_{EE} only on layer 3 at the centroid top of the sense resistors (RST1 to RST4 and RSU1 to RSU4) common V_{EE} copper area (Figure 30). A 10mil keepout must be placed around the RK1 solder pad that leads to V_{EE} (Figure 28); around the trace from RK1 to the centroid (Figures 28 and 30); on all layers around any vias that connect the trace to different layers (Figures 28, 29, and 30).

At each of the sense resistors, on the side facing SENSEnM, a power via is placed as close to the respective solder pads as allowed by the layout DRC. This power via connects the top and bottom sense resistor pair for a channel. A Kelvin sense small signal trace connects SENSEnM directly to the respective sense resistor pair via shown in Figure 30. A separate power path wide trace connects from the sense resistor pair to the MOSFET. SENSEnM must not connect to anywhere else on the power path between the sense resistor and the MOSFET.



NOTES: DRAWING NOT TO SCALE.
VSSK12 VIA ISOLATED ON TOP AND BOTTOM LAYERS.

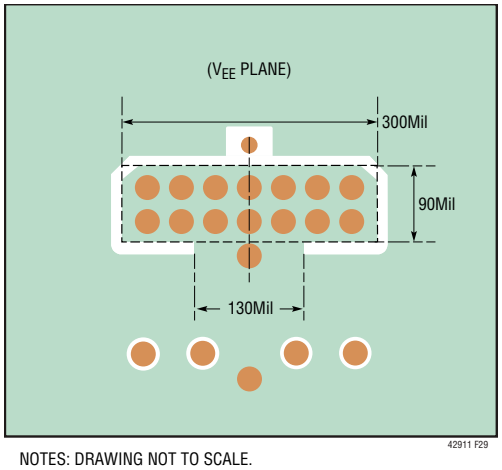
Figure 27. Top Component Layer Sense Resistors Placement



NOTES: DRAWING NOT TO SCALE.
RK1 ONLY ON TOP LAYER.

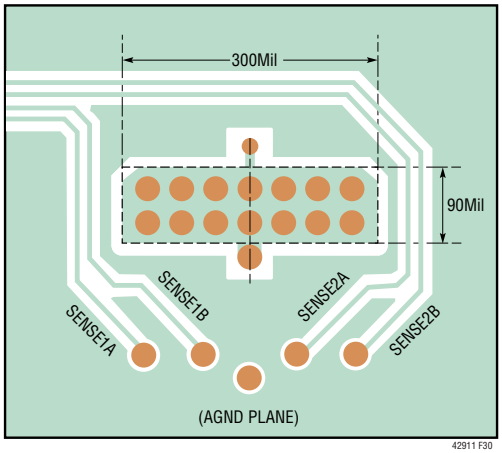
Figure 28. Top and Bottom Layer Sense Resistor Block Layout

APPLICATIONS INFORMATION



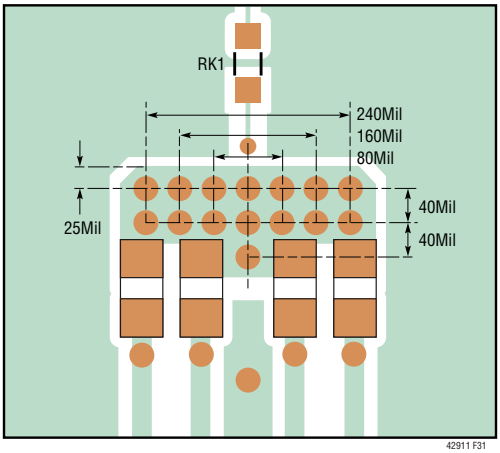
NOTES: DRAWING NOT TO SCALE.
VSSK12 VIA ISOLATED.

Figure 29. Inner Layer 2 Sense Resistor Block Layout (V_{EE} Plane)



NOTES: DRAWING NOT TO SCALE.
VSSK12 VIA CONNECTS V_{EE}.

Figure 30. Inner Layer 3 Sense Resistor Block Layout (AGND/Signal Plane)



NOTE: DRAWING NOT TO SCALE.

Figure 31. Sense Resistor Block Via Specifications

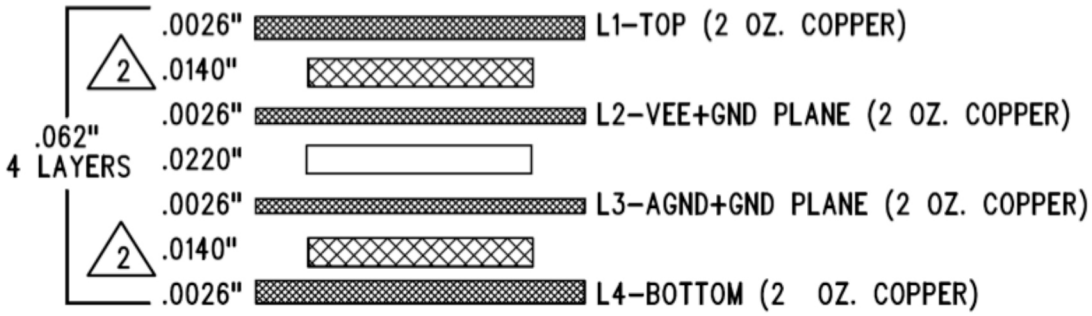
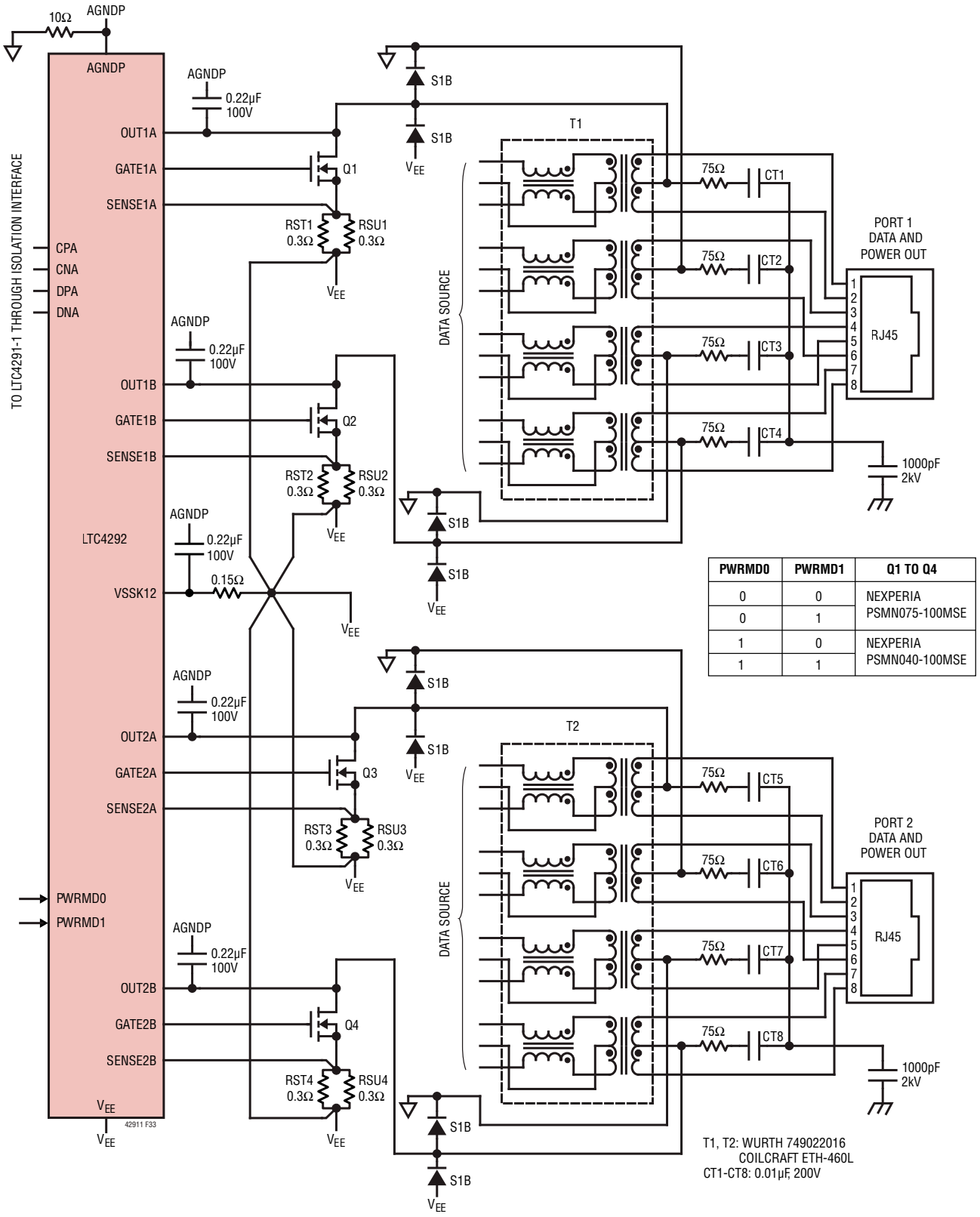


Figure 32. PCB Layer Structure

TYPICAL APPLICATION

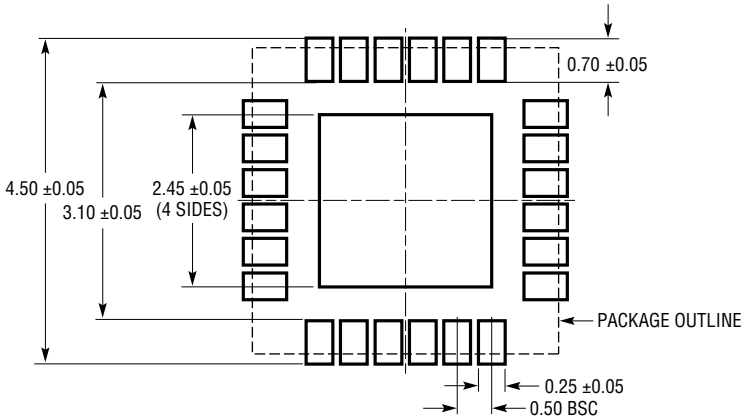
Figure 33. Alternative A (MDI-X) and Alternative B(S), 1000BASE-T, IEEE 802.3bt, Type 3 or Type 4 PSE, Ports 1 and 2 Shown



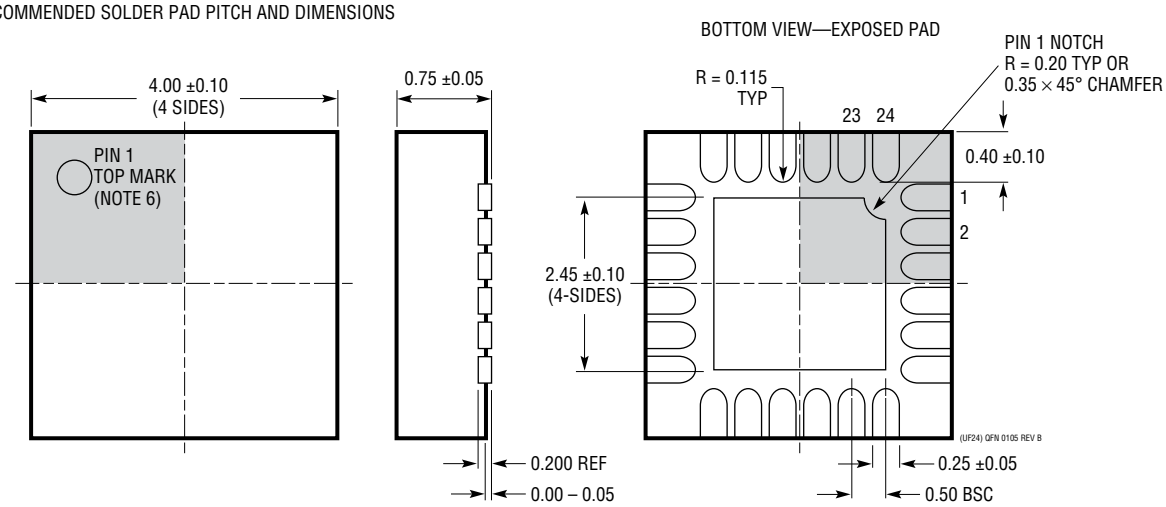
Rev 0

PACKAGE DESCRIPTION

UF Package
24-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1697 Rev B)



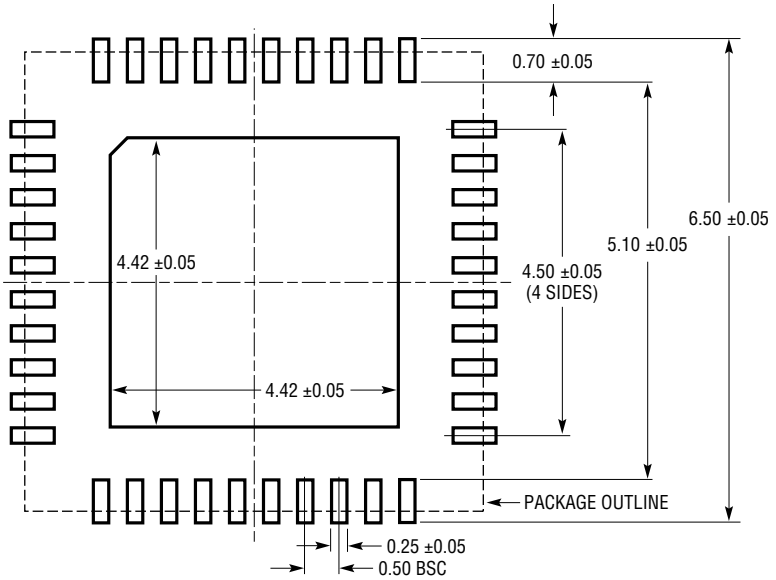
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



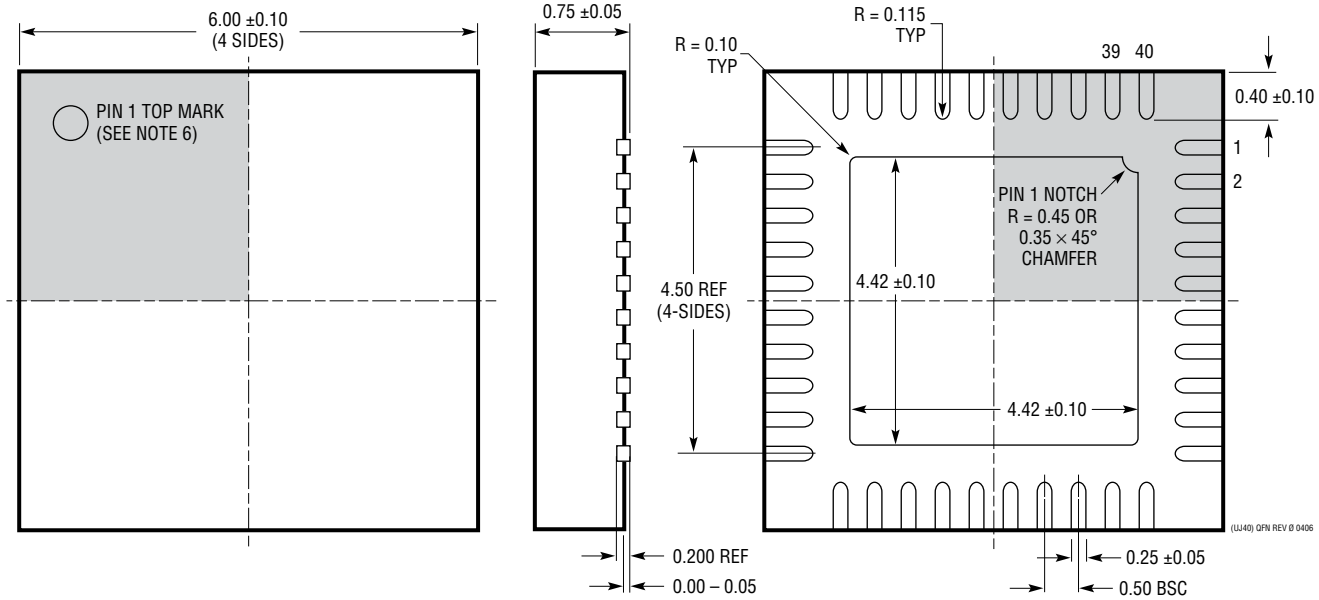
NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-X)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

UJ Package
40-Lead Plastic QFN (6mm × 6mm)
(Reference LTC DWG # 05-08-1728 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

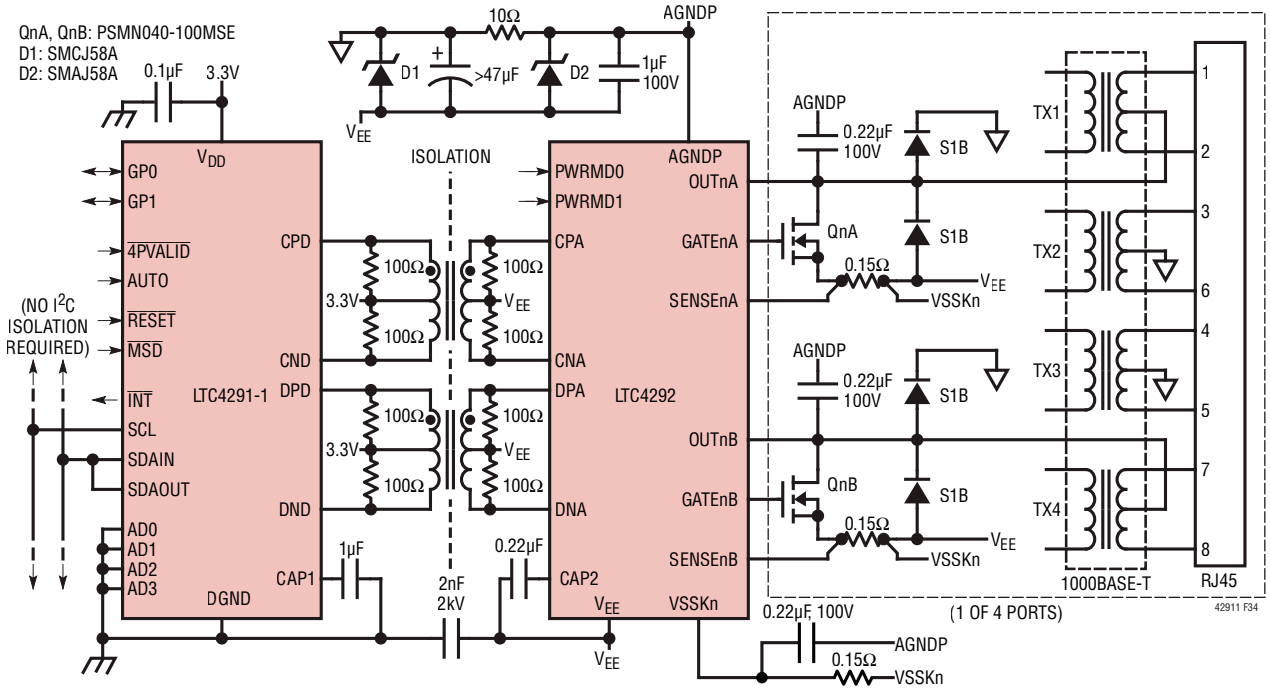


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS A JEDEC PACKAGE OUTLINE VARIATION OF (WJJD-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

Figure 34. IEEE 802.3bt Type 3 or Type 4 PSE, Alternative A (MDI-X) and Alternative B(S), 1000BASE-T, 1 of 4 Ports Shown



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT4294	LTPoE++/PoE+/PoE PD Controller	External Switch, IEEE 802.3bt Support Configurable Class
LT4295	IEEE 802.3bt PD with Forward/Flyback Switching Regulator Controller	External Switch, IEEE 802.3bt Support, Configurable Class, Forward or No-Opto Flyback Operation, Frequency, PG/SG Delays, Soft-Start, and Aux Support as Low as 9V, Including Housekeeping Buck, Slope Compensation
LTC4257-1	IEEE 802.3af PD Interface Controller	Internal 100V, 400mA Switch, Dual Current Limit, Programmable Class
LTC4263	Single IEEE 802.3af PSE Controller	Internal FET Switch
LTC4265	IEEE 802.3at PD Interface Controller	Internal 100V, 1A Switch, 2-Event Classification Recognition
LTC4266	Quad IEEE 802.3at PoE PSE Controller	With Programmable I_{CUT}/I_{LIM}, 2-Event Classification, and Port Current and Voltage Monitoring
LTC4267	IEEE 802.3af PD Interface with Integrated Switching Regulator	Internal 100V, 400mA Switch, Dual Inrush Current, Programmable Class
LTC4269-1	IEEE 802.3at PD Interface with Integrated Flyback Switching Regulator	2-Event Classification, Programmable Class, Synchronous No-Opto Flyback Controller, 50kHz to 250kHz, Aux Support
LTC4269-2	IEEE 802.3at PD Interface with Integrated Forward Switching Regulator	2-Event Classification, Programmable Class, Synchronous Forward Controller, 100kHz to 500kHz, Aux Support
LTC4270/ LTC4271	12-Port PoE/PoE+/LTPoE++® PSE Controller	Transformer Isolation, Supports Type 1, Type 2 and LTPoE++ PDs
LTC4278	IEEE 802.3at PD Interface with Integrated Flyback Switching Regulator	2-Event Classification, Programmable Class, Synchronous No-Opto Flyback Controller, 50kHz to 250kHz, 12V Aux Support
LTC4279	Single PoE/PoE+/LTPoE++ PSE Controller	Supports IEEE 802.3af, IEEE 802.3at, LTPoE++ and Proprietary PDs
LTC4290/ LTC4271	8-Port PoE/PoE+/LTPoE++ PSE Controller	Transformer Isolation, Supports IEEE 802.3af, IEEE 802.3at and LTPoE++ PDs