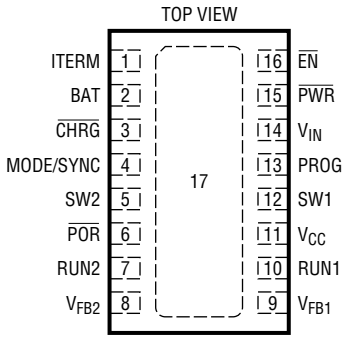
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Charger Input Supply (V_{IN}) ..... –0.3V to 10V
PROG, ITERM ..... –0.3V to V_{IN} + 0.3V
BAT ..... –0.3V to 7V
$\overline{CHRG}$, $\overline{PWR}$, $\overline{EN}$..... –0.3V to 10V
BAT Short-Circuit Duration.....Continuous
BAT Pin Current 1A
PROG Pin Current 1mA
Converter Input Supply (V_{CC})..... –0.3V to 6V
V_{FB1}, V_{FB2}, RUN1, RUN2.....–0.3V to V_{CC} +0.3V
MODE/SYNC .....–0.3V to V_{CC} + 0.3V
$\overline{SW1}$, SW2 .....–0.3V to V_{CC} + 0.3V
$\overline{POR}$ ..... –0.3V to 6V
Ambient Operating Temperature
Range (Note 2) ..... –40°C to 85°C
Maximum Junction Temperature (Note 8) ..... 125°C
Storage Temperature Range..... –65°C to 125°C

PACKAGE/ORDER INFORMATION



DHC PACKAGE
16-LEAD (5mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 40°C/W (Note 3)
EXPOSED PAD IS GROUND (PIN 17)
MUST BE SOLDERED TO PCB

ORDER PART NUMBER	DHC PART MARKING
LTC3552EDHC	3552

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 5V, V_{CC} = 3.6V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Battery Charger							
V_{IN}	Input Supply Voltage		●	4.25		8	V
I_{IN}	Input Supply Current						
	Charge Mode (Note 4)	R_{PROG} = 10k	●		0.4	1	mA
	Standby Mode	Charge Terminated	●		200	500	µA
	Shutdown Mode	$\overline{EN}$ = 5V, V_{IN} < V_{BAT} or V_{IN} < V_{UV}	●		25	50	µA
V_{FLOAT}	Regulated Output (Float) Voltage	0°C ≤ T_A ≤ 85°C, 4.3V < V_{IN} < 8V		4.158	4.2	4.242	V
I_{BAT}	BAT Pin Current	R_{PROG} = 10k, Current Mode	●	92	100	105	mA
		R_{PROG} = 2k, Current Mode	●	465	500	535	mA
		Standby Mode, V_{BAT} = 4.2V	●		–2.5	–6	µA
		Shutdown Mode ($\overline{EN}$ = 5V, V_{IN} < V_{BAT} or V_{IN} < V_{UV})			±1	±2	µA
		Sleep Mode, V_{IN} = 0V			±1	±2	µA
I_{TRIKL}	Trickle Charge Current	V_{BAT} < V_{TRIKL}, R_{PROG} = 2k	●	30	45	60	mA
V_{TRIKL}	Trickle Charge Threshold Voltage	R_{PROG} = 10k, V_{BAT} Rising		2.8	2.9	3	V
V_{TRHYS}	Trickle Charge Hysterisis Voltage	R_{PROG} = 10k			80		mV
V_{UV}	V_{IN} Undervoltage Lockout Voltage	From V_{IN} Low to High	●	3.7	3.8	3.92	V
V_{UVHYS}	V_{IN} Undervoltage Lockout Hysteresis		●	150	200	300	mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 5V, V_{CC} = 3.6V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{\overline{EN}(IL)}$	$\overline{EN}$ Pin Input Low Voltage		●	0.4	0.7		V
$V_{\overline{EN}(IH)}$	$\overline{EN}$ Pin Input High Voltage		●		0.7	1	V
$R_{\overline{EN}}$	$\overline{EN}$ Pin Pull-Down Resistor		●	1.2	2	5	MΩ
V_{ASD}	V_{IN} – V_{BAT} Lockout Threshold Voltage	V_{IN} from Low to High V_{IN} from High to Low		70 5	100 30	140 50	mV mV
I_{TERM}	Charge Termination Current Threshold	R_{TERM} = 1k R_{TERM} = 5k	● ●	90 17.5	100 20	110 22.5	mA mA
V_{PROG}	PROG Pin Voltage	R_{PROG} = 10k, Current Mode		0.93	1	1.07	V
$V_{\overline{CHRG}}$	$\overline{CHRG}$ Pin Output Low Voltage	$I_{\overline{CHRG}}$ = 5mA			0.35	0.6	V
$V_{\overline{PWR}}$	$\overline{PWR}$ Pin Output Low Voltage	$I_{\overline{PWR}}$ = 5mA			0.35	0.6	V
ΔV_{RECHRG}	Recharge Battery Threshold Voltage	V_{FLOAT} – V_{RECHRG}, 0°C < T_A < 85°C		60	100	140	mV
T_{LIM}	Junction Temperature in Constant-Temperature Mode				120		°C
$R_{ON-CHRG}$	Charger's Power FET On-Resistance (Between V_{IN} and BAT)				600		mΩ
$t_{SS-CHRG}$	Charger Soft-Start Time	I_{BAT} = 0 to I_{BAT} = 1000V/R_{PROG}			100		µs
t_{RECHRG}	Recharge Comparator Filter Time	V_{BAT} High to Low		0.75	2	4.5	ms
t_{TERM}	Termination Comparator Filter Time	I_{BAT} Drops Below Charge Termination Threshold		0.4	1	2.5	ms
Switching Regulator							
V_{CC}	Operating Voltage Range for Regulator		●	2.5		5.5	V
I_{FB}	Feedback Pin Input Current		●			30	nA
V_{FB}	Feedback Voltage (Note 5)	0°C ≤ T_A ≤ 85°C –40°C ≤ T_A ≤ 85°C	 ●	0.588 0.585	0.6 0.6	0.612 0.612	V V
ΔV_{LINE_REG}	Reference Voltage Line Regulation	V_{CC} = 2.5V to 5.5V (Note 5)			0.3	0.5	%/V
ΔV_{LOAD_REG}	Output Voltage Load Regulation	(Note 5)			0.5		%
I_S	Input DC Supply Current Active Mode Sleep Mode Shutdown	 V_{FB1} = V_{FB2} = 0.5V V_{FB1} = V_{FB2} = 0.63V, MODE/SYNC = 3.6V RUN = 0V, V_{CC} = 5.5V, MODE/SYNC = 0V		 	 700 40 0.1	 950 60 1	 µA µA µA
f_{OSC}	Oscillator Frequency	V_{FB} = 0.6V	●	1.8	2.25	2.7	MHz
f_{SYNC}	Synchronization Frequency				2.25		MHz
I_{LIM}	Peak Switch Current Limit Regulator 1 Peak Switch Current Limit Regulator 2	V_{CC} = 3V, V_{FB} = 0.5V, Duty Cycle < 35% V_{CC} = 3V, V_{FB} = 0.5V, Duty Cycle < 35%		0.95 0.6	1.2 0.7	1.6 0.9	A A
$R_{DS(ON)}$	Top Switch On-Resistance Bottom Switch On-Resistance	(Note 6) (Note 6)			0.35 0.30	0.45 0.45	Ω Ω
$I_{SW(LKG)}$	Switch Leakage Current	V_{CC} = 5V, V_{RUN} = 0V, V_{FB} = 0V			0.01	1	µA
POR	Power-On Reset Threshold	V_{FB} Ramping Down, MODE/SYNC = 0V			–8.5		%
	Power-On Reset On-Resistance				100	200	Ω
	Power-On Reset Delay				262,144		Cycles
V_{RUN}	RUN Threshold Voltage		●	0.3	1	1.5	V
I_{RUN}	RUN Leakage Current		●		0.01	1	µA

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime. Pins of regulators should not exceed 6V.

Note 2: The LTC3552E is guaranteed to meet performance specifications from 0°C to 85°C Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: Failure to solder the exposed backside of the package to the PC board will result in a thermal resistance much higher than 40°C/W. See Thermal Considerations.

Note 4: Supply current includes PROG pin current and ITERM pin current (approximately 100µA each) but does not include any current delivered to the battery through the BAT pin (approximately 100mA).

Note 5: The regulator is tested in a proprietary test mode that connects V_{FB} to the output of the error amplifier.

Note 6: Dynamic supply current is higher due to the internal gate charge being delivered at the switching frequency.

Note 7: The regulator power switch on-resistances are guaranteed by correlation to wafer level measurements.

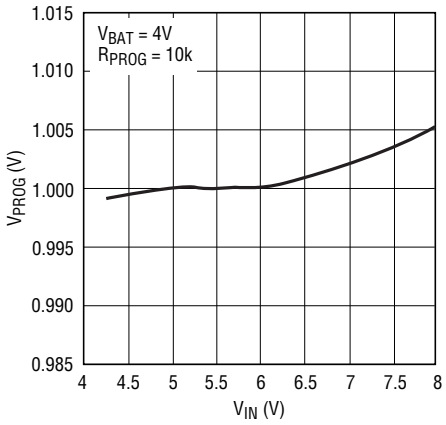
Note 8: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

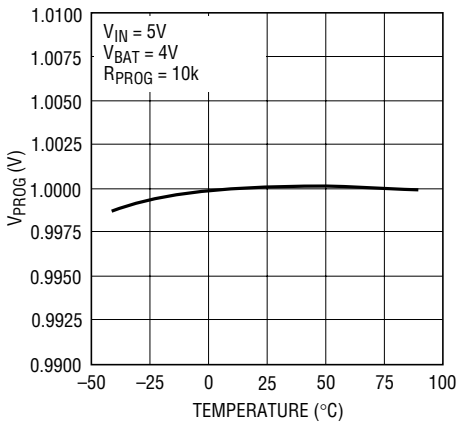
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C Unless Otherwise Specified.

Battery Charger

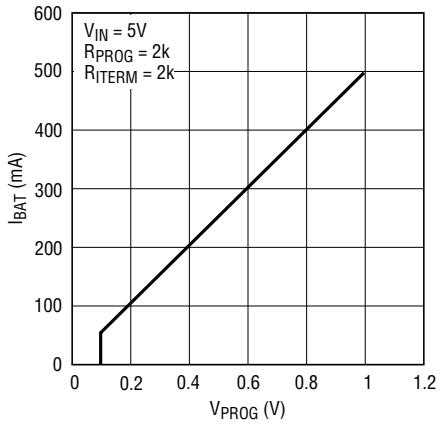
PROG Pin Voltage vs V_{IN} (Constant-Current Mode)



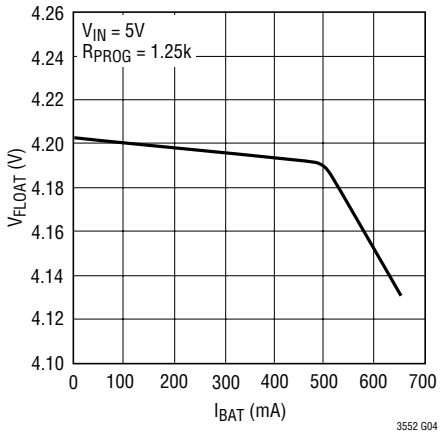
PROG Pin Voltage vs Temperature



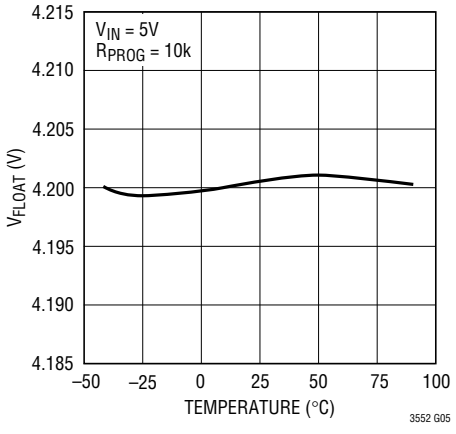
Charge Current vs PROG Pin Voltage



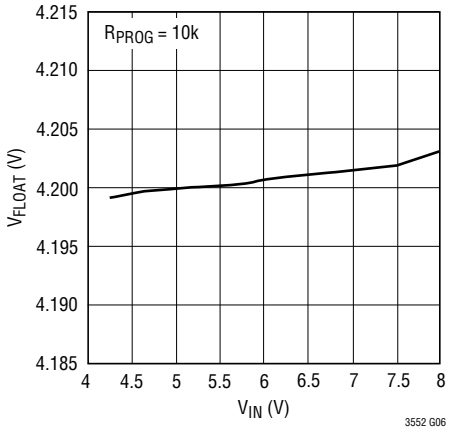
Regulated Output (Float) Voltage vs Charge Current



Regulated Output (Float) Voltage vs Temperature



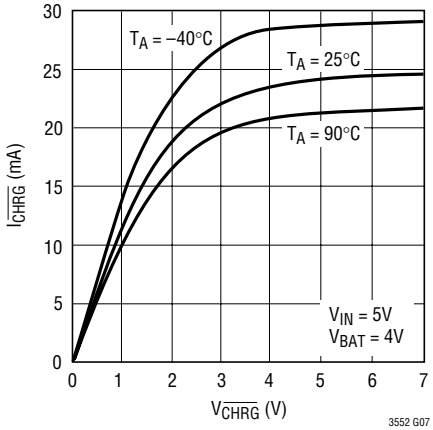
Regulated Output (Float) Voltage vs V_{IN}



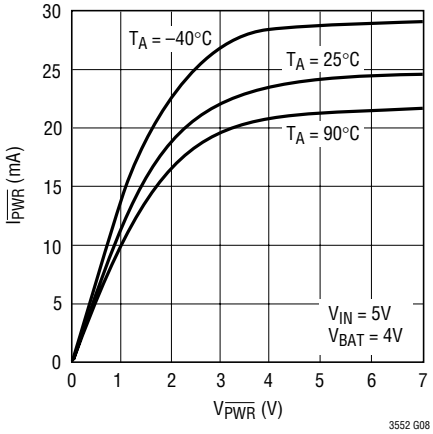
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C Unless Otherwise Specified.

Battery Charger

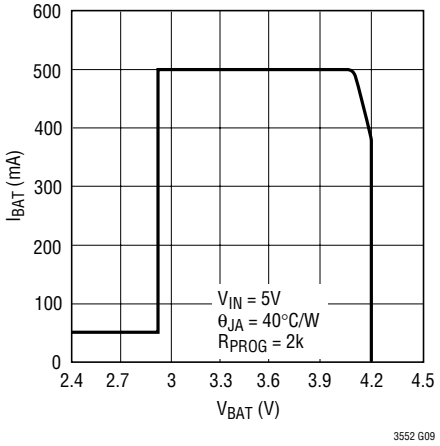
$\overline{CHRG}$ Pin I-V Curve (Pull-Down State)



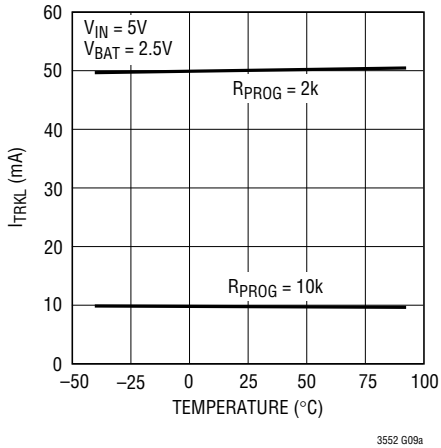
$\overline{PWR}$ Pin I-V Curve (Pull-Down State)



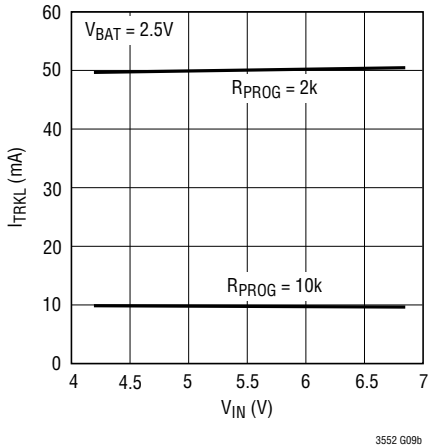
Charge Current vs Battery Voltage



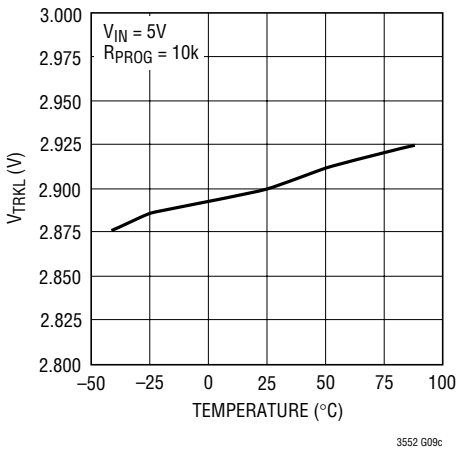
Trickle Charge Current vs Temperature



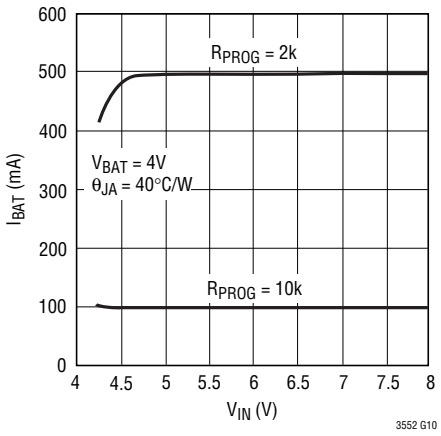
Trickle Charge Current vs V_{IN}



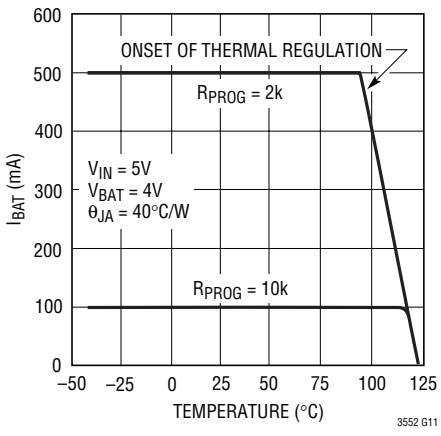
Trickle Charge Threshold Voltage vs Temperature



Charge Current vs V_{IN}



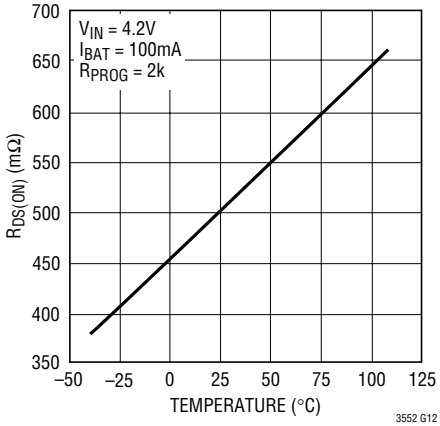
Charge Current vs Ambient Temperature



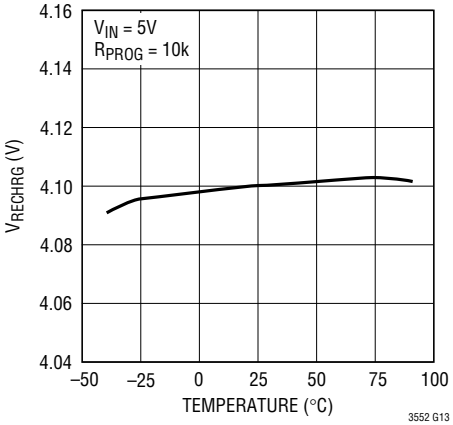
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C Unless Otherwise Specified.

Battery Charger

Power FET On-Resistance vs Temperature

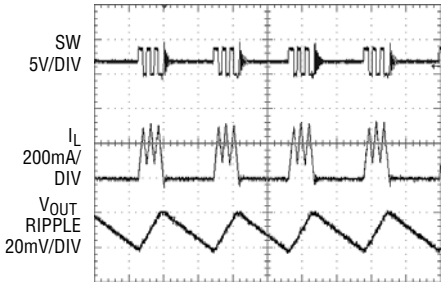


Recharge Threshold Voltage vs Temperature



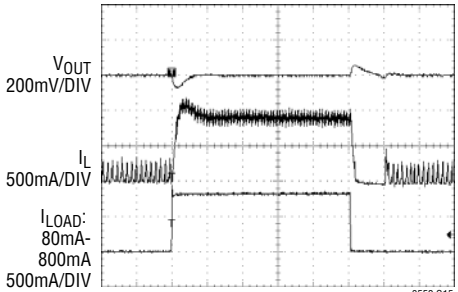
Switching Regulator

Burst Mode Operation



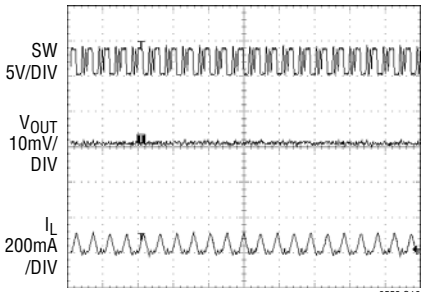
VCC = 3.6V 2µs/DIV
VOUT1 = 1.8V
ILOAD = 60mA, MODE/SYNC = 3.6V
REGULATOR 1; CIRCUIT OF FIGURE 2

Load Step



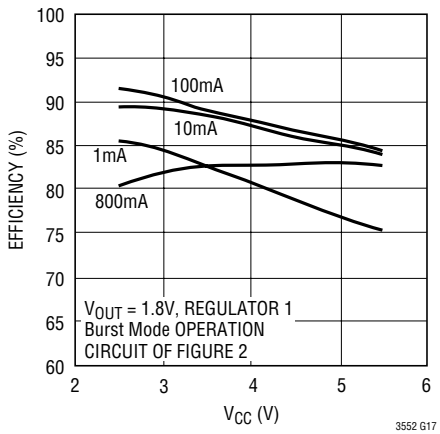
VCC = 3.6V 20µs/DIV
VOUT1 = 1.8V
ILOAD = 80mA TO 800mA
REGULATOR 1; CIRCUIT OF FIGURE 2

Pulse-Skipping Mode

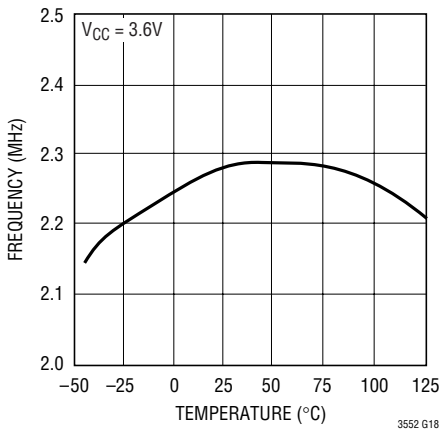


VCC = 3.6V 1µs/DIV
VOUT1 = 1.8V
ILOAD = 30mA, MODE/SYNC = 0V
REGULATOR 1; CIRCUIT OF FIGURE 2

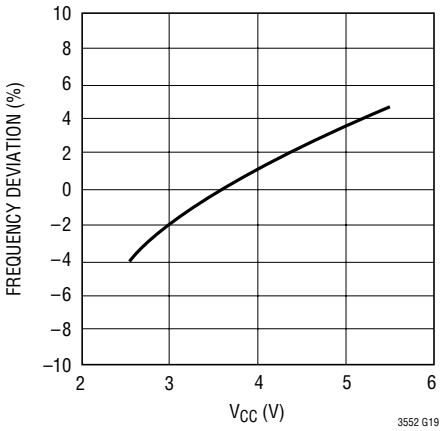
Efficiency vs V_{CC}



Oscillator Frequency vs Temperature



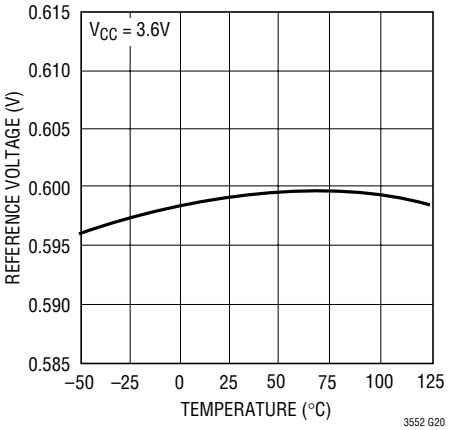
Oscillator Frequency Error vs V_{CC}



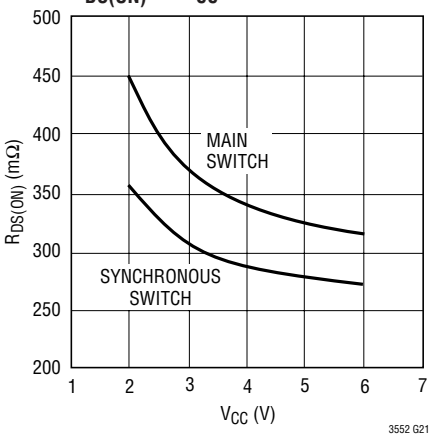
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C Unless Otherwise Specified.

Switching Regulator

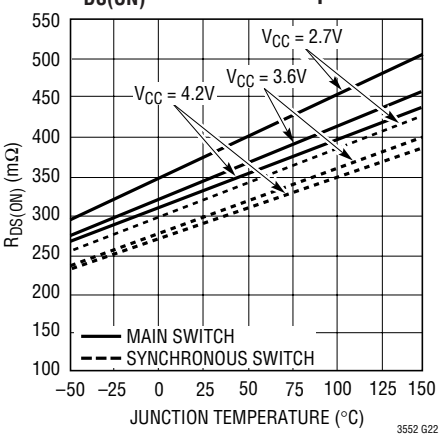
Reference Voltage vs Temperature



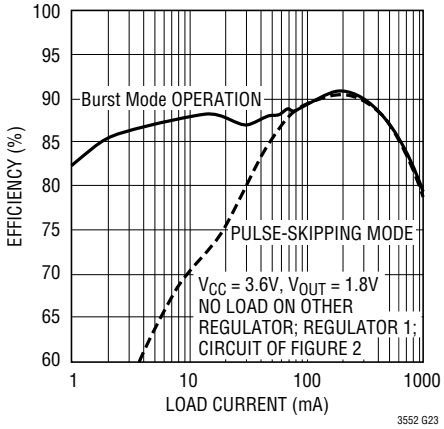
$R_{DS(ON)}$ vs V_{CC}



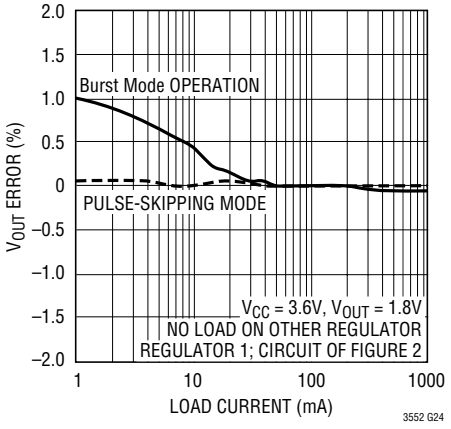
$R_{DS(ON)}$ vs Junction Temperature



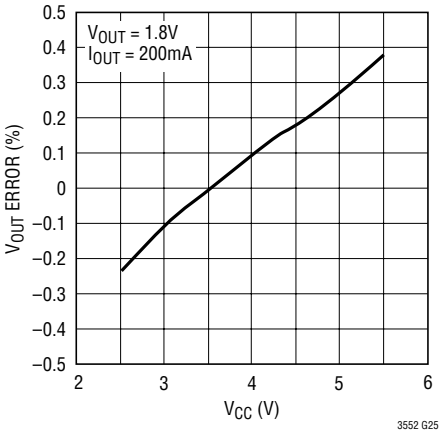
Efficiency vs Load Current



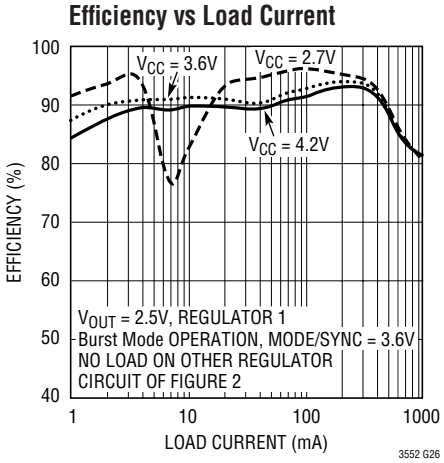
Load Regulation



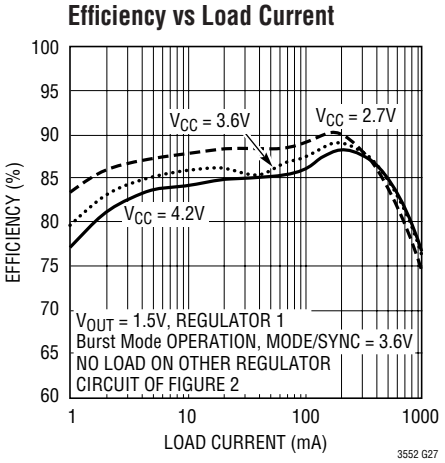
Line Regulation



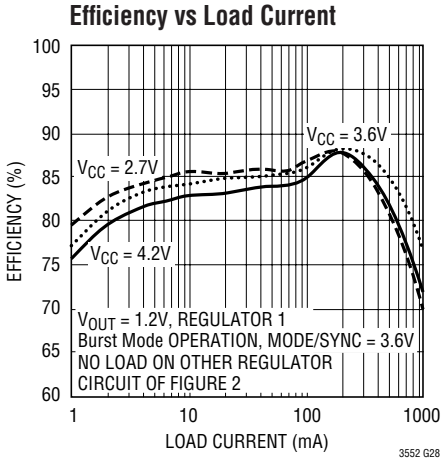
Efficiency vs Load Current



Efficiency vs Load Current



Efficiency vs Load Current



PIN FUNCTIONS

ITERM (Pin 1): Charge Termination Program. The charge termination current threshold is programmed by connecting a 1% resistor, R_{TERM}, to ground. The current threshold ITERM, is set by the following formula:

$$I_{TERM} = \frac{100V}{R_{TERM}}, R_{TERM} = \frac{100V}{I_{TERM}}$$

BAT (Pin 2): Charge Current Output. Provides charge current to the battery from the internal P-channel MOSFET, and regulates the final float voltage to 4.2V. An internal precision resistor divider from this pin sets the float voltage. This divider is disconnected in shutdown mode to minimize current drain from the battery.

$\overline{\text{CHRG}}$ (Pin 3): Charge Status Open-Drain Output. When the battery is charging, the $\overline{\text{CHRG}}$ pin is pulled low by an internal N-channel MOSFET. When the charge cycle is completed, $\overline{\text{CHRG}}$ becomes high impedance.

MODE/SYNC (Pin 4): Combination Mode Selection and Oscillator Synchronization. This pin controls the operation of the buck regulators. When tied to V_{CC} or GND, Burst Mode operation or pulse-skipping mode is selected, respectively. Do not float this pin. The oscillation frequency can be synchronized to an external oscillator applied to this pin and pulse-skipping mode is automatically selected.

SW2 (Pin 5): Regulator 2 Switch Node Connection to the Inductor. This pin swings from V_{CC} to GND.

$\overline{\text{POR}}$ (Pin 6): Power-On Reset. This open-drain logic output is pulled to GND when either output voltage drops 8.5% from the regulated voltage and goes high after 262,144 clock cycles when both regulators are within regulation.

RUN2 (Pin 7): Regulator 2 Enable. Forcing this pin to V_{CC} enables regulator 2, while forcing it to GND causes regulator 2 to shut down. This pin must be driven; do not float.

V_{FB2} (Pin 8): Output Feedback for Regulator 2. Receives the feedback voltage from the external resistive divider across the output. Normal voltage for this pin is 600mV.

V_{FB1} (Pin 9): Output Feedback for Regulator 1. Receives the feedback voltage from the external resistive divider across the output. Normal voltage for this pin is 600mV.

RUN1 (Pin 10): Regulator 1 Enable. Forcing this pin to V_{CC} enables regulator 1, while forcing it to GND causes regulator 1 to shut down. This pin must be driven; do not float.

V_{CC} (Pin 11): Buck Regulators Input Supply. Provides power to the switchers. Must be closely decoupled to GND.

SW1 (Pin 12): Regulator 1 Switch Node Connection to the Inductor. This pin swings from V_{CC} to GND.

PROG (Pin 13): Charge Current Program and Charge Current Monitor. Charge current is programmed by connecting a 1% resistor, R_{PROG}, to ground. When charging in constant-current mode, this pin servos to 1V. In all modes, the voltage on this pin can be used to measure the charge current using the following formula:

$$I_{BAT} = \frac{V_{PROG}}{I_{PROG}} \bullet 1000$$

This pin is clamped to approximately 2.4V. Driving this pin to voltages beyond the clamp voltage should be avoided.

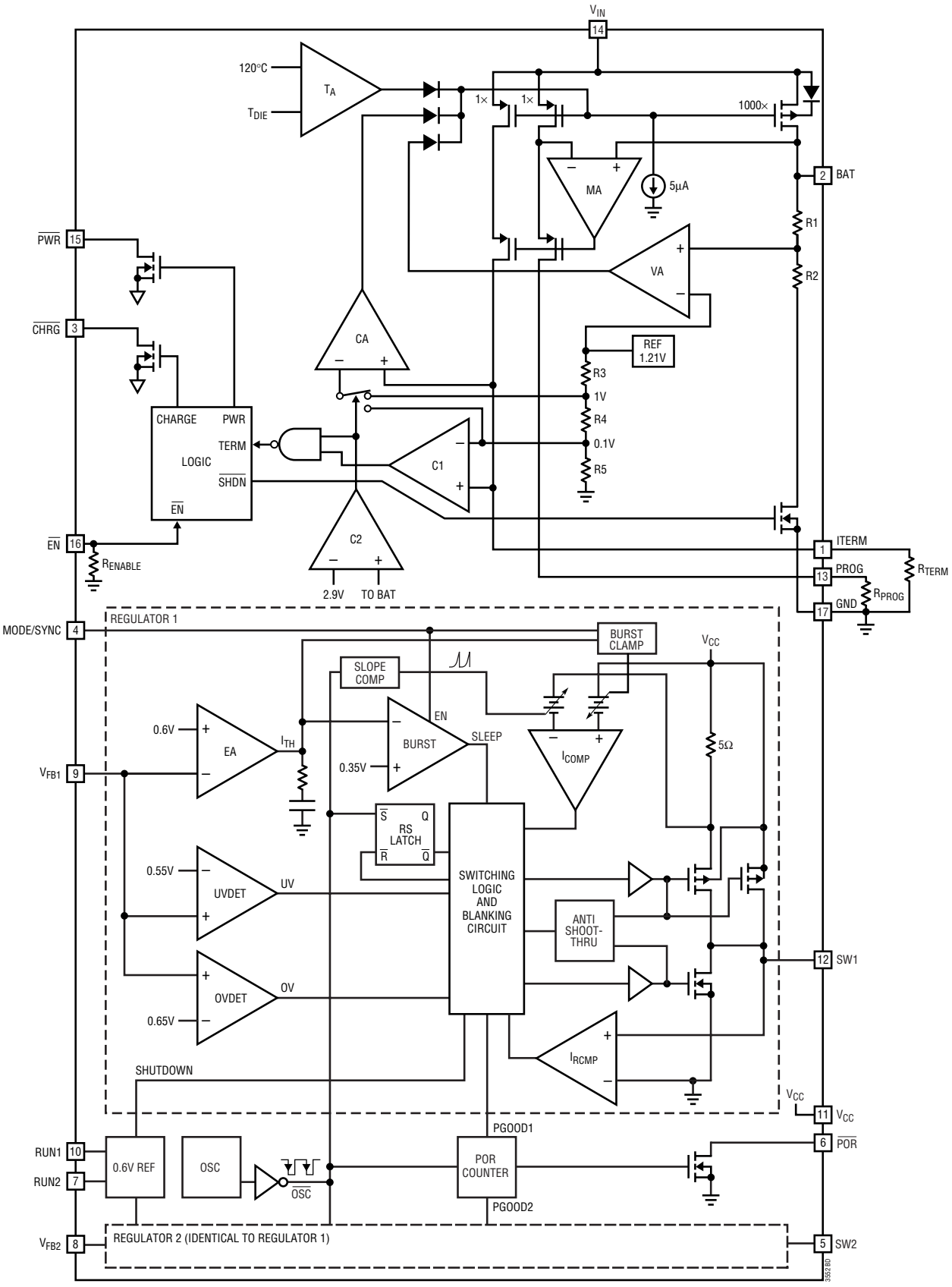
V_{IN} (Pin 14): Charger Input Supply. Provides power to the charger. V_{IN} can range from 4.25V to 8V. This pin should be bypassed with at least a 1µF capacitor. When V_{IN} is within 100mV of the BAT pin voltage, the charger enters shutdown mode dropping the battery drain current to less than 2µA.

$\overline{\text{PWR}}$ (Pin 15): Charger Power Supply Status Open-Drain Output. When V_{IN} is greater than the undervoltage lockout threshold and at least 100mV above V_{BAT}, the $\overline{\text{PWR}}$ pin is pulled to ground; otherwise, the pin is high impedance.

$\overline{\text{EN}}$ (Pin 16): Enable Input. A logic high on the $\overline{\text{EN}}$ pin will put the charger into shutdown mode where the battery drain current is reduced to less than 2µA and the supply current is reduced to less than 50µA. A logic low or floating the $\overline{\text{EN}}$ pin (allowing an internal 2MΩ pull-down resistor to pull this pin low) enables charging.

Exposed Pad (GND) (Pin 17): Ground. The exposed backside of the package (Pin 17) is ground and must be soldered to the PCB for maximum heat transfer.

BLOCK DIAGRAM



OPERATION

The LTC3552 is made up of two parts: a standalone constant-current/constant-voltage linear charger for a single-cell lithium-ion battery and a high efficiency dual DC/DC switching regulator. The charger can deliver up to 950mA of charge current (using a good thermal PCB layout) with a final float voltage accuracy of ±1%. An internal P-channel power MOSFET and thermal regulation circuitry are included. No blocking diode or external current sense resistor is required; furthermore, the charger is capable of operating from a USB power source.

The switching regulators use a constant frequency, current mode step-down architecture. Both main (P-channel MOSFET) and synchronous (N-channel MOSFET) switches are internal.

LITHIUM-ION BATTERY CHARGER

Normal Charge Cycle

A charge cycle begins when the voltage at the V_{IN} pin rises above the UVLO threshold level and a 1% program resistor is connected from the PROG pin to ground. If the BAT pin is less than 2.9V, the charger enters trickle charge mode. In this mode, the charger supplies approximately one-tenth the programmed charge current to bring the battery voltage up to a safe level for full current charging.

When the BAT pin voltage rises above 2.9V, the charger enters constant-current mode where the programmed charge current is supplied to the battery. When the BAT pin approaches the final float voltage (4.2V), the charger enters constant-voltage mode and the charge current begins to decrease. When the charge current drops to the programmed termination threshold (set by the external resistor R_{TERM}), the charge cycle ends. Figure 1 shows the state diagram of a typical charge cycle.

Charge Status Indicator ($\overline{CHRG}$)

The open drain charge status output has two states: pull-down and high impedance. The pull-down state indicates that the charger is in a charge cycle. Once the charge cycle has terminated or the charger is disabled, the pin becomes high impedance.

Automatic Recharge

Once the charge cycle terminates, the charger continuously monitors the voltage on the BAT pin using a comparator with a 2ms filter time ($t_{RECHARGE}$). A charge cycle restarts when the battery voltage falls below 4.10V (which corresponds to approximately 80% to 90% battery capacity). This ensures that the battery is kept at, or near, a fully charged condition and eliminates the need for periodic charge cycle initiations. The $\overline{CHRG}$ output enters a pull-down state during recharge cycles. If the battery is removed from the charger, a sawtooth waveform of approximately 100mV appears at the charger output. This is caused by the repeated cycling between termination and recharge events. This cycling results in pulsing at the $\overline{CHRG}$ output; an LED connected to this pin will exhibit a pulsing pattern, indicating to the user that a battery is not present. The frequency of the sawtooth is dependent on the amount of output capacitance.

Power Supply Status Indicator ($\overline{PWR}$)

The power supply status output has two states: pull-down and high impedance. The pull-down state indicates that V_{IN} is above the UVLO threshold (3.8V) and is also 100mV above the battery voltage. If these conditions are not met, the $\overline{PWR}$ pin is high impedance indicating that the charger is unable to charge the battery.

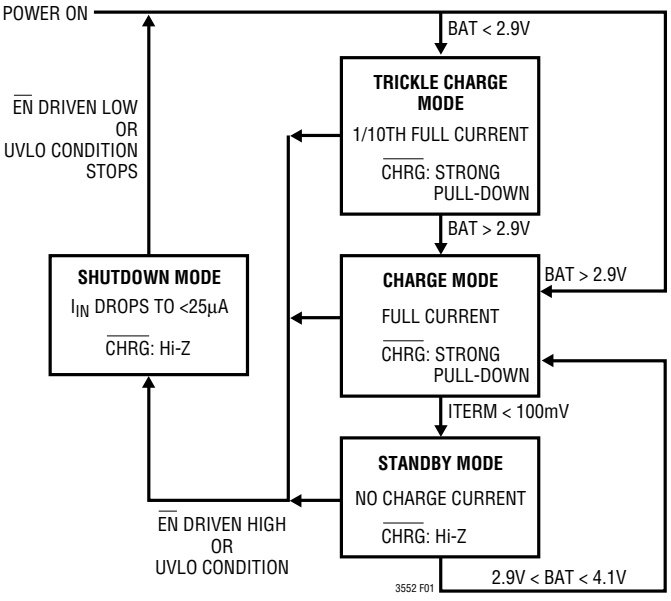


Figure 1. State Diagram of a Typical Charge Cycle

OPERATION

Charge Current Soft-Start

The charger includes a soft-start circuit to minimize the inrush current at the start of a charge cycle. When a charge cycle is initiated, the charge current ramps from zero to full-scale current over a period of approximately 100µs. This has the effect of minimizing the transient current load on the power supply during start-up.

Thermal Limiting

An internal thermal feedback loop reduces the programmed charge current if the die temperature attempts to rise above a preset value of approximately 120°C. This feature protects the charger from excessive temperature and allows the user to push the limits of the power handling capability of a given circuit board without risk of damaging the charger. The charge current can be set according to typical (not worst case) ambient temperature with the assurance that the charger will automatically reduce the current in worst-case conditions. DFN package power considerations are discussed further in the Applications Information section.

Undervoltage Lockout (UVLO)

An internal undervoltage lockout circuit monitors the input voltage and keeps the charger in shutdown mode until V_{IN} rises above the undervoltage lockout threshold. The UVLO circuit has a hysteresis of 200mV. Also, to protect against reverse current in the power MOSFET, the UVLO circuit keeps the charger in shutdown mode if V_{IN} falls to within 30mV of the BAT voltage. If the UVLO comparator is tripped, the charger will not come out of shutdown mode until V_{IN} rises 100mV above the BAT voltage.

Manual Shutdown

At any point in the charge cycle, the charger can be put into shutdown mode by driving the $\overline{EN}$ pin high. This reduces the battery drain current to less than 2µA and the V_{IN} supply current to less than 50µA. When in shutdown mode, the $\overline{CHRG}$ pin is in the high impedance state. A new charge cycle can be initiated by driving the $\overline{EN}$ pin low. An internal resistor pull-down on this pin forces the charger to be enabled if the pin is allowed to float.

DUAL SWITCHING REGULATOR

The regulators use a current mode architecture with a constant operating frequency of 2.25MHz. Both regulators share the same clock and run in-phase. To suit a variety of applications, the MODE/SYNC pin allows the user to choose between low noise or high efficiency. The output voltages are set by external resistive dividers returned to the V_{FB} pins. An error amplifier compares the divided output voltage (V_{FB}) with a reference voltage of 0.6V and adjusts the peak inductor current accordingly. An undervoltage comparator will pull the $\overline{POR}$ output low if V_{FB} is less than 91.5% of the reference voltage. The $\overline{POR}$ output will go high after 262,144 clock cycles (about 117ms in pulse-skipping mode) of achieving regulation.

Main Regulator Control Loop

During normal operation, the top power switch (P-channel MOSFET) is turned on at the beginning of a clock cycle when the feedback voltage is below the reference voltage. The current into the inductor and the load increases until the current limit is reached. The switch turns off and energy stored in the inductor flows through the bottom switch (N-channel MOSFET) into the load until the next clock cycle. The peak inductor current is controlled by the internally compensated I_{TH} voltage, which is the output of the error amplifier. This amplifier compares V_{FB} to the 0.6V reference (see Block Diagram). When the load current increases, the V_{FB} voltage decreases slightly below the reference. This decrease causes the error amplifier to increase the I_{TH} voltage until the average inductor current matches the new load current. The main control loop can be shut down by pulling the RUN pin to ground.

Low Load Current Operation

The MODE/SYNC pin provides two modes of operation at low currents. Both modes automatically switch from continuous operation to the selected mode when the load current is low. For highest efficiency at low current, connecting the MODE/SYNC pin to V_{CC} makes the regulator operate in Burst Mode, where the PMOS switch operates intermittently based on load demand with a

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fixed peak inductor current. By running cycles periodically, the switching losses which are dominated by the gate charge losses of the power MOSFETs are minimized. The main control loop is interrupted when the output voltage reaches the desired regulated value. A voltage comparator trips when I_{TH} is below 0.35V, shutting off the switch and reducing the power. The output capacitor and the inductor supply the power to the load until I_{TH} exceeds 0.65V, turning on the switch and the main control loop which starts another cycle.

For lower ripple noise at low currents, the pulse-skipping mode can be selected by grounding the MODE/SYNC pin. In this mode, the regulator continues to switch at a constant frequency down to very low currents, where it will begin skipping pulses. The efficiency in pulse-skipping mode can be improved slightly by connecting the SW node to the MODE/SYNC input which reduces the clock frequency by approximately 30%. Do not float the MODE/SYNC pin.

Dropout Operation

When the V_{CC} input supply voltage decreases toward the output voltage, the duty cycle increases to 100% which is the dropout condition. In dropout, the PMOS switch is turned on continuously with the output voltage being equal to the input voltage minus the voltage drops across the internal P-channel MOSFET and the inductor. An important design consideration is that the $R_{DS(ON)}$ of the P-channel switch increases with decreasing input supply voltage (see Typical Performance Characteristics). Therefore, the user should calculate the power dissipation when the regulator is used at 100% duty cycle with low input voltage (see Thermal Considerations in the Applications Information section).

Low Supply Voltage Operation

To prevent unstable operation, the regulators incorporate an undervoltage lockout circuit which shuts them down when the V_{CC} voltage drops below approximately 1.65V.

APPLICATIONS INFORMATION

A typical LTC3552 application circuit is shown in Figure 2. External component selection is driven by the charging requirements and the switching regulators load requirements.

Programming Charge Current

The charge current is programmed using a single resistor from the PROG pin to ground. The charge current out of the BAT pin is 1000 times the current out of the PROG pin. The program resistor and the charge current are calculated using the following equations:

$$R_{PROG} = \frac{1000V}{I_{CHG}}, I_{CHG} = \frac{1000V}{R_{PROG}}$$

Charge current out of the BAT pin can be determined anytime by monitoring the PROG pin voltage and using the following equation:

$$I_{BAT} = \frac{V_{PROG}}{R_{PROG}} \bullet 1000$$

Programming Charge Termination

The charge cycle terminates when the charge current falls below the programmed termination threshold. This threshold is set by connecting an external resistor, R_{TERM}, from the ITERM pin to ground. The charge termination current threshold (I_{TERM}) is set by the following equation:

$$I_{TERM} = \frac{100V}{R_{TERM}} = \frac{I_{CHG}}{10} \bullet \frac{R_{PROG}}{R_{TERM}},$$

$$R_{TERM} = \frac{100V}{I_{TERM}}$$

The termination condition is detected by using an internal filtered comparator to monitor the ITERM pin. When the ITERM pin voltage drops below 100mV* for longer than t_{TERM} (typically 1ms), charging is terminated. The charge current is latched off and the charger enters standby mode where the input supply current drops to 200µA. (Note: Termination is disabled in trickle charging and thermal limiting modes).

I_{TERM} can be set to one tenth of I_{CHG} by shorting the ITERM pin to the PROG pin, thus eliminating the need for external resistor R_{TERM}. When configured in this way, I_{TERM} is always set to $I_{CHG}/10$, and the programmed charge current is set by the equation:

$$I_{CHG} = \frac{500V}{R_{PROG}}, R_{PROG} = \frac{500V\ **}{I_{CHG}}$$

* Any external sources that hold the ITERM pin above 100mV will prevent the LTC3552 from terminating a charge cycle.

** These equations apply only when the ITERM pin is shorted to the PROG pin.

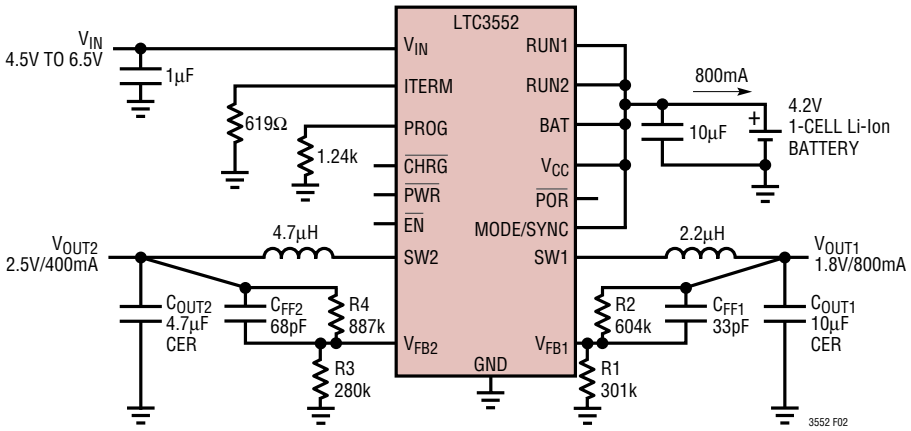

Figure 2. LTC3552 Basic Application Circuit

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When charging, transient loads on the BAT pin can cause the ITERM pin to fall below 100mV for short periods of time before the DC charge current has dropped to 10% of the programmed value. The 1ms filter time (t_{TERM}) on the termination comparator ensures that transient loads of this nature do not result in premature charge cycle termination. Once the average charge current drops below the programmed termination threshold, the charger terminates the charge cycle and stops providing current out of the BAT pin. In this state, any load on the BAT pin must be supplied by the battery.

The charger constantly monitors the BAT pin voltage in standby mode. If this voltage drops below the 4.1V recharge threshold (V_{RECHRG}), another charge cycle begins and charge current is once again supplied to the battery. To manually restart a charge cycle when in standby mode, the input voltage must be removed and reapplied, or the charger must be shut down and restarted using the $\overline{EN}$ pin.

Switching Regulator Inductor Selection

The inductor value has a direct effect on inductor ripple current ΔI_L, which decreases with higher inductance and increases with higher V_{CC} or V_{OUT}:

$$\Delta I_L = \frac{V_{OUT}}{f_0 \bullet L}\left(1-\frac{V_{OUT}}{V_{CC}}\right)$$

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output ripple voltage, greater core losses, and lower output current capability. A reasonable starting point for setting ripple current is

$$\Delta I_L = 0.3 \bullet I_{OUT(MAX)},$$

where $I_{OUT(MAX)}$ is 800mA for regulator 1 and 400mA for regulator 2. The largest ripple current ΔI_L occurs at the maximum input voltage. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation:

$$L = \frac{V_{OUT}}{f_0 \bullet \Delta I_L}\left(1-\frac{V_{OUT}}{V_{CC(MAX)}}\right)$$

The inductor value will also have an effect on Burst Mode operation. The transition from low current operation begins when the peak inductor current falls below a level set by the burst clamp. Lower inductor values result in higher ripple current which causes this to occur at lower load currents. This causes a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to increase.

Inductor Core Selection

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and do not radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends more on the price vs size requirements and any radiated field/EMI requirements than on what the LTC3552 requires to operate. Table 1 shows some typical surface mount inductors that work well in LTC3552 applications.

Table 1. Representative Surface Mount Inductors

PART NUMBER	VALUE (µH)	DCR (Ω MAX)	MAX DC CURRENT (A)	SIZE W × L × H (mm)
Sumida CDRH3D16	2.2 3.3 4.7	0.075 0.110 0.162	1.20 1.10 0.90	3.8 × 3.8 × 1.8
Sumida CDRH2D11	1.5 2.2	0.068 0.170	0.900 0.780	3.2 × 3.2 × 1.2
Sumida CMD4D11	2.2 3.3	0.116 0.174	0.950 0.770	4.4 × 5.8 × 1.2
Murata LQH32CN	1.0 2.2	0.060 0.097	1.00 0.79	2.5 × 3.2 × 2.0
Toko D312F	2.2 3.3	0.060 0.260	1.08 0.92	2.5 × 3.2 × 2.0
Murata ELT5KT	3.3 4.7	0.17 0.20	1.00 0.95	4.5 × 5.4 × 1.2

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Input Capacitor (C_{IN}) Selection

In continuous mode, the input current of the converter is a square wave with a duty cycle of approximately V_{OUT}/V_{CC}. To prevent large voltage transients, a low equivalent series resistance (ESR) input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$I_{RMS} \approx I_{MAX} \frac{\sqrt{V_{OUT}(V_{CC} - V_{OUT})}}{V_{CC}}$$

where the maximum average output current I_{MAX} equals the peak current minus 1/2 the peak-to-peak ripple current, $I_{MAX} = I_{LIM} - \Delta I_L/2$. This formula has a maximum at $V_{CC} = 2 \bullet V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case is commonly used to design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours life-time. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet the size or height requirements of the design. An additional 0.1µF to 1µF ceramic capacitor is also recommended on V_{CC} for high frequency decoupling, when not using an all ceramic capacitor solution.

Output Capacitor (C_{OUT}) Selection

The selection of C_{OUT} is driven by the required ESR to minimize ripple voltage and load step transients. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is determined by

$$\Delta V_{OUT} \approx \Delta I_L \left(ESR + \frac{1}{8 f_O C_{OUT}} \right)$$

where f_O = operating frequency, C_{OUT} = output capacitance and ΔI_L = ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. With $\Delta I_L = 0.3 \bullet I_{OUT(MAX)}$ the output ripple will be less than 100mV at maximum V_{CC} and f_O = 2.25MHz with $ESR_{COUT} < 150m\Omega$.

Once the ESR requirements for C_{OUT} have been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement, except for an all ceramic solution. In surface mount applications, multiple capacitors may have to be paralleled to meet the capacitance, ESR or RMS current handling requirement of the application. Aluminum electrolytic, special polymer, ceramic and solid tantalum capacitors are all available in surface mount packages.

The OSCON semiconductor dielectric capacitor available from Sanyo has the lowest ESR (size) product of any aluminum electrolytic at a somewhat higher price. Special polymer capacitors, such as Sanyo POSCAP, Panasonic Special Polymer (SP), and Kemet A700, offer very low ESR, but have a lower capacitance density than other types. Tantalum capacitors have the highest capacitance density, but they have a larger ESR and it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalums, available in case heights ranging from 2mm to 4mm. Aluminum electrolytic capacitors have a significantly larger ESR, and are often used in extremely cost-sensitive applications provided that consideration is given to ripple current ratings and long term reliability. Ceramic capacitors have the lowest ESR and cost, but also have the lowest capacitance density, a high voltage and temperature coefficient, and exhibit audible piezoelectric effects. In addition, the high Q of ceramic capacitors along with trace inductance can lead to significant ringing. In most cases, 0.1µF to 1µF of X5R dielectric ceramic capacitors should also be placed close to the LTC3552 in parallel with the main capacitors for high frequency decoupling.

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Ceramic Input and Output Capacitors

Higher value, lower cost ceramic capacitors are now becoming available in smaller case sizes. These are tempting for switching regulator use because of their very low ESR. Unfortunately, the ESR is so low that it can cause loop stability problems. Solid tantalum capacitor ESR generates a loop "zero" at 5kHz to 50kHz that is instrumental in giving acceptable loop phase margin. Ceramic capacitors remain capacitive to beyond 300kHz and usually resonate with their ESL before ESR becomes effective. Also, ceramic caps are prone to temperature effects which requires the designer to check loop stability over the operating temperature range. To minimize their large temperature and voltage coefficients, only X5R or X7R ceramic capacitors should be used. A good selection of ceramic capacitors is available from Taiyo Yuden, AVX, Kemet, TDK, and Murata.

Great care must be taken when using only ceramic input and output capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the V_{CC} pin. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, the ringing at the input can be large enough to damage the part.

Since the ESR of a ceramic capacitor is very low, the input and output capacitor must instead fulfill a charge storage requirement. During a load step, the output capacitor must instantaneously supply the current to support the load until the feedback loop raises the switch current enough to support the load. The time required for the feedback loop to respond is dependent on the compensation and the output capacitor size. Typically, 3-4 cycles are required to respond to a load step, but only in the first cycle does the output drop linearly. The output droop, V_{DROOP}, is usually about 2-3 times the linear drop of the first cycle. Thus, a good place to start is with the output capacitor size of approximately:

$$C_{OUT} \approx 2.5\left(\frac{\Delta I_{OUT}}{f_0 \bullet V_{DROOP}}\right)$$

More capacitance may be required depending on the duty cycle and load step requirements. In most applications, the input capacitor is merely required to supply high frequency bypassing, since the impedance to the supply is very low. A 10µF ceramic capacitor is usually enough for these conditions.

Setting the Output Voltage

The switching regulator develops a 0.6V reference voltage between the feedback pin, V_{FB}, and the ground as shown in Figure 2. The output voltage is set by a resistive divider according to the following formula:

$$V_{OUT} = 0.6V\left(1+\frac{R2}{R1}\right)$$

Keeping the current low (< 5µA) in these resistors maximizes efficiency, but making it too low may allow stray capacitance to cause noise problems and reduce the phase margin of the error amplifier loop.

To improve the frequency response, a feed-forward capacitor, C_{FF}, may also be used. Great care should be taken to route the V_{FB} line away from noise sources, such as the inductor or the SW line.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to $\Delta I_{LOAD} \bullet$ ESR, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT}, generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the

APPLICATIONS INFORMATION

actual overall supply performance. A feedforward capacitor, C_{FF}, is added to improve the high frequency response. Capacitor C_{FF} provides phase lead by creating a high frequency zero with the top feedback resistor, which improves the phase margin. For a detailed explanation of optimizing the compensation components, including a review of control loop theory, refer to Application Note 76.

In some applications, a more severe transient can be caused by switching loads with large (>1µF) input capacitors. The discharged load input capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem, if the switch connecting the load has low resistance and is driven quickly. The solution is to limit the turn-on speed of the load switch driver. A Hot Swap™ controller is designed specifically for this purpose and usually incorporates current limiting, short-circuit protection, and soft-starting.

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\% \text{ Efficiency} = 100\% - (L1 + L2 + L3 + ...)$$

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC3552 circuits: 1) V_{CC} quiescent current, 2) switching losses, 3) I^2R losses, 4) other losses.

1) The V_{CC} current is the DC supply current given in the Electrical Characteristics which excludes MOSFET driver and control currents. V_{CC} current results in a small (<0.1%) loss that increases with V_{CC}, even at no load.

2) The switching current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from V_{CC} to ground. The resulting dQ/dt is a current out of V_{CC} that is typically much larger than the DC bias current. In continuous mode, $I_{GATECHG} = f_O(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the internal top and bottom MOSFET switches. The gate charge losses are proportional to V_{CC} and thus their effects will be more pronounced at higher supply voltages.

3) I^2R losses are calculated from the DC resistances of the internal switches, R_{SW}, and external inductor, R_L. In continuous mode, the average output current flows through inductor L, but is "chopped" between the internal top and bottom switches. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (D) as follows:

$$R_{SW} = (R_{DS(ON)TOP})(D) + (R_{DS(ON)BOT})(1 - D)$$

The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain I^2R losses:

$$I^2R \text{ losses} = I_{OUT}^2(R_{SW} + R_L)$$

4) Other "hidden" losses such as copper trace and internal battery resistances can account for additional efficiency degradations in portable systems. It is very important to include these "system" level losses in the design of a system. The internal battery and fuse resistance losses can be minimized by making sure that C_{IN} has adequate charge storage and very low ESR at the switching frequency. Other losses include diode conduction losses during dead-time and inductor core losses generally account for less than 2% total additional loss.

Hot Swap is a trademark of Linear Technology Corporation.

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Thermal Considerations

The battery charger's thermal regulation feature and the switching regulator's high efficiency make it unlikely that the LTC3552 will dissipate enough power to exceed its maximum junction temperature. However, in applications where the LTC3552 is running at high ambient temperature with low supply voltage and high duty cycles, the power dissipated may result in excessive junction temperatures. To prevent the LTC3552 from exceeding the maximum junction temperature, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated will raise the junction temperature above the maximum rating. The temperature rise is given by:

$$T_{RISE} = P_D \bullet \theta_{JA}$$

where P_D is the power dissipated and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature. The junction temperature, T_J, is given by:

$$T_J = T_{RISE} + T_{AMBIENT}$$

As an example, consider the case when the battery charger is idle, and both regulators are operating at an input voltage of 2.7V with a load current of 400mA and 800mA and an ambient temperature of 70°C. From the Typical Performance Characteristics graph of Switch Resistance, the $R_{DS(ON)}$ resistance of the main switch is 0.425Ω. Therefore, power dissipated by each regulator is:

$$P_D = I^2 \bullet R_{DS(ON)} = 272mW \text{ and } 68mW$$

The DHC16 package junction-to-ambient thermal resistance, θ_{JA}, is 40°C/W. Therefore, the junction temperature of the regulator operating in a 70°C ambient temperature is approximately:

$$T_J = (0.272 + 0.068) \bullet 40 + 70 = 83.6°C$$

which is below the absolute maximum junction temperature of 125°C.

The majority of the LTC3552 power dissipation comes from the battery charger. Fortunately, the LTC3552 automatically reduces the charge current during high power conditions using a patented thermal regulation circuit. Thus, it is not necessary to design for worst-case power dissipation scenarios. The conditions that cause the LTC3552 to reduce charge current through thermal feedback can be approximated by considering the power dissipated in the IC. The approximate ambient temperature at which the thermal feedback begins to protect the IC is:

$$T_A = 120°C - P_D\theta_{JA}$$

$$T_A = 120°C - (P_{D(CHARGER)} + P_{D(REGULATOR)}) \bullet \theta_{JA}$$

Most of the charger's power dissipation is generated from the internal charger MOSFET. Thus, the power dissipation is calculated to be:

$$P_{D(CHARGER)} = (V_{IN} - V_{BAT}) \bullet I_{BAT}$$

V_{IN} is the charger supply voltage, V_{BAT} is the battery voltage and I_{BAT} is the charge current.

Example: An LTC3552 operating from a 5V supply is programmed to supply 800mA full-scale current to a discharged Li-Ion battery with a voltage of 3.3V. For simplicity, assume the regulators are disabled and dissipate no power.

The charger power dissipation is calculated to be:

$$P_{D(CHARGER)} = (5V - 3.3V) \bullet 800mA = 1.36W$$

Thus, the ambient temperature at which the LTC3552 charger begins to reduce the charge current is approximately:

$$T_A = 120°C - 1.36W \bullet 40°C/W$$

$$T_A = 120°C - 54.4°C$$

$$T_A = 65.6°C$$

The LTC3552 can be used above 65°C ambient but the charge current will be reduced from the programmed 800mA. The approximate current at a given ambient temperature can be approximated by:

$$I_{BAT} = \frac{120°C - T_A}{(V_{IN} - V_{BAT}) \bullet \theta_{JA}}$$

Using the previous example with an ambient temperature of 70°C (and no heat dissipation from the regulator), the charge current will be reduced to approximately:

$$I_{BAT} = \frac{120°C - 70°C}{(5V - 3.3V) \bullet 40°C/W} = \frac{50°C}{68°C/A}$$

$$I_{BAT} = 735mA$$

APPLICATIONS INFORMATION

The previous analysis can be repeated to take into account the power dissipation of the regulator by:

$$I_{BAT} = \frac{120°C - T_A - T_{RISE(REGULATOR)}}{(V_{IN} - V_{BAT}) \bullet \theta_{JA}}$$

However, the regulator typically dissipates significantly less heat than the charger (even in worst-case situations), the calculations here should work well as an approximation.

Moreover, when thermal feedback reduces the charge current, the voltage at the PROG pin is also reduced proportionally. It is important to remember that LTC3552 applications do not need to be designed for worst-case thermal conditions since the IC will automatically reduce charge current when the junction temperature reaches approximately 120°C.

In order to deliver maximum charge current under all conditions, it is critical that the exposed metal pad on the backside of the LTC3552 package is soldered to relatively large areas of PC board copper with vias to inner copper layers. Failure to make thermal contact between the exposed pad on the backside of the package and the copper board will result in thermal resistances far greater than 40°C/W. As an example, a correctly soldered LTC3552 can deliver over 800mA to a battery from a 5V supply at room temperature. Without a good backside thermal connection, this number will drop considerably.

Battery Charger Stability Considerations

The constant-voltage mode feedback loop is stable without an output capacitor, provided a battery is connected to the charger output. With no battery present, an output capacitor on the BAT pin is recommended to reduce ripple voltage. When using high value, low ESR ceramic capacitors, it is recommended to add a 1Ω resistor in series with the capacitor. No series resistor is needed if tantalum capacitors are used. In constant-current mode, the PROG pin is in the feedback loop, not the battery. The constant-current mode stability is affected by the impedance at the PROG pin. With no additional capacitance on the PROG pin, the charger is stable with program resistor values as high as 20k; however, additional capacitance on this node reduces the maximum allowed program resistor. The pole frequency at the PROG pin should be kept above 100kHz. Therefore, if the PROG pin is loaded with a capacitance, C_{PROG}, the following equation can be used to calculate the maximum resistance value for R_{PROG}:

$$R_{PROG} \leq \frac{1}{2\pi \bullet 10^5 \bullet C_{PROG}}$$

Average, rather than instantaneous charge current may be of interest to the user. For example, if a switching power supply operating in low current mode is connected in parallel with the battery, the average current being pulled out of the BAT pin is typically of more interest than the instantaneous current pulses. In such a case, a simple RC filter can be used on the PROG pin to measure the average battery current, as shown in Figure 3. A 10k resistor has been added between the PROG pin and the filter capacitor to ensure stability.

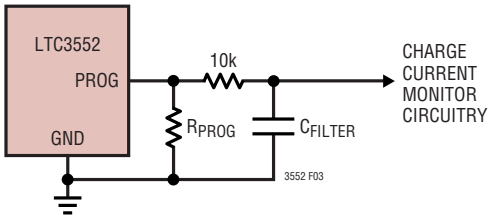


Figure 3. Isolating Capacitive Load on PROG Pin and Filtering

V_{IN} Bypass Capacitor

Many types of capacitors can be used for input bypassing; however, caution must be exercised when using multilayer ceramic capacitors. Because of the self-resonant and high Q characteristics of some types of ceramic capacitors, high voltage transients can be generated under some start-up conditions such as connecting the charger input to a live power source. Adding a 1.5Ω resistor in series with an X5R ceramic capacitor will minimize start-up voltage transients. For more information, see Application Note 88.

APPLICATIONS INFORMATION

Reverse Polarity Input Voltage Protection

In some applications, protection from reverse polarity voltage on V_{IN} is desired. If the supply voltage is high enough, a series blocking diode can be used. In other cases, where the voltage drop must be kept low, a P-regulator MOSFET can be used (as shown in Figure 4).

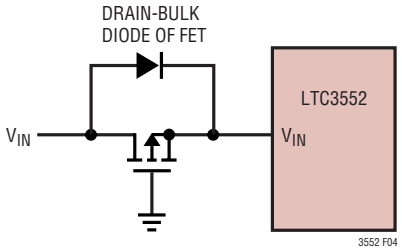


Figure 4. Low Loss Input Reverse Polarity Protection

Design Example

As a design example, assume the LTC3552 is used in a single lithium-ion battery-powered cellular phone application.

Starting with the charger, choosing R_{PROG} to be 1.24k programs the charger for 806mA. A good rule of thumb for $I_{TERMINATE}$ is one tenth the full charge current, so R_{ITERM} is picked to be 1.24k ($I_{TERMINATE}$ = 80mA).

For the switching regulator, V_{CC} will be operating from a maximum of 4.2V down to about 2.7V. The load requires a maximum of 800mA in active mode and 2mA in standby mode. Regulator 1 output voltage is 1.8V. Since the load still needs power in standby, Burst Mode operation is selected for good low load efficiency (connect MODE/SYNC to V_{CC}). First, calculate the inductor value for about 30% ripple current at maximum V_{CC}:

$$L = \frac{1.8V}{2.25MHz \bullet 240mA}\left(1 - \frac{1.8V}{4.2V}\right) = 1.9\mu H$$

Choosing a vendor's closest inductor value of 2.2µH, results in a maximum ripple current of:

$$\Delta I_L = \frac{1.8V}{2.25MHz \bullet 2.2\mu H}\left(1 - \frac{1.8V}{4.2V}\right) = 208mA$$

For cost reasons, a ceramic capacitor will be used. C_{OUT} selection is then based on load step droop instead of ESR requirements. For a 5% output droop:

$$C_{OUT} = 2.5\frac{800mA}{2.25MHz \bullet (5\% \bullet 2.5V)} = 7.1\mu F$$

A good standard value is 10µF. Since the impedance of a Li-Ion battery is very low, C_{IN} is typically 10µF. The output voltage can now be programmed by choosing the values of R1 and R2. To maintain high efficiency, the current in these resistors should be kept small. Choosing 2µA with 0.6V feedback voltage makes R1 ~300k. A close standard 1% resistor is 301k, and R2 is then 604k. The $\overline{POR}$ pin is an open-drain output and requires a pull-up resistor. A 100k resistor is used for adequate speed. Figure 2 shows the complete schematic for this design example.

APPLICATIONS INFORMATION

Board Layout Considerations

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3552. These items are also illustrated graphically in the layout diagram of Figure 5. Check the following in your layout:

1. Does the capacitor C_S connect to the power V_{CC} and GND (exposed pad) as closely as possible? This capacitor provides the AC current to the internal power MOSFETs and their drivers.
2. The feedback signals V_{FB} should be routed away from noisy components and traces, such as the SW line, and its trace should be minimized.
3. Are the C_{OUT} and L1 closely connected? The (–) plate of C_{OUT} returns current to GND and the (–) plate of C_S.
4. Keep sensitive components away from the SW pins. The input capacitor C_S should be routed away from the SW traces and the inductors.
5. A ground plane is preferred, but if not available, keep the signal and power grounds segregated with small signal components returning to the GND pin at one point and should not share the high current path of C_S or C_{OUT}.
6. Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. These copper areas should be connected to V_{CC} or GND.

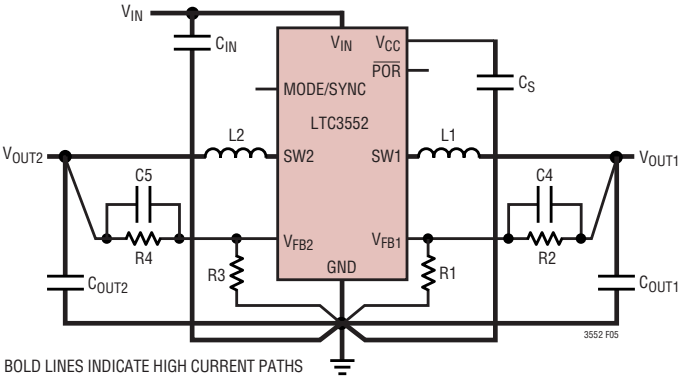


Figure 5. Layout Diagram

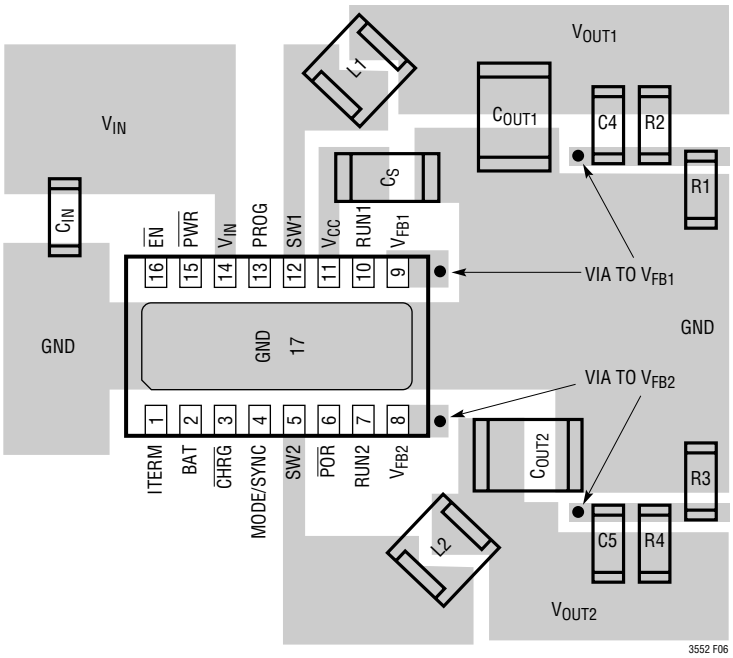
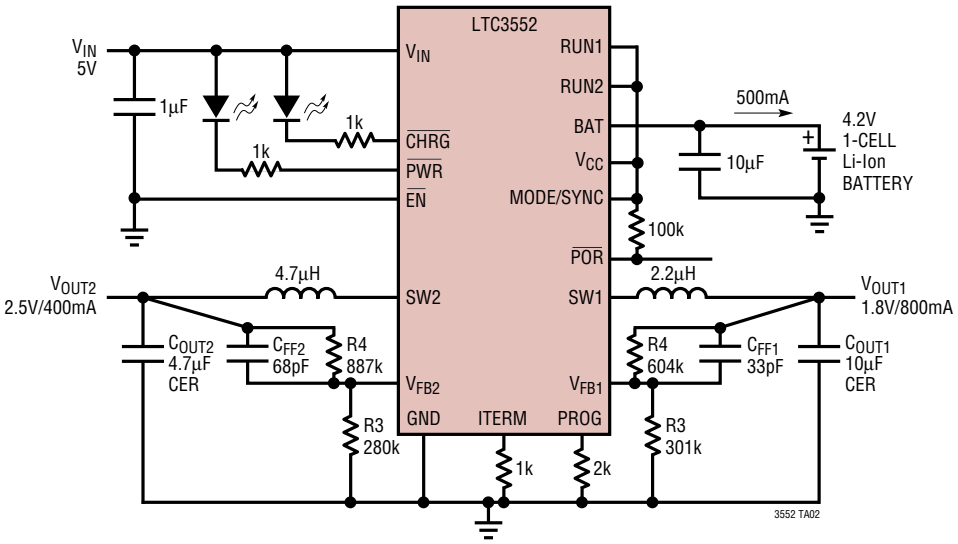


Figure 6. Suggested Layout

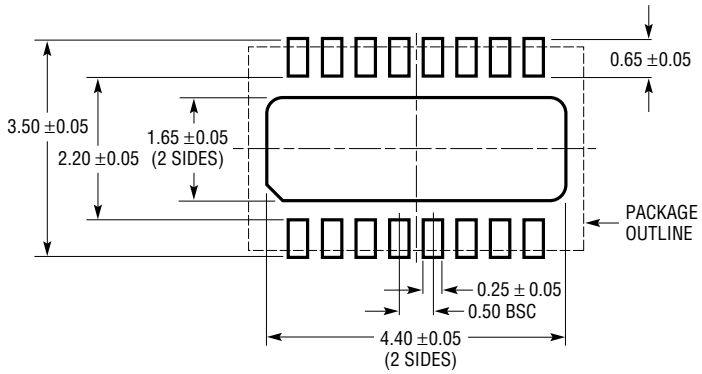
TYPICAL APPLICATION

Full-Featured Single-Cell Li-Ion Charger Plus Dual Step-Down Converter

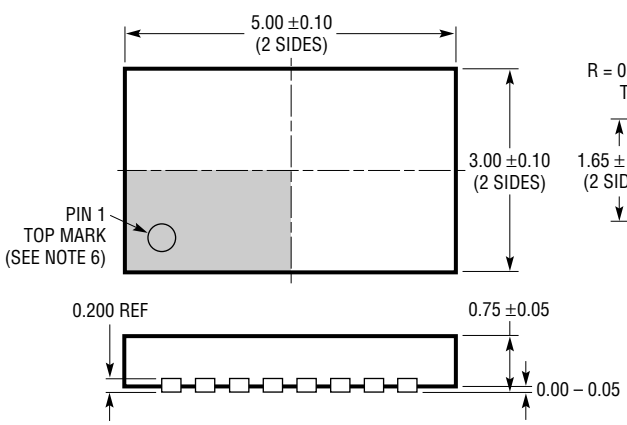


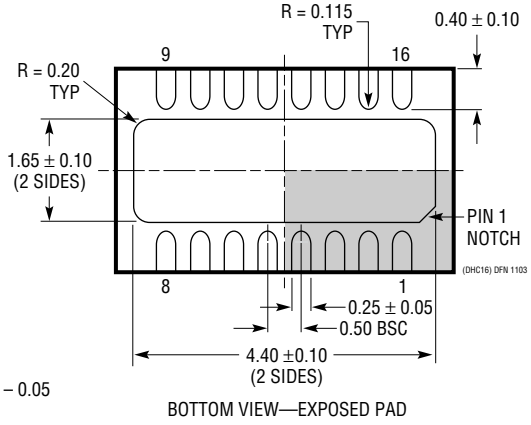
PACKAGE DESCRIPTION

DHC Package
16-Lead Plastic DFN (5mm × 3mm)
(Reference LTC DWG # 05-08-1706)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



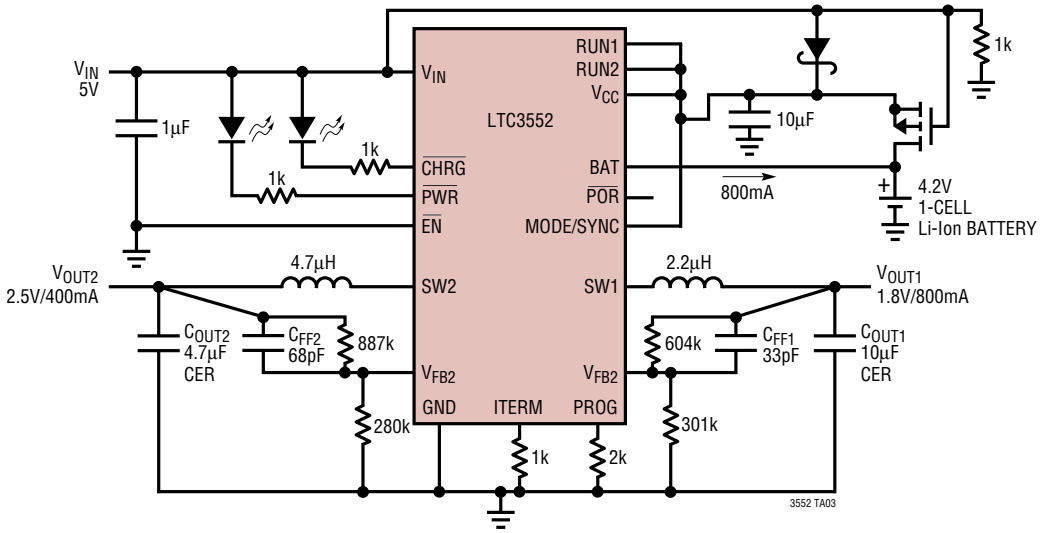


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WJED-1) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

Li-Ion Charger and Step-Down Converters with PowerPath™



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3455	Dual DC/DC Converter with USB Power Management and Li-Ion Battery Charger	Efficiency >96%, Accurate USB Current Limiting (500mA/100mA), 4mm × 4mm QFN-24 Package
LTC3548	Dual Synchronous, 400mA/800mA, 2.25HMz Step-Down DC/DC Regulator	High Efficiency: Up to 95%, I_Q: 40µA, 2.25MHz Frequency, MSOP-10 and 3mm × 3mm DFN-10 Packages
LTC3550	Dual Input USB/AC Adapter Li-Ion Battery Charger with adjustable output 600mA Buck Converter	Synchronous Buck Converter, Efficiency: 93%, Adjustable Output at 600mA; Charge Current: 950mA Programmable, USB Compatible, Automatic Input Power Detection and Selection, 5mm × 3mm DFN-16 Package
LTC3550-1	Dual Input USB/AC Adapter Li-Ion Battery Charger with 600mA Buck Converter	Synchronous Buck Converter, Efficiency: 93%, Output: 1.875V at 600mA; Charge Current: 950mA Programmable, USB Compatible, Automatic Input Power Detection and Selection, 5mm × 3mm DFN-16 Package
LTC3552-1	Standalone Linear Li-Ion Battery Charger with Dual Synchronous Buck Converter	Synchronous Buck Converter, Efficiency: >90%, Output: 1.8V at 800mA, 1.575V at 400mA; Charge Current Programmable Up to 950mA, USB Compatible, 5mm × 3mm DFN-16 Package
LTC4053-4.2	USB Compatible Li-Ion Battery Charger with Thermal Regulation	Charges Single-Cell Li-Ion Batteries, From USB, MS Package
LTC4054/LTC4054X	Standalone Linear Li-Ion Battery Charger with Integrated Pass Transistor in ThinSOT™	Thermal Regulation Prevents Overheating, C/10 Termination, C/10 Indicator, Up to 800mA Charge Current
LTC4055	USB Power Controller and Battery Charger	Charges Single-Cell Li-Ion Batteries Directly From USB Port, Thermal Regulation, 4mm × 4mm QFN-16 Package
LTC4058/LTC4058X	Standalone 950mA Lithium-Ion Charger in DFN	C/10 Charge Termination, Battery Kelvin Sensing, ±7% Charge Accuracy
LTC4061	Standalone Linear Li-Ion Battery Charger with Thermistor Input	Charge Current Programmable Up to 1A
LTC4066	Standalone Linear Li-Ion Battery Charger with Thermistor Input	Charges Single-Cell Li-Ion From USB Port, DFN Package
LTC4068/LTC4068X	Standalone Linear Li-Ion Battery Charger with Programmable Termination	Charge Current Up to 950mA, Thermal Regulation, 3mm × 3mm DFN-8 Package
LTC4412	Low-Loss PowerPath™ Controller in ThinSOT	V_{IN}: 3V to 28V, Automatic Switching Between DC Sources

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Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

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