

LTC2051/LTC2052

ABSOLUTE MAXIMUM RATINGS (Note 1)

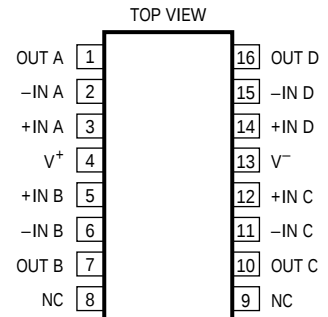
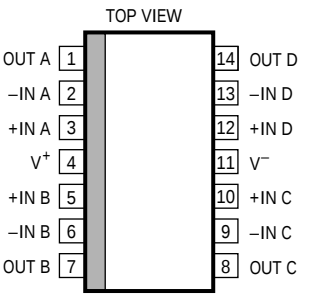
Total Supply Voltage (V^+ to V^-)	Operating Temperature Range	-40°C to 125°C
LTC2051/LTC2052	Specified Temperature Range (Note 3)	-40°C to 125°C
LTC2051HV/LTC2052HV	Storage Temperature Range	-65°C to 150°C
Input Voltage (Note 5)	DD Package	-65°C to 125°C
Output Short-Circuit Duration	Lead Temperature (Soldering, 10 sec)	300°C

PACKAGE/ORDER INFORMATION

TOP VIEW DD PACKAGE 8-LEAD (3mm x 3mm) PLASTIC DFN $T_{JMAX} = 125^{\circ}\text{C}$, $\theta_{JA} = 160^{\circ}\text{C/W}$ EXPOSED PAD (PIN 9) IS CONNECTED TO V^{-} (PIN 4)		TOP VIEW MS8 PACKAGE 8-LEAD PLASTIC MSOP $T_{JMAX} = 125^{\circ}\text{C}$, $\theta_{JA} = 250^{\circ}\text{C/W}$		TOP VIEW MS10 PACKAGE 10-LEAD PLASTIC MSOP $T_{JMAX} = 125^{\circ}\text{C}$, $\theta_{JA} = 250^{\circ}\text{C/W}$	
ORDER PART NUMBER*	DD PART MARKING	ORDER PART NUMBER	MS8 PART MARKING	ORDER PART NUMBER	MS10 PART MARKING
LTC2051CDD LTC2051IDD LTC2051HVCDD LTC2051HVIDD	LAAN LAEL	LTC2051CMS8 LTC2051IMS8 LTC2051HVCMS8 LTC2051HVIMS8 LTC2051HMS8 LTC2051HVHMS8	LTMN LTMP LTPJ LTPK LTVF LTVH	LTC2051CMS10 LTC2051IMS10 LTC2051HVCMS10 LTC2051HVIMS10	LTMQ LTMR LTRB LTRC
TOP VIEW S8 PACKAGE 8-LEAD PLASTIC SO $T_{JMAX} = 125^{\circ}\text{C}$, $\theta_{JA} = 190^{\circ}\text{C/W}$			ORDER PART NUMBER	S8 PART MARKING	
			LTC2051CS8 LTC2051IS8 LTC2051HVCS8 LTC2051HVIS8 LTC2051HS8 LTC2051HVHS8	2051 2051I 2051HV 051HVI 2051H 051HVH	
Order Options Tape and Reel: Add #TR Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF Lead Free Part Marking: http://www.linear.com/leadfree/					

Consult LTC Marketing for parts specified with wider operating temperature ranges.

PACKAGE/ORDER INFORMATION

 GN PACKAGE 16-LEAD PLASTIC SSOP $T_{JMAX} = 125^{\circ}\text{C}$, $\theta_{JA} = 110^{\circ}\text{C/W}$	ORDER PART NUMBER	 S PACKAGE 14-LEAD PLASTIC SO $T_{JMAX} = 125^{\circ}\text{C}$, $\theta_{JA} = 110^{\circ}\text{C/W}$	ORDER PART NUMBER
	LTC2052CGN LTC2052IGN LTC2052HVCGN LTC2052HVIGN LTC2052HGN LTC2052HVHGN		LTC2052CS LTC2052IS LTC2052HVCS LTC2052HVIS LTC2052HS LTC2052HVHS
GN PART MARKING			
2052 2052I 2052HV 052HVI 2052H 052HVH			

AVAILABLE OPTIONS

PART NUMBER	AMPS/PACKAGE	SPECIFIED TEMP RANGE	SPECIFIED VOLTAGE	PACKAGE
LTC2051CDD	2	0°C to 70°C	3V, 5V	DD
LTC2051CS8	2	0°C to 70°C	3V, 5V	SO-8
LTC2051CMS8	2	0°C to 70°C	3V, 5V	8-Lead MSOP
LTC2051CMS10	2	0°C to 70°C	3V, 5V	10-Lead MSOP
LTC2051HVCDD	2	0°C to 70°C	3V, 5V, $\pm 5\text{V}$	DD
LTC2051HVCS8	2	0°C to 70°C	3V, 5V, $\pm 5\text{V}$	SO-8
LTC2051HVCMS8	2	0°C to 70°C	3V, 5V, $\pm 5\text{V}$	8-Lead MSOP
LTC2051HVCMS10	2	0°C to 70°C	3V, 5V, $\pm 5\text{V}$	10-Lead MSOP
LTC2051IDD	2	-40°C to 85°C	3V, 5V	DD
LTC2051IS8	2	-40°C to 85°C	3V, 5V	SO-8
LTC2051IMS8	2	-40°C to 85°C	3V, 5V	8-Lead MSOP
LTC2051IMS10	2	-40°C to 85°C	3V, 5V	10-Lead MSOP
LTC2051HVIDD	2	-40°C to 85°C	3V, 5V, $\pm 5\text{V}$	DD
LTC2051HVIS8	2	-40°C to 85°C	3V, 5V, $\pm 5\text{V}$	SO-8
LTC2051HVIMS8	2	-40°C to 85°C	3V, 5V, $\pm 5\text{V}$	8-Lead MSOP
LTC2051HVIMS10	2	-40°C to 85°C	3V, 5V, $\pm 5\text{V}$	10-Lead MSOP
LTC2051HS8	2	-40°C to 125°C	3V, 5V	SO-8
LTC2051HMS8	2	-40°C to 125°C	3V, 5V	8-Lead MSOP
LTC2051HVHS8	2	-40°C to 125°C	3V, 5V, $\pm 5\text{V}$	SO-8
LTC2051HVHMS8	2	-40°C to 125°C	3V, 5V, $\pm 5\text{V}$	8-Lead MSOP
LTC2052CS	4	0°C to 70°C	3V, 5V	14-Lead SO
LTC2052CGN	4	0°C to 70°C	3V, 5V	16-Lead SSOP
LTC2052HVCS	4	0°C to 70°C	3V, 5V, $\pm 5\text{V}$	14-Lead SO
LTC2052HVCGN	4	0°C to 70°C	3V, 5V, $\pm 5\text{V}$	16-Lead SSOP

LTC2051/LTC2052

AVAILABLE OPTIONS

PART NUMBER	AMPS/PACKAGE	SPECIFIED TEMP RANGE	SPECIFIED VOLTAGE	PACKAGE
LTC2052IS	4	–40°C to 85°C	3V, 5V	14-Lead SO
LTC2052IGN	4	–40°C to 85°C	3V, 5V	16-Lead SSOP
LTC2052HVIS	4	–40°C to 85°C	3V, 5V, ±5V	14-Lead SO
LTC2052HVIGN	4	–40°C to 85°C	3V, 5V, ±5V	16-Lead SSOP
LTC2052HS	4	–40°C to 125°C	3V, 5V	14-Lead SO
LTC2052HGN	4	–40°C to 125°C	3V, 5V	16-Lead SSOP
LTC2052HVHS	4	–40°C to 125°C	3V, 5V, ±5V	14-Lead SO
LTC2052HVHGN	4	–40°C to 125°C	3V, 5V, ±5V	16-Lead SSOP

ELECTRICAL CHARACTERISTICS (LTC2051/LTC2052, LTC2051HV/LTC2052HV) The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_S = 3\text{V}, 5\text{V}$ unless otherwise noted. (Note 3)

PARAMETER	CONDITIONS		LTC2051C/LTC2052C LTC2051I/LTC2052I			LTC2051H/LTC2052H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	(Note 2)			±0.5	±3		±0.5	±3	μV
Average Input Offset Drift	(Note 2)	●		0.01	±0.03		0.01	±0.05	μV/°C
Long-Term Offset Drift				50			50		nV/√mo
Input Bias Current (Note 4)	$V_S = 3\text{V}$	●		±8	±50		±8	±50	pA
	$V_S = 3\text{V}$	●			±100			±3000	pA
	$V_S = 5\text{V}$	●		±25	±75		±25	±75	pA
	$V_S = 5\text{V}$	●			±150			±3000	pA
Input Offset Current (Note 4)	$V_S = 3\text{V}$	●			±100			±100	pA
	$V_S = 3\text{V}$	●			±150			±700	pA
	$V_S = 5\text{V}$	●			±150			±150	pA
	$V_S = 5\text{V}$	●			±200			±700	pA
Input Noise Voltage	$R_S = 100\Omega$, DC to 10Hz			1.5			1.5		μV _{p-p}
Common Mode Rejection Ratio	$V_{CM} = \text{GND to } V^+ - 1.3$, $V_S = 3\text{V}$	●	115	130		115	130		dB
			110	130		110	130		dB
	$V_{CM} = \text{GND to } V^+ - 1.3$, $V_S = 5\text{V}$	●	120	130		120	130		dB
			115	130		115	130		dB
Power Supply Rejection Ratio		●	120	130		120	130		dB
			115	130		115	130		dB
Large-Signal Voltage Gain	$R_L = 10\text{k}$, $V_S = 3\text{V}$	●	120	140		120	140		dB
			115	140		115	140		dB
	$R_L = 10\text{k}$, $V_S = 5\text{V}$	●	125	140		125	140		dB
			120	140		120	140		dB
Output Voltage Swing High	$R_L = 2\text{k to GND}$	●	$V^+ - 0.15$	$V^+ - 0.06$		$V^+ - 0.15$	$V^+ - 0.06$		V
	$R_L = 10\text{k to GND}$	●	$V^+ - 0.05$	$V^+ - 0.02$		$V^+ - 0.05$	$V^+ - 0.02$		V
Output Voltage Swing Low	$R_L = 2\text{k to GND}$	●	2	15		2	15		mV
	$R_L = 10\text{k to GND}$	●	2	15		2	15		mV
Slew Rate				2			2		V/μs
Gain Bandwidth Product				3			3		MHz
Supply Current (Per Amplifier)	No Load, $V_S = 3\text{V}$, $V_{SHDN} = V_{IH}$	●	0.75	1.0		0.75	1.1		mA
	No Load, $V_S = 5\text{V}$, $V_{SHDN} = V_{IH}$	●	0.85	1.2		0.85	1.3		mA
Supply Current, Shutdown	$V_{SHDN} = V_{IL}$, $V_S = 3\text{V}$	●	2	5		2	5		μA
	$V_{SHDN} = V_{IL}$, $V_S = 5\text{V}$	●	4	10		4	10		μA

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ELECTRICAL CHARACTERISTICS

(LTC2051/LTC2052, LTC2051HV/LTC2052HV) The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_S = 3\text{V}$, 5V unless otherwise noted. (Note 3)

PARAMETER	CONDITIONS		LTC2051C/LTC2052C LTC2051I/LTC2052I			LTC2051H/LTC2052H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Shutdown Pin Input Low Voltage (V_{IL})		●			$V^- + 0.5$			$V^- + 0.5$	V
Shutdown Pin Input High Voltage (V_{IH})		●	$V^+ - 0.5$			$V^+ - 0.5$			V
Shutdown Pin Input Current	$V_{SHDN} = V_{IL}$, $V_S = 3\text{V}$ $V_{SHDN} = V_{IL}$, $V_S = 5\text{V}$	●		-1 -2	-3 -5		-1 -2	-3 -5	μA μA
Internal Sampling Frequency				7.5			7.5		kHz

(LTC2051HV/LTC2052HV) The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_S = \pm 5\text{V}$ unless otherwise noted. (Note 3)

PARAMETER	CONDITIONS		LTC2051C/LTC2052C LTC2051I/LTC2052I			LTC2051H/LTC2052H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	(Note 2)			± 1	± 3		± 1	± 3	μV
Average Input Offset Drift	(Note 2)	●		0.01	± 0.03		0.01	± 0.05	$\mu\text{V}/^\circ\text{C}$
Long-Term Offset Drift				50			50		nV/ $\sqrt{\text{mo}}$
Input Bias Current (Note 4)		●		± 90	± 150 ± 300		± 90	± 150 ± 3000	pA pA
Input Offset Current (Note 4)		●			± 300 ± 500			± 300 ± 700	pA pA
Input Noise Voltage	$R_S = 100\Omega$, DC to 10Hz			1.5			1.5		$\mu\text{V}_{\text{P-P}}$
Common Mode Rejection Ratio	$V_{\text{CM}} = V^-$ to $V^+ - 1.3$	●	125 120	130 130		125 120	130 130		dB dB
Power Supply Rejection Ratio		●	120 115	130 130		120 115	130 130		dB dB
Large-Signal Voltage Gain	$R_L = 10\text{k}$	●	125 120	140 140		125 120	140 140		dB dB
Maximum Output Voltage Swing	$R_L = 2\text{k}$ to GND $R_L = 10\text{k}$ to GND	● ●	± 4.75 ± 4.90	± 4.92 ± 4.98		± 4.50 ± 4.85	± 4.92 ± 4.98		V V
Slew Rate				2			2		V/ μs
Gain Bandwidth Product				3			3		MHz
Supply Current (Per Amplifier)	No Load, $V_{\text{SHDN}} = V_{\text{IH}}$	●		1	1.5		1	1.5	mA
Supply Current, Shutdown	$V_{\text{SHDN}} = V_{\text{IL}}$	●		15	30		15	30	μA
Shutdown Pin Input Low Voltage (V_{IL})		●			$V^- + 0.5$			$V^- + 0.5$	V
Shutdown Pin Input High Voltage (V_{IH})		●	$V^+ - 0.5$			$V^+ - 0.5$			V
Shutdown Pin Input Current	$V_{\text{SHDN}} = V_{\text{IL}}$	●		-7	-15		-7	-15	μA
Internal Sampling Frequency				7.5			7.5		kHz

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: These parameters are guaranteed by design. Thermocouple effects preclude measurements of these voltage levels during automated testing.

Note 3: All versions of the LTC2051/LTC2052 are designed, characterized and expected to meet the extended temperature limits of -40°C and 125°C . The LTC2051C/LTC2052C/LTC2051HVC/LTC2052HVC are guaranteed to meet the temperature limits of 0°C and 70°C . The LTC2051I/LTC2052I/LTC2051HVI/LTC2052HVI are guaranteed to meet temperature limits of -40°C and 85°C . The LTC2051H/LTC2051HVH and LTC2052H/LTC2052HVH

are guaranteed to meet the temperature limits of -40°C and 125°C .

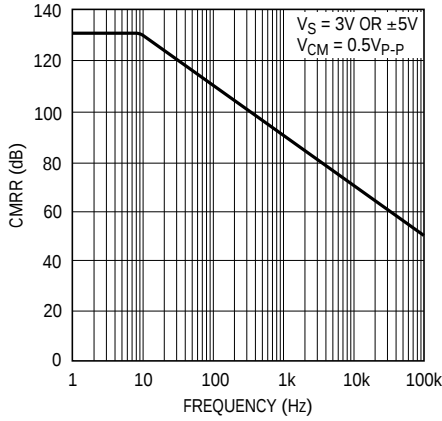
Note 4: The bias current measurement accuracy depends on the proximity of the negative supply bypass capacitors to the device under test. Because of this, only the bias current of channel B (LTC2051) and channels A and B (LTC2052) are 100% tested to the data sheet specifications. The bias currents of the remaining channels are 100% tested to relaxed limits, however, their values are guaranteed by design to meet the data sheet limits.

Note 5: This parameter is guaranteed to meet specified performance through design and characterization. It has not been tested.

Note 6: The θ_{JA} specified for the DD package is with minimal PCB heat spreading metal. Using expanded metal area on all layers of a board reduces this value.

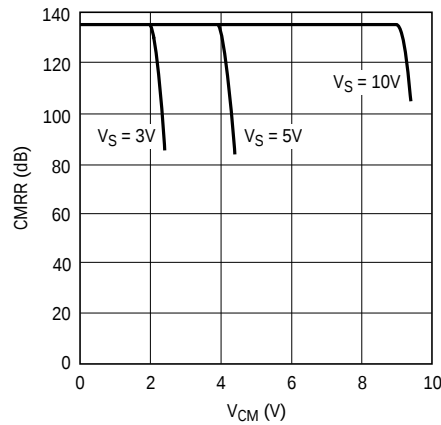
TYPICAL PERFORMANCE CHARACTERISTICS

Common Mode Rejection Ratio vs Frequency



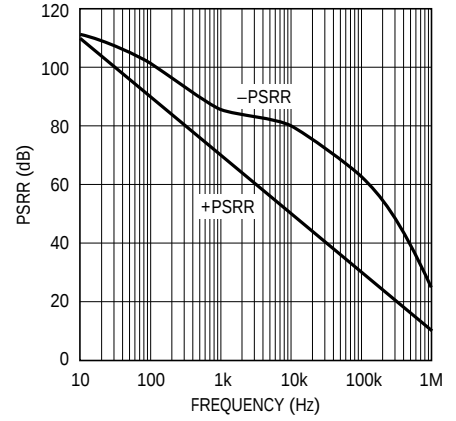
20512 G01

DC CMRR vs Common Mode Input Range



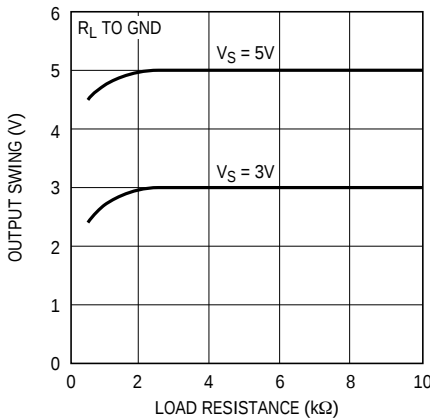
20512 G02

PSRR vs Frequency



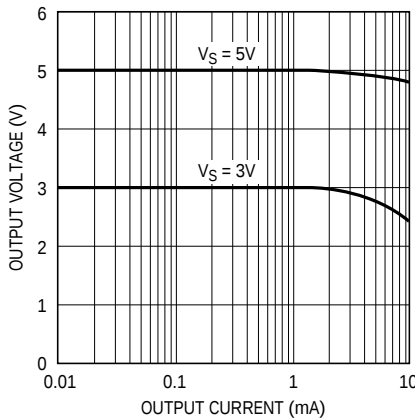
20512 G03

Output Voltage Swing vs Load Resistance



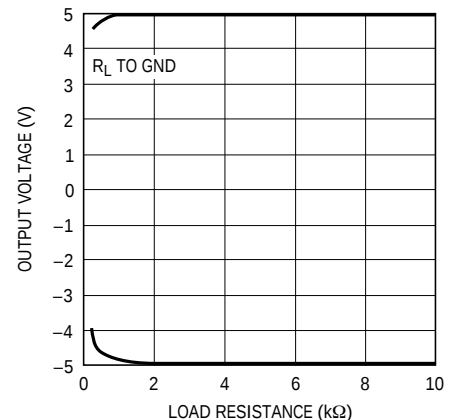
20512 G04

Output Swing vs Output Current



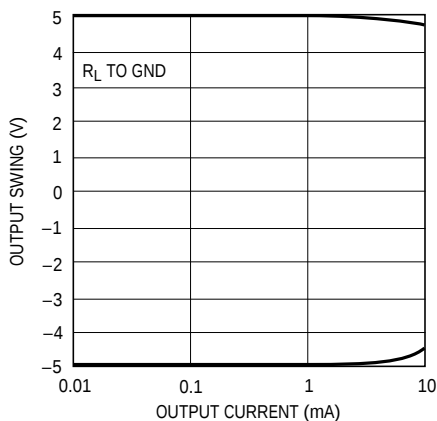
20512 G05

Output Swing vs Load Resistance $\pm 5V$



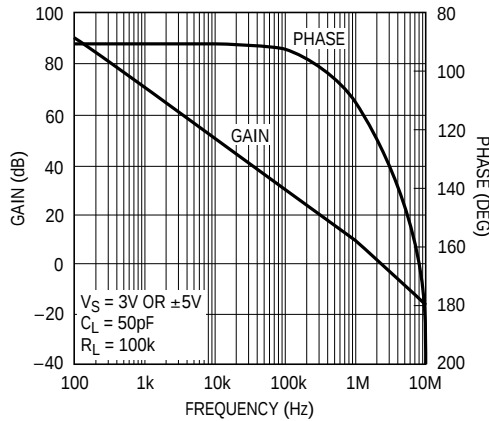
20512 G06

Output Swing vs Output Current, $\pm 5V$ Supply



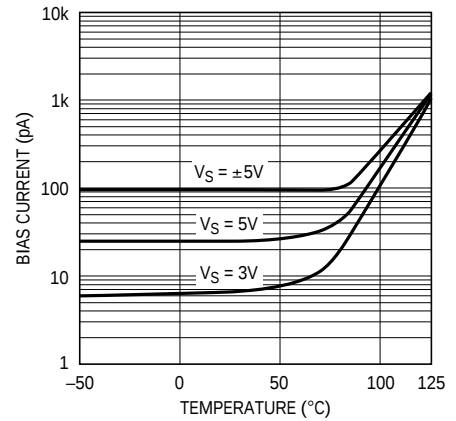
20512 G07

Gain/Phase vs Frequency



20512 G08

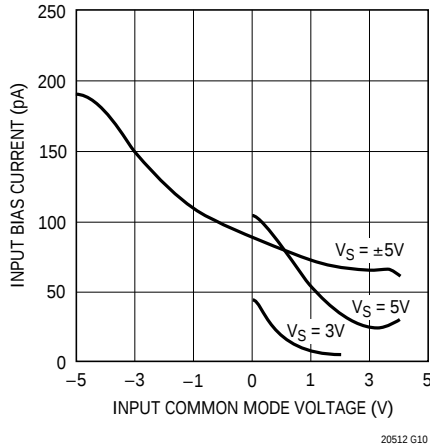
Bias Current vs Temperature



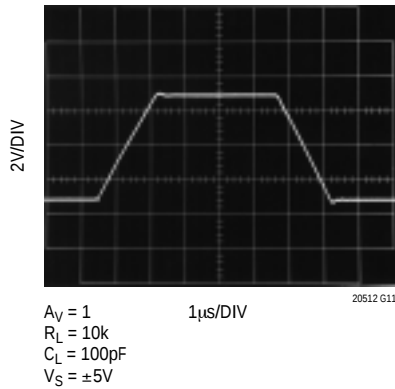
20512 G09

20512fd

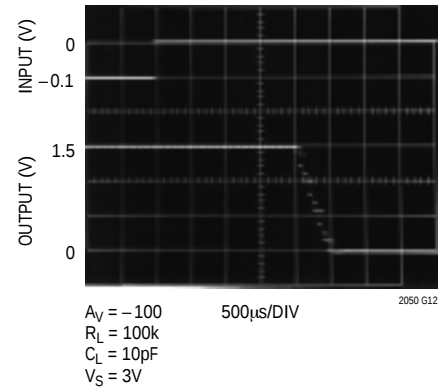
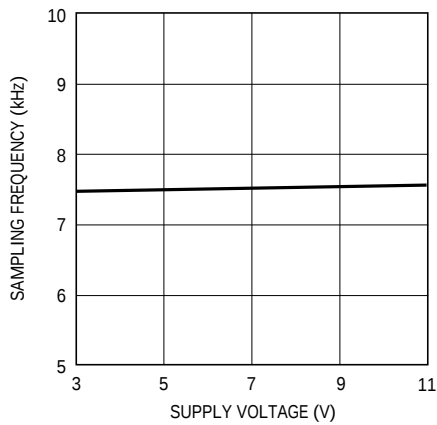
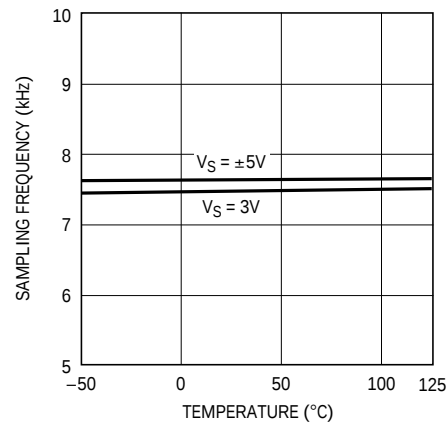
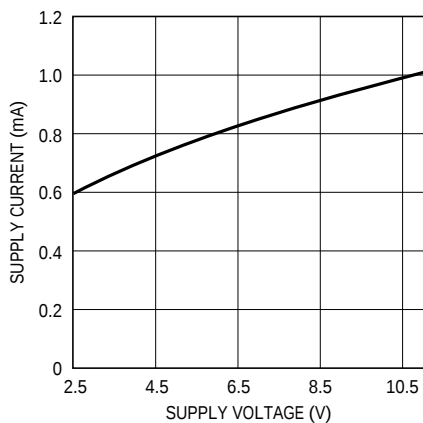
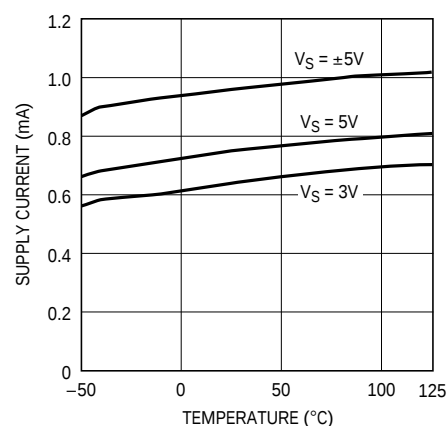
TYPICAL PERFORMANCE CHARACTERISTICS

Input Bias Current
vs Input Common Mode Voltage

Transient Response



Input Overload Recovery

Sampling Frequency
vs Supply VoltageSampling Frequency
vs TemperatureSupply Current (Per Amplifier)
vs Supply VoltageSupply Current (Per Amplifier)
vs Temperature

APPLICATIONS INFORMATION

Shutdown

The LTC2051 includes a shutdown pin in the 10-lead MSOP. When this active low pin is high or allowed to float, the device operates normally. When the shutdown pin is pulled low, the device enters shutdown mode; supply current drops to $3\mu\text{A}$, all clocking stops and the output assumes a high impedance state.

Clock Feedthrough, Input Bias Current

The LTC2051/LTC2052 use autozeroing circuitry to achieve an almost zero DC offset over temperature, common mode voltage and power supply voltage. The frequency of the clock used for autozeroing is typically 7.5kHz. The term clock feedthrough is broadly used to indicate visibility of this clock frequency in the op amp output spectrum. There are typically two types of clock feedthrough in autozeroed op amps like the LTC2051/LTC2052.

The first form of clock feedthrough is caused by the settling of the internal sampling capacitor and is input referred; that is, it is multiplied by the closed-loop gain of the op amp. This form of clock feedthrough is independent of the magnitude of the input source resistance or the magnitude of the gain setting resistors. The LTC2051/LTC2052 have a residue clock feedthrough of less than $1\mu\text{V}_{\text{RMS}}$ input referred at 7.5kHz.

The second form of clock feedthrough is caused by the small amount of charge injection occurring during the sampling and holding of the op amps input offset voltage. The current spikes are multiplied by the impedance seen at the input terminals of the op amp, appearing at the output multiplied by the closed-loop gain of the op amp.

To reduce this form of clock feedthrough, use smaller valued gain setting resistors and minimize the source resistance at the input. If the resistance seen at the inputs is less than 10k, this form of clock feedthrough is less than $1\mu\text{V}_{\text{RMS}}$ input referred at 7.5kHz, or less than the amount of residue clock feedthrough from the first form previously described.

Placing a capacitor across the feedback resistor reduces either form of clock feedthrough by limiting the bandwidth of the closed-loop gain.

Input bias current is defined as the DC current into the input pins of the op amp. The same current spikes that cause the second form of clock feedthrough previously described, when averaged, dominate the DC input bias current of the op amp below 70°C.

At temperatures above 70°C, the leakage of the ESD protection diodes on the inputs increase the input bias currents of both inputs in the positive direction, while the current caused by the charge injection stays relatively constant. At elevated temperatures (above 85°C) the leakage current begins to dominate and both the negative and positive pin's input bias currents are in the positive direction (into the pins).

Input Pins, ESD Sensitivity

ESD voltages above 700V on the input pins of the op amp will cause the input bias currents to increase (more DC current into the pins). At these voltages, it is possible to damage the device to a point where the input bias current exceeds the maximums specified in this data sheet.

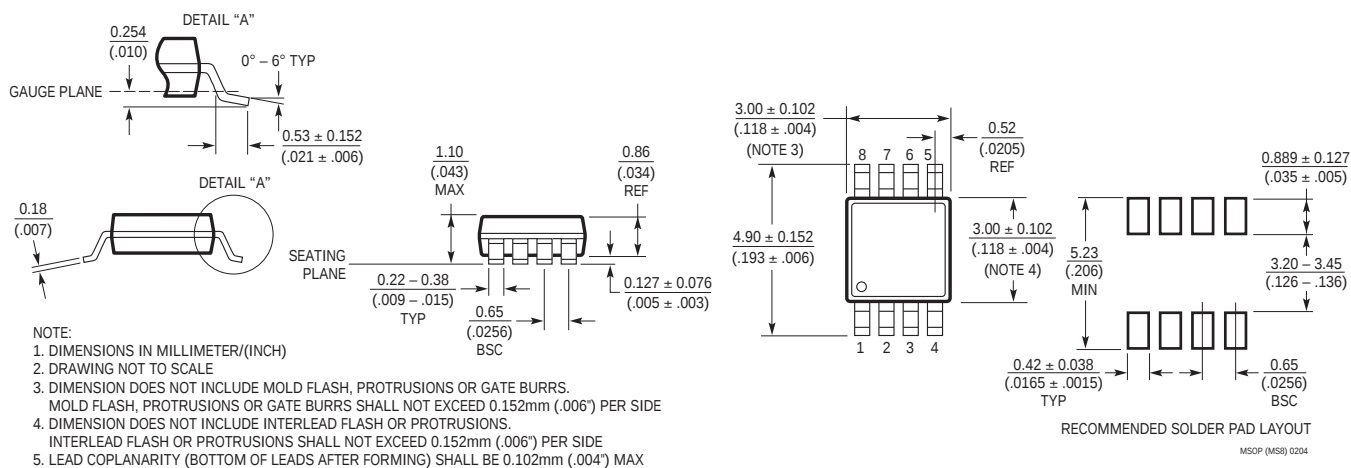
TYPICAL APPLICATION

The dual chopper op amp buffers the inputs of A1 and corrects its offset voltage and offset voltage drift. With the RC values shown, the power-up warm-up time is typically 20 seconds. The step response of the composite amplifier does not present settling tails. The LT[®]1677 should be used when extremely low noise, V_{OS} and V_{OS} drift are

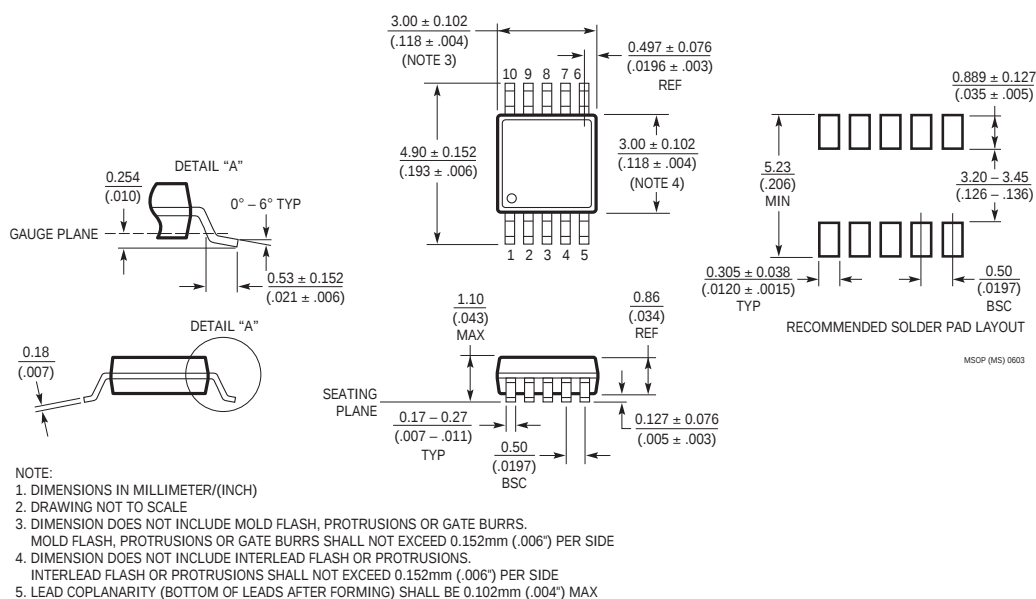
needed and the input source resistance is low. (For instance a 350Ω strain gauge bridge.) The LT1012 or equivalent should be used when low bias current (100pA) is also required in conjunction with DC to 10Hz low noise, low V_{OS} and V_{OS} drift. The measured typical input offset voltages are less than $1\mu\text{V}$.

PACKAGE DESCRIPTION

MS8 Package
8-Lead Plastic MSOP
 (Reference LTC DWG # 05-08-1660)

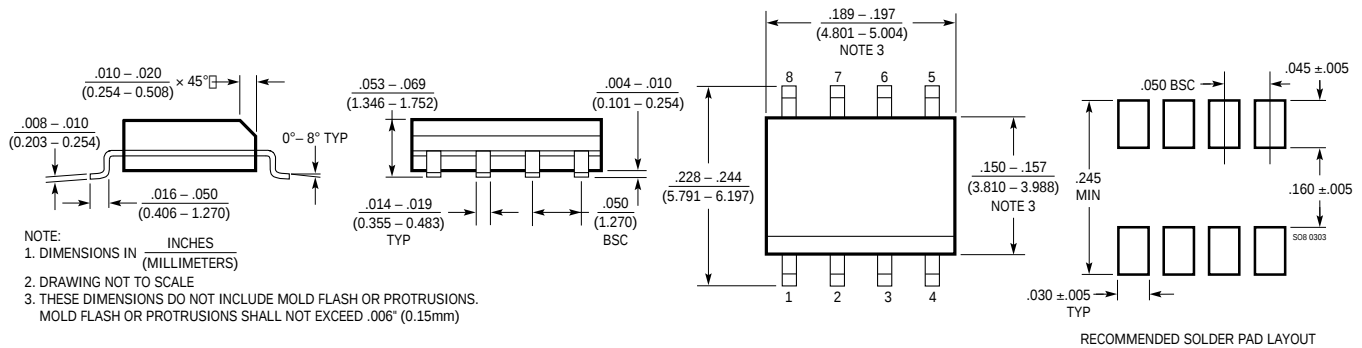


MS Package
10-Lead Plastic MSOP
 (Reference LTC DWG # 05-08-1661)

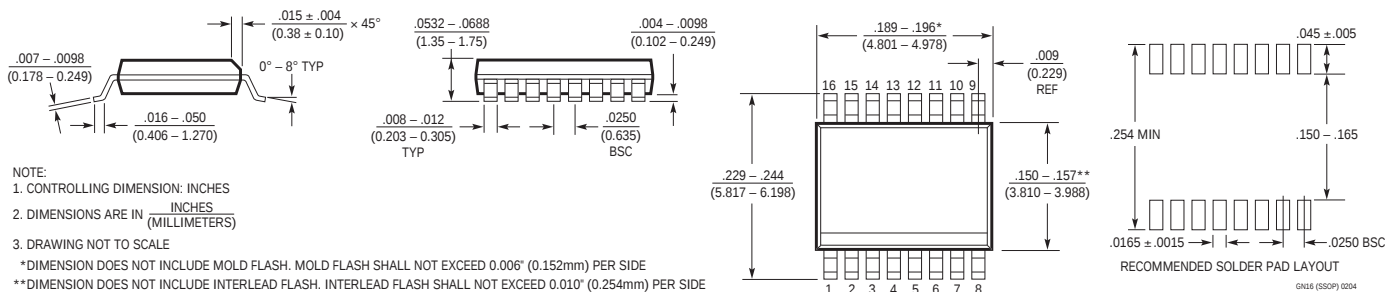


PACKAGE DESCRIPTION

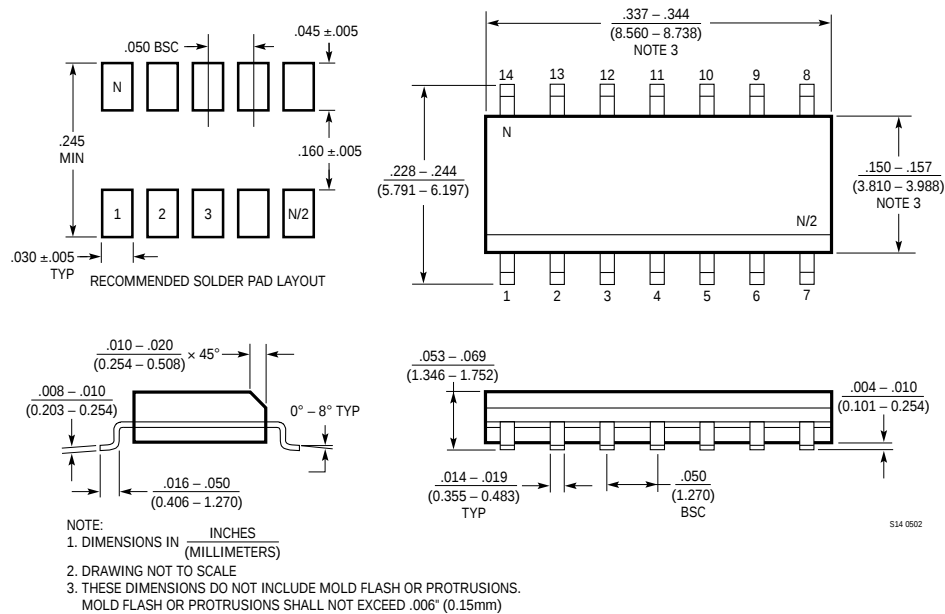
S8 Package 8-Lead Plastic Small Outline (Narrow .150 Inch) (Reference LTC DWG # 05-08-1610)



GN Package 16-Lead Plastic SSOP (Narrow .150 Inch) (Reference LTC DWG # 05-08-1641)

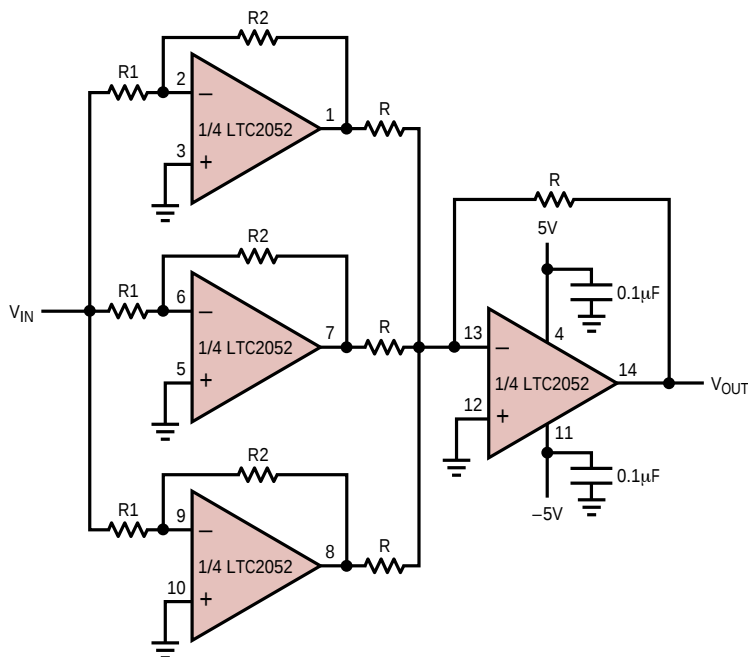


S Package 14-Lead Plastic Small Outline (Narrow .150 Inch) (Reference LTC DWG # 05-08-1610)



TYPICAL APPLICATION

Paralleling Amplifiers to Improve Noise



$$\frac{V_{OUT}}{V_{IN}} = 3 \frac{R2}{R1} ; \text{ INPUT DC - 10Hz NOISE } \approx 0.8\mu\text{V}_{p-p} = \frac{\text{NOISE OF EACH PARALLEL OP AMP}}{\sqrt{3}}$$

20512 F02

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1051/LTC1053	Precision Zero-Drift Op Amp	Dual/Quad
LTC1151	±15V Zero-Drift Op Amp	Dual High Voltage Operation ±18V
LTC1152	Rail-to-Rail Input and Output Zero-Drift Op Amp	Single Zero-Drift Op Amp with Rail-to-Rail Input and Output and Shutdown
LTC2050	Zero-Drift Op Amp in SOT-23	Single Supply Operation 2.7V to ±5V, Shutdown
LTC2053	Zero-Drift Precision Instrumentation Amp	MS8, 116dB CMRR, Two External Resistors Set Gain
LTC6800	Rail-to-Rail Input and Output Instrumentation Amp	Low Cost, MS8, Two External Resistors Set Gain