

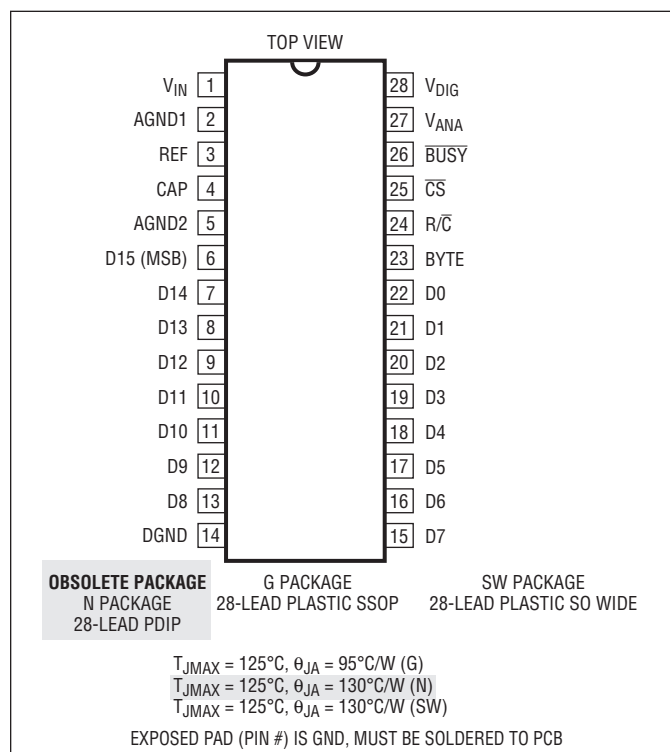
LTC1605

ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

V_{ANA}	7V
V_{DIG} to V_{ANA}	0.3V
V_{DIG}	7V
Ground Voltage Difference	
DGND, AGND1 and AGND2	$\pm 0.3V$
Analog Inputs (Note 3)	
V_{IN}	$\pm 25V$
CAP	$V_{ANA} + 0.3V$ to $AGND2 - 0.3V$
REF	Indefinite Short to AGND2
.....	Momentary Short to V_{ANA}
Digital Input Voltage (Note 4)	
Digital Output Voltage	
Power Dissipation	
Operating Ambient Temperature Range	
LTC1605C	0°C to 70°C
LTC1605I	-40°C to 85°C
Storage Temperature Range	
Lead Temperature (Soldering, 10 sec)	

PIN CONFIGURATION



ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC1605ACG#PBF	LTC1605ACG#TRPBF	1605ACG	28-Lead Plastic SSOP	0°C to 70°C
LTC1605AIG#PBF	LTC1605AIG#TRPBF	1605AIG	28-Lead Plastic SSOP	-40°C to 85°C
LTC1605CG#PBF	LTC1605CG#TRPBF	1605CG	28-Lead Plastic SSOP	0°C to 70°C
LTC1605IG#PBF	LTC1605IG#TRPBF	1605IG	28-Lead Plastic SSOP	-40°C to 85°C
LTC1605ACSW#PBF	LTC1605ACSW#TRPBF	1605ACSW	28-Lead Plastic SO Wide	0°C to 70°C
LTC1605AISW#PBF	LTC1605AISW#TRPBF	1605AISW	28-Lead Plastic SO Wide	-40°C to 85°C
LTC1605CSW#PBF	LTC1605CSW#TRPBF	1605CSW	28-Lead Plastic SO Wide	0°C to 70°C
LTC1605ISW#PBF	LTC1605ISW#TRPBF	1605ISW	28-Lead Plastic SO Wide	-40°C to 85°C
OBSOLETE PACKAGE				
LTC1605CN#PBF	LTC1605CN#TRPBF	1605CN	28-Lead PDIP	0°C to 70°C
LTC1605IN#PBF	LTC1605IN#TRPBF	1605IN	28-Lead PDIP	-40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. (Notes 5, 6)

PARAMETER	CONDITIONS		LTC1605			LTC1605A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Resolution		●	16			16			Bits
No Missing Codes		●	15			16			Bits
Transition Noise				1.0			1.0		LSB
Integral Linearity Error	(Note 7)	●			± 3			± 2	LSB
Bipolar Zero Error	Ext. Reference = 2.5V (Note 8)	●			± 10			± 10	mV
Bipolar Zero Error Drift				± 2			± 2		ppm/ $^\circ\text{C}$
Full-Scale Error Drift				± 7			± 5		ppm/ $^\circ\text{C}$
Full-Scale Error	Ext. Reference = 2.5V (Notes 12, 13)	●			± 0.50			± 0.25	%
Full-Scale Error Drift	Ext. Reference = 2.5V			± 2			± 2		ppm/ $^\circ\text{C}$
Power Supply Sensitivity $V_{ANA} = V_{DIG} = V_{DD}$	$V_{DD} = 5V \pm 5\%$ (Note 9)				± 8			± 8	LSB

ANALOG INPUT

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		LTC1605/LTC1605A			UNITS
				MIN	TYP	MAX	
V_{IN}	Analog Input Range (Note 9)	$4.75V \leq V_{ANA} \leq 5.25V$, $4.75V \leq V_{DIG} \leq 5.25V$	●		± 10		V
C_{IN}	Analog Input Capacitance				10		pF
R_{IN}	Analog Input Impedance				20		k Ω

DYNAMIC ACCURACY

(Notes 5, 14)

SYMBOL	PARAMETER	CONDITIONS		LTC1605/LTC1605A			UNITS
				MIN	TYP	MAX	
S/(N + D)	Signal-to-(Noise + Distortion) Ratio	1kHz Input Signal (Note 14)			87.5		dB
		10kHz Input Signal			87		dB
		20kHz, -60dB Input Signal			30		dB
THD	Total Harmonic Distortion	1kHz Input Signal, First 5 Harmonics			-102		dB
		10kHz Input Signal, First 5 Harmonics			-94		dB
	Peak Harmonic or Spurious Noise	1kHz Input Signal			-102		dB
		10kHz Input Signal			-94		dB
	Full-Power Bandwidth	(Note 15)			275		kHz
	Aperture Delay				40		ns
	Aperture Jitter				Sufficient to Meet AC Specs		
	Transient Response	Full-Scale Step (Note 9)				2	μs
	Overvoltage Recovery	(Note 16)			150		ns

INTERNAL REFERENCE CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. (Note 5)

PARAMETER	CONDITIONS		LTC1605/LTC1605A			UNITS
			MIN	TYP	MAX	
V_{REF} Output Voltage	$I_{\text{OUT}} = 0$	●	2.470	2.500	2.520	V
V_{REF} Output Tempco	$I_{\text{OUT}} = 0$			±5		ppm/°C
Internal Reference Source Current				1		μA
External Reference Voltage for Specified Linearity	(Notes 9, 10)		2.30	2.50	2.70	V
External Reference Current Drain	Ext. Reference = 2.5V (Note 9)	●			100	μA
CAP Output Voltage	$I_{\text{OUT}} = 0$			2.50		V

DIGITAL INPUTS AND OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. (Note 5)

SYMBOL	PARAMETER	CONDITIONS			LTC1605/LTC1605A			UNITS
					MIN	TYP	MAX	
V_{IH}	High Level Input Voltage	$V_{\text{DD}} = 5.25\text{V}$		●	2.4			V
V_{IL}	Low Level Input Voltage	$V_{\text{DD}} = 4.75\text{V}$		●			0.8	V
I_{IN}	Digital Input Current	$V_{\text{IN}} = 0\text{V to } V_{\text{DD}}$		●			±10	μA
C_{IN}	Digital Input Capacitance					5		pF
V_{OH}	High Level Output Voltage	$V_{\text{DD}} = 4.75\text{V}$	$I_{\text{O}} = -10\mu\text{A}$			4.5		V
			$I_{\text{O}} = -200\mu\text{A}$	●	4.0			V
V_{OL}	Low Level Output Voltage	$V_{\text{DD}} = 4.75\text{V}$	$I_{\text{O}} = 160\mu\text{A}$			0.05		V
			$I_{\text{O}} = 1.6\text{mA}$	●		0.10	0.4	V
I_{OZ}	Hi-Z Output Leakage D15 to D0	$V_{\text{OUT}} = 0\text{V to } V_{\text{DD}}, \overline{\text{CS}} \text{ High}$		●			±10	μA
C_{OZ}	Hi-Z Output Capacitance D15 to D0	$\overline{\text{CS}} \text{ High (Note 9)}$		●			15	pF
I_{SOURCE}	Output Source Current	$V_{\text{OUT}} = 0\text{V}$				-10		mA
I_{SINK}	Output Sink Current	$V_{\text{OUT}} = V_{\text{DD}}$				10		mA

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		LTC1605/LTC1605A			UNITS
				MIN	TYP	MAX	
$f_{\text{SAMPLE(MAX)}}$	Maximum Sampling Frequency		●	100			kHz
t_{CONV}	Conversion Time		●			8	μs
t_{ACQ}	Acquisition Time		●			2	μs
t_1	Convert Pulse Width	(Note 11)	●	40			ns
t_2	Data Valid Delay After $R/\overline{C}\downarrow$	(Note 9)	●			8	μs
t_3	BUSY Delay from $R/\overline{C}\downarrow$	$C_L = 50\text{pF}$	●			65	ns
t_4	BUSY Low					8	μs
t_5	BUSY Delay After End of Conversion				220		ns
t_6	Aperture Delay				40		ns
t_7	Bus Relinquish Time		●	10	35	83	ns
t_8	BUSY Delay After Data Valid		●	50	200		ns
t_9	Previous Data Valid After $R/\overline{C}\downarrow$				7.4		μs
t_{10}	$R/\overline{C}$ to $\overline{CS}$ Setup Time	(Notes 9, 10)		10			ns
t_{11}	Time Between Conversions			10			μs
t_{12}	Bus Access and Byte Delay	(Notes 9, 10)		10		83	ns

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		LTC1605/LTC1605A			UNITS
				MIN	TYP	MAX	
V_{DD}	Positive Supply Voltage	(Notes 9, 10)		4.75		5.25	V
I_{DD}	Positive Supply Current		●		11	16	mA
P_{DIS}	Power Dissipation				55	80	mW

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to ground with DGND, AGND1 and AGND2 wired together (unless otherwise noted).

Note 3: When these pin voltages are taken below ground or above $V_{\text{ANA}} = V_{\text{DIG}} = V_{\text{DD}}$, they will be clamped by internal diodes. This product can handle input currents of greater than 100mA below ground or above V_{DD} without latch-up.

Note 4: When these pin voltages are taken below ground, they will be clamped by internal diodes. This product can handle input currents of 90mA below ground without latchup. These pins are not clamped to V_{DD} .

Note 5: $V_{\text{DD}} = 5\text{V}$, $f_{\text{SAMPLE}} = 100\text{kHz}$, $t_r = t_f = 5\text{ns}$ unless otherwise specified.

Note 6: Linearity, offset and full-scale specifications apply for a V_{IN} input with respect to ground.

Note 7: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual end points of the transfer curve. The deviation is measured from the center of the quantization band.

Note 8: Bipolar offset is the offset voltage measured from -0.5LSB when the output code flickers between 0000 0000 0000 0000 and 1111 1111 1111 1111.

Note 9: Guaranteed by design, not subject to test.

Note 10: Recommended operating conditions.

Note 11: With $\overline{CS}$ low the falling $R/\overline{C}$ edge starts a conversion. If $R/\overline{C}$ returns high at a critical point during the conversion it can create small errors. For best results ensure that $R/\overline{C}$ returns high within $3\mu\text{s}$ after the start of the conversion.

Note 12: As measured with fixed resistors shown in Figure 4. Adjustable to zero with external potentiometer.

Note 13: Full-scale error is the worst-case of $-FS$ or $+FS$ untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error.

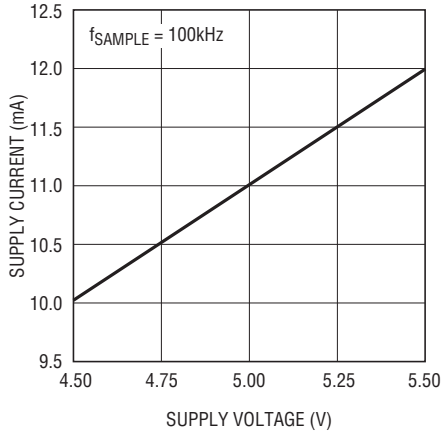
Note 14: All specifications in dB are referred to a full-scale $\pm 10\text{V}$ input.

Note 15: Full-power bandwidth is defined as full-scale input frequency at which a signal-to-(noise + distortion) degrades to 60dB or 10 bits of accuracy.

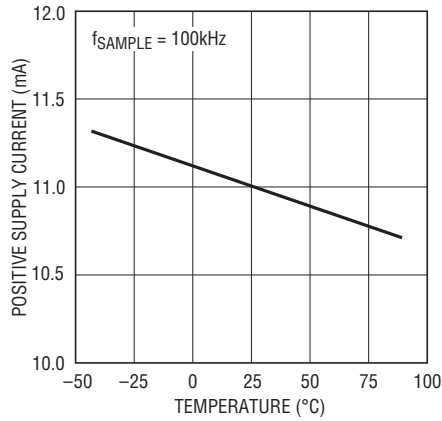
Note 16: Recovers to specified performance after $(2 \cdot FS)$ input overvoltage.

TYPICAL PERFORMANCE CHARACTERISTICS

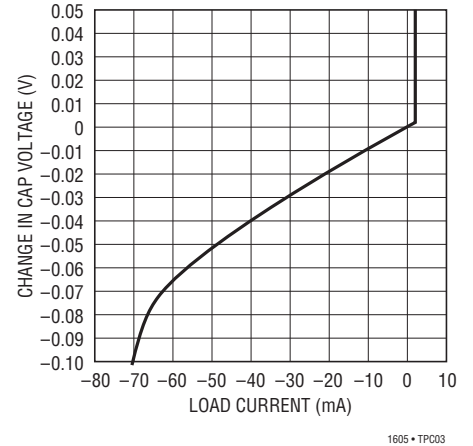
Supply Current vs Supply Voltage



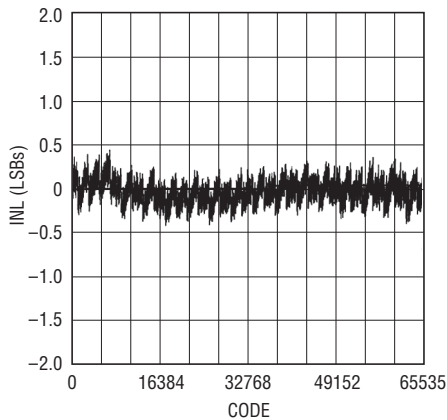
Supply Current vs Temperature



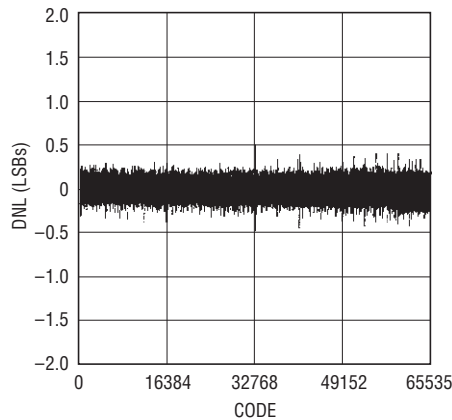
Change in CAP Voltage vs Load Current



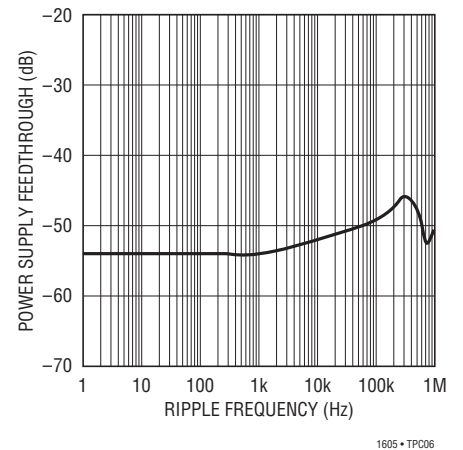
Typical INL Curve



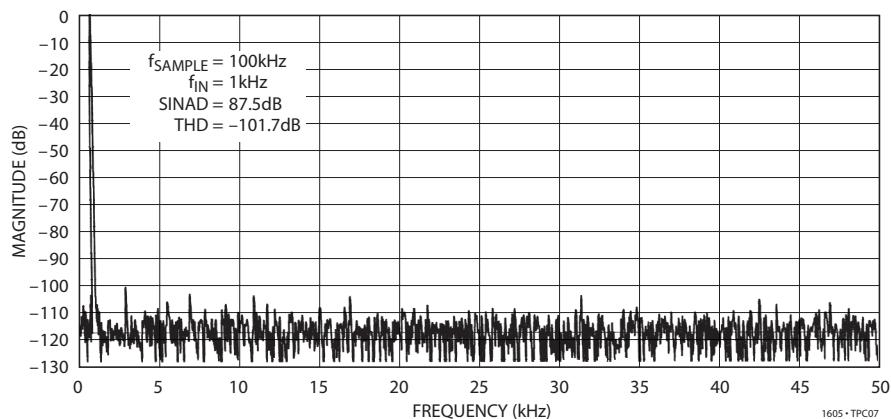
Typical DNL Curve



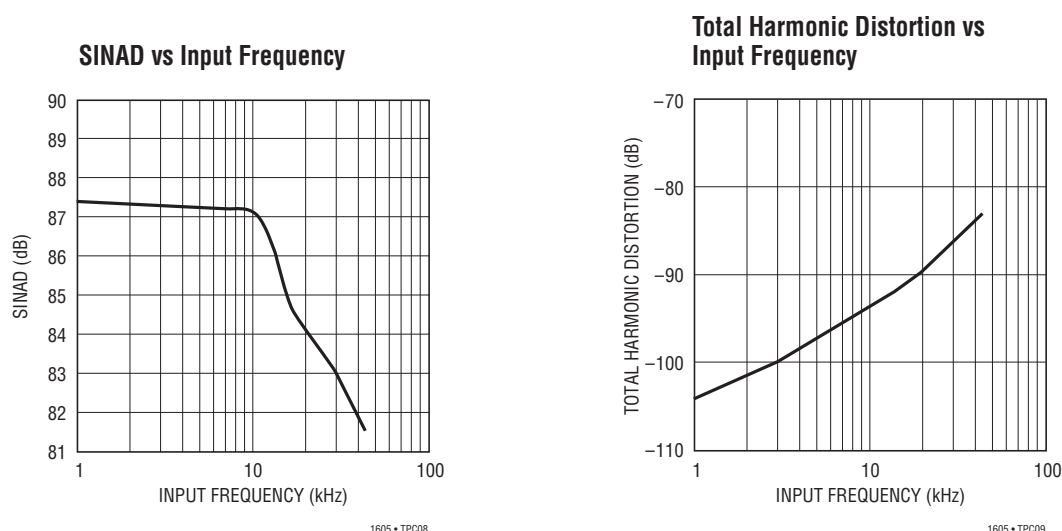
Power Supply Feedthrough vs Ripple Frequency



LTC1605 Nonaveraged 4096 Point FFT Plot



TYPICAL PERFORMANCE CHARACTERISTICS



PIN FUNCTIONS

V_{IN} (Pin 1): Analog Input. Connect through a 200Ω resistor to the analog input. Full-scale input range is ±10V.

AGND1 (Pin 2): Analog Ground. Tie to analog ground plane.

REF (Pin 3): 2.5V Reference Output. Bypass with 2.2μF tantalum capacitor. Can be driven with an external reference.

CAP (Pin 4): Reference Buffer Output. Bypass with 2.2μF tantalum capacitor.

AGND2 (Pin 5): Analog Ground. Tie to analog ground plane.

D15 to D8 (Pins 6 to 13): Three-State Data Outputs. Hi-Z state when $\overline{CS}$ is high or when $R/\overline{C}$ is low.

DGND (Pin 14): Digital Ground.

D7 to D0 (Pins 15 to 22): Three-State Data Outputs. Hi-Z state when $\overline{CS}$ is high or when $R/\overline{C}$ is low.

BYTE (Pin 23): Byte Select. With BYTE low, data will be output with Pin 6 (D15) being the MSB and Pin 22 (D0) being the LSB. With BYTE high the upper eight bits and the lower eight bits will be switched. The MSB is output on Pin 15 and bit 8 is output on Pin 22. Bit 7 is output on Pin 6 and the LSB is output on Pin 13.

$R/\overline{C}$ (Pin 24): Read/Convert Input. With $\overline{CS}$ low, a falling edge on $R/\overline{C}$ puts the internal sample-and-hold into the hold state and starts a conversion. With $\overline{CS}$ low, a rising edge on $R/\overline{C}$ enables the output data bits.

$\overline{CS}$ (Pin 25): ChipSelect. Internally OR'd with $R/\overline{C}$. With $R/\overline{C}$ low, a falling edge on $\overline{CS}$ will initiate a conversion. With $R/\overline{C}$ high, a falling edge on $\overline{CS}$ will enable the output data.

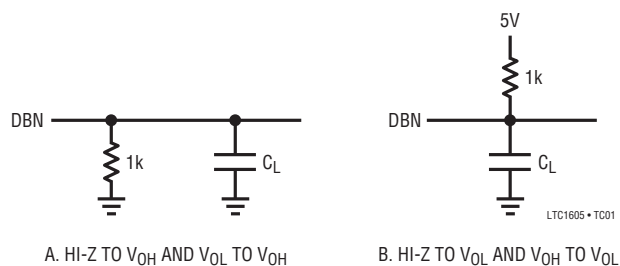
$\overline{BUSY}$ (Pin 26): Output Shows Converter Status. It is low when a conversion is in progress. Data valid on the rising edge of $\overline{BUSY}$. $\overline{CS}$ or $R/\overline{C}$ must be high when $\overline{BUSY}$ rises or another conversion will start without time for signal acquisition.

V_{ANA} (Pin 27): 5V Analog Supply. Bypass to ground with a 0.1μF ceramic and a 10μF tantalum capacitor.

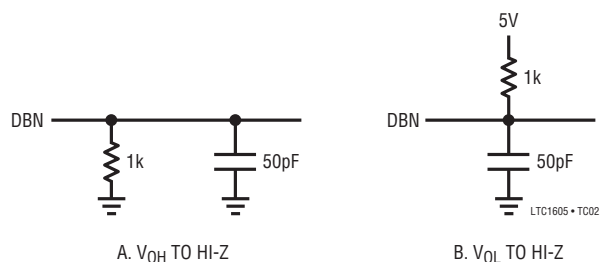
V_{DIG} (Pin 28): 5V Digital Supply. Connect directly to Pin 27.

TEST CIRCUIT

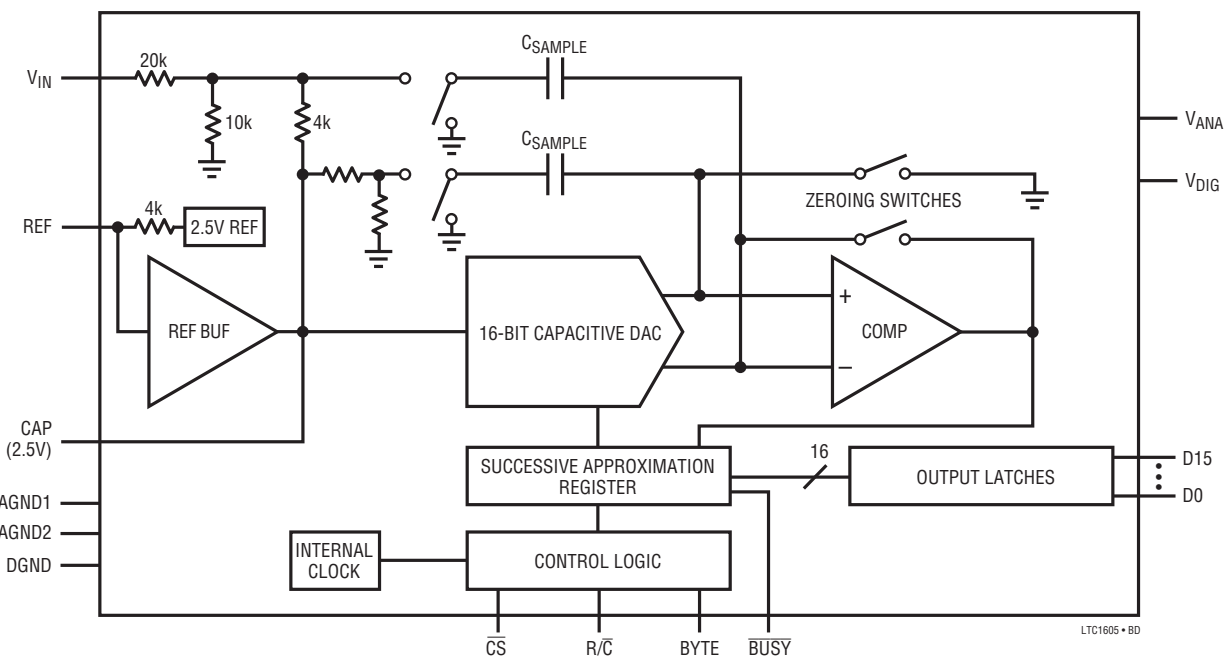
Load Circuit for Access Timing



Load Circuit for Output Float Delay



FUNCTIONAL BLOCK DIAGRAM



APPLICATIONS INFORMATION

Conversion Details

The LTC1605 uses a successive approximation algorithm and an internal sample-and-hold circuit to convert an analog signal to a 16-bit or two byte parallel output. The ADC is complete with a precision reference and an internal clock. The control logic provides easy interface to microprocessors and DSPs. (Please refer to the Digital Interface section for the data format.)

Conversion start is controlled by the $\overline{CS}$ and $R/\overline{C}$ inputs. At the start of conversion the successive approximation register (SAR) is reset. Once a conversion cycle has begun it cannot be restarted.

During the conversion, the internal 16-bit capacitive DAC output is sequenced by the SAR from the most significant bit (MSB) to the least significant bit (LSB). Referring to Figure 1, V_{IN} is connected through the resistor divider to the sample-and-hold capacitor during the acquire phase and the comparator offset is nulled by the autozero switches. In this acquire phase, a minimum delay of $2\mu s$ will provide enough time for the sample-and-hold capacitor to acquire the analog signal. During the convert phase, the autozero switches open, putting the comparator into the compare mode. The input switch switches C_{SAMPLE} to ground, injecting the analog input charge onto the summing junction. This input charge is successively compared with the binary-weighted charges supplied by the capacitive DAC. Bit decisions are made by the high speed comparator. At

the end of a conversion, the DAC output balances the V_{IN} input charge. The SAR contents (a 16-bit data word) that represents the V_{IN} are loaded into the 16-bit output latches.

Driving the Analog Inputs

The nominal input range for the LTC1605 is $\pm 10V$ or $(\pm 4 \cdot V_{REF})$ and the input is overvoltage protected to $\pm 25V$. The input impedance is typically $20k\Omega$, therefore, it should be driven with a low impedance source. Wideband noise coupling into the input can be minimized by placing a $1000pF$ capacitor at the input as shown in Figure 2. An NPO-type capacitor gives the lowest distortion. Place the capacitor as close to the device input pin as possible. If an amplifier is to be used to drive the input, care should be taken to select an amplifier with adequate accuracy, linearity and noise for the application. The following list is a summary of the op amps that are suitable for driving the LTC1605. More detailed information is available at www.linear.com.

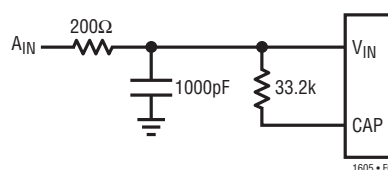


Figure 2. Analog Input Filtering

LT®1007: Low noise precision amplifier. 2.7mA supply current $\pm 5V$ to $\pm 15V$ supplies. Gain bandwidth product 8MHz. DC applications.

LT1097: Low cost, low power precision amplifier. 300 μA supply current. $\pm 5V$ to $\pm 15V$ supplies. Gain bandwidth product 0.7MHz. DC applications.

LT1227: 140MHz video current feedback amplifier. 10mA supply current. $\pm 5V$ to $\pm 15V$ supplies. Low noise and low distortion.

LT1360: 37MHz voltage feedback amplifier. 3.8mA supply current. $\pm 5V$ to $\pm 15V$ supplies. Good AC/DC specs.

LT1363: 50MHz voltage feedback amplifier. 6.3mA supply current. Good AC/DC specs.

LT1364/LT1365: Dual and quad 50MHz voltage feedback amplifiers. 6.3mA supply current per amplifier. Good AC/DC specs.

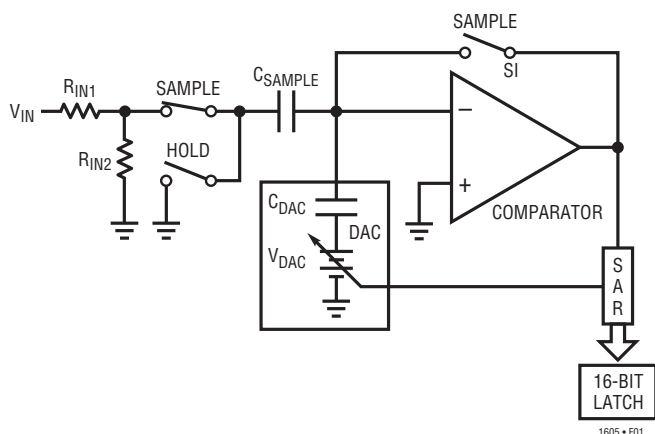


Figure 1. LTC1605 Simplified Equivalent Circuit

APPLICATIONS INFORMATION

Internal Voltage Reference

The LTC1605 has an on-chip, temperature compensated, curvature corrected, bandgap reference, which is factory trimmed to 2.50V. The full-scale range of the ADC is equal to $(\pm 4 \cdot V_{REF})$ or nominally $\pm 10V$. The output of the reference is connected to the input of a unity-gain buffer through a 4k resistor (see Figure 3). The input to the buffer or the output of the reference is available at REF (Pin 3). The internal reference can be overdriven with an external reference if more accuracy is needed. The buffer output drives the internal DAC and is available at CAP (Pin 4). The CAP pin can be used to drive a steady DC load of less than 2mA. Driving an AC load is not recommended because it can cause the performance of the converter to degrade.

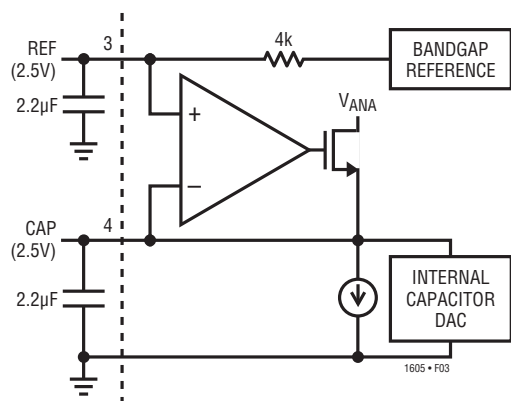


Figure 3. Internal or External Reference Source

For minimum code transition noise the REF pin and the CAP pin should each be decoupled with a capacitor to filter wideband noise from the reference and the buffer (2.2µF tantalum).

Offset and Gain Adjustments

The LTC1605 offset and full-scale errors have been trimmed at the factory with the external resistors shown in Figure 4. This allows for external adjustment of offset and full scale in applications where absolute accuracy is important. See Figure 5 for the offset and gain trim circuit. First adjust the offset to zero by adjusting resistor R3. Apply an input voltage of $-152.6mV$ ($-0.5LSB$) and adjust R3 so the code is changing between 1111 1111 1111 1111 and 0000 0000 0000 0000. The gain error is trimmed by adjusting resistor R4. An input voltage of $9.999542V$ ($+FS - 1.5LSB$) is applied to V_{IN} and R4

is adjusted until the output code is changing between 0111 1111 1110 and 0111 1111 1111 1111. Figure 6 shows the bipolar transfer characteristic of the LTC1605.

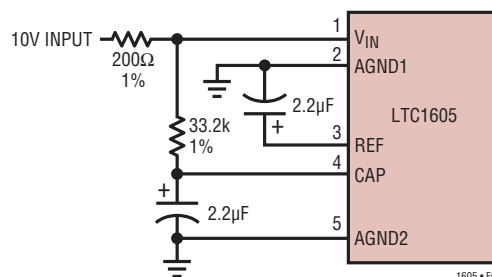


Figure 4. $\pm 10V$ Input Without Trim

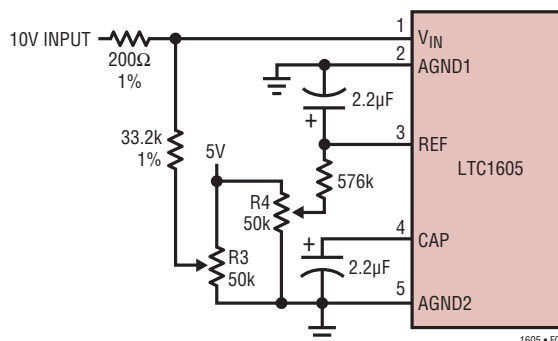


Figure 5. $\pm 10V$ Input with Offset and Gain Trim

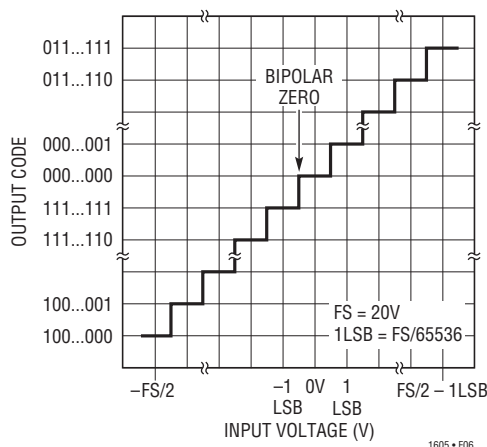


Figure 6. LTC1605 Bipolar Transfer Characteristics

DC Performance

One way of measuring the transition noise associated with a high resolution ADC is to use a technique where a DC signal is applied to the input of the ADC and the resulting output codes are collected over a large number of conversions. For example in Figure 7 the distribution of

TYPICAL APPLICATIONS

output code is shown for a DC input that has been digitized 10000 times. The distribution is Gaussian and the RMS code transition is about 1LSB.

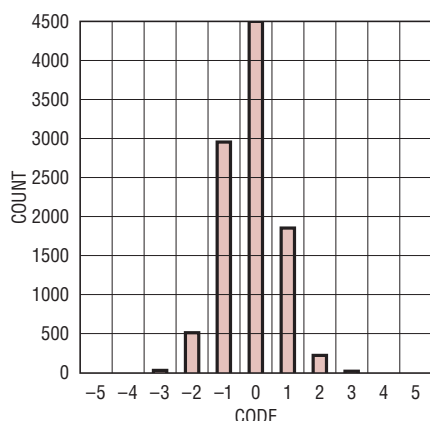


Figure 7. Histogram for 10000 Conversions

DIGITAL INTERFACE

Internal Clock

The ADC has an internal clock that is trimmed to achieve a typical conversion time of 7 μ s. No external adjustments are required and, with the typical acquisition time of 1 μ s, throughput performance of 100ksps is assured.

Timing and Control

Conversion start and data read are controlled by two digital inputs: $\overline{CS}$ and $R/\overline{C}$. To start a conversion and put the sample-and-hold into the hold mode bring $\overline{CS}$ and $R/\overline{C}$ low for no less than 40ns. Once initiated it cannot be restarted until the conversion is complete. Converter status is indicated by the $\overline{BUSY}$ output and this is low while the conversion is in progress.

There are two modes of operation. The first mode is shown in Figure 8. The digital input $R/\overline{C}$ is used to control the start of conversion. $\overline{CS}$ is tied low. When $R/\overline{C}$ goes low the sample-and-hold goes into the hold mode and a conversion is started. $\overline{BUSY}$ goes low and stays low during the conversion and will go back high after the conversion has been completed and the internal output shift registers have been updated. $R/\overline{C}$ should remain low for no less than 40ns. During the time $R/\overline{C}$ is low the digital outputs are in a Hi-Z state. $R/\overline{C}$ should be brought back high within 3 μ s after the start of the conversion to ensure that no errors occur in the digitized result. The second mode, shown in Figure 9, uses the $\overline{CS}$ signal to control the start of a conversion and the reading of the digital output. In this mode the $R/\overline{C}$ input signal should be brought low no less than 10ns before the falling edge of $\overline{CS}$. The minimum pulse width for $\overline{CS}$ is 40ns. When $\overline{CS}$ falls, $\overline{BUSY}$ goes low and will stay low until the end of the conversion. $\overline{BUSY}$ will go high after the conversion has been completed. The new data is valid when $\overline{CS}$ is brought back low again to initiate

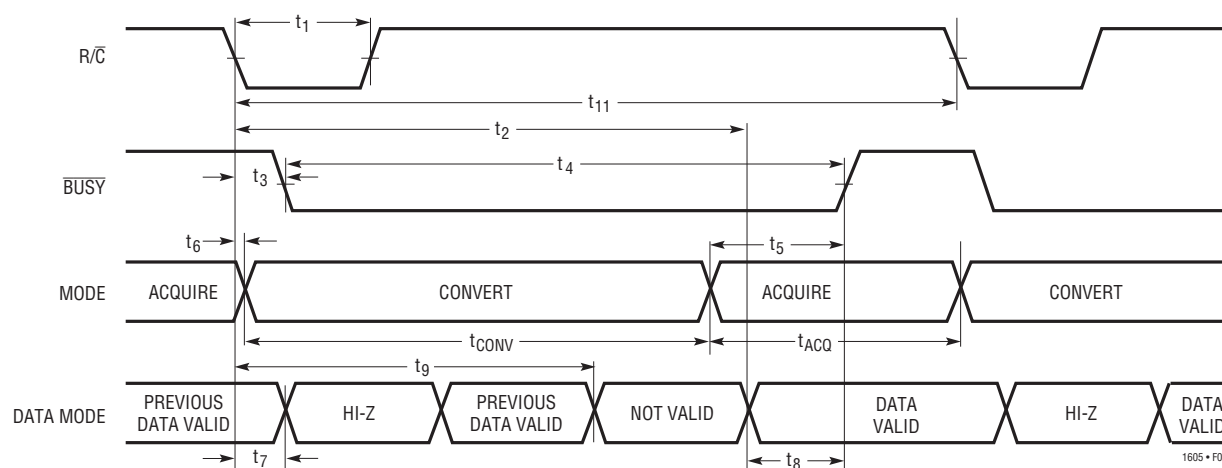


Figure 8. Conversion Timing with Outputs Enabled After Conversion ($\overline{CS}$ Tied Low)

APPLICATIONS INFORMATION

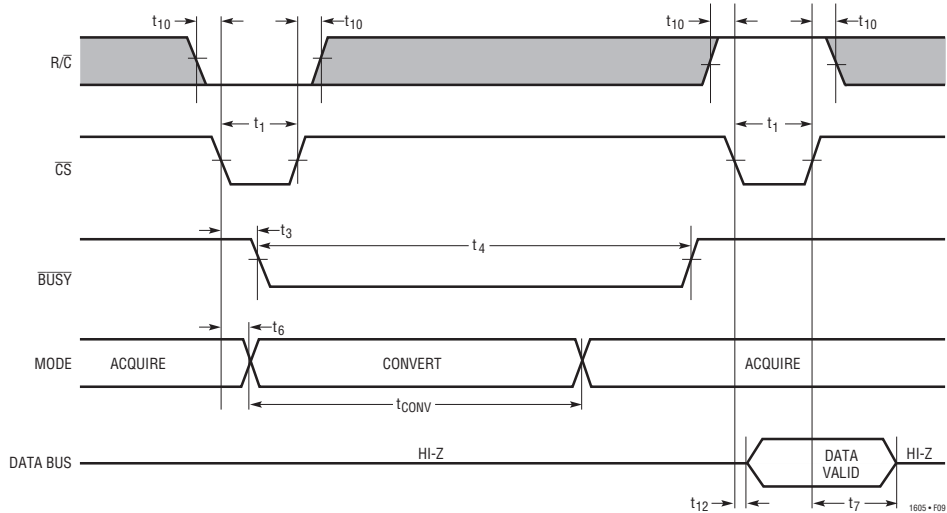


Figure 9. Using $\overline{CS}$ to Control Conversion and Read Timing

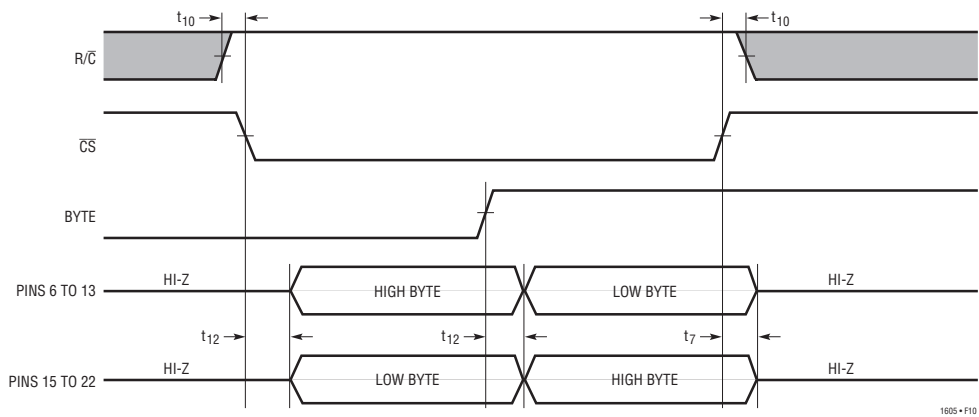


Figure 10. Using $\overline{CS}$ and **BYTE** to Control Data Bus Read Timing

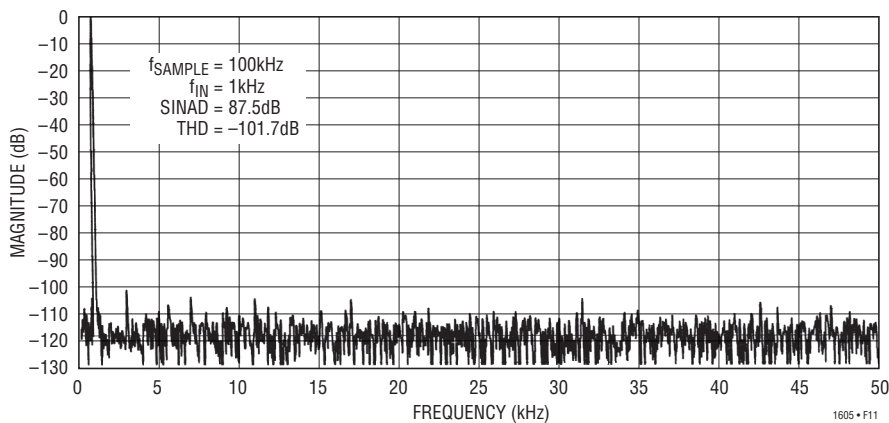


Figure 11. LTC1605 Nonaveraged 4096 Point FFT Plot

APPLICATIONS INFORMATION

a read. Again it is recommended that both $\overline{R/\overline{C}}$ and $\overline{CS}$ return high within 3 μ s after the start of the conversion.

Output Data

The output data can be read as a 16-bit word or it can be read as two 8-bit bytes. The format of the output data is two's complement. The digital input pin BYTE is used to control the two byte read. With the BYTE pin low the first eight MSBs are output on the D15 to D8 pins and the eight LSBs are output on the D7 to D0 pins. When the BYTE pin is taken high the eight LSBs replace the eight MSBs (Figure 10).

Dynamic Performance

FFT (Fast Fourier Transform) test techniques are used to test the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. Figure 11 shows a typical LTC1605 FFT plot which yields a SINAD of 87.5dB and THD of -102dB.

Signal-to-Noise Ratio

The Signal-to-Noise and Distortion Ratio (SINAD) is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other frequency components at the A/D output. The output is band limited to frequencies from above DC and below half the sampling frequency. Figure 11 shows a typical SINAD of 87.5dB with a 100kHz sampling rate and a 1kHz input.

Total Harmonic Distortion

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency

band between DC and half the sampling frequency. THD is expressed as:

$$THD = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \dots + V_N^2}}{V_1}$$

where V_1 is the RMS amplitude of the fundamental frequency and V_2 through V_N are the amplitudes of the second through Nth harmonics.

Board Layout, Power Supplies and Decoupling

Wire wrap boards are not recommended for high resolution or high speed A/D converters. To obtain the best performance from the LTC1605, a printed circuit board is required. Layout for the printed circuit board should ensure the digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or underneath the ADC. The analog input should be screened by AGND.

Figures 12 through 15 show a layout for a suggested evaluation circuit which will help obtain the best performance from the 16-bit ADC. Pay particular attention to the design of the analog and digital ground planes. The DGND pin of the LTC1605 can be tied to the analog ground plane. Placing the bypass capacitor as close as possible to the power supply, the reference and reference buffer output is very important. Low impedance common returns for these bypass capacitors are essential to low noise operation of the ADC, and the foil width for these tracks should be as wide as possible. Also, since any potential difference in grounds between the signal source and ADC appears as an error voltage in series with the input signal, attention should be paid to reducing the ground circuit impedance as much as possible. The digital output latches and the onboard sampling clock have been placed on the digital ground plane. The two ground planes are tied together at the power supply ground connection.

TYPICAL APPLICATIONS

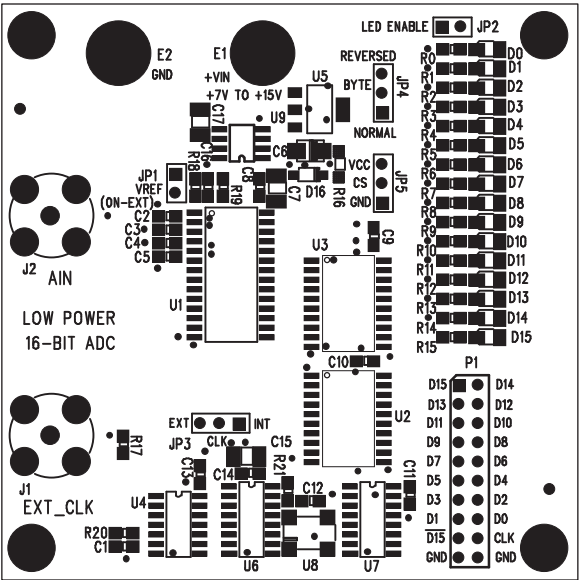


Figure 12. Component Side Silkscreen for the Suggested LTC1605 Evaluation Circuit

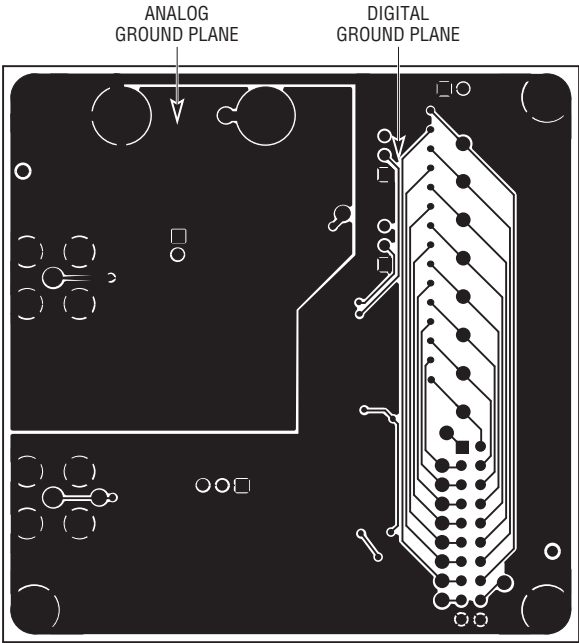


Figure 13. Bottom Side Showing Analog Ground Plane

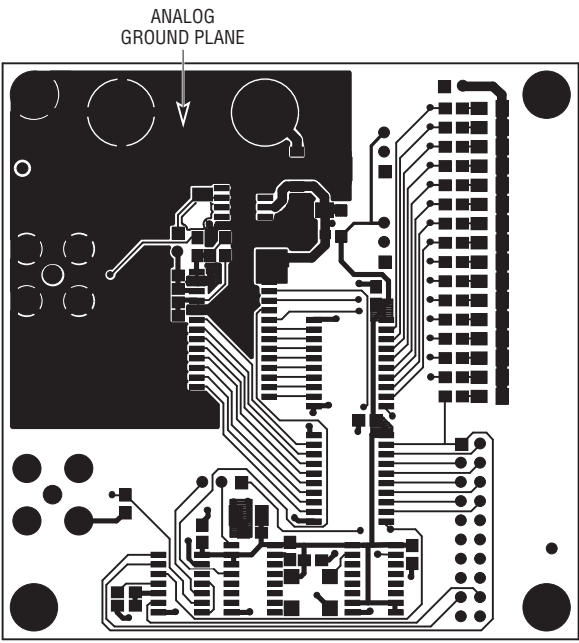


Figure 14. Component Side Showing Separate Analog and Digital Ground Plane

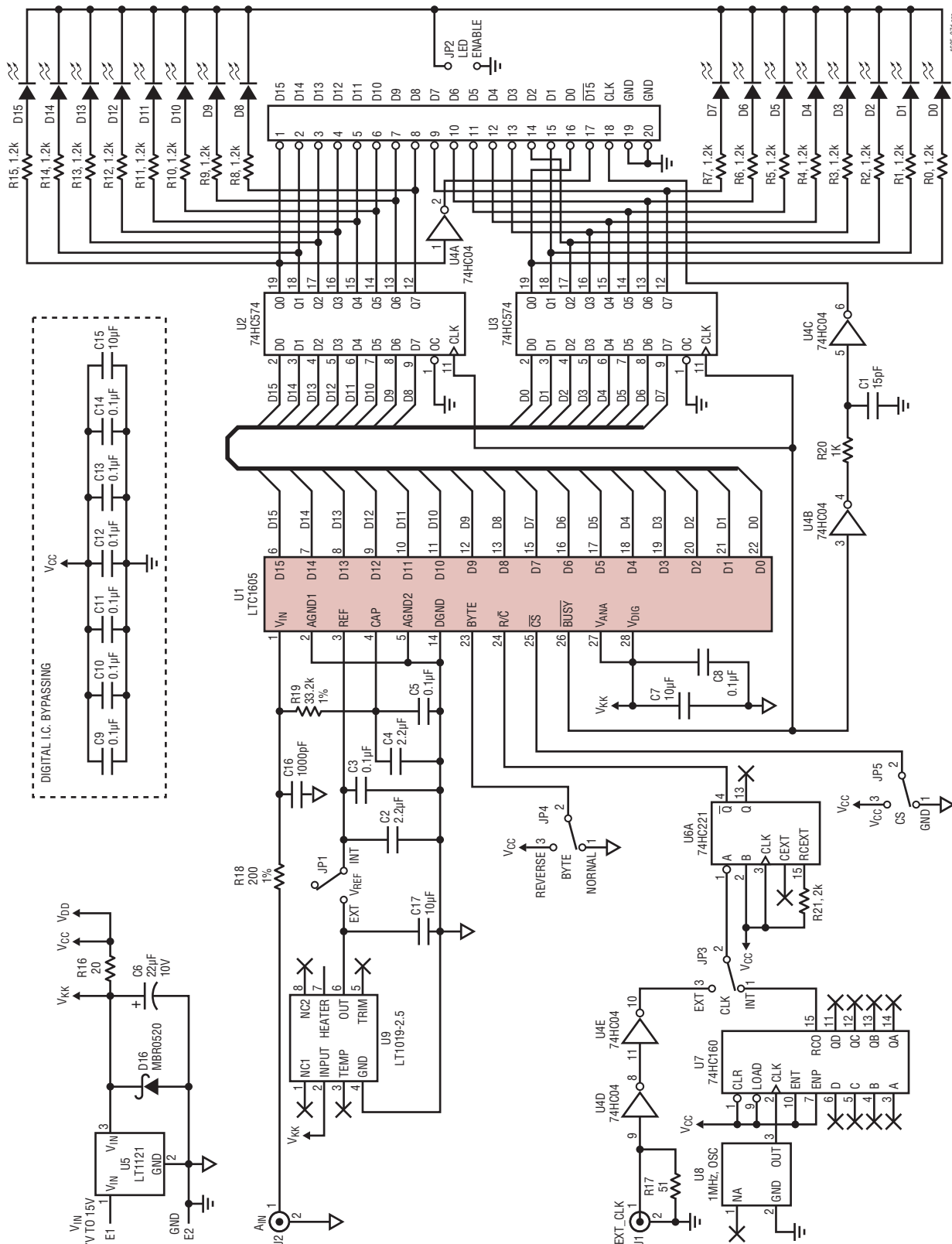
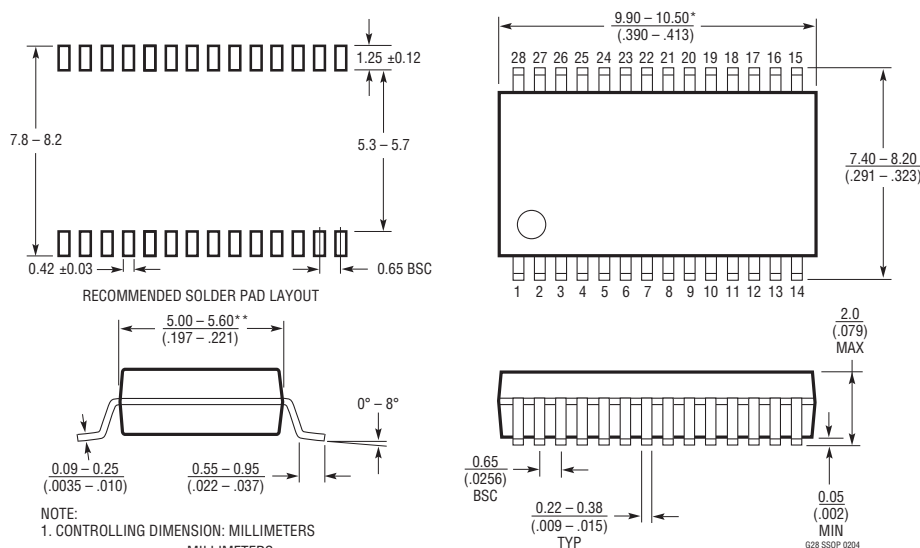


Figure 15. LTC1605 Suggested Evaluation Circuit Schematic

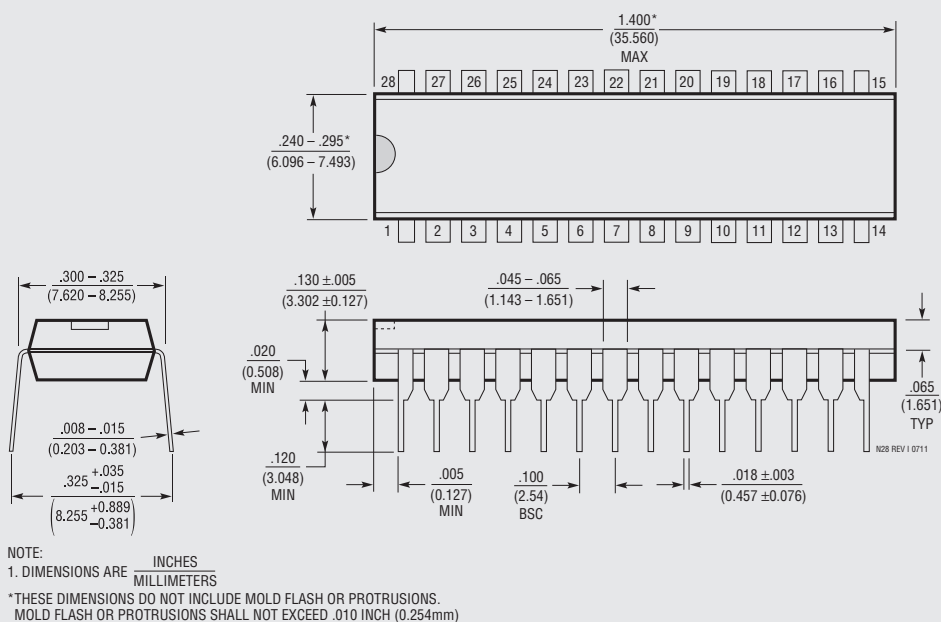
PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

G Package 28-Lead Plastic SSOP (5.3mm) (Reference LTC DWG # 05-08-1640)



N Package 28-Lead Plastic PDIP (Narrow .300 Inch) (Reference LTC DWG # 05-08-1510 Rev I)



OBSOLETE PACKAGE

REVISION HISTORY (Revision history begins at Rev D)

REV	DATE	DESCRIPTION	PAGE NUMBER
D	07/15	Obsoleted 28-Lead PDIP Package	2, 16

