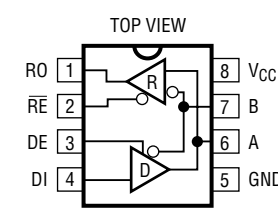


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC})	12V
Control Input Voltage	$-0.5V$ to $V_{CC} + 0.5V$
Driver Input Voltage	$-0.5V$ to $V_{CC} + 0.5V$
Driver Output Voltage	$\pm 14V$
Receiver Input Voltage	$\pm 14V$
Receiver Output Voltage	$-0.5V$ to $V_{CC} + 0.5V$
Operating Temperature Range	
LTC1483C	$0^{\circ}C \leq T_A \leq 70^{\circ}C$
LTC1483I	$-40^{\circ}C \leq T_A \leq 85^{\circ}C$
Storage Temperature Range	$-65^{\circ}C$ to $150^{\circ}C$
Lead Temperature (Soldering, 10 sec)	$300^{\circ}C$

PACKAGE/ORDER INFORMATION

 N8 PACKAGE 8-LEAD PDIP S8 PACKAGE 8-LEAD PLASTIC SO $T_{JMAX} = 125^{\circ}C$, $\theta_{JA} = 130^{\circ}C/W$ (N8) $T_{JMAX} = 125^{\circ}C$, $\theta_{JA} = 150^{\circ}C/W$ (S8)	ORDER PART NUMBER
	LTC1483CN8 LTC1483IN8 LTC1483CS8 LTC1483IS8
	S8 PART MARKING
	1483 1483I

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS $V_{CC} = 5V$, (Notes 2, 3) unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OD1}	Differential Driver Output Voltage (Unloaded)	$I_O = 0$	●		5	V
V_{OD2}	Differential Driver Output Voltage (with Load)	$R = 50\Omega$ (RS422) $R = 27\Omega$ (RS485), Figure 1	● ●	2 1.5	5	V
ΔV_{OD}	Change in Magnitude of Driver Differential Output Voltage for Complementary Output States	$R = 27\Omega$ or $R = 50\Omega$, Figure 1	●		0.2	V
V_{OC}	Driver Common-Mode Output Voltage	$R = 27\Omega$ or $R = 50\Omega$, Figure 1	●		3	V
$\Delta V_{OC} $	Change in Magnitude of Driver Common-Mode Output Voltage for Complementary Output States	$R = 27\Omega$ or $R = 50\Omega$, Figure 1	●		0.2	V
V_{IH}	Input High Voltage	DE, DI, $\overline{RE}$	●	2		V
V_{IL}	Input Low Voltage	DE, DI, $\overline{RE}$	●		0.8	V
I_{IN1}	Input Current	DE, DI, $\overline{RE}$	●		± 2	μA
I_{IN2}	Input Current (A, B)	DE = 0, $V_{CC} = 0V$ or $5.25V$, $V_{IN} = 12V$ DE = 0, $V_{CC} = 0V$ or $5.25V$, $V_{IN} = -7V$	● ●		1.0 -0.8	mA
V_{TH}	Differential Input Threshold Voltage for Receiver	$-7V \leq V_{CM} \leq 12V$	●	-0.2	0.2	V
ΔV_{TH}	Receiver Input Hysteresis	$V_{CM} = 0V$	●	45		mV
V_{OH}	Receiver Output High Voltage	$I_O = -4mA$, $V_{ID} = 200mV$	●	3.5		V
V_{OL}	Receiver Output Low Voltage	$I_O = 4mA$, $V_{ID} = -200mV$	●		0.4	V
I_{OZR}	Three-State (High Impedance) Output Current at Receiver	$V_{CC} = \text{Max}$, $0.4V \leq V_O \leq 2.4V$	●		± 1	μA
R_{IN}	Receiver Input Resistance	$-7V \leq V_{CM} \leq 12V$	●	12	25	k Ω
I_{CC}	Supply Current	No Load, Output Enabled No Load, Output Disabled	● ●	300 80	500 120	μA
I_{SHDN}	Supply Current in Shutdown Mode	DE = 0, $\overline{RE} = V_{CC}$		1	10	μA
I_{OSD1}	Driver Short-Circuit Current, $V_{OUT} = \text{HIGH}$	$-7V \leq V_O \leq 12V$	●	35	250	mA
I_{OSD2}	Driver Short-Circuit Current, $V_{OUT} = \text{LOW}$	$-7V \leq V_O \leq 12V$	●	35	250	mA
I_{OSR}	Receiver Short-Circuit Current	$0V \leq V_O \leq V_{CC}$	●	7	85	mA

SWITCHING CHARACTERISTICS $V_{CC} = 5V$, (Notes 2, 3) unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1483			UNITS
				MIN	TYP	MAX	
t _{PLH}	Driver Input to Output	R _{DIFF} = 54Ω, C _{L1} = C _{L2} = 100pF, (Figures 3, 5)	●	150		1200	ns
t _{PHL}	Driver Input to Output		●	150		1200	ns
t _{SKEW}	Driver Output to Output		●		100	600	ns
t _r , t _f	Driver Rise or Fall Time		●	150		1200	ns
t _{ZH}	Driver Enable to Output High	C _L = 100pF (Figures 4, 6), S2 Closed	●	100		1500	ns
t _{ZL}	Driver Enable to Output Low	C _L = 100pF (Figures 4, 6), S1 Closed	●	100		1500	ns
t _{LZ}	Driver Disable Time from Low	C _L = 15pF (Figures 4, 6), S1 Closed	●	150		1500	ns
t _{HZ}	Driver Disable Time from High	C _L = 15pF (Figures 4, 6), S2 Closed	●	150		1500	ns
t _{PLH}	Receiver Input to Output	R _{DIFF} = 54Ω, C _{L1} = C _{L2} = 100pF, (Figures 3, 7)	●	30	140	200	ns
t _{PHL}	Receiver Input to Output		●	30	140	200	ns
t _{SKD}	t _{PLH} – t _{PHL} Differential Receiver Skew		●		13		ns
t _{ZL}	Receiver Enable to Output Low	C _{RL} = 15pF (Figures 2, 8), S1 Closed	●		20	50	ns
t _{ZH}	Receiver Enable to Output High	C _{RL} = 15pF (Figures 2, 8), S2 Closed	●		20	50	ns
t _{LZ}	Receiver Disable from Low	C _{RL} = 15pF (Figures 2, 8), S1 Closed	●		20	50	ns
t _{HZ}	Receiver Disable from High	C _{RL} = 15pF (Figures 2, 8), S2 Closed	●		20	50	ns
f _{MAX}	Maximum Data Rate		●	250			kbits/s
t _{SHDN}	Time to Shutdown	DE = 0, RE = 1	●	50	200	600	ns
t _{ZH(SHDN)}	Driver Enable from Shutdown to Output High	C _L = 100pF (Figures 4, 6), S2 Closed	●			2000	ns
t _{ZL(SHDN)}	Driver Enable from Shutdown to Output Low	C _L = 100pF (Figures 4, 6), S1 Closed	●			2000	ns
t _{ZH(SHDN)}	Receiver Enable from Shutdown to Output High	C _L = 15pF (Figures 2, 8), S2 Closed	●			3500	ns
t _{ZL(SHDN)}	Receiver Enable from Shutdown to Output Low	C _L = 15pF (Figures 2, 8), S1 Closed	●			3500	ns

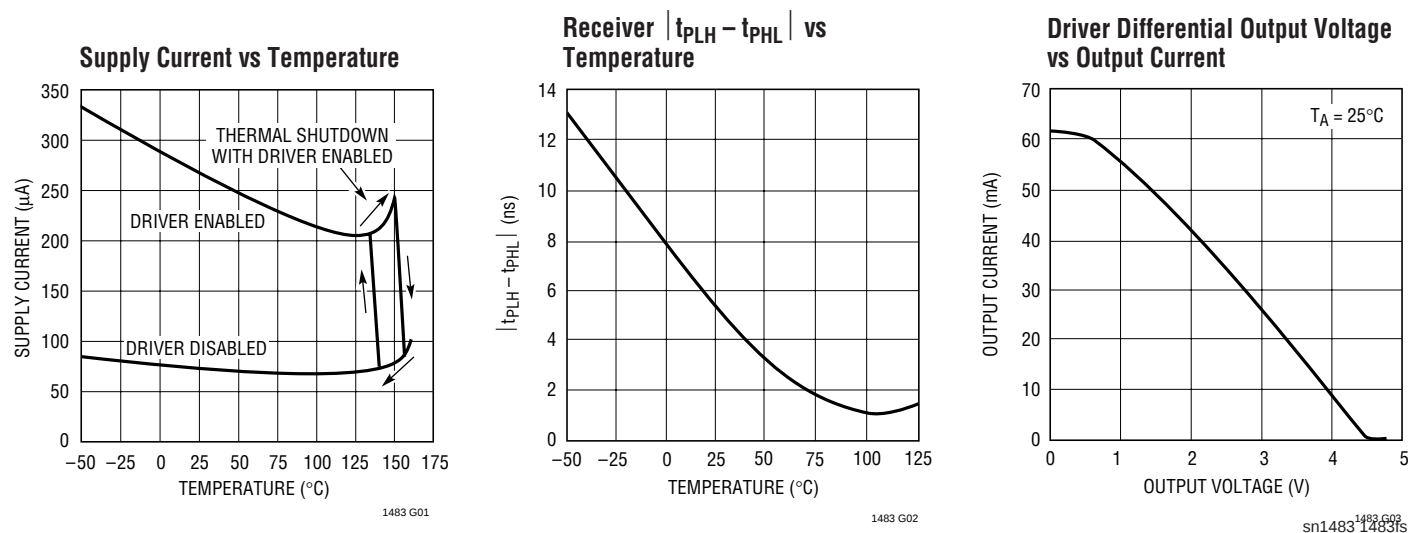
The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute maximum ratings are those beyond which the safety of the device cannot be guaranteed.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

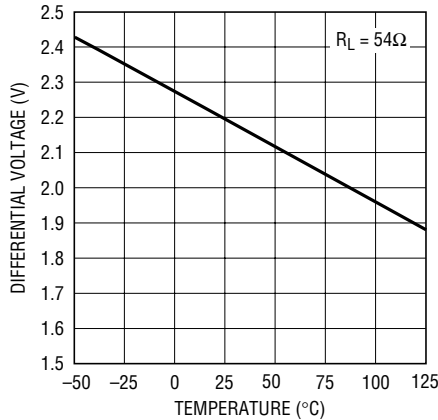
Note 3: All typicals are given for $V_{CC} = 5V$ and $T_A = 25^\circ C$.

TYPICAL PERFORMANCE CHARACTERISTICS



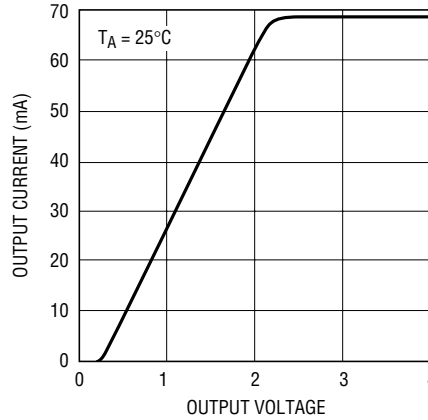
TYPICAL PERFORMANCE CHARACTERISTICS

Driver Differential Output Voltage
vs Temperature



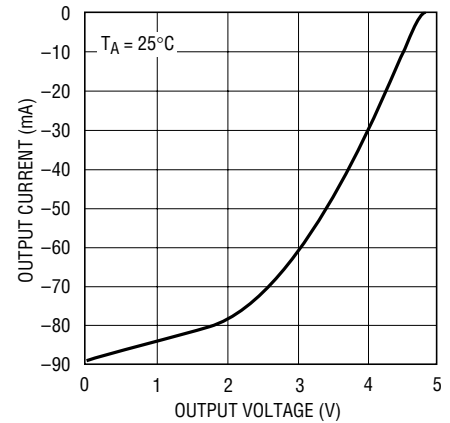
1483 G04

Driver Output Low Voltage
vs Output Current



1483 G05

Driver Output High Voltage
vs Output Current



1483 G06

PIN FUNCTIONS

RO (Pin 1): Receiver Output. If the receiver output is enabled ($\overline{RE}$ low), then if $A > B$ by 200mV, RO will be high. If $A < B$ by 200mV, then RO will be low.

$\overline{RE}$ (Pin 2): Receiver Output Enable. A low enables the receiver output, RO. A high input forces the receiver output into a high impedance state.

DE (Pin 3): Driver Outputs Enable. A high on DE enables the driver output. A, B and the chip will function as a line driver. A low input will force the driver outputs into a high impedance state and the chip will function as a line receiver. If $\overline{RE}$ is high and DE is low, the part will enter a low power ($1\mu A$) shutdown state.

DI (Pin 4): Driver Input. If the driver outputs are enabled (DE high) then a low on DI forces the outputs A low and B high. A high on DI with the driver outputs enabled will force A high and B low.

GND (Pin 5): Ground.

A (Pin 6): Driver Output/Receiver Input.

B (Pin 7): Driver Output/Receiver Input.

V_{CC} (Pin 8): Positive Supply. $4.75V < V_{CC} < 5.25V$.

FUNCTION TABLES

LTC1483 Transmitting

INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	B	A
X	1	1	0	1
X	1	0	1	0
0	0	X	Z	Z
1	0	X	Z*	Z*

*Shutdown mode for LTC1483

LTC1483 Receiving

INPUTS			OUTPUTS
$\overline{RE}$	DE	A - B	RO
0	0	$\geq 0.2V$	1
0	0	$\leq -0.2V$	0
0	0	Inputs Open	1
1	0	X	Z*

*Shutdown mode for LTC1483

TEST CIRCUITS

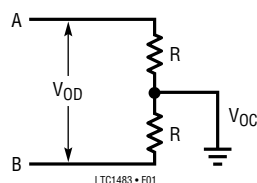


Figure 1. Driver DC Test Load

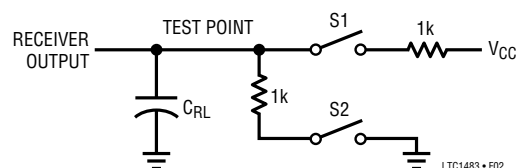


Figure 2. Receiver Timing Test Load

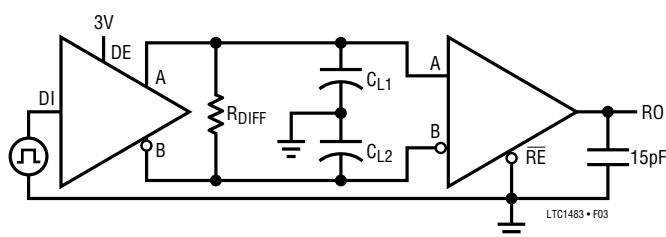


Figure 3. Driver/Receiver Timing Test Circuit

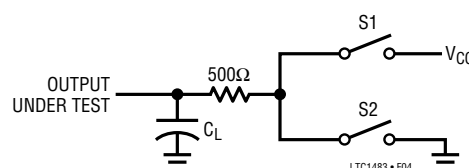


Figure 4. Driver Timing Test Load

SWITCHING TIME WAVEFORMS

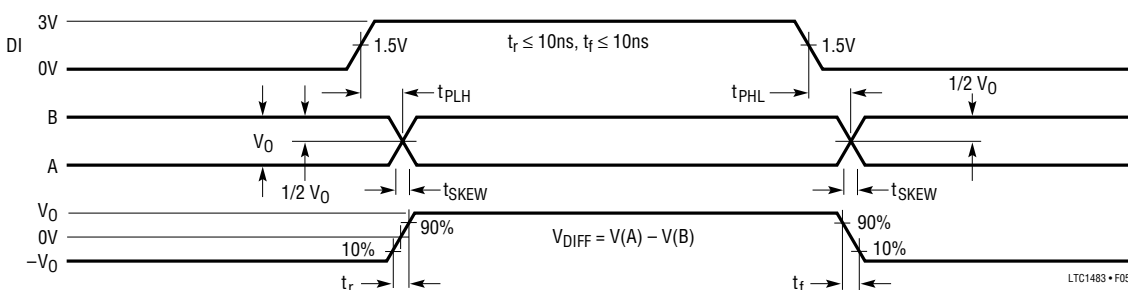


Figure 5. Driver Propagation Delays

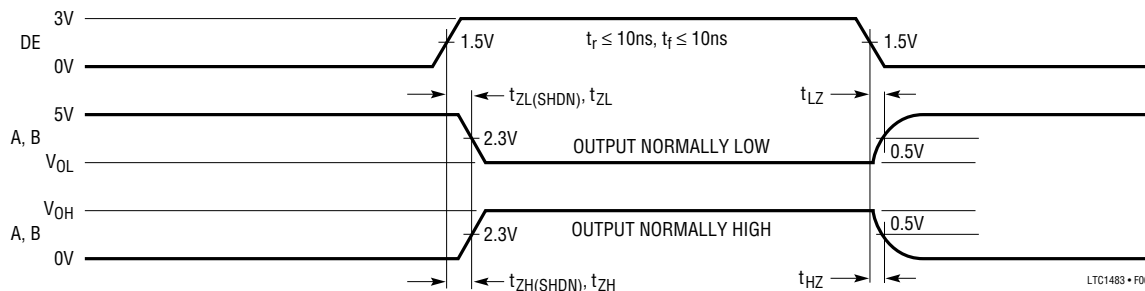


Figure 6. Driver Enable and Disable Times

SWITCHING TIME WAVEFORMS

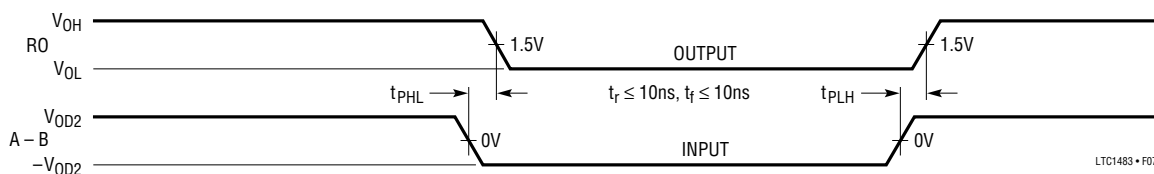


Figure 7. Receiver Propagation Delays

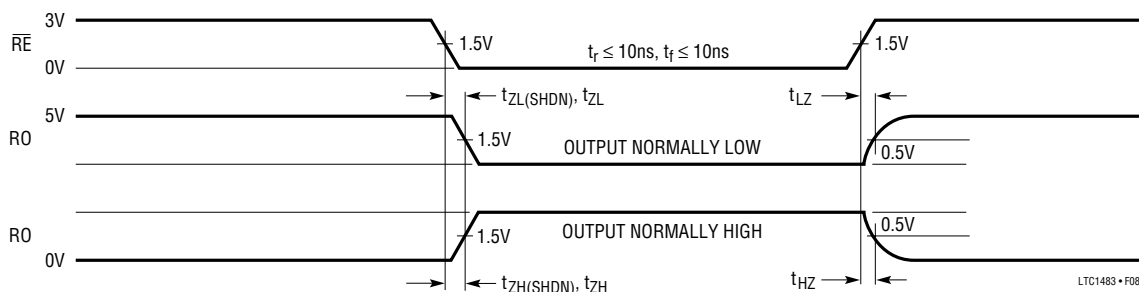


Figure 8. Receiver Enable and Disable Times

APPLICATIONS INFORMATION

Basic Theory of Operation

Traditionally RS485 transceivers have been designed using bipolar technology because the common-mode range of the device must extend beyond the supplies and the device must be immune to ESD damage and latch-up. Unfortunately, most bipolar devices draw a large amount of supply current, which is unacceptable for the numerous applications that require low power consumption. The LTC1483 is a CMOS RS485/RS422 transceiver which features ultra-low power consumption without sacrificing ESD and latch-up immunity.

The LTC1483 uses a proprietary driver output stage, which allows a common-mode range that extends beyond the power supplies while virtually eliminating latch-up and providing excellent ESD protection. Figure 9 shows the LTC1483 output stage while Figure 10 shows a conventional CMOS output stage.

When the conventional CMOS output stage of Figure 10 enters a high impedance state, both the P-channel (P1) and the N-channel (N1) are turned off. If the output is then driven above V_{CC} or below ground, the P+/N-well diode

(D1) or the N+/P-substrate diode (D2) respectively will turn on and clamp the output to the supply. Thus, the output stage is no longer in a high impedance state and is not able to meet the RS485 common-mode range requirement. In addition, the large amount of current flowing through either diode will induce the well-known CMOS latch-up condition, which could destroy the device.

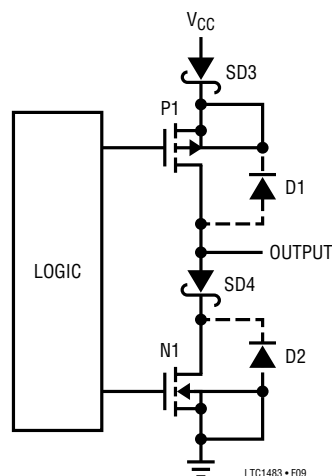


Figure 9. LTC1483 Output Stage

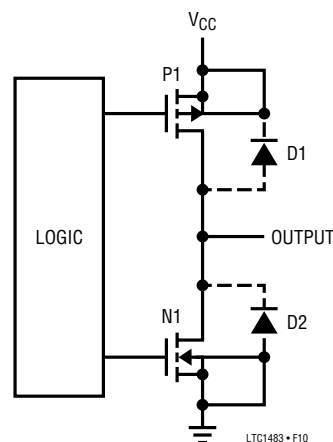


Figure 10. Conventional CMOS Output Stage

sn1483 1483fs

APPLICATIONS INFORMATION

The LTC1483 output stage of Figure 9 eliminates these problems by adding two Schottky diodes, SD3 and SD4. The Schottky diodes are fabricated by a proprietary modification to the standard N-well CMOS process. When the output stage is operating normally, the Schottky diodes are forward biased and have a small voltage drop across them. When the output is in the high impedance state and is driven above V_{CC} or below ground, the parasitic diode D1 or D2 still turns on, but SD3 or SD4 will reverse bias and prevent current from flowing into the N-well or the substrate. Thus the high impedance state is maintained even with the output voltage beyond the supplies. With no minority carrier current flowing into the N-well or substrate, latch-up is virtually eliminated under power-up or power-down conditions.

The LTC1483 output stage will maintain a high impedance state until the breakdown of the N-channel or P-channel is reached when going positive or negative respectively. The output will be clamped to either V_{CC} or ground by a Zener voltage plus a Schottky diode drop, but this voltage is well beyond the RS485 operating range. An ESD cell protects output against multiple $\pm 10\text{kV}$ human body model ESD strikes. Because the ESD injected current in the N-well or substrate consists of majority carriers, latch-up is prevented by careful layout techniques.

Slew Rate

The LTC1483 is designed for systems that are sensitive to electromagnetic radiation. The part features a slew rate limited driver that reduces high frequency electromagnetic emissions, while improving signal fidelity by reducing reflections due to misterminated cables. Figures 11 and 12 show the spectrum of the signal at the driver output for a standard slew rate RS485 driver and the slew rate limited LTC1483. The LTC1483 shows significant reduction of the high frequency harmonics. Because the driver is slew rate limited, the maximum operating frequency is limited to 250kbits/s.

Low Power Operation

The LTC1483 is designed to operate with a quiescent current of $120\mu\text{A}$ max. With the driver in three-state I_{CC} will

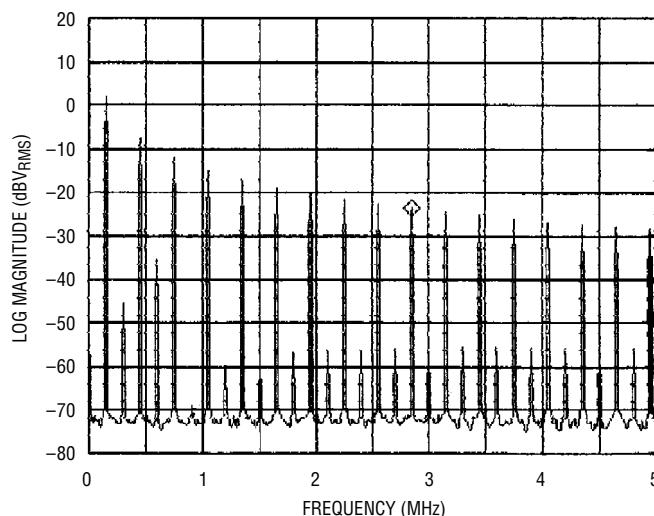


Figure 11. Typical RS485 Driver Output Spectrum Transmitting at 150kHz

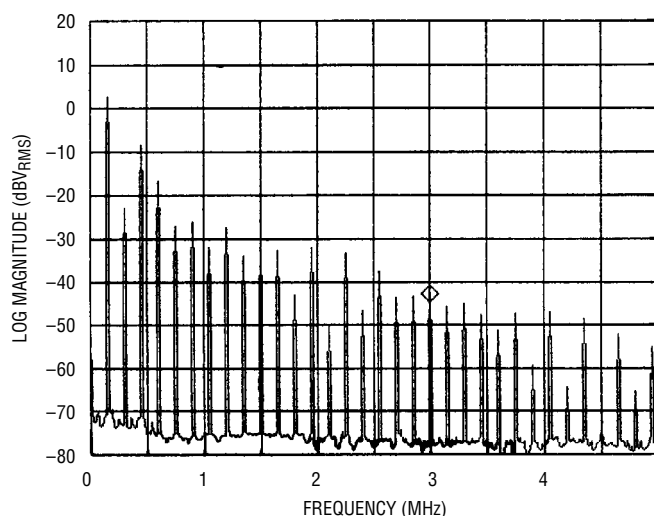


Figure 12. Slew Rate Limited LTC1483 Driver Output Spectrum Transmitting at 150kHz

drop to this $120\mu\text{A}$ level. With the driver enabled there will be additional current drawn by the internal 12k resistor. Under normal operating conditions this additional current is overshadowed by the current drawn by the external bus impedance.

