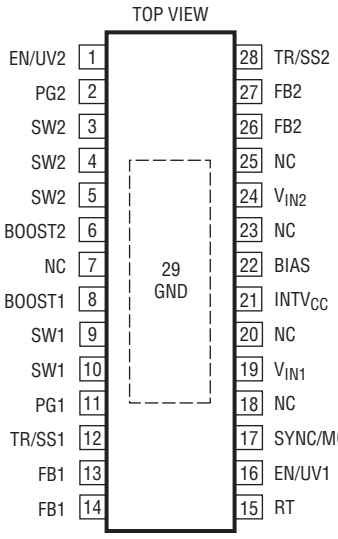
ABSOLUTE MAXIMUM RATINGS (Note 1)

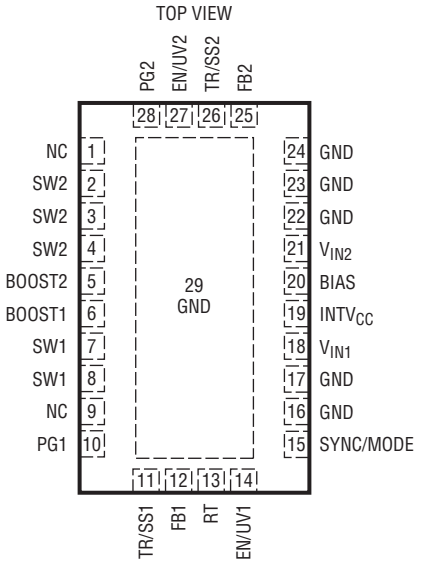
V_{IN1}, V_{IN2}, EN/UV1, EN/UV2, PG1, PG2.....42V
BIAS.....30V
BST1 Above SW1, BST2 Above SW2, FB1, FB2,
TR/SS1, TR/SS2.....4V
SYNC/MODE.....6V

Operating Junction Temperature Range (Note 2)
LT8616E.....–40°C to 125°C
LT8616I.....–40°C to 125°C
LT8616H.....–40°C to 150°C
Storage Temperature Range.....–60°C to 150°C

PIN CONFIGURATION



FE PACKAGE
28-LEAD PLASTIC TSSOP
θ_{JA} = 30°C/W, $\theta_{JC(PAD)}$ = 10°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB



UDE PACKAGE
28-LEAD (3mm × 6mm) PLASTIC QFN
θ_{JA} = 40°C/W, $\theta_{JC(PAD)}$ = 5°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8616EFE#PBF	LT8616EFE#TRPBF	LT8616FE	28-Lead Plastic TSSOP	–40 to 125°C
LT8616IFE#PBF	LT8616IFE#TRPBF	LT8616FE	28-Lead Plastic TSSOP	–40 to 125°C
LT8616HFE#PBF	LT8616HFE#TRPBF	LT8616FE	28-Lead Plastic TSSOP	–40 to 150°C
LT8616EUDE#PBF	LT8616EUDE#TRPBF	LGMM	28-Lead 3mm × 6mm Plastic QFN	–40 to 125°C
LT8616IUDE#PBF	LT8616IUDE#TRPBF	LGMM	28-Lead 3mm × 6mm Plastic QFN	–40 to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Common						
Quiescent Current	EN/UV1 = EN/UV2 = 0V, Current from V_{IN1}	 ●		1.7 1.7	4.0 8.0	µA µA
	EN/UV1 = EN/UV2 = 2V, SYNC = 0V (Burst Mode), Not Switching, Current from V_{IN1}	 ●		3.0 3.0	5.0 12.0	µA µA
	EN/UV1 = EN/UV2 = 2V, SYNC = 3V (Pulse-Skipping Mode), Not Switching, Current from BIAS or V_{IN1}	●		0.5	1.0	mA
FB Voltage	V_{IN} = 6V, Load = 0.5A	 ●	782 778	790 790	798 802	mV mV
FB Voltage Line Regulation	V_{IN} = 4V to 25V, Load = 0.5A			0.005		%/V
FB Pin Input Current	FB = 0.79V		–20		20	nA
EN/UV Pin Threshold	Rising	●	0.97	1.03	1.09	V
EN/UV Pin Hysteresis				50		mV
EN/UV Pin Current	EN/UV = 2V		–20		20	nA
PG Upper Threshold from V_{FB}	FB Rising	●	6	10	13	%
PG Lower Threshold from V_{FB}	FB Falling	●	–6	–10	–13	%
PG Hysteresis				1		%
PG Leakage	PG = 3.3V		–100		100	nA
PG Pull-Down Resistance	PG = 0.1V			350		Ω
TR/SS Source Current			1	2	3	µA
TR/SS Pull-Down Resistance	TR/SS = 0.1V			250		Ω
BIAS Pin Current Consumption	V_{OUT1} = 3.3V, Load1 = 0.5A, V_{OUT2} = 3.3V, Load2 = 0.5A, f_{SW} = 1MHz			7		mA
Oscillator Frequency	R_T = 14.7kΩ R_T = 37.4kΩ R_T = 221kΩ	● ● ●	1.85 900 160	2.05 1000 200	2.25 1100 240	MHz kHz kHz
SYNC Threshold	SYNC Falling SYNC Rising		0.4		 2.4	V V
SYNC Pin Current	SYNC = 3V		–100		100	nA
Channel 1						
Minimum V_{IN1} Voltage		●		3.0	3.4	V
Supply Current in Regulation	V_{IN} = 6V, V_{OUT1} = 3.3V, Load = 100µA V_{IN} = 6V, V_{OUT1} = 3.3V Load = 1mA			80 620	110 910	µA µA
SW1 Minimum On-Time	Load = 0.25A, Pulse-Skipping Mode	●	20	35	55	ns
SW1 Top NMOS On-Resistance				310		mΩ
SW1 Peak Current Limit	(Note 3)	●	3.2	4.2	5.2	A
SW1 Bottom NMOS On-Resistance				190		mΩ
SW1 Valley Current Limit		●	1.5	2.0	3.0	A
SW1 Leakage Current	V_{IN1} = 42V, V_{SW1} = 0V, 42V		–2		2	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Channel 2						
Minimum V_{IN1} Voltage to Use Channel2		●		3.0	3.4	V
Supply Current in Regulation	V_{IN} = 6V, V_{OUT2} = 3.3V, Load2 = 100µA V_{IN} = 6V, V_{OUT2} = 3.3V Load2 = 1mA			80 620	110 910	µA µA
SW2 Minimum On-Time	Load = 0.25A, Pulse-Skipping Mode	●	20	35	55	ns
SW2 Top NMOS On-Resistance				145		mΩ
SW2 Peak Current Limit	(Note 3)	●	4.5	5.5	6.5	A
SW2 Bottom NMOS On-Resistance				120		mΩ
SW2 Valley Current Limit		●	2.5	3.5	4.5	A
SW2 Leakage Current	V_{IN2} = 42V, V_{SW2} = 0V, 42V		–2		2	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

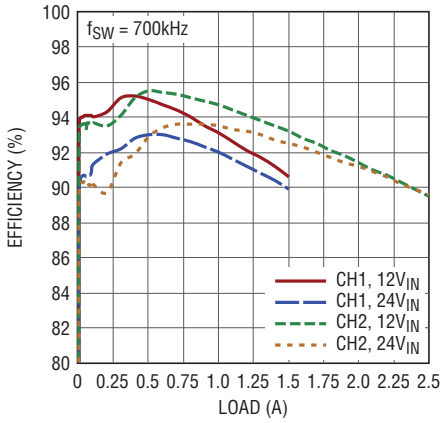
Note 2: The LT8616E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT8616I is guaranteed over the full –40°C to 125°C operating junction temperature range. The LT8616H is guaranteed over the full –40°C to 150°C operating junction temperature range.

Note 3: Current limit guaranteed by design and/or correlation to static test. Slope compensation reduces current limit at higher duty cycle.

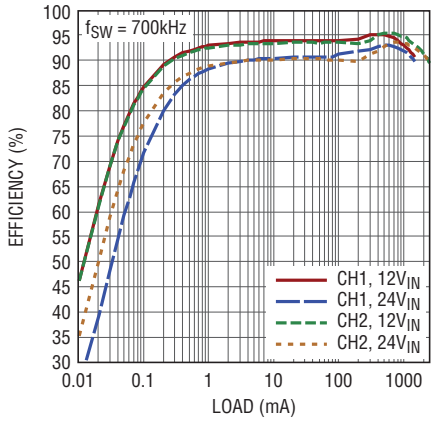
Note 4: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed the maximum operating junction temperature when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability. See High Temperature Considerations section.

TYPICAL PERFORMANCE CHARACTERISTICS

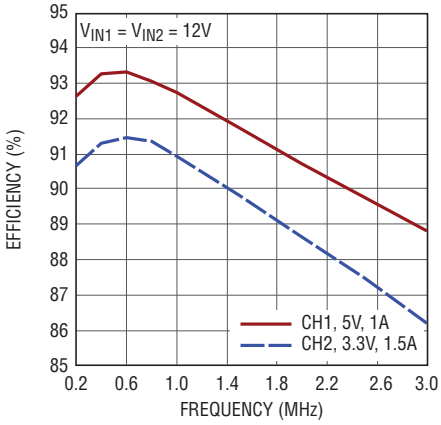
Efficiency at $5V_{OUT}$



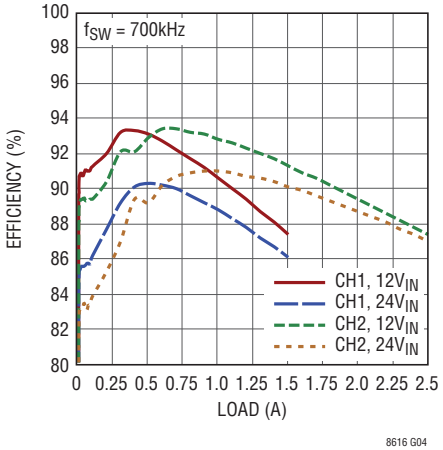
Efficiency at $5V_{OUT}$



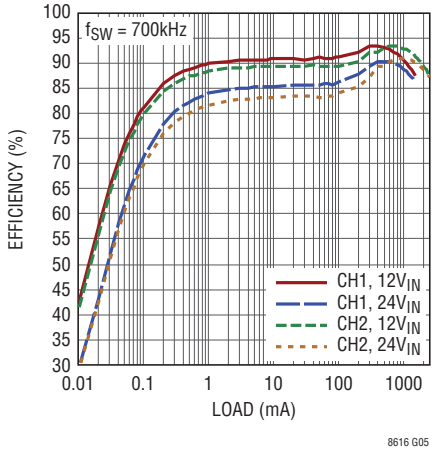
Efficiency vs Frequency



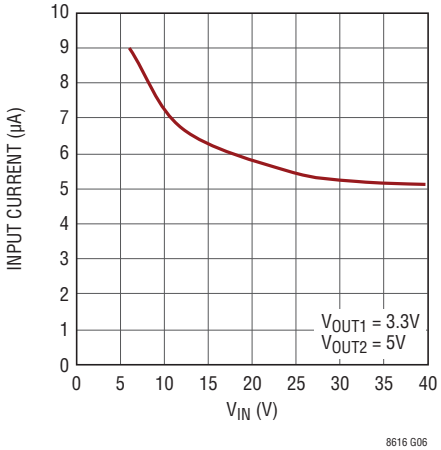
Efficiency at $3.3V_{OUT}$



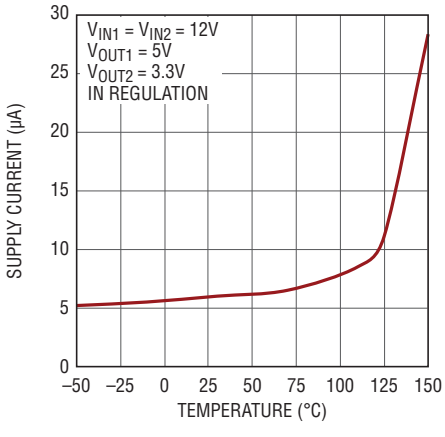
Efficiency at $3.3V_{OUT}$



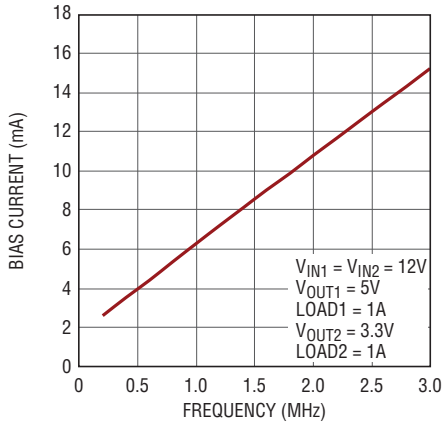
No Load Supply Current



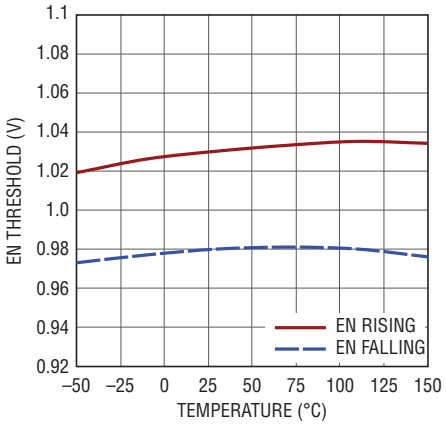
No Load Supply Current



BIAS Current vs Switching Frequency

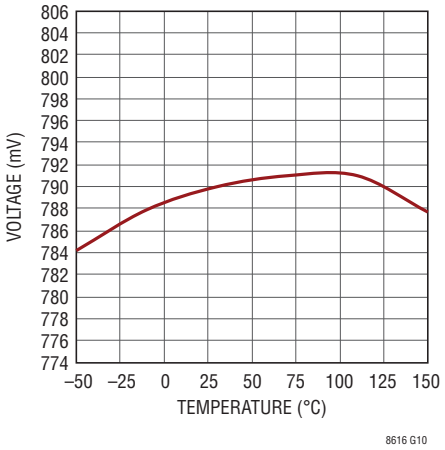


EN/UV Threshold

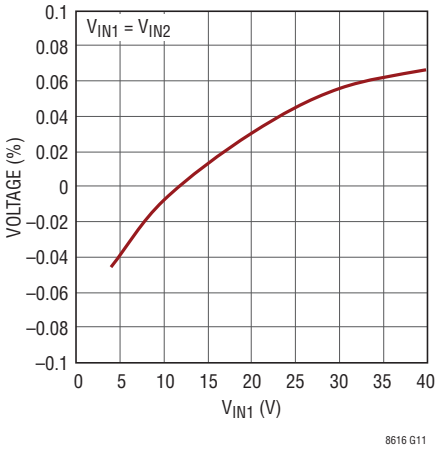


TYPICAL PERFORMANCE CHARACTERISTICS

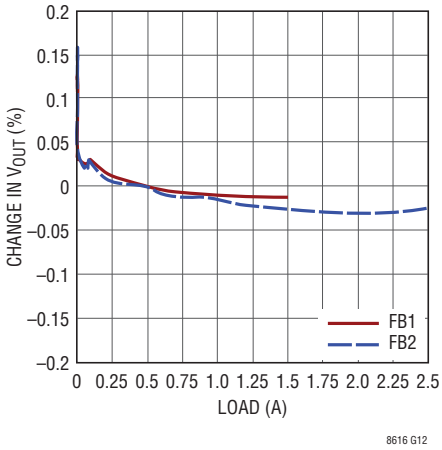
FB Voltage vs Temperature



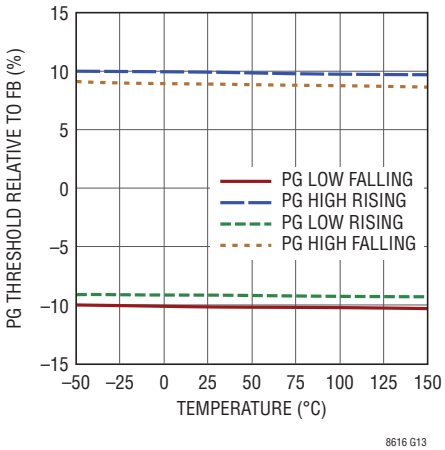
Line Regulation vs V_{IN1}



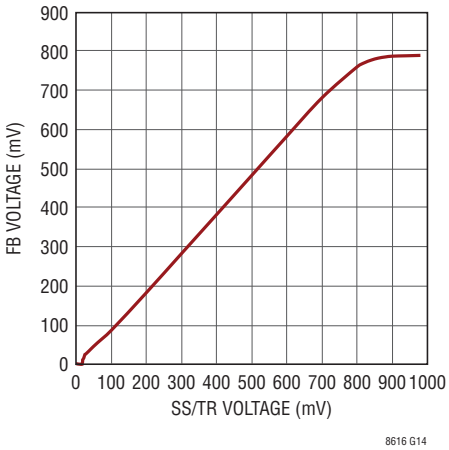
Load Regulation



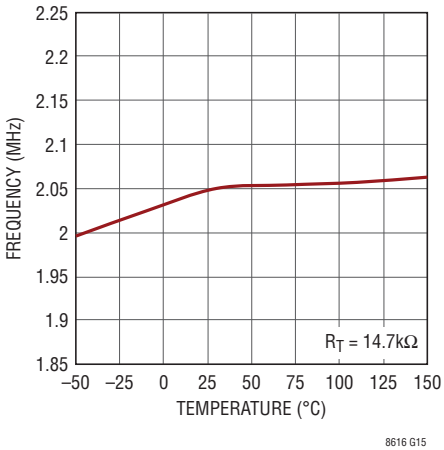
Power-Good Thresholds



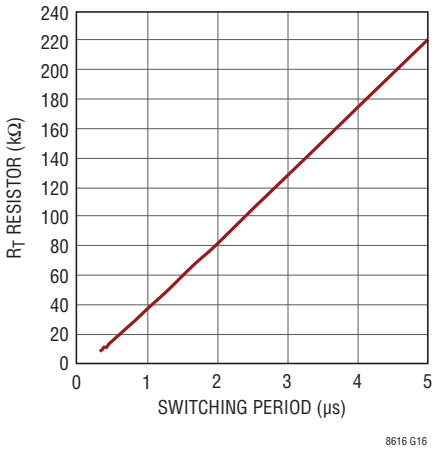
Soft-Start Tracking



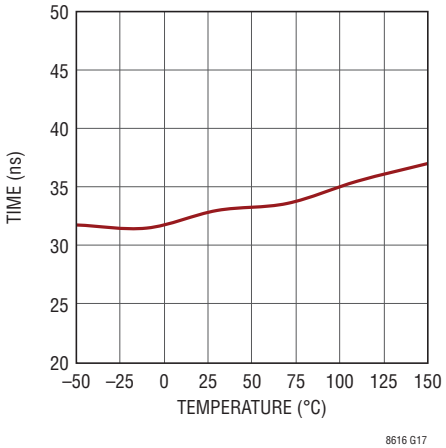
Switching Frequency



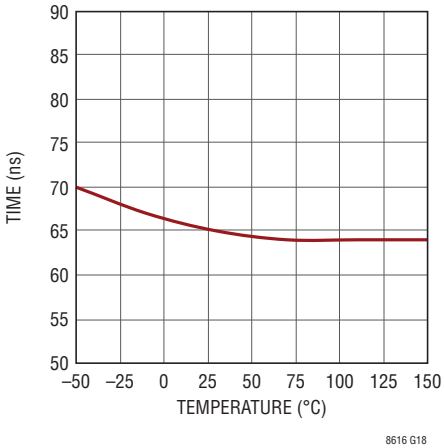
Switching Period vs R_T



Minimum On-Time

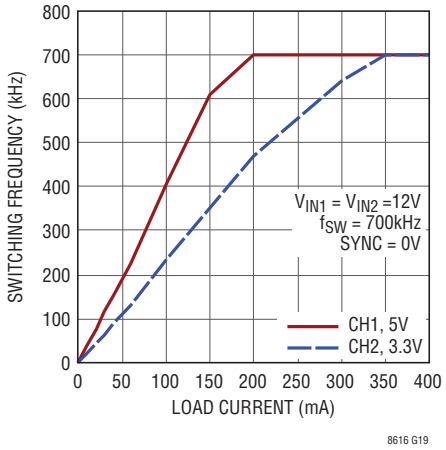


Minimum Off-Time

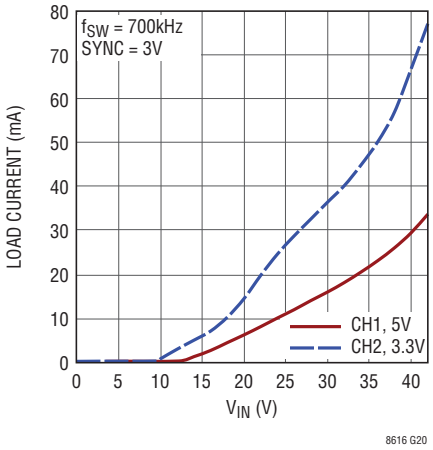


TYPICAL PERFORMANCE CHARACTERISTICS

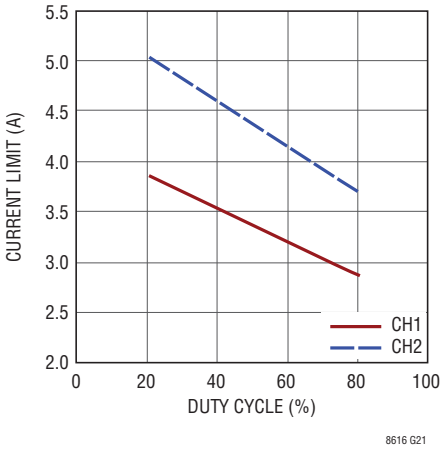
Burst Frequency vs Load



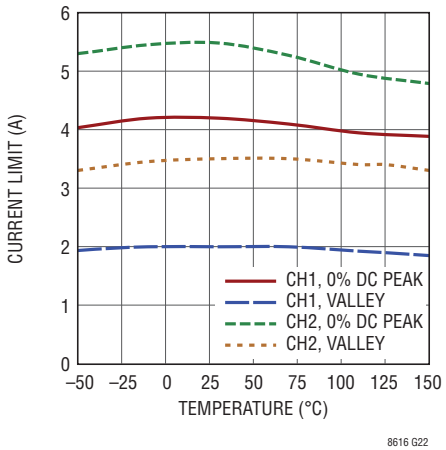
Minimum Load for Full Frequency



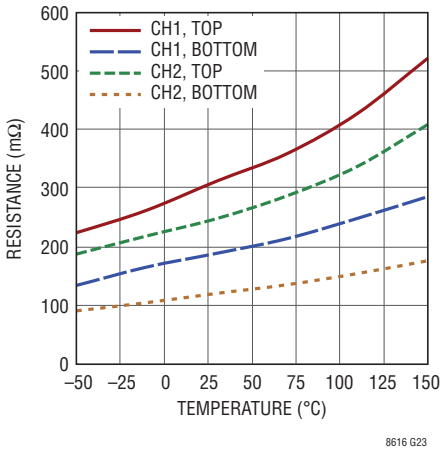
Top FET Current Limit vs Duty Cycle



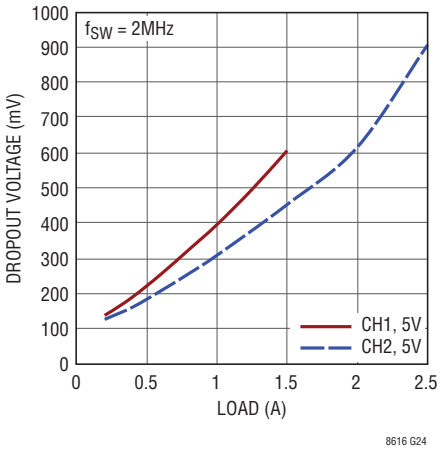
Current Limit vs Temperature



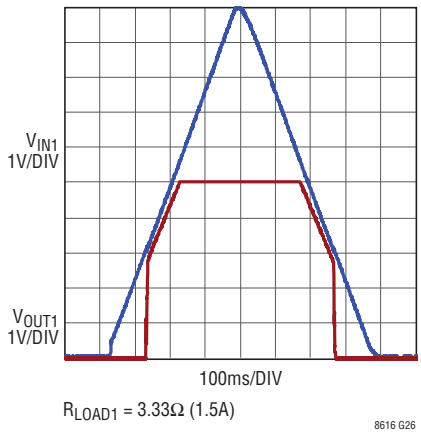
Switch Resistance vs Temperature



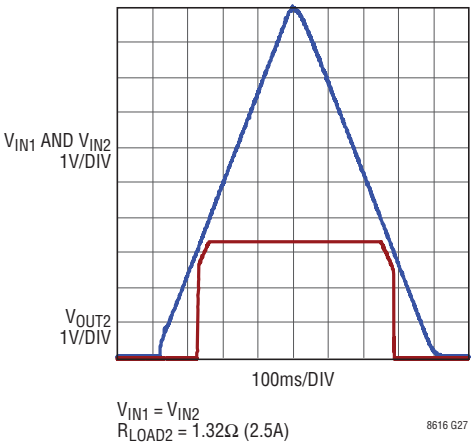
Dropout Voltage vs Load



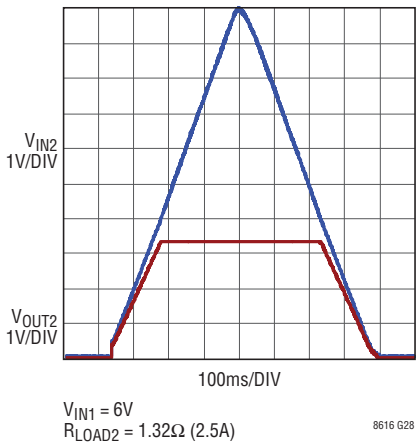
Start-Up Dropout (CH1, 5V)



Start-Up Dropout (CH2, 3.3V)

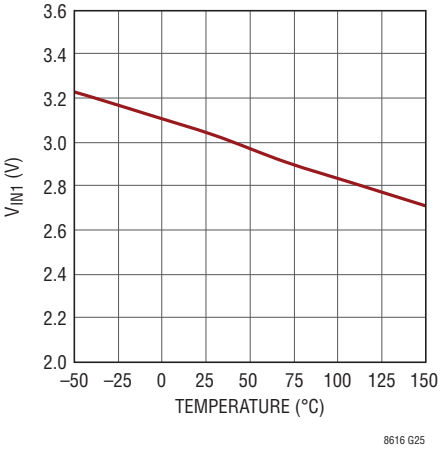


Start-Up Dropout (CH2, 3.3V)

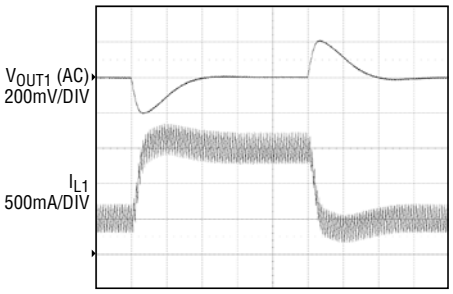


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN1} UVLO

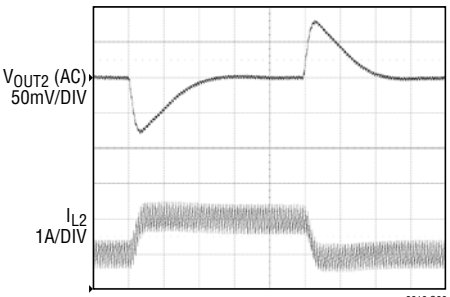


Transient CH1, 5V



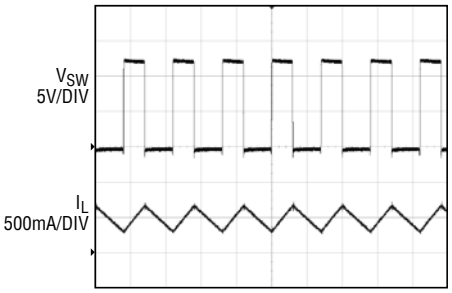
V_{IN1} = 12V
V_{OUT1} = 5V
L1 = 10µH
C_{OUT1} = 47µF
C_{FF} = 5.6pF

Transient CH2, 3.3V



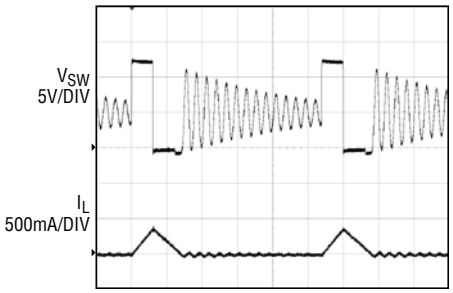
V_{IN2} = 12V
V_{OUT2} = 3.3V
L2 = 4.7µH
C_{OUT2} = 2 x 47µF
C_{FF2} = 10pF

CCM



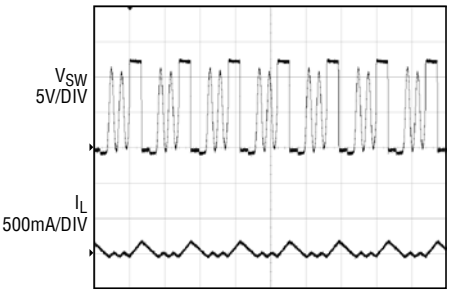
$12V_{IN}$ TO $5V_{OUT}$ AT 500mA

Burst Mode



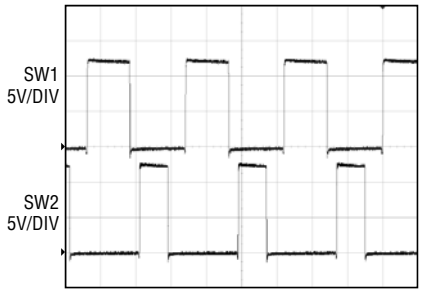
$12V_{IN}$ TO $5V_{OUT}$ AT 50mA
SYNC = 0V

DCM



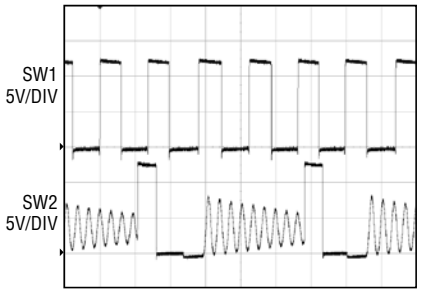
$12V_{IN}$ TO $5V_{OUT}$ AT 50mA
SYNC = 3V

CH1 CCM, CH2 CCM



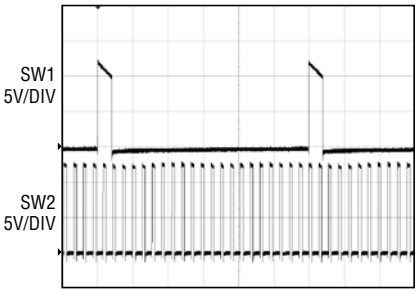
V_{IN} = 12V
CH1 = 5V, 1A
CH2 = 3.3V, 1A
SYNC = 0V

CH1 CCM, CH2 Burst Mode



V_{IN} = 12V
CH1 = 5V, 1A
CH2 = 3.3V, 0.1A
SYNC = 0V

CH1 Shorted, CH2 CCM



V_{IN} = 12V
CH1 = 0V SHORT
CH2 = 3.3V, 1A
SYNC = 0V

PIN FUNCTIONS

BIAS: The BIAS pin supplies the internal regulator when tied to a voltage higher than 3.1V. For output voltages of 3.3V and above this pin should be tied to the appropriate V_{OUT}. Connect a 1µF bypass capacitor to this pin if it is connected to a supply other than V_{OUT1} or V_{OUT2}. Ground if unused.

BOOST1, BOOST2: The BOOST pins are used to provide drive voltages, higher than the input voltage, to the internal topside power switches. Place 0.1µF capacitors between BOOST and its corresponding SW pin as close as possible to the IC. BOOST nodes should be kept small on the PCB for good performance.

EN/UV1, EN/UV2: The EN/UV pins are used to independently disable each channel when pulled low and enable when pulled high. The hysteretic threshold voltage is 1.03V going up and 0.98V going down. Tie to V_{IN} supply if the shutdown feature is not used. External resistor dividers from V_{IN} can be used to program thresholds below which each channel is disabled. Don't float these pins.

FB1, FB2: The FB pins are regulated to 0.790V. Connect the feedback resistor divider taps to the FB pins. Also connect phase lead capacitors between FB pins and V_{OUT} nodes. Typical phase lead capacitors are 1.5pF to 10pF.

GND: The GND pins and exposed pad must be connected to the negative terminal of the input capacitors and soldered to the PCB in order to lower the thermal resistance.

$INTV_{CC}$: The $INTV_{CC}$ pin provides power to internal gate drivers and control circuits. $INTV_{CC}$ current will be supplied from BIAS if $V_{BIAS} > 3.1V$, otherwise current will be drawn from V_{IN1}. Decouple this pin to ground with at least a 1µF low ESR ceramic capacitor. Do not load the $INTV_{CC}$ pin with external circuitry.

NC: The NC pins have no internal connection. Float NC pins to increase fault tolerance or connect to ground to facilitate PCB layout.

PG1, PG2: The PG pins are the open-drain outputs of the internal power good comparators. Each channel's PG pin remains low until the respective FB pin is within ±10% of the final regulation voltage and there are no fault conditions.

RT: A resistor is tied between RT and ground to set the switching frequency.

SW1, SW2: The SW pins are the outputs of each channel's internal power switches. Connect these pins to the inductors and boost capacitors. SW nodes should be kept small on the PCB for good performance.

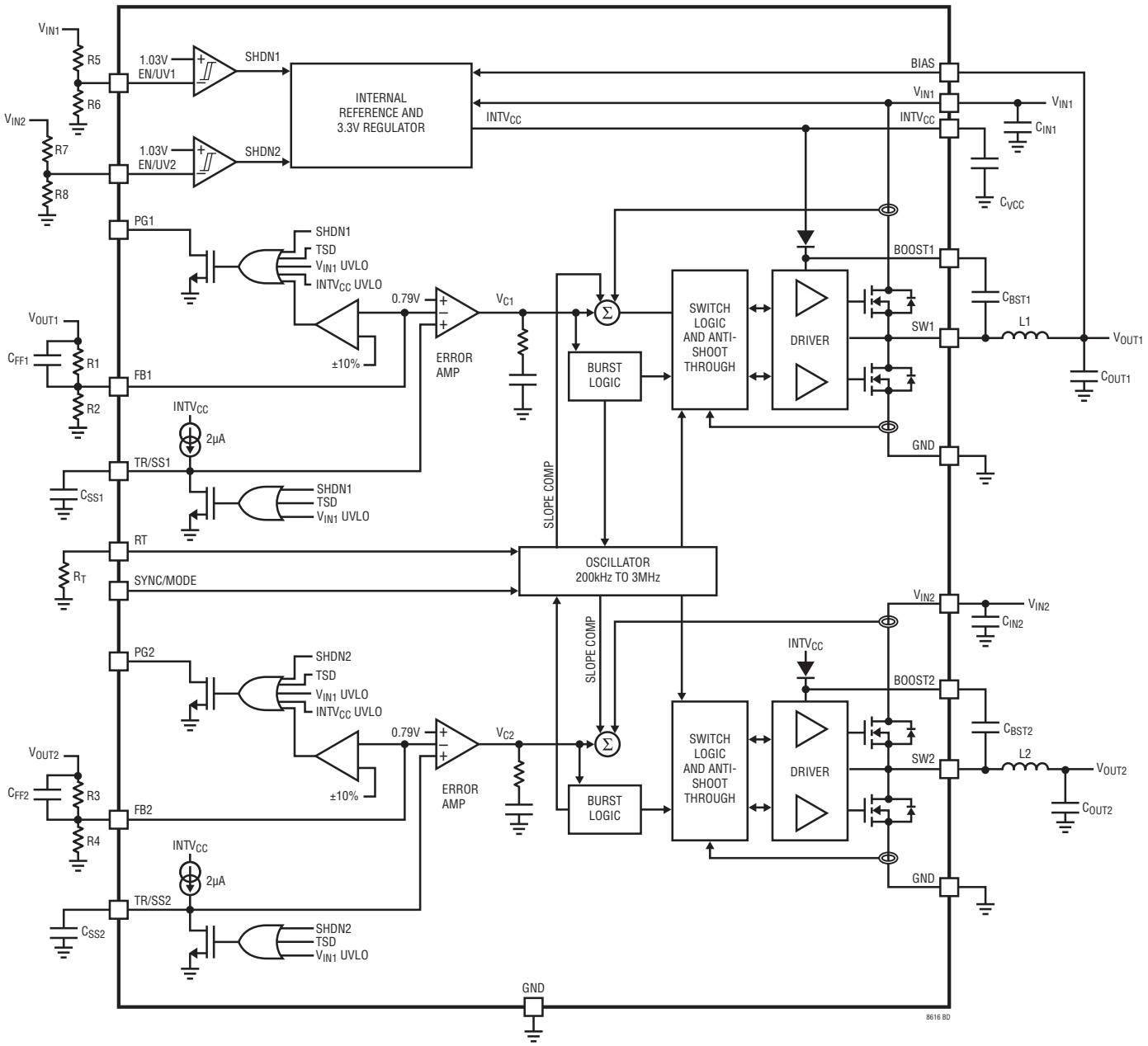
SYNC/MODE: Ground the SYNC/MODE pin for low ripple Burst Mode operation at low output loads. Tie to a clock source for synchronization to an external frequency. Apply a DC voltage of 2.4V or higher or tie to $INTV_{CC}$ for pulse-skipping mode. When in pulse-skipping mode, the I_Q will increase to several hundred µA. Channel 1 will align its positive switching edge to the positive edge of the external clock and channel 2 will align its positive switching edge to the negative external clock edge. Do not float this pin.

TR/SS1, TR/SS2: The TR/SS pins are used to soft-start the two channels, to allow one channel to track the other output, or to allow both channels to track another output. For tracking, tie a resistor divider to the TR/SS pin from the tracked output. For soft-start, tie a capacitor to TR/SS. Internal 2µA pull-up currents from $INTV_{CC}$ charge soft-start capacitors to create voltage ramps. A TR/SS voltage below 0.79V forces the LT8616 to regulate the corresponding FB pins to equal the TR/SS pin voltage. When TR/SS voltages are above 0.79V, the tracking function is disabled and the internal reference resumes control of the error amplifiers. TR/SS pins are individually pulled to ground with internal 250Ω MOSFETs during shutdown and fault conditions; use series resistors if driving from a low impedance output.

V_{IN1}: V_{IN1} supplies current to the LT8616's internal circuitry and to channel 1's topside power switch. This pin must be locally bypassed. Be sure to place the positive terminal of the input capacitor as close as possible to the pin, and the negative capacitor terminal as close as possible to the GND pins. V_{IN1} must be connected to 3.4V or above even if only channel 2 is in use.

V_{IN2}: V_{IN2} supplies current to internal channel 2's topside power switch. This pin must be locally bypassed. Be sure to place the positive terminal of the input capacitor as close as possible to the pin, and the negative capacitor terminal as close as possible to the GND pins. Please note V_{IN1} must be 3.4V or above to operate channel 2.

BLOCK DIAGRAM



OPERATION

Foreword

The LT8616 is a dual monolithic step down regulator. The two channels differ in maximum current and input range. The following sections describe the operation of channel 1 and common circuits. They will highlight channel 2 differences and interactions only when relevant. To simplify the application, both V_{IN1} and V_{IN2} are assumed to be connected to the same input supply. However, note that V_{IN1} must be greater than 3.4V for either channel to operate.

Operation

The LT8616 is a dual monolithic, constant frequency, peak current mode step-down DC/DC converter.

An oscillator, with frequency set using a resistor on the RT pin, turns on the internal top power switch at the beginning of each clock cycle. Current in the inductor then increases until the top switch current comparator trips and turns off the top power switch. The peak inductor current at which the top switch turns off is controlled by the voltage on the internal V_C node. The error amplifier servos the V_C node by comparing the voltage on the FB pin with an internal 0.790V reference. When the load current increases it causes a reduction in the feedback voltage relative to the reference, causing the error amplifier to raise the V_C voltage until the average inductor current matches the new load current. When the top power switch turns off, the synchronous power switch turns on until the next clock cycle begins or inductor current falls to zero. If overload conditions result in more than the valley current limit flowing through the bottom switch, the next clock cycle will be delayed until current returns to a safe level.

If either EN/UV pin is low, the corresponding channel is shut down. If both EN/UV pins are low, the LT8616 is fully shut down and draws 1.7µA from the input supply. When the EN/UV pins are above 1.03V, the corresponding switching regulators will become active. 1.3µA is supplied by V_{IN1} to common bias circuits for both channels.

Each channel can independently enter Burst Mode operation to optimize efficiency at light load. Between bursts, all circuitry associated with controlling the output switch is shut down, reducing the channel's contribution to input supply current. In a typical application, 6.5µA will be consumed from the input supply when regulating both channels with no load. Ground the SYNC/MODE pin for Burst Mode operation or apply a DC voltage above 2.4V to use pulse-skipping mode. If a clock is applied to the SYNC/MODE pin, both channels will synchronize to the external clock frequency and operate in pulse-skipping mode. While in pulse-skipping mode the oscillator operates continuously and SW transitions are aligned to the clock. During light loads, switch pulses are skipped to regulate the output and the quiescent current per channel will be several hundred µA.

To improve efficiency across all loads, supply current to internal circuitry can be sourced from the BIAS pin when biased at 3.1V or above. Otherwise, the internal circuitry will draw current exclusively from V_{IN1}. The BIAS pin should be connected to the lowest V_{OUT} programmed at 3.3V or above.

Comparators monitoring the FB pin voltage will pull the corresponding PG pin low if the output voltage varies more than ±10% (typical) from the regulation voltage or if a fault condition is present.

Tracking soft-start is implemented by providing constant current via the TR/SS pin to an external soft-start capacitor to generate a voltage ramp. FB voltage is regulated to the voltage at the TR/SS pin until it exceeds 0.790V; FB is then regulated to the 0.790V reference. Soft-start also reduces the valley current limit to avoid inrush current during start-up. The SS capacitor is reset during shutdown, V_{IN1} undervoltage, or thermal shutdown.

Channel 1 is designed for 1.5A load, whereas channel 2 is designed for 2.5A load. Channel 1 has a minimum V_{IN1} requirement of 3.4V, but channel 2 can operate with no minimum V_{IN2} provided that the minimum V_{IN1} has been satisfied.

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Achieving Ultralow Quiescent Current

To enhance efficiency at light loads, the LT8616 operates in low ripple Burst Mode operation, which keeps the output capacitor charged to the desired output voltage while minimizing the input quiescent current and output voltage ripple. 1.7µA is supplied by V_{IN1} to common bias circuits. In Burst Mode operation the LT8616 delivers single small pulses of current to the output capacitor followed by sleep periods where the output power is supplied by the output capacitor. While in sleep mode the LT8616 consumes 3µA.

As the output load decreases, the frequency of single current pulses decreases (see Figure 1a) and the percentage of time that the LT8616 is in sleep mode increases, resulting in much higher light load efficiency than for typical converters. By maximizing the time between pulses, the converter quiescent current approaches 6.5µA for a typical application when there is no output load. Therefore, to optimize the quiescent current performance at light loads, the current in the feedback resistor divider must be minimized as it appears to the output as load current.

While in Burst Mode operation the current limit of the top switch is approximately 400mA for channel 1 (600mA for channel 2) resulting in output voltage ripple shown in Figure 2. Increasing the output capacitance will decrease the output ripple. As load increases from zero the switching frequency will increase but only up to the switching frequency programmed by the resistor at the RT pin as shown in Figure 1a. The output load at which the LT8616 reaches the programmed frequency varies based on input voltage, output voltage, and inductor value.

For some applications it is desirable to select pulse-skipping mode to maintain full switching frequency at lower output load (see Figure 1b). See Pulse-Skipping Mode section.

FB Resistor Network

The output voltage is programmed with a resistor divider between the output and the FB pin (R1 to R2 for channel 1, R3 to R4 for channel 2). Choose the resistor values according to:

$$R1 = R2\left(\frac{V_{OUT1}}{0.790V} - 1\right) \quad (1)$$

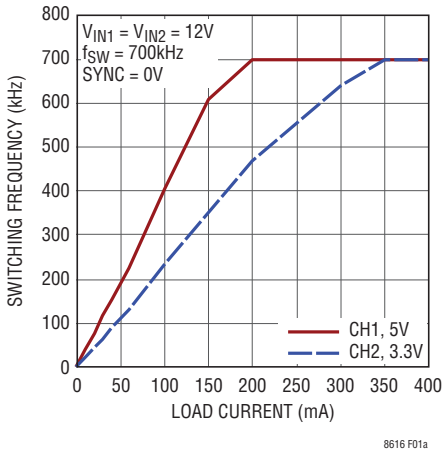

Figure 1a. Frequency vs Load in Burst Mode Operation

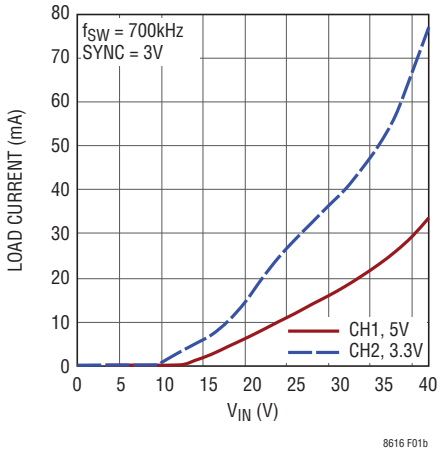

Figure 1b. Minimum Load for Full Frequency in Pulse-Skipping Mode

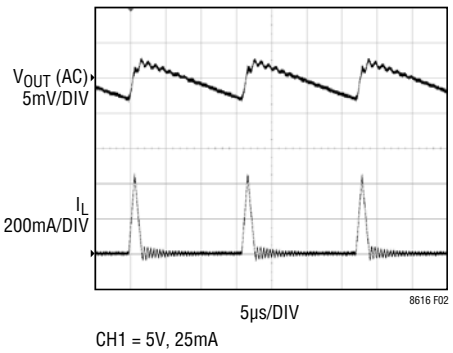

Figure 2. Burst Mode Operation

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Reference designators refer to the Block Diagram. 1% resistors are recommended to maintain output voltage accuracy.

If low input quiescent current and good light-load efficiency are desired, use large resistor values for the FB resistor divider. The current flowing in the divider acts as a load current and will increase the no-load input current to the converter, which is approximately:

$$I_Q = 3\mu A + \left(\frac{V_{OUT1}}{R1+R2}\right)\left(\frac{V_{OUT1}}{V_{IN1}}\right)\left(\frac{1}{\eta}\right) \quad (2)$$

where 3µA is the quiescent current, the second term is the current in the feedback divider reflected to the input of channel 1 operating at its light load efficiency η. For a 3.3V application with R1 = 1M and R2 = 316k, the feedback divider draws 2.5µA. With V_{IN} = 12V and η = 70%, this adds 1µA to the 3µA quiescent current resulting in 4µA no-load current from the 12V supply.

Substitute R1 and R2 with R3 and R4 in the above equation if V_{IN1} and V_{IN2} are connected to the same voltage.

Assuming channel 2 feedback divider contributes 2.5µA to the quiescent current, then the total quiescent current is 6.5µA.

For a typical FB resistor of 1MΩ, a 1.5pF to 10pF phase-lead capacitor should be connected from V_{OUT} to FB.

Setting the Switching Frequency

The LT8616 uses a constant frequency PWM architecture that can be programmed to switch from 200kHz to 3MHz by using a resistor tied from the RT pin to ground. Table 1 and Figure 3 show the necessary R_T value for a desired switching frequency.

The R_T resistor required for a desired switching frequency can be calculated using:

$$R_T = \frac{0.6}{f_{SW}^2} + \frac{42.6}{f_{SW}} - 6.1 \quad (3)$$

where R_T is in kΩ and f_{SW} is the desired switching frequency in MHz.

The two channels of the LT8616 operate 180° out of phase to avoid aligned switching edge noise and input current ripple.

Table 1. SW Frequency vs R_T Value

f_{SW} (MHz)	R_T kΩ)	f_{SW} (MHz)	R_T kΩ)
0.2	221	1.6	20.5
0.3	143	1.8	17.8
0.4	105	2.0	15.4
0.5	80.6	2.05	14.7
0.6	66.5	2.2	13.3
0.7	56.2	2.4	11.8
0.8	47.5	2.6	10.3
1.0	37.4	2.8	9.31
1.2	29.4	3.0	8.25
1.4	24.3		

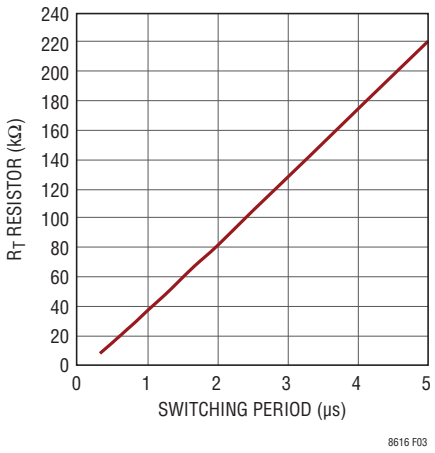

Figure 3. Switching Frequency vs R_T

Operating Frequency Selection and Trade-Offs

Selection of the operating frequency is a trade-off between efficiency, component size, and input voltage range. The advantage of high frequency operation is that smaller inductor and capacitor values may be used. The disadvantages are lower efficiency and a smaller input voltage range for full frequency operation.

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The highest switching frequency ($f_{SW(MAX)}$) for a given application can be calculated as follows:

$$f_{SW(MAX)} = \frac{V_{OUT} + V_{SW(BOT)}}{t_{ON(MIN)}\left(V_{IN} - V_{SW(TOP)} + V_{SW(BOT)}\right)} \quad (4)$$

where V_{IN} is the typical input voltage, V_{OUT} is the output voltage, $V_{SW(TOP)}$ and $V_{SW(BOT)}$ are the internal switch drops (~0.53V, ~0.38V, respectively at maximum load for channel 1 and ~0.78V, ~0.48V for channel 2) and $t_{ON(MIN)}$ is the minimum top switch on-time of 55ns (see the Electrical Characteristics). This equation shows that a lower switching frequency is necessary to accommodate a high V_{IN}/V_{OUT} ratio. Choose the lower frequency between channel 1 and 2.

For transient operation, V_{IN} may go as high as the absolute maximum rating of 42V regardless of the R_T value, however the LT8616 will reduce switching frequency on each channel independently as necessary to maintain control of inductor current to assure safe operation.

The LT8616 is capable of a maximum duty cycle of greater than 99%, and the V_{IN} to V_{OUT} dropout is limited by the $R_{DS(ON)}$ of the top switch. In this mode the channel that enters dropout skips switch cycles, resulting in a lower than programmed switching frequency.

For applications that cannot allow deviation from the programmed switching frequency at low V_{IN}/V_{OUT} ratios, use the following formula to set switching frequency:

$$V_{IN(MIN)} = \frac{V_{OUT} + V_{SW(BOT)}}{1 - f_{SW} \bullet t_{OFF(MIN)}} - V_{SW(BOT)} + V_{SW(TOP)} \quad (5)$$

where $V_{IN(MIN)}$ is the minimum input voltage without skipped cycles, V_{OUT} is the output voltage, $V_{SW(TOP)}$ and $V_{SW(BOT)}$ are the internal switch drops (~0.53V, ~0.38V, respectively at maximum load for channel 1 and ~0.78V, ~0.48V for channel 2), f_{SW} is the switching frequency (set by R_T), and $t_{OFF(MIN)}$ is the minimum switch off-time. Note that higher switching frequency will increase the minimum input voltage below which cycles will be dropped to achieve higher duty cycle.

Note there is no minimum V_{IN2} voltage requirement as it does not supply the internal common bias circuits, making channel 2 uniquely capable of operating from very low input voltages.

Inductor Selection and Maximum Output Current

The LT8616 is designed to minimize solution size by allowing the inductor to be chosen based on the output load requirements of the application. During overload or short-circuit conditions the LT8616 safely tolerates operation with a saturated inductor through the use of a high speed peak-current mode architecture.

A good first choice for the inductor value is:

$$L1 = \frac{V_{OUT1} + V_{SW1(BOT)}}{f_{SW}} \bullet 1.6 \quad (6a)$$

$$L2 = \frac{V_{OUT2} + V_{SW2(BOT)}}{f_{SW}} \quad (6b)$$

where f_{SW} is the switching frequency in MHz, V_{OUT} is the output voltage, $V_{SW(BOT)}$ is the bottom switch drop (~0.38V, ~0.48V) and L is the inductor value in µH. To avoid overheating and poor efficiency, an inductor must be chosen with an RMS current rating that is greater than the maximum expected output load of the application. In addition, the saturation current (typically labeled I_{SAT}) rating of the inductor must be higher than the load current plus 1/2 of in inductor ripple current:

$$I_{L(PEAK)} = I_{LOAD(MAX)} + \frac{1}{2}\Delta I_L \quad (7)$$

where ΔI_L is the inductor ripple current as calculated in equation 9 and $I_{LOAD(MAX)}$ is the maximum output load for a given application.

As a quick example, an application requiring 1A output should use an inductor with an RMS rating of greater than 1A and an I_{SAT} of greater than 1.3A. During long duration overload or short-circuit conditions, the inductor RMS rating requirement is greater to avoid overheating of the inductor. To keep the efficiency high, the series resistance (DCR) should be less than 0.04Ω, and the core material should be intended for high frequency applications.

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The LT8616 limits the peak switch current in order to protect the switches and the system from overload faults. The top switch current limit (I_{LIM}) is 4.2A at 0% duty cycle and decreases linearly to 2.9A at DC = 80% (channel 2 current limit are 5.5A at 0% duty cycle and 3.7A at DC = 80%). The inductor value must then be sufficient to supply the desired maximum output current ($I_{OUT(MAX)}$), which is a function of the switch current limit (I_{LIM}) and the ripple current.

$$I_{OUT(MAX)} = I_{LIM} - \frac{\Delta I_L}{2} \quad (8)$$

The peak-to-peak ripple current in the inductor can be calculated as follows:

$$\Delta I_L = \frac{V_{OUT}}{L \bullet f_{SW}} \bullet \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) \quad (9)$$

where f_{SW} is the switching frequency of the LT8616, and L is the value of the inductor. Therefore, the maximum output current that the LT8616 will deliver depends on the switch current limit, the inductor value, and the input and output voltages.

Each channel has a secondary valley current limit. After the top switch has turned off, the bottom switch carries the inductor current. If for any reason the inductor current is too high, the bottom switch will remain on, delaying the top switch turning on until the inductor current returns to a safe level. This level is specified as the valley Current Limit, and is independent of duty cycle. Maximum output current in the application circuit is limited to this valley current plus one half of the inductor ripple current.

In most cases current limit is enforced by the top switch. The bottom switch limit controls the inductor current when the minimum on-time condition is violated (high input voltage, high frequency or saturated inductor).

The bottom switch current limit is designed to avoid any contribution to the maximum rated current of the LT8616.

The optimum inductor for a given application may differ from the one indicated by this design guide. A larger value inductor provides a higher maximum load current and reduces the output voltage ripple. For applications requiring smaller load currents, the value of the inductor may be lower and the LT8616 may operate with higher ripple current. This allows use of a physically smaller inductor, or one with a lower DCR resulting in higher efficiency. Be aware that low inductance may result in discontinuous mode operation, which further reduces maximum load current.

For more information about maximum output current and discontinuous operation, see Linear Technology's Application Note 44.

Finally, for duty cycles greater than 50% ($V_{OUT}/V_{IN} > 0.5$), a minimum inductance is required to avoid sub-harmonic oscillation. See Application Note 19.

Table 2. Inductor Manufacturers

VENDOR	URL
Coilcraft	www.coilcraft.com
Sumida	www.sumida.com
Toko	www.toko.com
Würth Elektronik	www.we-online.com
Vishay	www.vishay.com

Input Capacitor

Bypass the input of the LT8616 circuit with a ceramic capacitor of X7R or X5R type placed as close as possible to the V_{IN} and GND pins. Y5V types have poor performance over temperature and applied voltage, and should not be used. A 2.2µF to 10µF ceramic capacitor is adequate to bypass the LT8616 and will easily handle the ripple current. Note that larger input capacitance is required when a lower switching frequency is used. If the input power source has high impedance, or there is significant inductance due to long wires or cables, additional bulk capacitance may be necessary. This can be provided with a low performance electrolytic capacitor.

Step-down regulators draw current from the input supply in pulses with very fast rise and fall times. The input capacitor is required to reduce the resulting voltage ripple at the LT8616 and to force this very high frequency

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switching current into a tight local loop, minimizing EMI. A 2.2µF capacitor is capable of this task, but only if it is placed close to the LT8616 (see the PCB Layout section). A second precaution regarding the ceramic input capacitor concerns the maximum input voltage rating of the LT8616. A ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the LT8616 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT8616's voltage rating. This situation is easily avoided (see Linear Technology Application Note 88).

Output Capacitor and Output Ripple

The output capacitor has two essential functions. Along with the inductor, it filters the square wave generated by the LT8616 to produce the DC output. In this role it determines the output voltage ripple, thus, low impedance at the switching frequency is important. The second function is to store energy in order to satisfy transient loads and stabilize the LT8616's control loop. Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. For good starting values, see the Typical Applications section.

Use X5R or X7R types. This choice will provide low output ripple and good transient response. Transient performance can be improved with a higher value output capacitor and the addition of a feed forward capacitor placed between V_{OUT} and FB. Increasing the output capacitance will also decrease the output voltage ripple. A lower value of output capacitor can be used to save space and cost but transient performance will suffer and may cause loop instability. See the Typical Applications in this data sheet for suggested capacitor values.

When choosing a capacitor, special attention should be given to the data sheet to calculate the effective capacitance under the relevant operating conditions of voltage bias and temperature. A physically larger capacitor or one with a higher voltage rating may be required.

Ceramic Capacitors

Ceramic capacitors are small, robust and have very low ESR. However, ceramic capacitors can cause problems when used with the LT8616 due to their piezoelectric nature. When in Burst Mode operation, the LT8616's switching frequency depends on the load current, and at very light loads the LT8616 can excite the ceramic capacitor at audio frequencies, generating audible noise. Since the LT8616 operates at a lower current limit during Burst Mode operation, the noise is typically very quiet to a casual ear. If this is unacceptable, use a high performance tantalum or electrolytic capacitor at the output. Low noise ceramic capacitors are also available.

Table 3. Ceramic Capacitor Manufacturers

MANUFACTURER	WEB
Taiyo Yuden	www.t-yuden.com
AVX	www.avxcorp.com
Murata	www.murata.com
TDK	www.tdk.com

Enable Pin

The LT8616 is in shutdown when both EN/UV pins are low and active when either pin is high. The rising threshold of the EN/UV comparator is 1.03V, with 50mV of hysteresis. The EN/UV pins can be tied to V_{IN} if the shutdown feature is not used, or tied to a logic level if shutdown control is required.

Adding a resistor divider from V_{IN} to EN/UV programs the LT8616 to operate only when V_{IN} is above a desired voltage (see the Block Diagram). Typically, this threshold, $V_{IN(EN)}$, is used in situations where the input supply is current limited, or has a relatively high source resistance. A switching regulator draws constant power from the source, so source current increases as source voltage drops. This looks like a negative resistance load to the source and can cause the source to current limit or latch low under low

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source voltage conditions. The $V_{IN(EN)}$ threshold prevents the regulator from operating at source voltages where the problems might occur. This threshold can be adjusted by setting the values R5 and R6 (R7, R8 for channel 2) such that they satisfy the following equation:

$$R5 = R6\left(\frac{V_{IN1(EN)}}{1.03V} - 1\right) \quad (10)$$

where the corresponding channel will remain off until V_{IN} is above $V_{IN(EN)}$. Due to the comparator's hysteresis, switching will not stop until the input falls slightly below $V_{IN(EN)}$.

When operating in Burst Mode operation for light load currents, the current through the $V_{IN(EN)}$ resistor network can easily be greater than the supply current consumed by the LT8616. Therefore, the $V_{IN(EN)}$ resistors should be large to minimize their effect on efficiency at low loads.

$INTV_{CC}$ Regulator

An internal low dropout (LDO) regulator produces the 3.4V supply from V_{IN1} that powers the drivers and the internal bias circuitry. For this reason, V_{IN1} must be present and valid to use either channel. The $INTV_{CC}$ pin supplies current for the LT8616's circuitry and must be bypassed to ground with a 1µF ceramic capacitor. Good bypassing is necessary to supply the high transient currents required by the power MOSFET gate drivers. To improve efficiency, the internal LDO will draw current from the BIAS pin when the BIAS pin is at 3.1V or higher. Typically, the BIAS pin is tied to the lowest output or external supply above 3.1V. If BIAS is connected to a supply other than V_{OUT}, bypass it with a local ceramic capacitor. If the BIAS pin is below 3.0V, the internal LDO will consume current from V_{IN1}.

Applications with high input voltage and high switching frequency where the internal LDO pulls current from V_{IN1} will increase die temperature because of the higher power dissipation across the LDO. Do not connect an external load to the $INTV_{CC}$ pin.

Output Voltage Tracking and Soft-Start

The LT8616 allows the user to program its output voltage ramp rate with the TR/SS pin. An internal 2µA current pulls up the TR/SS pin to $INTV_{CC}$. Putting an external capacitor on TR/SS enables soft starting the output to prevent current surge on the input supply. During the soft-start ramp the output voltage will proportionally track the TR/SS pin voltage. For output tracking applications, TR/SS can be externally driven by another voltage source. From 0V to 0.790V, the TR/SS voltage will override the internal 0.790V reference input to the error amplifier, thus regulating the FB pin voltage to that of TR/SS pin (figure 4). When TR/SS is above 0.790V, tracking is disabled and the feedback voltage will regulate to the internal reference voltage. The TR/SS pin may be left floating if the function is not needed. Note the LT8616 will not discharge the output to regulate to a lower TR/SS voltage (figure 5).

An active pull-down circuit is connected to the TR/SS pin which will discharge the external soft-start capacitor in the case of fault conditions and restart the ramp when the faults are cleared. Fault conditions that clear the soft-start capacitor are the corresponding EN/UV pin below 0.92V, V_{IN1} voltage falling too low, or thermal shutdown.

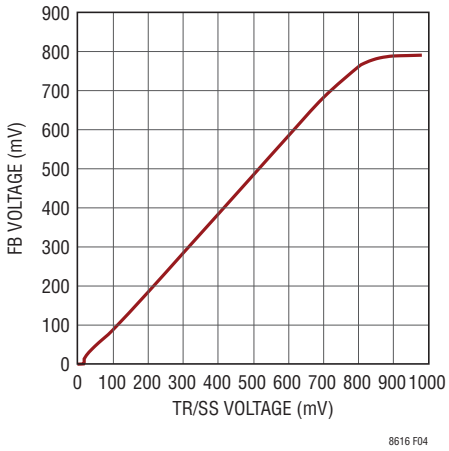

Figure 4. FB Tracking TR/SS Voltage Until 0.790V

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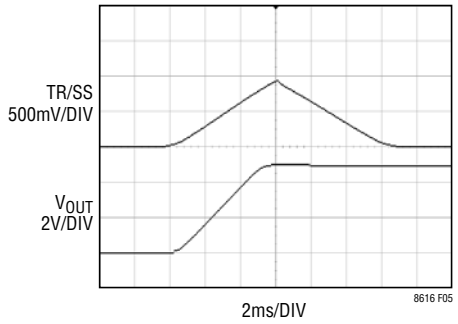


Figure 5. TR/SS Does Not Discharge V_{OUT}

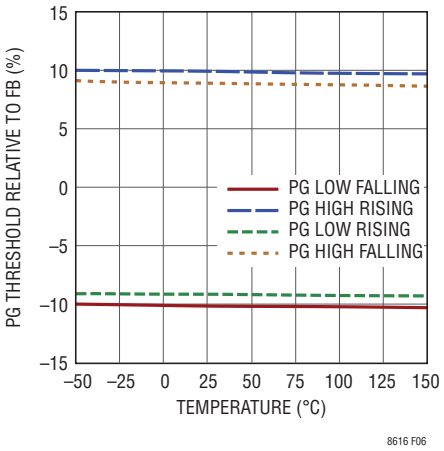


Figure 6. Power-Good Thresholds

Output Power Good

When the LT8616's output voltage is within the ±10% window of the regulation point, which is a FB voltage in the range of 0.72V to 0.88V (typical), the output voltage is considered good and the open-drain PG pin goes high impedance and is typically pulled high with an external resistor. Otherwise, the internal pull-down device will pull the PG pin low. To prevent glitching, both the upper and lower thresholds include 1% of hysteresis. See figure 6.

The PG pin is also actively pulled low during several fault conditions: corresponding EN/UV pin below 0.92V, $INTV_{CC}$ voltage falling too low, V_{IN1} UVLO, or thermal shutdown.

Synchronization

To select low ripple Burst Mode operation, tie the SYNC/MODE pin below 0.4V (this can be ground or a logic low output). To select pulse skip mode, tie the SYNC/MODE pin above 2.4V (SYNC/MODE can be tied to $INTV_{CC}$). To synchronize the LT8616 oscillator to an external frequency connect a square wave (with 20% to 80% duty cycle) to the SYNC/MODE pin. The square wave amplitude should have valleys that are below 0.4V and peaks above 2.4V (up to 6V).

Channel 1 will synchronize its positive switch edge transitions to the positive edge of the SYNC signal, and channel 2 will synchronize to the negative edge of the SYNC signal.

The LT8616 will not enter Burst Mode operation at low output loads while synchronized to an external clock, but instead will pulse skip to maintain regulation. The LT8616 may be synchronized over a 250kHz to 3MHz range. The R_T resistor should be chosen to set the LT8616 switching frequency to 20% below the lowest synchronization input. For example, if the synchronization signal will be 500kHz and higher, the R_T should be selected for 400kHz.

The slope compensation is set by the R_T value, while the minimum slope compensation required to avoid subharmonic oscillations is established by the inductor size, input voltage, and output voltage. Since the synchronization frequency will not change the slopes of the inductor current waveform, if the inductor is large enough to avoid subharmonic oscillations at the frequency set by R_T, then the slope compensation will be sufficient for all synchronization frequencies.

The duty cycle of the SYNC signal can be used to set the relative phasing of the two channels for minimizing input ripple.

The LT8616 does not operate in forced continuous mode regardless of the SYNC signal. Never leave the SYNC/MODE pin floating.

APPLICATIONS INFORMATION

Pulse-Skipping Mode

Pulse-skipping mode is activated by applying logic high (above 2.4V) or an external clock to the SYNC/MODE pin.

While in pulse-skipping mode, the oscillator operates continuously and SW transitions are aligned to the clock. During light loads, switch pulses are skipped to regulate the output and the quiescent current per channel will be several hundred µA. Full switching frequency is reached at lower output load than in Burst Mode operation.

Shorted and Reversed Input Protection

The LT8616 will tolerate a shorted output. The bottom switch current is monitored such that if inductor current is beyond safe levels, turn on of the top switch will be delayed until the inductor current falls to safe levels. A fault condition of one channel will not affect the operation of the other.

There is another situation to consider in systems where the output will be held high when the input to the LT8616 is absent. This may occur in battery charging applications or in battery-backup systems where a battery or some other supply is OR-ed with channel 1's output. If the V_{IN1} pin is allowed to float and either EN/UV pin is held high (either by a logic signal or because it is tied to V_{IN1}), then the LT8616's internal circuitry will pull its quiescent current through its SW1 pin. This is acceptable if the system can tolerate current draw in this state. If both EN/UV pins are grounded the SW1 pin current will drop to near 1µA. However, if the V_{IN1} pin is grounded while channel 1 output is held high, regardless of EN/UV1, parasitic body diodes inside the LT8616 can pull current from the output through the SW1 pin and the V_{IN1} pin, damaging the IC

V_{IN2} is not connected to the shared internal supply and will not draw any current if left floating. If both V_{IN1} and V_{IN2} are floating, regardless of EN/UV pins states, no-load will be present at the output of channel 2. However, if the V_{IN2} pin is grounded while channel 2 output is held high, parasitic body diodes inside the LT8616 can pull current from the output through the SW2 pin and the V_{IN2} pin, damaging the IC

Figure 7 shows a connection of the V_{IN} and EN/UV pins that will allow the LT8616 to run only when the input voltage is present and that protects against a shorted or reversed input.

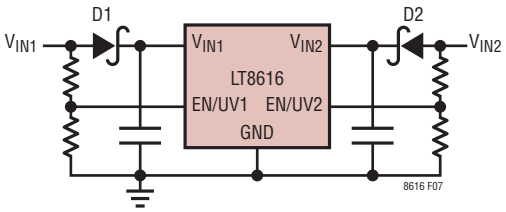


Figure 7. Reverse V_{IN} Protection for Two Independent Input Voltages

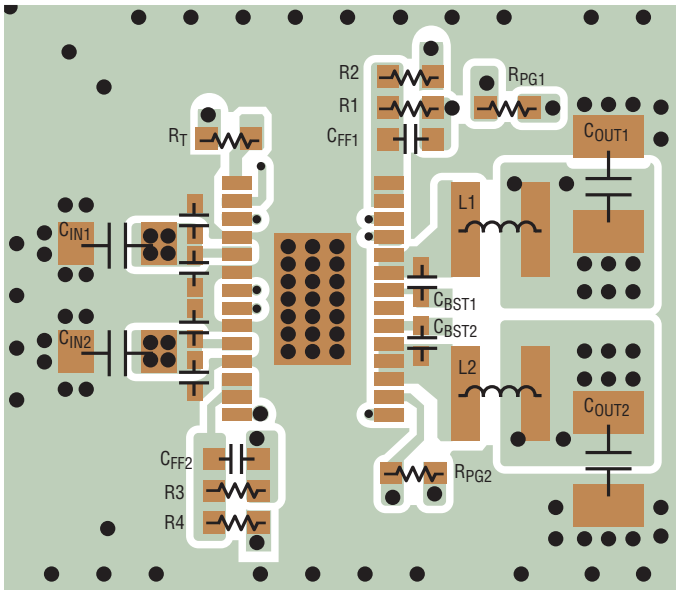
PCB Layout

For proper operation and minimum EMI, care must be taken during printed circuit board layout. Figure 8 shows the recommended component placement with trace, ground plane and via locations. Note that large, switched currents flow in the LT8616's V_{IN} pins, GND pins, and the input capacitors (C_{IN1} and C_{IN2}). The loop formed by the input capacitor should be as small as possible. When using a physically large input capacitor the resulting loop may become too large in which case using a small case/value capacitor placed close to the V_{IN} and GND pins plus a larger capacitor further away is preferred. These components, along with the inductor and output capacitor, should be placed on the same side of the circuit board, and their connections should be made on that layer. Place a local, unbroken ground plane under the application circuit on the layer closest to the surface layer. The SW and BOOST nodes should be as small as possible. Finally, keep the FB and R_T nodes small so that the ground traces will shield them from the SW and BOOST nodes. The exposed pad acts as a heat sink and is connected electrically to ground. The exposed pad of the TSSOP package is the only electrical connection to ground and must be soldered to ground. To keep thermal resistance low, extend the ground plane as much as possible, and add thermal vias under and near the LT8616 to additional ground planes within the circuit board and on the bottom side.

APPLICATIONS INFORMATION

High Temperature Considerations

For higher ambient temperatures, care should be taken in the layout of the PCB to ensure good heat sinking of the LT8616. The exposed pad on the bottom of the package must be soldered to a ground plane. This ground should be tied to large copper layers below with thermal vias; these layers will spread heat dissipated by the LT8616. Placing additional vias can reduce thermal resistance further. The maximum load current should be derated as the ambient temperature approaches the maximum junction rating. Power dissipation within the LT8616 can be estimated by calculating the total power loss from an efficiency measurement and subtracting the inductor loss. The die temperature is calculated by multiplying the LT8616 power dissipation by the thermal resistance from junction to ambient. The LT8616 will stop switching and indicate a fault condition if safe junction temperature is exceeded.



NOTE: C_{VCC} IS BELOW THE PACKAGE ON THE BACK SIDE

Figure 8. Recommended Layout

Open Pins and Shorting Neighboring Pins

The LT8616 in TSSOP package is designed to tolerate faults to each pin. Output voltages will stay at or below regulation if adjacent pins are shorted or a pin is left floating. See Table 4 for pin fault behavior when the LT8616 in the TSSOP package is connected in the application shown on Figure 9.

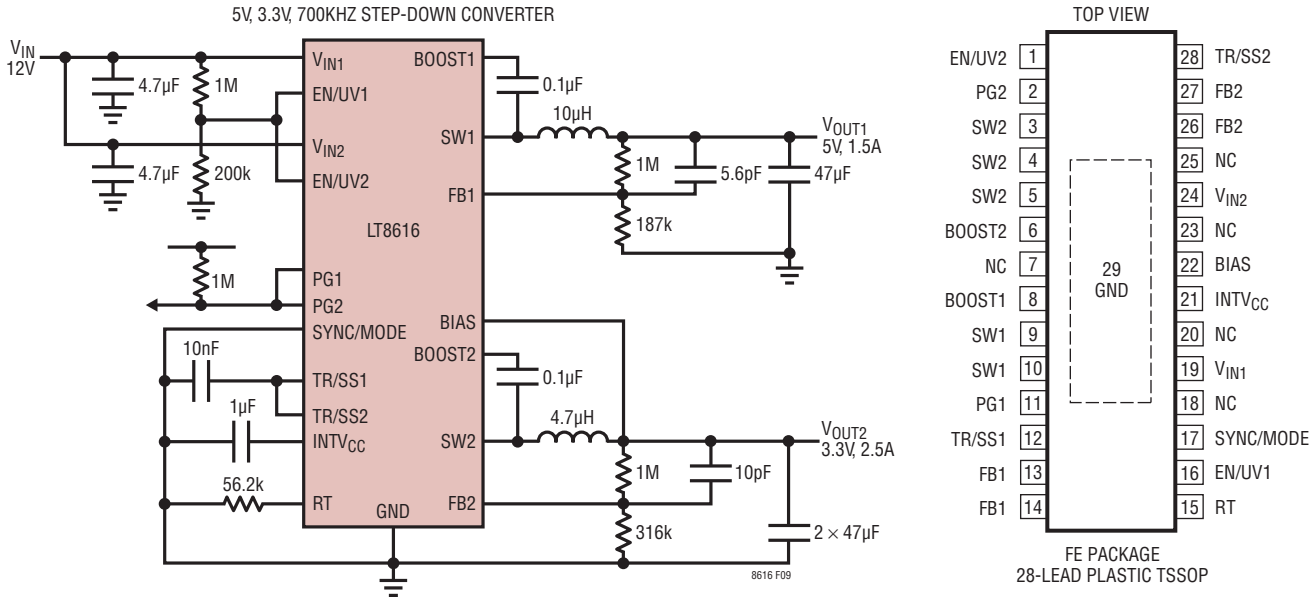


Figure 9. See Table 4 for Open and Short Pin Behavior of this Application in the TSSOP Package

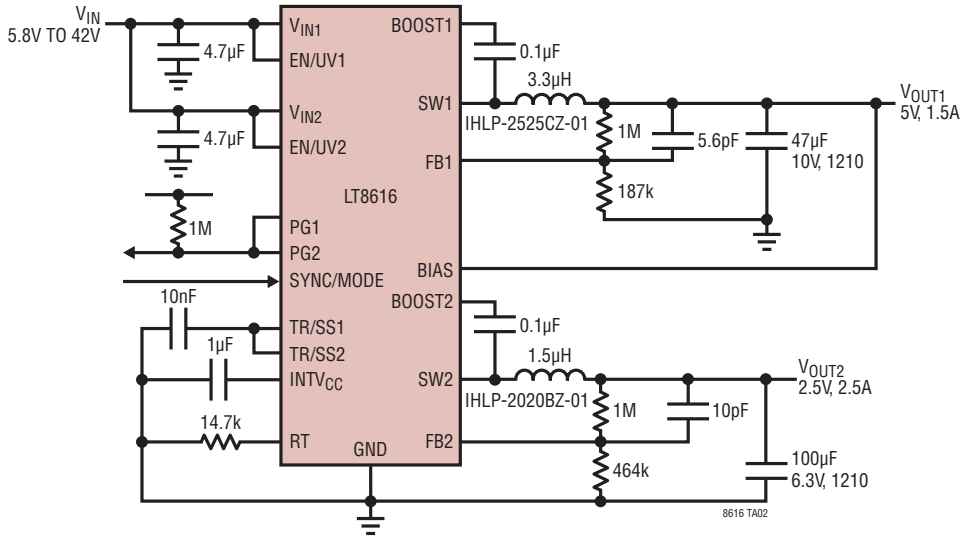
APPLICATIONS INFORMATION

Table 4. LT8616xFE Pin Fault Behavior For Circuit In Figure 9

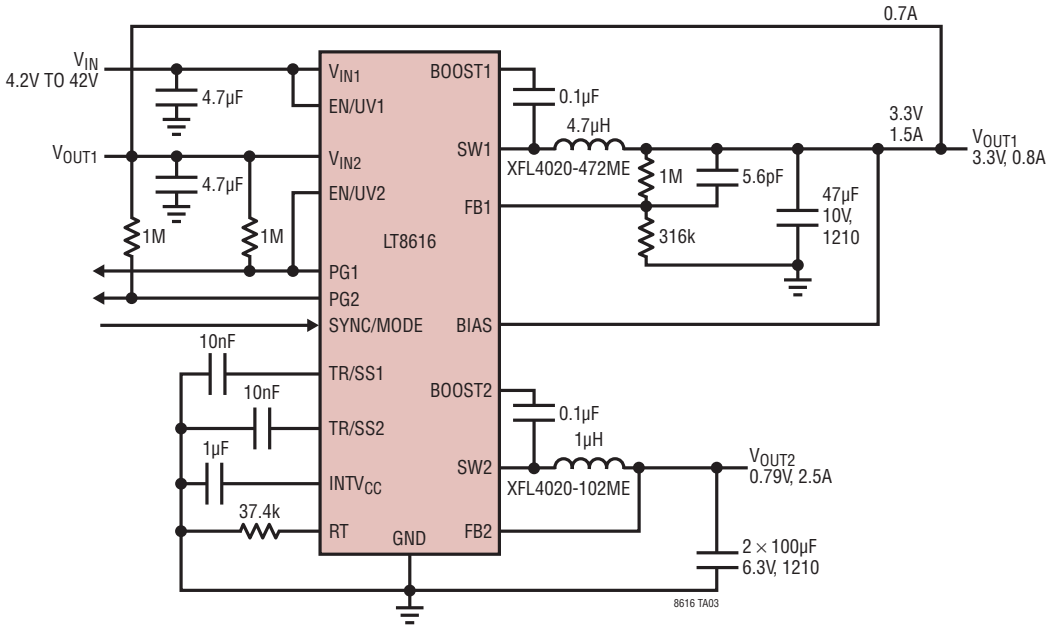
LT8616	Pin	Float	Short to Next Pin
EN/UV2	1	Part May Be On or Off	Part May Be On or Off
PG2	2	No Change	No Change
SW2	3	No Change	No Change
SW2	4	No Change	No Change
SW2	5	No Change	OUT2 Below Regulation
BOOST2	6	OUT2 Below Regulation	No Change
NC	7	No Change	No Change
BOOST1	8	OUT1 Below Regulation	OUT1 Below Regulation
SW1	9	No Change	No Change
SW1	10	No Change	No Change
PG1	11	No Change	No Change
TR/SS1	12	No Change	No Change
FB1	13	No Change	OUT1 Below Regulation
FB1	14	No Change	
RT	15	Switching Frequency Reduces	CH1, CH2 Off
EN/UV1	16	Part May Be On or Off	CH1, CH2 Off
SYNC/MODE	17	No Change	No Change
NC	18	No Change	No Change
V_{IN1}	19	CH1, CH2 Off	No Change
NC	20	No Change	No Change
$INTV_{CC}$	21	OUT1, OUT2 Below Regulation	No Change
BIAS	22	No Change	No Change
NC	23	No Change	No Change
V_{IN2}	24	CH2 Off	No Change
NC	25	No Change	No Change
FB2	26	No Change	No Change
FB2	27	No Change	OUT2 Below Regulation
TR/SS2	28	No Change	

TYPICAL APPLICATIONS

5V, 2.5V, 2.05MHz Step-Down Converter



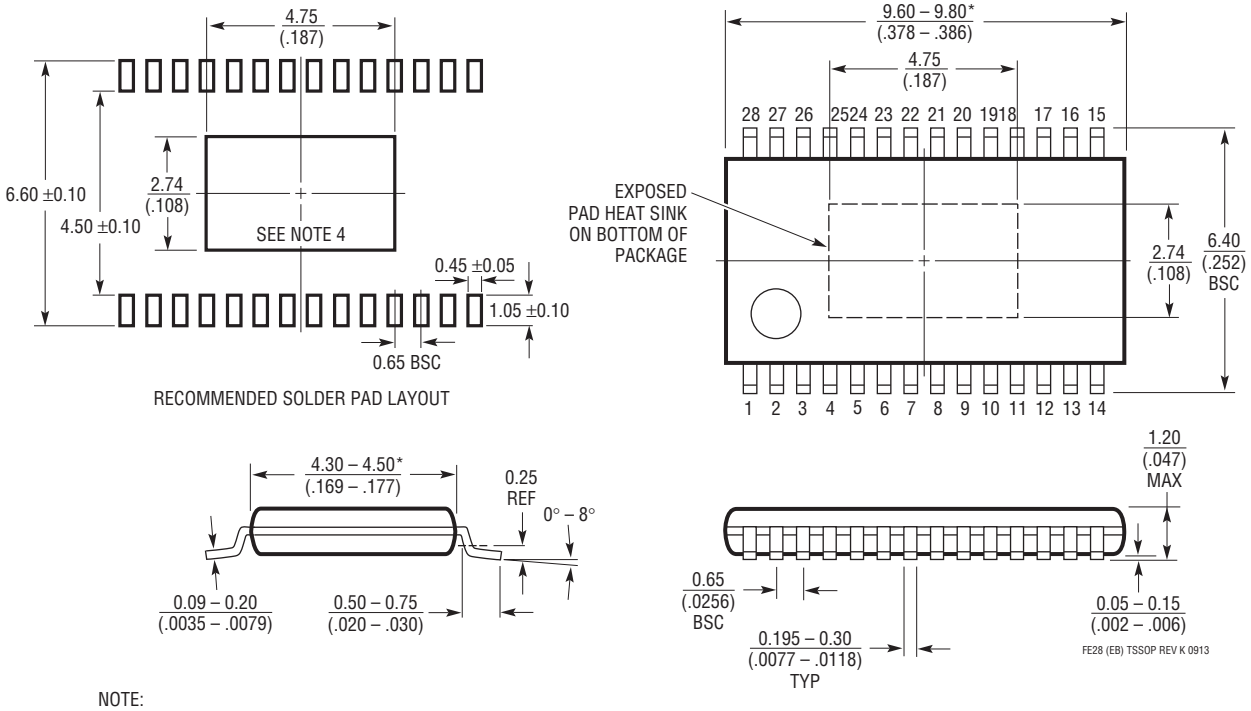
3.3V, 0.79V, 1MHz 2-Stage Step-Down Converter, Sequenced Start-Up



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LT8616#packaging for the most recent package drawings.

FE Package
28-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev K)
Exposed Pad Variation EB



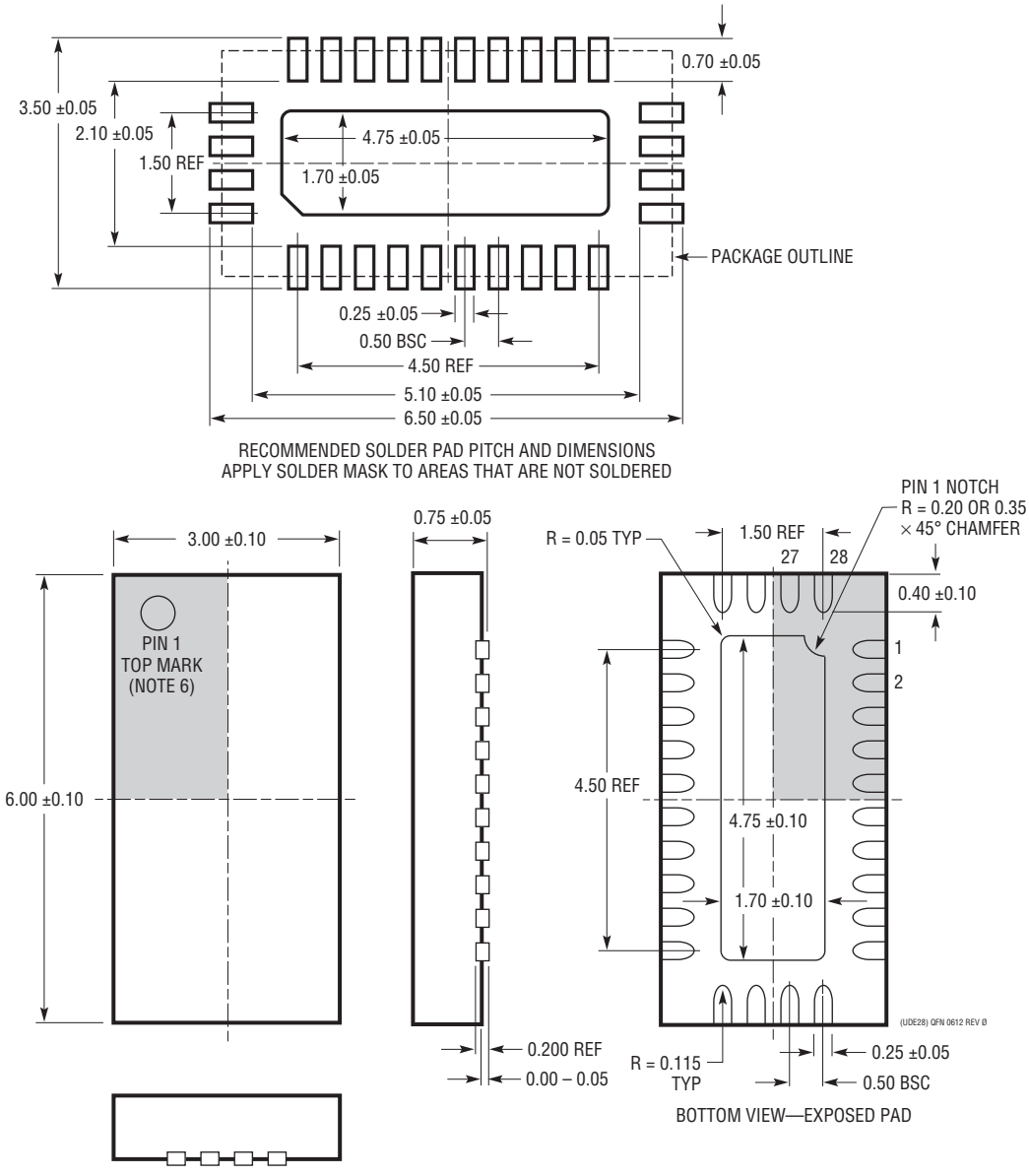
NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LT8616#packaging for the most recent package drawings.

UDE Package
28-Lead Plastic QFN (3mm × 6mm)
(Reference LTC DWG # 05-08-1926 Rev Ø)



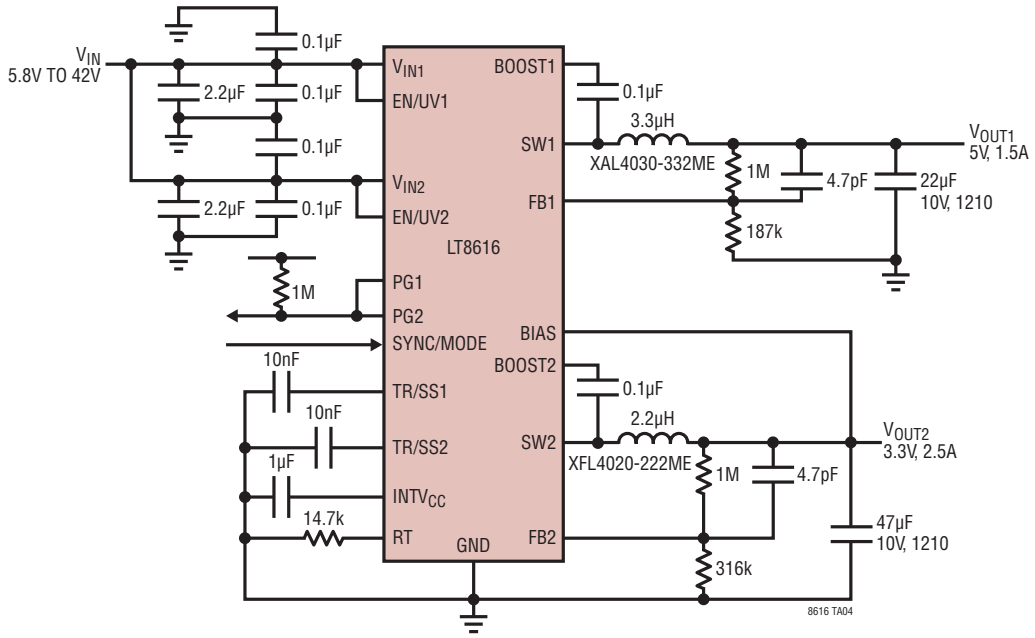
NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	10/16	Added 3mm × 6mm QFN package option.	1, 2, 24

TYPICAL APPLICATION

5V, 3.3V, 2.05MHz Step-Down Converter



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT8609	42V, 2A, 95% Efficiency, 2.2MHz Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 2.5µA	$V_{IN(MIN)}$ = 3V, $V_{IN(MAX)}$ = 42V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 2.5µA, I_{SD} = <1µA, MSOP-10E Package
LT8610A/AB	42V, 3.5A, 96% Efficiency, 2.2MHz Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 2.5µA	$V_{IN(MIN)}$ = 3.4V, $V_{IN(MAX)}$ = 42V, $V_{OUT(MIN)}$ = 0.97V, I_Q = 2.5µA, I_{SD} = <1µA, MSOP-10E Package
LT8610AC	42V, 3.5A, 96% Efficiency, 2.2MHz Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 2.5µA	$V_{IN(MIN)}$ = 3V, $V_{IN(MAX)}$ = 42V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 2.5µA, I_{SD} = <1µA, MSOP-10E Package
LT8610	42V, 2.5A, 96% Efficiency, 2.2MHz Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 2.5µA	$V_{IN(MIN)}$ = 3.4V, $V_{IN(MAX)}$ = 42V, $V_{OUT(MIN)}$ = 0.97V, I_Q = 2.5µA, I_{SD} = <1µA, MSOP-10E Package
LT8611	42V, 2.5A, 96% Efficiency, 2.2MHz Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 2.5µA and Input/Output Current Limit/Monitor	$V_{IN(MIN)}$ = 3.4V, $V_{IN(MAX)}$ = 42V, $V_{OUT(MIN)}$ = 0.97V, I_Q = 2.5µA, I_{SD} = <1µA, 3 × 5 QFN-24 Package
LT8620	65V, 2.5A, 96% Efficiency, 2.2MHz Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 2.5µA	$V_{IN(MIN)}$ = 3.4V, $V_{IN(MAX)}$ = 65V, $V_{OUT(MIN)}$ = 0.97V, I_Q = 2.5µA, I_{SD} = <1µA, 3 × 5 QFN-24 Package
LT8614	42V, 4A, 96% Efficiency, 2.2MHz Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 2.5µA	$V_{IN(MIN)}$ = 3.4V, $V_{IN(MAX)}$ = 42V, $V_{OUT(MIN)}$ = 0.97V, I_Q = 2.5µA, I_{SD} = <1µA, 3 × 5 QFN-18 Package
LT8612	42V, 6A, 96% Efficiency, 2.2MHz Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 2.5µA	$V_{IN(MIN)}$ = 3.4V, $V_{IN(MAX)}$ = 42V, $V_{OUT(MIN)}$ = 0.97V, I_Q = 3.0µA, I_{SD} = <1µA, 3 × 6 QFN-28 Package
LT8640	42V, 6A, 96% Efficiency, 3MHz Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 2.5µA	$V_{IN(MIN)}$ = 3.4V, $V_{IN(MAX)}$ = 42V, $V_{OUT(MIN)}$ = 0.97V, I_Q = 2.5µA, I_{SD} = <1µA, 3 × 4 QFN-18 Package
LT8602	42V, Quad Output (2.5A+1.5A+1.5A+1.5A) 95% Efficiency, 2.2MHz Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 25µA	$V_{IN(MIN)}$ = 3V, $V_{IN(MAX)}$ = 42V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 25µA, I_{SD} = <1µA, 6 × 6 QFN-40 Package

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