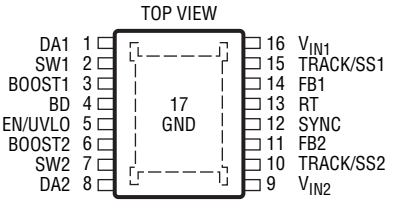
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} (Notes 7, 8) ..... –0.3V to 80V
BOOST 80V
EN/UVLO (Note 7) 80V
BOOST above SW 30V
EN/UVLO above V_{IN1} 6V
RT, SYNC 6V
TRACK/SS, FB 5V
BD 20V
Operating Junction Temperature Range (Note 2)
LT3988E ..... –40°C to 125°C
LT3988I ..... –40°C to 125°C
LT3988H ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



MSE PACKAGE
16-LEAD PLASTIC MSOP
θ_{JA} = 40°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE*
LT3988EMSE#PBF	LT3988EMSE#TRPBF	3988	16-Lead Plastic MSOP	–40°C to 125°C
LT3988IMSE#PBF	LT3988IMSE#TRPBF	3988	16-Lead Plastic MSOP	–40°C to 125°C
LT3988HMSE#PBF	LT3988HMSE#TRPBF	3988	16-Lead Plastic MSOP	–40°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. $V_{IN1/2}$ = 12V, unless otherwise noted. (Notes 2, 5, 6)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN1} Undervoltage Lockout (Note 3)	V_{IN1} Rising	●		3.9	4.1	V
V_{IN1} Undervoltage Lockout Hysteresis				260		mV
V_{IN1} Overvoltage Lockout (Note 3)	V_{IN1} Rising	●	60	64	66	V
V_{IN1} Overvoltage Lockout Hysteresis				2.1		V
V_{IN2} Undervoltage Lockout (Note 3)	V_{IN2} Rising, V_{IN1} = 4.1V	●	2	2.6	3.1	V
V_{IN2} Undervoltage Lockout Hysteresis				135		mV
EN/UVLO Input Current	$V_{EN/UVLO}$ = 1.2V		–0.5		0.5	µA
EN/UVLO Enable Threshold			300	500		mV
EN/UVLO Undervoltage Threshold	$V_{EN/UVLO}$ = Rising	●	1.1	1.2	1.3	V
EN/UVLO Undervoltage Threshold Hysteresis				120		mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN1}/V_{IN2} = 12V, unless otherwise noted. (Notes 2, 5, 6)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN1} Quiescent Current	V_{FB1} = 0.9V, V_{BD} = 0V			2.7	4.5	mA
V_{IN1} Quiescent Current	V_{FB1} = 0.9V, V_{BD} = 5V			1.6	3	mA
V_{IN2} Quiescent Current	V_{FB2} = 0.9V, V_{BD} = 5V			250	1000	µA
BD Pin Current	V_{BD} = 0V			–8	–30	µA
BD Pin Quiescent Current	V_{BD} = 5V			1.1	2.2	mA
Shutdown Current (I_{VIN1}+I_{VIN2})	$V_{EN/UVLO} \leq$ 0.3V			0.1	1	µA
FB Voltage		 ●	0.74 0.735	0.75 0.75	0.76 0.765	V V
FB Pin Bias Current	V_{FB} = 0.75V	●		–5	–100	nA
FB Line Voltage Regulation	5V < V_{IN} < 60V			0.01		%/V
Switching Frequency	R_T = 40.2k	●	0.9	1	1.1	MHz
Switching Frequency	R_T = 200k			250		kHz
Switching Frequency	R_T = 14.7k			2.15		MHz
Switching Phase, SW1 to SW2	R_T = 40.2k		150	180	210	Deg
DA Comparator Current Threshold		●	1.1	1.32	1.58	A
Switch V_{SAT}	I_{SW} = 1A			850		mV
Switch Current Limit (Note 4)	Duty Cycle = 35%		1.4	1.87	2.25	A
Switch Leakage Current				0.01	1	µA
Minimum Boost Voltage				2	2.5	V
Boost Pin Current	I_{SW} = 1A			20	50	mA
Boost Diode Forward Voltage	I_{BD} = 50mA			0.7	0.9	V
Boost Diode Leakage Current	V_R = 5V			0.1	5	µA
TRACK/SS Pin Current	$V_{TRACK/SS}$ = 1V		–0.8	–1.3	–2.2	µA
SYNC Input High Voltage	V_{IH}	●	1.5			V
SYNC Input Low Voltage	V_{IL}	●			0.4	V
SYNC Input Frequency			0.25		2.5	MHz
SYNC Pin Input Current	V_{SYNC} = 1.5V			0.3		µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3988E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3988I is guaranteed over the full –40°C to 125°C operating junction temperature range. The LT3988H is guaranteed over the full –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

Note 3: Undervoltage lockout occurs when V_{IN} is lower than the undervoltage threshold. Overvoltage lockout occurs when V_{IN} exceeds the threshold voltage. See Applications Information.

Note 4: Current limit is guaranteed by design and/or correlation to static test. Slope compensation reduces current at higher duty cycles.

Note 5: Polarity specification for all currents into pins is positive. All voltages are referenced to GND unless otherwise specified.

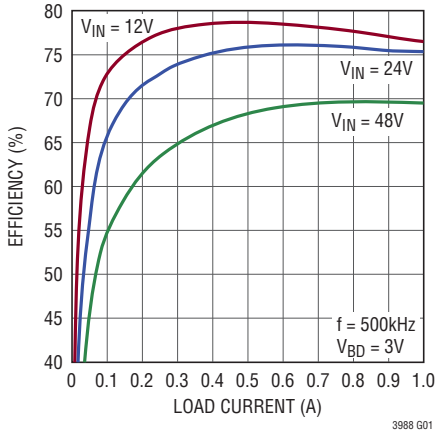
Note 6: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed the maximum operating junction temperature when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 7: Absolute Maximum Voltage at V_{IN} and EN/UVLO is 80V for nonrepetitive 1 second transients, and 60V for continuous operation.

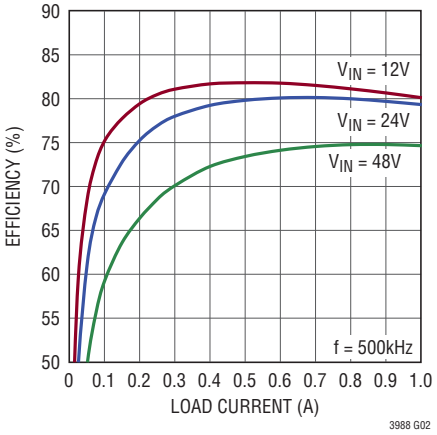
Note 8: If V_{IN2} is driven above 60V, V_{IN2} must be connected to V_{IN1}.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

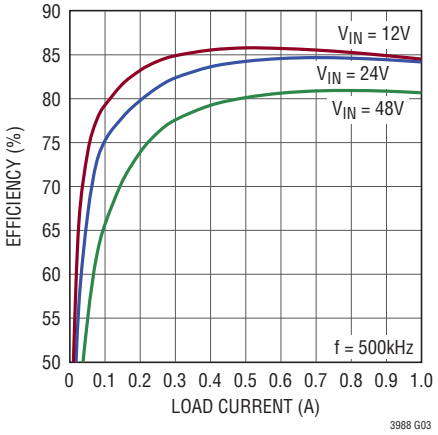
Efficiency, V_{OUT} = 2.5V



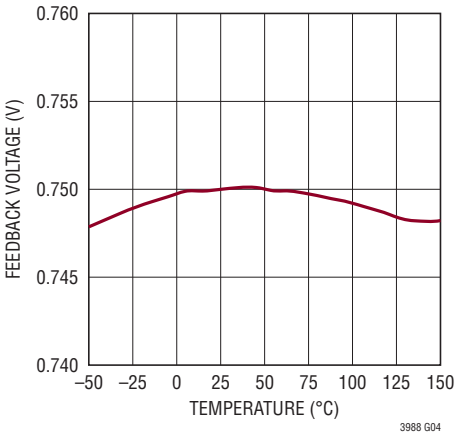
Efficiency, V_{OUT} = 3.3V



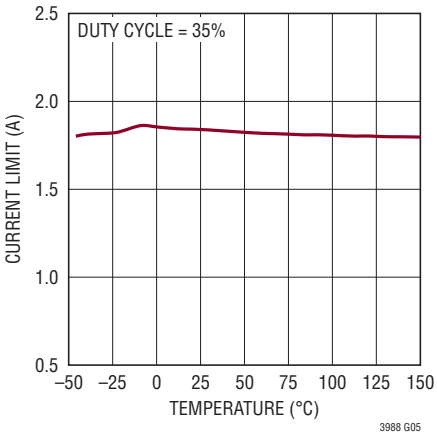
Efficiency, V_{OUT} = 5V



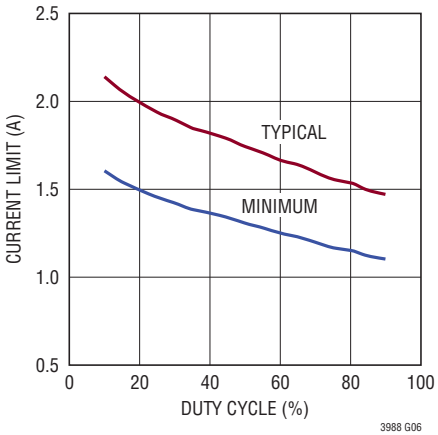
Feedback Voltage vs Temperature



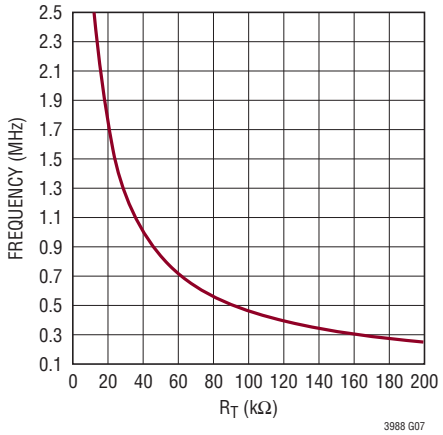
Switch Current Limit vs Temperature



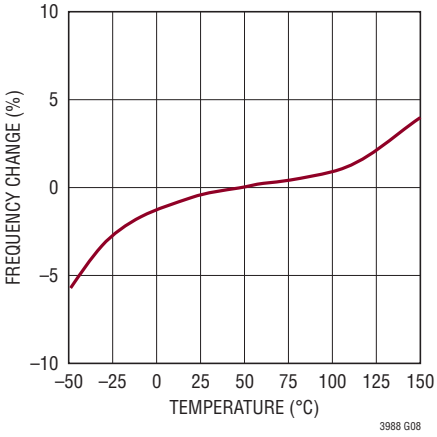
Switch Current Limit vs Duty Cycle



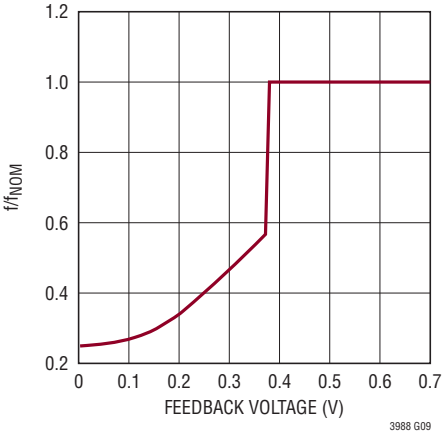
Switching Frequency vs R_T



Switching Frequency vs Temperature

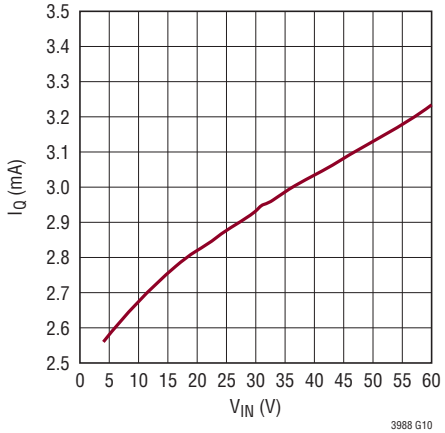


Switching Frequency Foldback

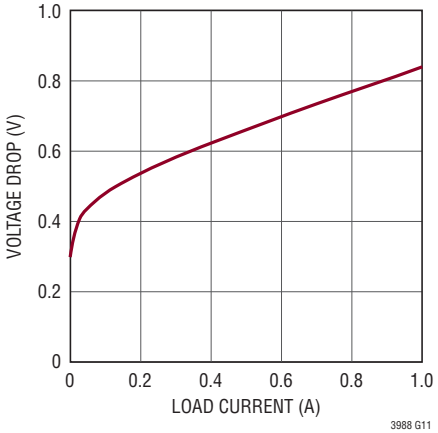


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

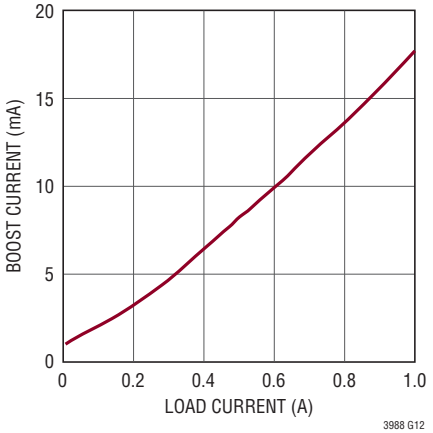
No-Load Supply Current vs Input Voltage



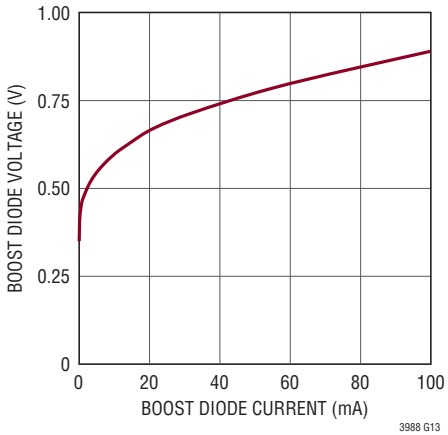
Switch Voltage Drop vs Load Current



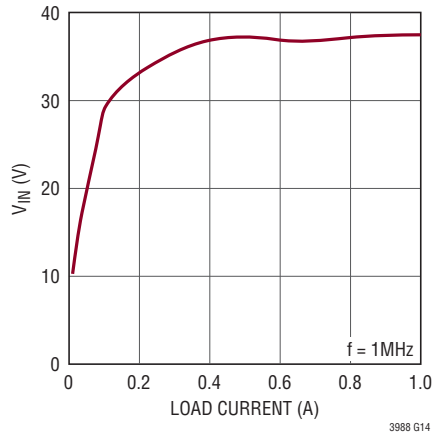
Boost Current vs Load Current



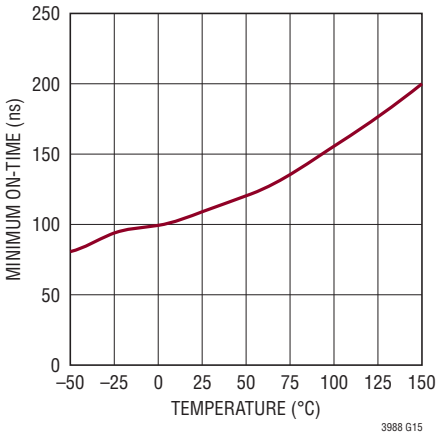
Boost Diode Voltage vs Boost Diode Current



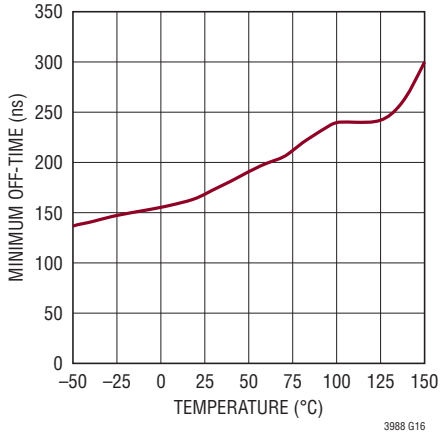
Maximum V_{IN} for Full Frequency vs Load Current



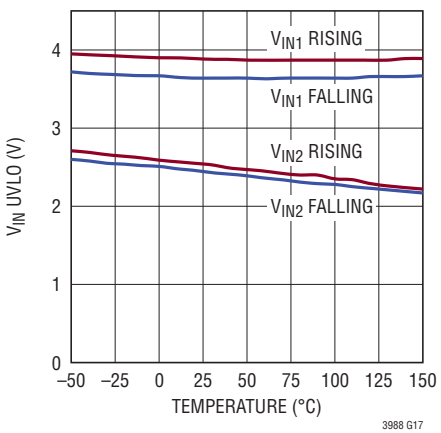
Minimum Switch On-Time vs Temperature



Minimum Switch Off-Time vs Temperature

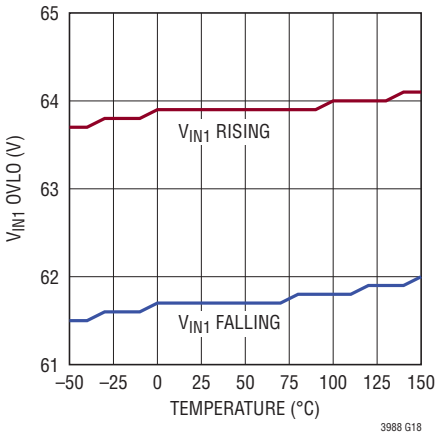


Undervoltage Lockout vs Temperature

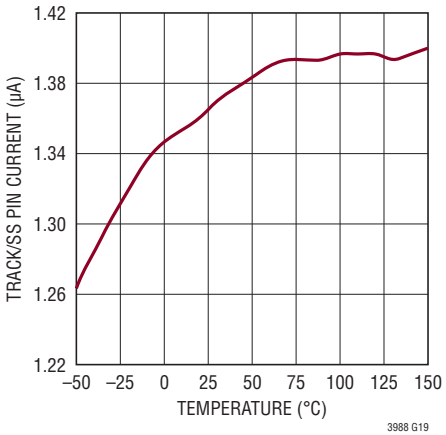


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN1} Overvoltage Lockout vs Temperature



TRACK/SS Pin Current vs Temperature



PIN FUNCTIONS

BD: Internal boost diodes are connected between the BD pin and the BOOST pins. Connect BD to a 3V or higher supply, such as V_{OUT}.

BOOST1, BOOST2: The BOOST pins are used to provide drive voltages, higher than the input voltage, to the internal NPN power switches.

DA1, DA2: Tie the DA pin to the anode of the external Schottky catch diode. If the DA pin current exceeds 1.32A, which could occur in an overload or short-circuit condition, switching is disabled until the DA pin current falls below 1.32A.

EN/UVLO: This pin is used to shut down the LT3988. It can be driven from a logic level, tied directly to the input, or used as an undervoltage lockout by connecting a resistor divider from V_{IN1}.

FB1, FB2: The LT3988 regulates each feedback pin to 0.750V. Connect the feedback resistor divider taps to these pins.

GND: The exposed pad metal of the package provides both electrical contact to ground and good thermal contact to the printed circuit board. The exposed pad must be soldered to the circuit board for proper operation.

RT: The RT pin is used to set the internal oscillator frequency. Tie a resistor from RT to GND for the desired switching frequency.

SYNC: To synchronize the part to an external frequency, drive the SYNC pin with a logic-level signal with positive and negative pulse widths of at least 100ns. If the SYNC function is not used, connect the SYNC pin to ground. If using SYNC, minimize coupling to RT and FB2, and add decoupling capacitors as needed up to 22pF.

SW1, SW2: The SW pins are the outputs of the internal power switches. Connect these pins to the inductors, catch diodes and boost capacitors.

TRACK/SS1, TRACK/SS2: The TRACK/SS pins are used to soft-start the two channels, to allow one channel to track the other output, or to allow both channels to track another output. For tracking, tie a resistor divider to this pin from the tracked output. For soft-start, tie a capacitor to this pin. An internal –1.2µA soft-start current charges the capacitor to create a voltage ramp at the pin. Leave these pins disconnected if unused.

V_{IN1}: The V_{IN1} pin supplies current to the LT3988 internal circuitry and to the internal power switch connected to SW1 and must be locally bypassed. V_{IN1} must be greater than 3.9V (typ) for channel 1 or channel 2 to operate.

V_{IN2}: The V_{IN2} pin supplies current to the internal power switch connected to SW2 and must be locally bypassed. Connect this pin directly to V_{IN1} unless power for channel 2 is coming from a different source. V_{IN2} must be greater than 2.6V (typ) and V_{IN1} must be greater than 3.9V (typ) for channel 2 to operate. If V_{IN2} is driven above 60V, V_{IN2} must be connected to V_{IN1}.

BLOCK DIAGRAM

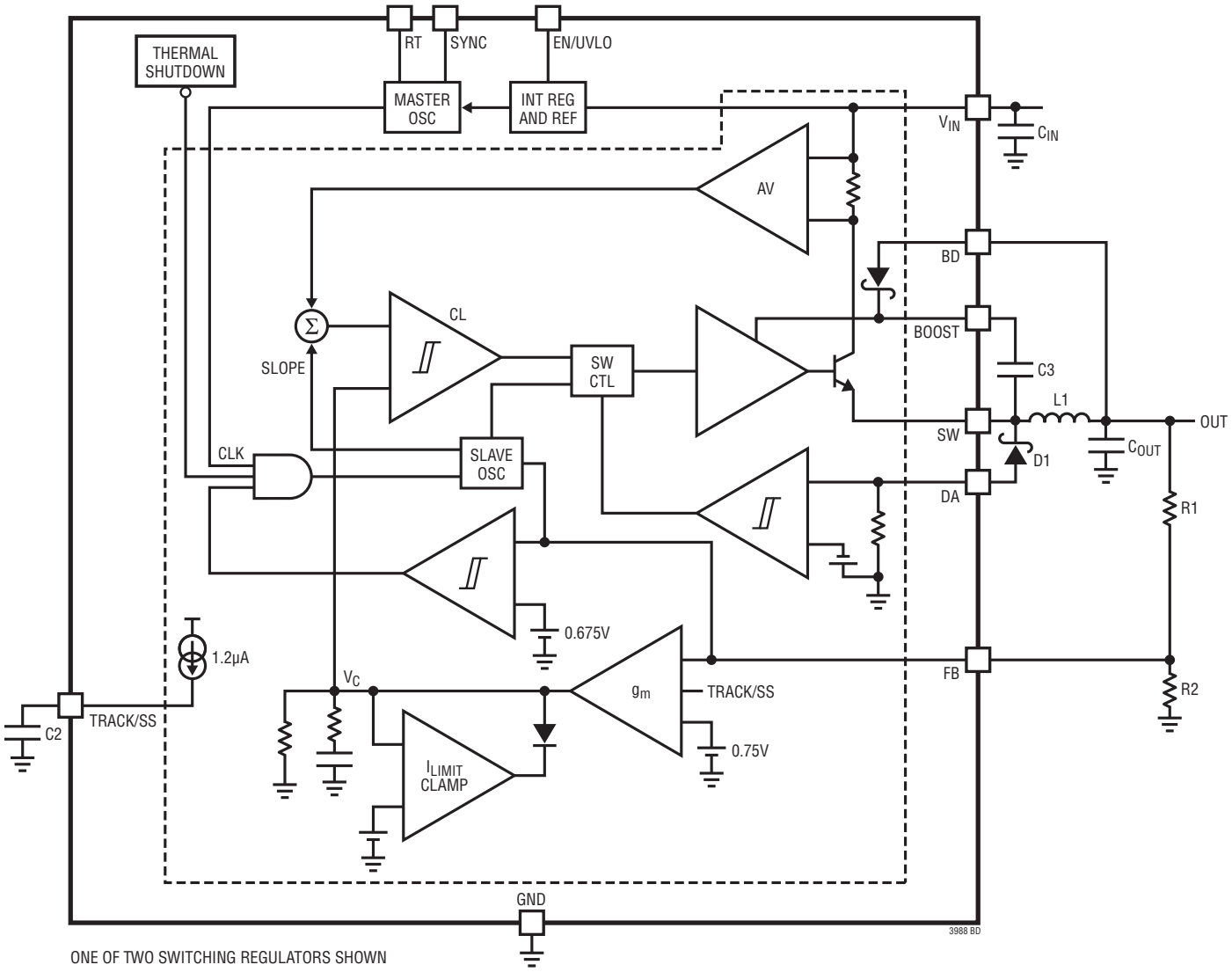


Figure 1. Block Diagram of the LT3988 with Associated External Components

OPERATION

The LT3988 is a dual, constant frequency, current mode regulator with internal power switches. Operation can be best understood by referring to the Block Diagram in Figure 1.

If the EN/UVLO pin is pulled low, the LT3988 is shut down and draws minimal current from the input source(s) tied to the V_{IN} pins. If the EN/UVLO pin exceeds 0.5V (typ), the internal bias circuits turn on, including the internal regulator, reference and master oscillator. The switching regulators will only begin to operate when the EN/UVLO pin exceeds 1.2V (typ).

The switcher is a current mode regulator. Instead of directly modulating the duty cycle of the power switch, the feedback loop controls the peak current in the switch during each cycle. Compared to voltage mode control, current mode control improves loop dynamics and provides cycle-by-cycle current limit.

An oscillator enables an RS flip flop, turning on the internal power switch. An amplifier and comparator monitor the current flowing between the V_{IN} and SW pins, turning the switch off when this current reaches a level determined by the voltage at V_C. An error amplifier measures the output voltage through an external resistor divider tied to the FB pin and servos the V_C voltage. If the error amplifier's output increases, more current is delivered to the output; if it decreases, less current is delivered. An active clamp on the V_C voltage provides a current limit.

The switching frequency is set either by the resistance to GND at the RT pin or by the frequency of the logic-level signal driving the SYNC pin. A detection circuit monitors for the presence of a SYNC signal on the pin and switches between the two modes upon detection of a clock applied to the SYNC pin. Use of the SYNC pin as a frequency input requires the use of an R_T resistor as well. This requirement is detailed in the Switching Frequency section. Onboard circuitry generates the appropriate slope compensation ramps and generates the 180° out-of-phase clocks for the two channels.

Each switcher contains an extra, independent oscillator to perform frequency foldback during overload conditions. This slave oscillator is normally synchronized to the master oscillator. A comparator senses when V_{FB} is less than 50% of its regulated value and switches the regulator from the master oscillator to a slower slave oscillator. V_{FB} is less than 50% of its regulated value during start-up, short-circuit, and overload conditions. Frequency foldback helps limit switch current under these conditions.

The TRACK/SS pins override the 0.75V reference of the FB pins when the TRACK/SS pins are below 0.75V. This allows either coincident or ratiometric supply tracking on start-up as well as a soft-start capability.

The switch drivers operate either from V_{IN} or from the BOOST pin. An external capacitor and internal Schottky diode are used to generate a voltage at the BOOST pin that is higher than the input supply. This allows the driver to obtain a low V_{CE} across the internal bipolar NPN power switch for efficient operation.

The BD pin serves two purposes. The voltage at BD determines the BOOST1 and BOOST2 levels over the V_{IN1} and V_{IN2} supply voltages, and allows the internal circuitry to draw its current from a lower voltage supply than V_{IN1}. This reduces power dissipation and increases efficiency. If the voltage at BD falls below 3V, then quiescent current will flow from V_{IN1}.

The overvoltage and undervoltage detection shuts down the LT3988 if the input voltage on V_{IN1} goes above or below thresholds. The overvoltage detector shuts down the regulators when V_{IN1} exceeds 60V. An undervoltage detector monitoring V_{IN1} disables both regulators when V_{IN1} is under 3.7V, an undervoltage detector monitoring V_{IN2} shuts down channel 2 when V_{IN2} is under 2.5V. The higher voltage is required on V_{IN1} to accomodate internal bias circuits. Additionally, tying the EN/UVLO pin to a voltage divider from V_{IN1} to ground allows a programmable undervoltage threshold.

APPLICATIONS INFORMATION

STEP-DOWN CONSIDERATIONS

FB Resistor Network

The output voltage is programmed with a resistor divider (refer to the Block Diagram) between the output and the FB pin. Choose the resistors according to:

$$R1 = R2\left(\frac{V_{OUT}}{750mV} - 1\right)$$

The parallel combination of R1 and R2 should be 20k or less to minimize bias current errors. The maximum error due to V_{FB} bias current is $\Delta V_{OUT} = I_{FB(MAX)} \bullet R1$

Input Voltage Range

The minimum operating voltage is determined either by the LT3988's undervoltage lockout or by its maximum duty cycle. The duty cycle is the fraction of time that the internal switch is on and is determined by the input and output voltages:

$$DC = \frac{V_{OUT} + V_F}{V_{IN} - V_{SW} + V_F}$$

where V_F is the forward voltage drop of the catch diode (~0.4V) and V_{SW} is the voltage drop of the internal switch (~0.3V at maximum load). This leads to a minimum input voltage of:

$$V_{IN(MIN)} = \frac{V_{OUT} + V_F}{DC_{MAX}} - V_F + V_{SW}$$

The duty cycle is the fraction of time that the internal switch is on during a clock cycle. The maximum duty cycle is generally given by $DC_{MAX} = 1 - t_{OFF(MIN)} \bullet f$. However, unlike most fixed frequency regulators, the LT3988 will not switch off at the end of each clock cycle if there is sufficient voltage across the boost capacitor (C3 in Figure 1) to fully saturate the output switch. Forced switch-off for a minimum time will only occur at the end of a clock cycle when the boost capacitor needs to be recharged. This operation has the same effect as lowering the clock frequency for a fixed off time, resulting in a higher duty cycle and lower minimum input voltage. The resultant duty cycle depends on the charging times of the boost capacitor and can be approximated by the following equation:

$$DC_{MAX} = \frac{B}{B+1}$$

where B is the switch pin current divided by the typical boost current from the BOOST pin current vs switch current in the Typical Performance Characteristics section.

The maximum operating voltage without pulse-skipping is determined by the minimum duty cycle DC_{MIN}:

$$V_{IN(PS)} = \frac{V_{OUT} + V_F}{DC_{MIN}} - V_F + V_{SW}$$

with $DC_{MIN} = t_{ON(MIN)} \bullet f$.

The LT3988 will regulate the output current at input voltages greater than $V_{IN(PS)}$. Exceeding $V_{IN(PS)}$ is safe if the output is in regulation, if the external components have adequate ratings to handle the peak conditions and if the peak inductor current does not exceed 2.3A. A saturating inductor may further reduce performance. For robust operation under fault conditions at input voltages of 40V or greater, use an inductor value of 47µH or larger and a clock rate of 1MHz or lower.

Both the maximum and minimum input voltages are a function of the switching frequency and output voltages. Therefore the maximum switching frequency must be set to a value that accommodates all the input and output voltage parameters and must meet both of the following criteria for each channel:

$$f_{MAX1} = \frac{V_{OUT} + V_F}{V_{IN(PS)} - V_{SW} + V_F} \bullet \frac{1}{t_{ON(MIN)}}$$

$$f_{MAX2} = \left(1 - \frac{V_{OUT} + V_F}{V_{IN(MIN)} - V_{SW} + V_F}\right) \bullet \frac{1}{t_{OFF(MIN)}}$$

The values of $t_{ON(MIN)}$ and $t_{OFF(MIN)}$ are functions of I_{SW} and temperature (see chart in the Typical Performance Characteristics section). Worst-case values for switch currents greater than 0.5A are $t_{ON(MIN)}$ = 180ns (for $T_J > 125°C$ $t_{ON(MIN)}$ = 200ns) and $t_{OFF(MIN)}$ = 240ns. f_{MAX1} is the frequency at which the minimum duty cycle is exceeded. The regulator will skip ON pulses in order to reduce the overall duty cycle

APPLICATIONS INFORMATION

at frequencies above f_{MAX1}. It will continue to regulate but with increased inductor current and increased output ripple.

f_{MAX2} is the frequency at which the maximum duty cycle is exceeded. If there is sufficient charge on the BOOST capacitor, the regulator will skip OFF periods to increase the overall duty cycle at frequencies above f_{MAX2}. Note that the restriction on the operating input voltage refers to steady-state limits to keep the output in regulation; the circuit will tolerate input voltage transients up to the absolute maximum rating.

Switching Frequency

Once the upper and lower bounds for the switching frequency are found from the duty cycle requirements, the frequency may be set within those bounds. Lower frequencies result in lower switching losses, but require larger inductors and capacitors. The user must decide the best trade-off.

The switching frequency is set by a resistor connected from the RT pin to ground, or by forcing a clock signal into the SYNC pin. The LT3988 applies a voltage across this resistor and uses the current to set the oscillator speed. The R_T resistor value for a given switching frequency is given by:

$$R_T = \frac{1.31}{f^2} + \frac{46.56}{f} - 7.322$$

$250kHz \le f \le 2.5MHz$

where f is in MHz and R_T is in kΩ.

The frequency sync signal will support V_{IH} logic levels from 1.5V to 5V CMOS or TTL. The duty cycle is not important, but it needs a minimum on time of 100ns and a minimum off time of 100ns. R_T should be set to provide a frequency within ±25% of the final sync frequency.

The slope recovery circuit sets the slope compensation to the appropriate value for the synchronized frequency. Choose the inductor value based on the lowest potential switching frequency.

Inductor Selection and Maximum Output Current

A good first choice for the inductor value is:

$$L = \frac{V_{OUT} + V_F}{0.6A \bullet f}$$

where V_F is the voltage drop of the catch diode (~0.4V) and f is in MHz. The inductor's RMS current rating must be greater than the maximum load current and its saturation current

Table 1. Inductors

MFG	URL	PART SERIES	INDUCTANCE RANGE (µH)	SIZE (mm) (L × W × H)
Coilcraft	http://www.coilcraft.com	XPL7030 XFL4020 XAL50XX	0.13 to 22 1 to 4.7 0.16 to 22	7 × 7 × 3 4 × 4 × 2.15 5.28 × 5.48 × 5.1
Cooper	http://www.cooperbussmann.com	DRA74 DR1040	0.33 to 1000 1.5 to 330	7.6 × 7.6 × 4.35 10.5 × 10.3 × 4
CWS	http://www.coilws.com	SP-0703 SP-0704 SB-1004	3 to 100 2.2 to 100 10 to 1500	7 × 7 × 3 7 × 7 × 4 10.1 × 10.1 × 4.5
Murata	http://www.murata.com	LQH55D LQH6PP LQH88P	0.12 to 10000 1 to 100 1 to 100	5 × 5.7 × 4.7 6 × 6 × 4.3 8 × 8 × 3.8
Sumida	http://www.sumida.com	CDMC6D28 CDEIR8D38F	0.2 to 4.7 4 to 22	7.25 × 6.7 × 3 8.5 × 8.3 × 4
Toko	http://www.toko.co.jp	DS84LCB FDV0620	1 to 100 0.2 to 4.7	8.4 × 8.3 × 4 6.7 × 7.4 × 2
Vishay	http://www.vishay.com	IHLP-2020AB-11 IHLP-2020BZ-11 IHLP-2525CZ-11	0.1 to 4.7 0.1 to 10 1 to 22	5.49 × 5.18 × 1.2 5.49 × 5.18 × 2 6.86 × 6.47 × 3
Würth	http://www.we-online.de	WE-PD2-S WE-PD-M WE-PD2-XL	1 to 68 1 to 1000 10 to 820	4 × 4.5 × 3.2 7.3 × 7.3 × 4.5 9 × 10 × 5.4

APPLICATIONS INFORMATION

should be at least 30% higher. For highest efficiency, the series resistance (DCR) should be less than 0.1Ω. Table 1 lists several vendors and types that are suitable.

The current in the inductor is a triangle wave with an average value equal to the load current. The peak switch current is equal to the output current plus half the peak-to-peak inductor ripple current. The LT3988 limits its switch current in order to protect itself and the system from overload faults. Therefore, the maximum output current that the LT3988 will deliver depends on the switch current limit, the inductor value and the input and output voltages.

When the switch is off, the potential across the inductor is the output voltage plus the catch diode drop. This gives the peak-to-peak ripple current in the inductor:

$$\Delta I_L = (1-DC) \bullet \frac{V_{OUT} + V_F}{L \bullet f}$$

where f is the switching frequency of the LT3988 and L is the value of the inductor. In continuous mode, the peak inductor and switch current is:

$$I_{SWPK} = I_{LPK} = \frac{\Delta I_L}{2} + I_L$$

To maintain output regulation, this peak current must be less than the LT3988's switch current limit, I_{LIM}. For both switches, I_{LIM} is at least 1.5A at low duty cycle and decreases linearly to 1.1A at DC = 90%. (See chart in the Typical Performance Characteristics section).

The minimum inductance can now be calculated as:

$$L_{MIN} = \frac{1-DC_{MIN}}{2 \bullet f} \bullet \frac{V_{OUT} + V_F}{I_{LIM} - I_{OUT}}$$

However, it's generally better to use an inductor larger than the minimum value. The minimum inductor has large ripple currents which increase core losses and require large output capacitors to keep output voltage ripple low.

This analysis is valid for continuous mode operation ($I_{OUT} > \Delta I_L/2$). For details of maximum output current in discontinuous mode operation, see Linear Technology's Application Note AN44. Finally, for duty cycles greater than 50% ($V_{OUT}/V_{IN} > 0.5$), a minimum inductance is required to avoid subharmonic oscillations. This minimum inductance is:

$$L_{MIN} = \frac{V_{OUT} + V_F}{1.25A \bullet f}$$

with L_{MIN} in µH and f in MHz.

For robust operation under fault conditions at input voltages of 40V or greater, use an inductor value of 47µH or larger and a clock rate of 1MHz or lower.

Output Capacitor Selection

The output capacitor filters the inductor current to generate an output with low voltage ripple. It also stores energy in order to satisfy transient loads and stabilize the LT3988's control loop. Because the LT3988 operates at a high frequency, minimal output capacitance is necessary. In addition, the control loop operates well with or without the presence of output capacitor series resistance (ESR). Ceramic capacitors, which achieve very low output ripple and small circuit size, are therefore an option. You can estimate output ripple with the following equations:

$$V_{RIPPLE} = \frac{\Delta I_L}{8 \bullet f \bullet C_{OUT}} \text{ for ceramic capacitors}$$

and

$$V_{RIPPLE} = \Delta I_L \bullet ESR \text{ for electrolytic capacitors}$$

(tantalum and aluminum)

where ΔI_L is the peak-to-peak ripple current in the inductor. The RMS content of this ripple is very low so the RMS current rating of the output capacitor is usually not of concern. It can be estimated with the formula:

$$I_{C(RMS)} = \frac{\Delta I_L}{\sqrt{12}}$$

Another constraint on the output capacitor is that it must have greater energy storage than the inductor; if the stored energy in the inductor transfers to the output, the resulting voltage step should be small compared to the regulation voltage. For a 5% overshoot, this requirement indicates:

$$C_{OUT} > 10 \bullet L \bullet \left(\frac{I_{LIM}}{V_{OUT}} \right)^2$$

APPLICATIONS INFORMATION

The low ESR and small size of ceramic capacitors make them the preferred type for LT3988 applications. Not all ceramic capacitors are the same, however. Many of the higher value capacitors use poor dielectrics with high temperature and voltage coefficients. In particular, Y5V and Z5U types lose a large fraction of their capacitance with applied voltage and at temperature extremes. Because loop stability and transient response depend on the value of C_{OUT}, this loss may be unacceptable. Use X7R and X5R types.

Electrolytic capacitors are also an option. The ESRs of most aluminum electrolytic capacitors are too large to deliver low output ripple. Tantalum, as well as newer, lower-ESR organic electrolytic capacitors intended for power supply use are suitable. Choose a capacitor with a low enough ESR for the required output ripple. Because the volume of the capacitor determines its ESR, both the size and the value will be larger than a ceramic capacitor that would give similar ripple performance. One benefit is that the larger capacitance may give better transient response for large changes in load current. Table 2 lists several capacitor vendors.

Table 2. Low ESR Surface Mount Capacitors

MFG	TYPE	SERIES
AVX	Ceramic Tantalum	 TPS
Johansen	Ceramic	X7R, 1812 MLCC
Kemet	Tantalum Tantalum Organic Aluminum Organic	T491,T494,T498 T520,T521,T528 A700
Panasonic	Aluminum Organic	SP CAP
Sanyo	Tantalum Aluminum Organic	POSCAP
Taiyo-Yuden	Ceramic	
TDK	Ceramic	

Diode Selection

The catch diode (D1 from Figure 1) conducts the inductor current during the switch off time. Use a Schottky diode rated for 1A to 2A average current. Peak reverse voltage across the diode is equal to the regulator input voltage. Use a diode with a reverse voltage rating greater than the input voltage. The OVLO function of the LT3988 turns off the switch when V_{IN} > 64V (typ) allowing use of Schottky diodes with a 70V rating for input voltages up to 80V. Table 3 lists several Schottky diodes and their manufacturers.

Table 3. Schottky Diodes

PART NUMBER	V_R (V)	I_{AVG} (A)	V_F AT 1A (mV)	V_F AT 2A (mV)
On Semiconductor				
NSR10F40NXT5G	40	1	490	
MBRA160T3	60	1	510	
MBRS190T3	90	1	750	
MBRS260T3G	60	2		430
Diodes Inc				
B140	40	1	500	
B160	60	1	700	
B170	70	1	790	
B180	80	1	790	
B260	60	2		700
B280	80	2		790
DFLS140L	40	1	550	
DFLS160L	60	1	500	
DFLS260	60	2		620

Boost Pin Considerations

The external capacitor and the internal diode tied to the BOOST pin generate a voltage that is higher than the input voltage. In most cases, a small ceramic capacitor will work well. The capacitor value is a function of the switching frequency, peak current, duty cycle and boost voltage. Figure 2 shows three ways to arrange the boost circuit. The BOOST pin must be more than 2.3V above the SW pin for full efficiency. For outputs of 3.3V and higher, the standard circuit (Figure 2a) is best. For lower output voltages, the BD pin can be tied to the input (Figure 2b). The circuit in Figure 2a is more efficient because the BOOST pin current comes from a lower voltage source. Finally, as shown in Figure 2c, the BD pin can be tied to another source that is at least 3V. For example, if you are generating 3.3V and 1.8V and the 3.3V is on whenever the 1.8V is on, the BD pin can be connected to the 3.3V output. (see Output Voltage Tracking). Be sure that the maximum voltage at the BOOST pin is less than 80V and the voltage difference between the BOOST and SW pins is less than 30V. The minimum operating voltage of an LT3988 application is limited by the internal 4V undervoltage lockout and by the maximum duty cycle.

APPLICATIONS INFORMATION

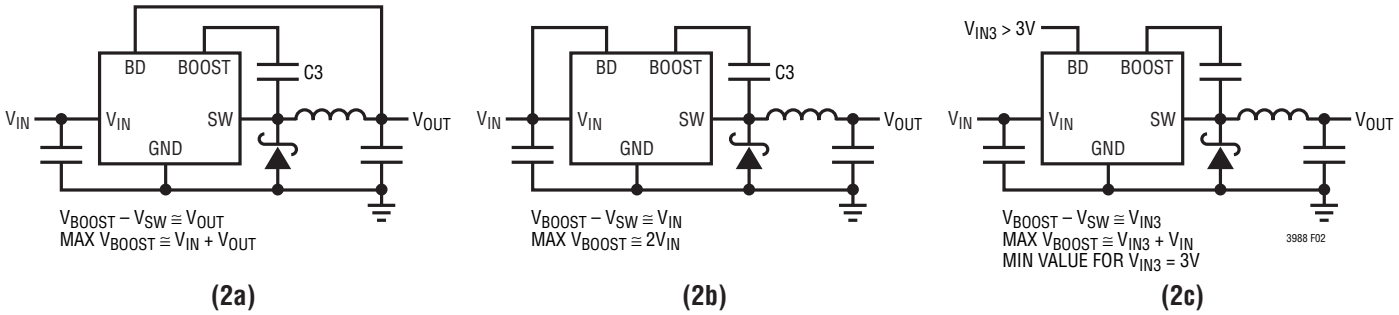


Figure 2. Generating the Boost Voltage

The boost circuit also limits the minimum input voltage for proper start-up. If the input voltage ramps slowly, or the LT3988 turns on when the output is already in regulation, the boost capacitor may not be fully charged. Because the boost capacitor charges with the energy stored in the inductor, the circuit will rely on some minimum load current to get the boost circuit running properly. This minimum load will depend on input and output voltages, and on the arrangement of the boost circuit. The minimum load current generally goes to zero once the circuit has started. Figure 4 shows a plot of input voltage to start and to run as a function of load current. Even without an output load current, in many cases the discharged output capacitor will present a load to the switcher that will allow it to start.

The boost current is generally small but can become significant at high duty cycles. The required boost current is:

$$I_{BOOST} = \left(\frac{V_{OUT}}{V_{IN}}\right)\left(\frac{I_{OUT}}{40}\right)$$

Converter with Backup Output Regulator

There is another situation to consider: systems where the output will be held high when the input to the LT3988 is absent. If the V_{IN} pin is grounded while the output is held high, then diodes inside the LT3988 can pull large currents from the output through the SW and V_{IN} pins. A Schottky diode in series with the input to the LT3988, as shown in Figure 3, will protect the LT3988 and the system from a shorted or reversed input.

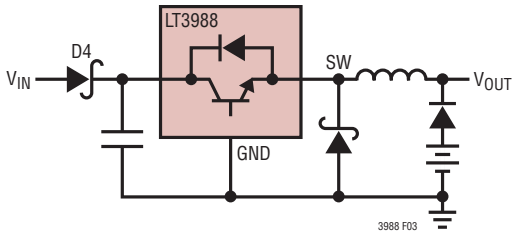


Figure 3. Diode D4 Prevents a Shorted Input from Discharging a Backup Battery Tied to the Output

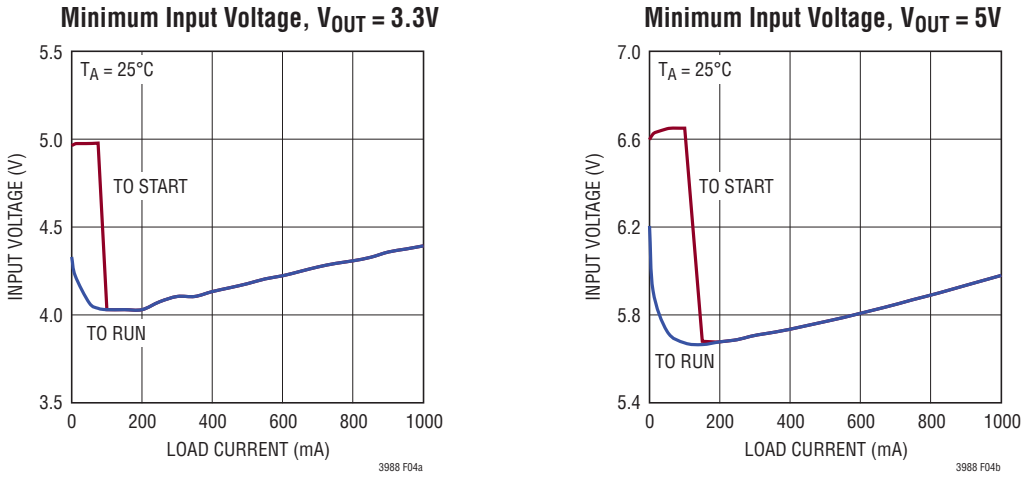


Figure 4. The Minimum Input Voltage Depends on Output Voltage, Load Current, and Boost Circuit

APPLICATIONS INFORMATION

Input Capacitor Selection

Bypass the input of the LT3988 circuit with a 4.7µF or higher ceramic capacitor of X7R or X5R type. A lower value or a less expensive Y5V type will work if there is additional bypassing provided by bulk electrolytic capacitors, or if the input source impedance is low. The following paragraphs describe the input capacitor considerations in more detail.

Step-down regulators draw current from the input supply in pulses with very fast rise and fall times. The input capacitor is required to reduce the resulting voltage ripple at the LT3988 input and to force this switching current into a tight local loop, minimizing EMI. The input capacitor must have low impedance at the switching frequency to do this effectively and it must have an adequate ripple current rating. With two switchers operating at the same frequency but with different phases and duty cycles, calculating the input capacitor RMS current is not simple; however, a conservative value is the RMS input current for the phase delivering the most power ($V_{OUT} \bullet I_{OUT}$):

$$I_{IN(RMS)} = I_{OUT} \bullet \frac{\sqrt{V_{OUT}\left(V_{IN} - V_{OUT}\right)}}{V_{IN}} < \frac{I_{OUT}}{2}$$

and is largest when $V_{IN} = 2V_{OUT}$ (50% duty cycle). As the second, lower power channel draws input current, the input capacitor's RMS current actually decreases as the out-of-phase current cancels the current drawn by the higher power channel. Considering that the maximum load current from a single phase (if SW1 and SW2 are both at maximum current) is ~1A, RMS ripple current will always be less than 0.5A.

The high frequency of the LT3988 reduces the energy storage requirements of the input capacitor, so that the capacitance required is often less than 10µF. The combination of small size and low impedance (low equivalent series resistance or ESR) of ceramic capacitors makes them the preferred choice. The low ESR results in very low voltage ripple. Ceramic capacitors can handle larger magnitudes of ripple current than other capacitor types of the same value.

An alternative to a high value ceramic capacitor is a lower value along with a larger electrolytic capacitor, for example a 1µF ceramic capacitor in parallel with a low ESR tantalum capacitor. For the electrolytic capacitor, a value larger than 10µF will be required to meet the ESR and ripple current requirements. Because the input capacitor is likely to see high surge currents when the input source is applied, tantalum capacitors should be surge rated. The manufacturer may also recommend operation below the rated voltage of the capacitor. Be sure to place the 1µF ceramic as close as possible to the V_{IN} and GND pins on the IC for optimal noise immunity.

A final caution is in order regarding the use of ceramic capacitors at the input. A ceramic input capacitor can combine with stray inductance to form a resonant tank circuit. If power is applied quickly (for example by plugging the circuit into a live power source), this tank can ring, doubling the input voltage and damaging the LT3988. The solution is to either clamp the input voltage or dampen the tank circuit by adding a lossy capacitor in parallel with the ceramic capacitor. For details, see Application Note 88.

Frequency Compensation

The LT3988 uses current mode control to regulate the output. This simplifies loop compensation. In particular, the LT3988 does not depend on the ESR of the output capacitor for stability, so you are free to use ceramic capacitors to achieve low output ripple and small circuit size. The LT3988 is internally compensated with the RC network tied to the VC node. The internal compensation network is optimized to provide stability over the full frequency range. Figure 5 shows an equivalent circuit for the LT3988 control loop. The error amplifier is a transconductance amplifier with

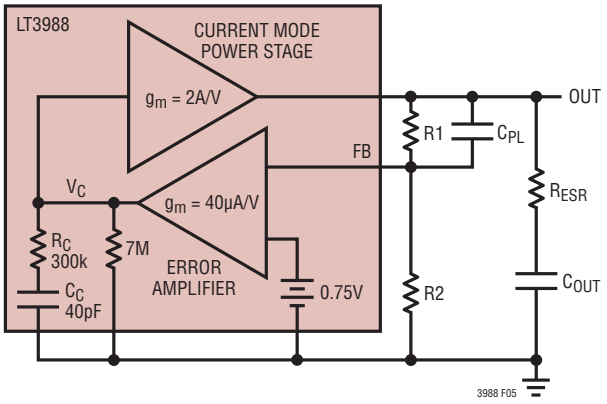


Figure 5. Model For Loop Response

APPLICATIONS INFORMATION

finite output impedance. The power section, consisting of the modulator, power switch and inductor, is modeled as a transconductance amplifier generating an output current proportional to the voltage at the V_C node.

Note that the output capacitor integrates this current, and that the capacitor on the V_C node (C_C) integrates the error amplifier output current, resulting in two poles in the loop. R_C provides a zero. With the recommended output capacitor, the loop crossover occurs above the R_CC_C zero. This simple model works well as long as the value of the inductor is not too high and the loop crossover frequency is much lower than the switching frequency. With a larger ceramic capacitor (very low ESR), crossover may be lower and a phase lead capacitor (CPL) across the feedback divider may improve the phase margin and transient response. Large electrolytic capacitors may have an ESR large enough to create an additional zero, and the phase lead may not be necessary. If the output capacitor is different than the recommended capacitor, stability should be checked across all operating conditions, including load current, input voltage and temperature. The LT1375 data sheet contains a more thorough discussion of loop compensation and describes how to test the stability using a transient load.

Shutdown

The EN/UVLO pin is used for two purposes, to place the LT3988 in a low current shutdown mode, and to override the internal undervoltage lockout thresholds with a user programmable threshold. When the EN/UVLO pin is pulled to under 0.5V (typ), the LT3988 is in shutdown mode and draws less than 1µA from the input supply. When the EN/UVLO pin is driven above 0.5V (typ) and less than 1.2V (typ), the internal regulator is activated and the oscillators are operating, but the switching operation of both channels remains inhibited. When the EV/UVLO pin is driven above 1.2V (typ), the undervoltage lockout asserted by the EN/UVLO function is released, allowing switching operation of both channels. Internal undervoltage detectors will still prevent switching operation on channel 1 until V_{IN1} is greater than 3.9V (typ) and on channel 2 until V_{IN2} is greater than 2.6V (typ). The EN/UVLO undervoltage lockout has 120mV (typ) of hysteresis. The EN/UVLO pin is rated up to 80V and can be connected directly to the input voltage.

The EN/UVLO pin may be driven by a voltage divider from V_{IN1}, allowing an externally programmable undervoltage lockout to be set above the internal 3.9V threshold. The undervoltage threshold and hysteresis are given by:

$$V_{UVTH} = 1.2\left(1+\frac{R1}{R2}\right);R1=R2\left(\frac{V_{UVTH}}{1.2}-1\right)$$

$$V_{UVHY} = 0.12\left(1+\frac{R1}{R2}\right);R1=R2\left(\frac{V_{UVHY}}{0.12}-1\right)$$

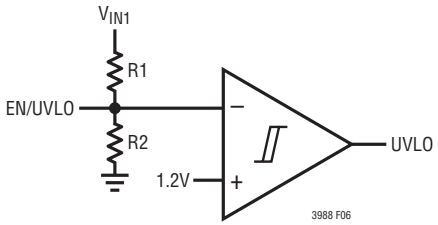


Figure 6. Undervoltage Lockout Circuit

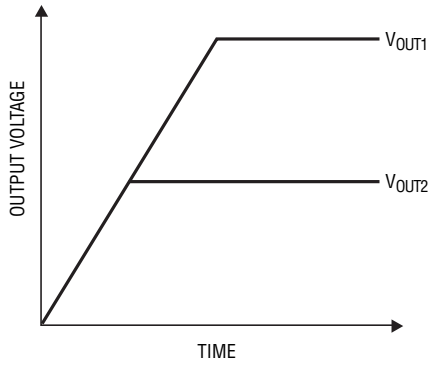
Output Voltage Tracking

The LT3988 allows the user to program how the output ramps up by means of the TRACK/SS pins. Through these pins, either channel output can be set up to either coincidently or ratiometrically track the other channel output. This example will show the channel 2 output tracking the channel 1 output, as shown in Figure 7.

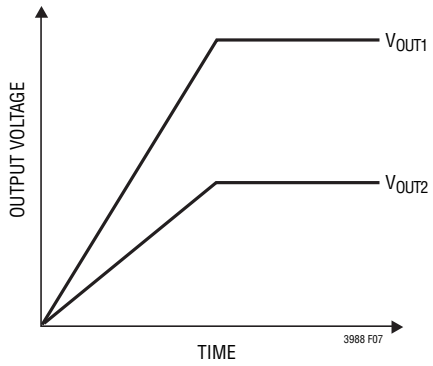
The TRACK/SS2 pin acts as a clamp on channel 2's reference voltage. V_{OUT2} is referenced to the TRACK/SS2 voltage when the TRACK/SS2 < 0.8V and to the internal precision reference when TRACK/SS2 > 0.8V. To implement the coincident tracking in Figure 7, connect an extra resistive divider to the output of channel 1 and connect its midpoint to the TRACK/SS2 pin (Figure 8).

The ratio of this divider should be selected to be the same as that of channel 2's feedback divider (R5 = R3 and R6 = R4). In this tracking mode, V_{OUT1} must be set higher than V_{OUT2}. To implement the ratiometric tracking in Figure 6, change the extra divider ratio to R5 = R1 and R6 = R2 + ΔR. The extra resistance on R6 should be set so that the TRACK/SS2 voltage is ≥1V when V_{OUT1} is at its final value. The need for this extra resistance is best understood with the help of the equivalent input circuit shown in Figure 9.

APPLICATIONS INFORMATION

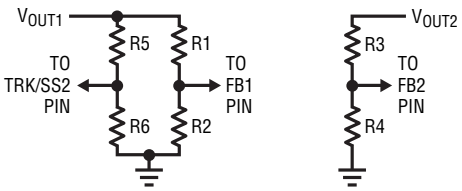


Coincident Tracking



Ratiometric Tracking

Figure 7. Two Different Modes of Output Voltage Tracking



SELECTING VALUES FOR R5 AND R6

	COINCIDENT	RATIOMETRIC
R5 =	R3	R1
R6 =	R4	$\frac{R1}{V_{OUT1}/1V-1}$

3988 F08

$$\frac{R1}{R2}=\frac{V_{OUT1}}{0.75}-1,\ \frac{R3}{R4}=\frac{V_{OUT2}}{0.75}-1$$

Figure 8. Setup for Coincident and Ratiometric Tracking

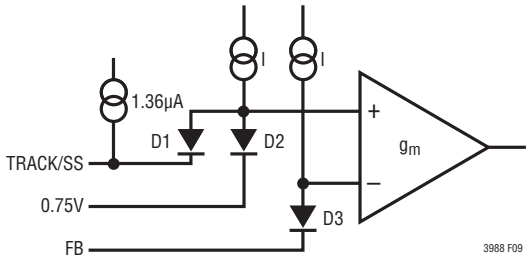


Figure 9. Equivalent Input Circuit of Error Amplifier

At the input stage of the error amplifier, two common anode diodes are used to clamp the equivalent reference voltage and an additional diode is used to match the shifted common mode voltage. The top two current sources are of the same amplitude. In the coincident mode, the TRACK/SS2 voltage is substantially higher than 0.75V at steady state and effectively turns off D1. D2 and D3 will therefore conduct the same current and offer tight matching between V_{FB2} and the internal precision 0.75V reference. In the ratiometric mode with R6 = R2, TRACK/SS2 equals 0.75V at steady state. D1 will divert part of the bias current and make V_{FB2} slightly lower than 0.75V. Although this error is minimized by the exponential I-V characteristic of the diodes, it does impose a finite amount of output voltage deviation. Further, when channel 1's output experiences dynamic excursions (under load transient, for example), channel 2 will be affected as well. Setting R6 to a value that pushes the TRK/SS2 voltage to 1V at steady state will eliminate these problems while providing near ratiometric tracking. The example shows channel 2 tracking channel 1, however either channel may be set up to track the other.

Soft-Start

If a capacitor is tied from the TRACK/SS pin to ground, then the internal pull-up current will generate a voltage ramp on this pin. This results in a ramp at the output, limiting the inductor current and therefore input current during start-up. A good value for the soft-start capacitor is $C_{OUT}/10{,}000$, where C_{OUT} is the value of the output capacitor.

APPLICATIONS INFORMATION

Independent Input Voltages

V_{IN1} and V_{IN2} are independent and can be powered with different voltages provided V_{IN1} is present when V_{IN2} is present. Each supply must be bypassed as close to the V_{IN} pins as possible. For applications requiring large inductors due to high V_{IN} to V_{OUT} ratios, a 2-stage step-down approach may reduce inductor size by allowing an increase in frequency. A dual step-down application steps down the input voltage (V_{IN1}) to the highest output voltage, then uses that voltage to power the other output (V_{IN2}). V_{OUT1} must be able to provide enough current for its output plus the input current at V_{IN2} when V_{OUT2} is at maximum load. Figure 10 shows a 12V to 5V, and 1.8V 2-stage converter using this approach.

PCB Layout

For proper operation and minimum EMI, care must be taken during printed circuit board (PCB) layout. Figure 11 shows the high current paths in the step-down regulator circuit. Note that in the step-down regulators large, switched currents flow in the power switch, the catch diode and the input capacitor. The loop formed by these

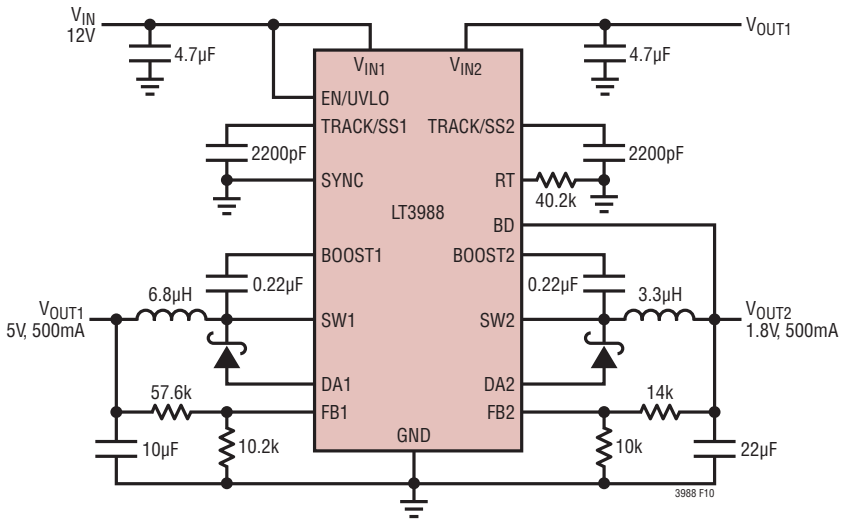


Figure 10. 1MHz, 2-Stage Step-Down 5V and 1.8V Outputs

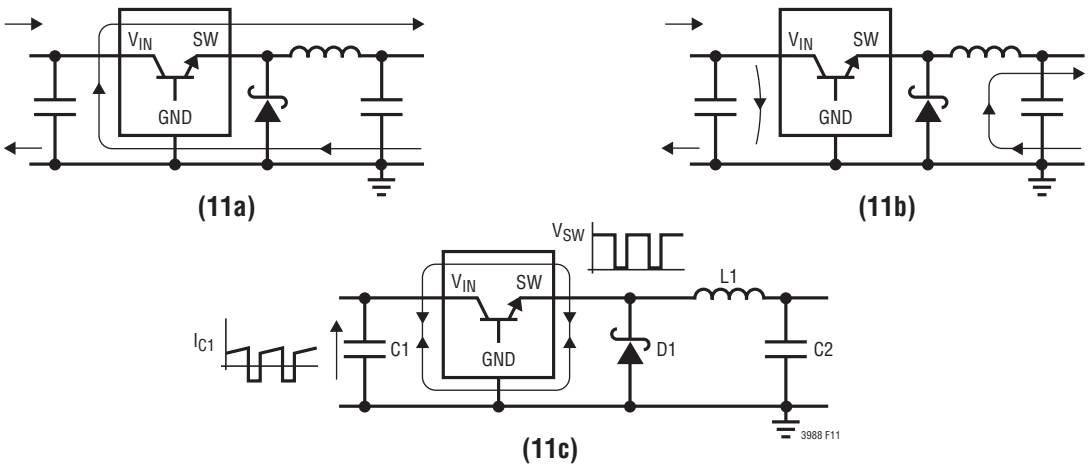


Figure 11. Subtracting the Current When the Switch Is ON (11a) From the Current When the Switch Is OFF (11b) Reveals the Path of the High Frequency Switching Current (11c). Keep this Loop Small. The Voltage on the SW and Boost Nodes Will Also Be Switched; Keep These Nodes as Small as Possible. Finally, Make Sure the Circuit Is Shielded with a Local Ground Plane

APPLICATIONS INFORMATION

components should be as small as possible. Place these components, along with the inductor and output capacitor, on the same side of the circuit board and connect them on that layer. Place a local, unbroken ground plane below these components and tie this ground plane to system ground at one location, ideally at the ground terminal of the output capacitor. Additionally, keep the SW and BOOST nodes as small as possible. Figure 12 shows an example of proper PCB layout.

Thermal Considerations

The die temperature of the LT3988 must be lower than the maximum rating of 125°C (150°C for the H-grade). This is generally not a concern unless the ambient temperature is above 85°C. For higher temperatures, care should be taken in the layout of the circuit to ensure good heat sinking of the LT3988. The maximum load current should be derated as the ambient temperature approaches 125°C (150°C for the H-grade). The die temperature is calculated by multiplying the LT3988 power dissipation by the thermal resistance from junction to ambient. Power dissipation within the LT3988 can be estimated by calculating the total power loss from an efficiency measurement and subtracting the catch diode loss. Thermal resistance depends on the layout of the circuit board, but values from 30°C/W to 60°C/W are typical.

Related Linear Technology Publications

Application Notes 19, 35, 44, 76 and 88 contain more detailed descriptions and design information for buck regulators and other switching regulators. The LT1375 data sheet has a more extensive discussion of output ripple, loop compensation, and stability testing. Design Note 318 shows how to generate a dual polarity output supply using a buck regulator.

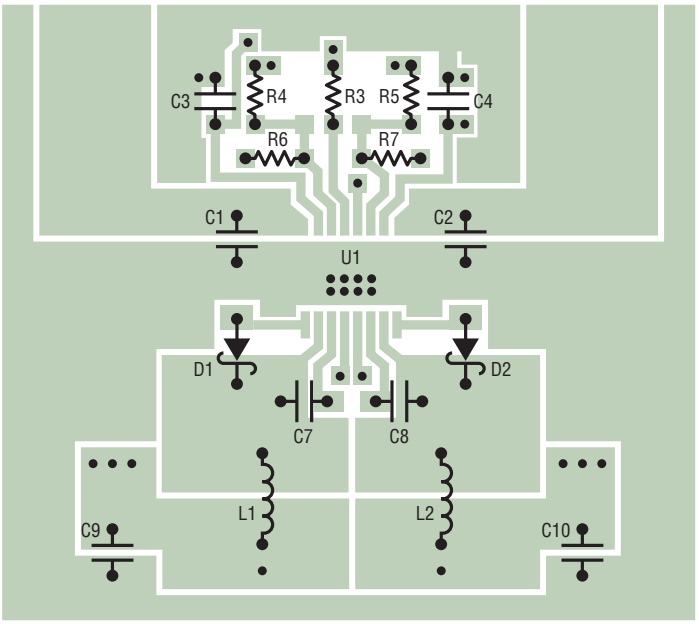
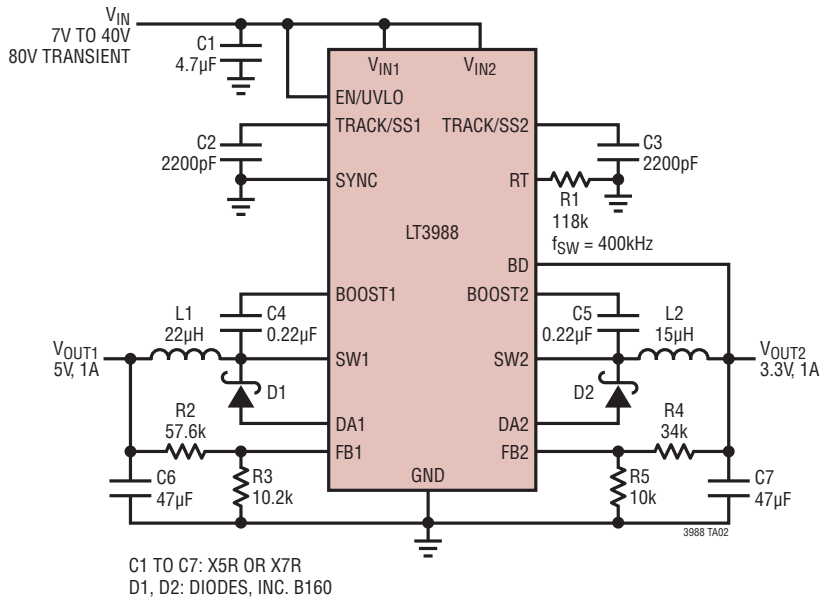


Figure 12. Sample PC Board Layout

TYPICAL APPLICATIONS

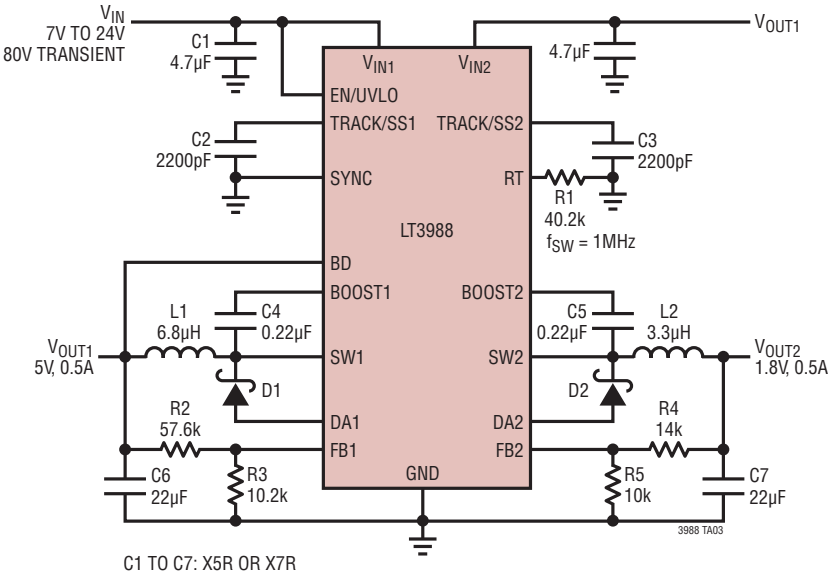
400kHz, 5V and 3.3V Outputs



C1 TO C7: X5R OR X7R
D1, D2: DIODES, INC. B160

TYPICAL APPLICATIONS

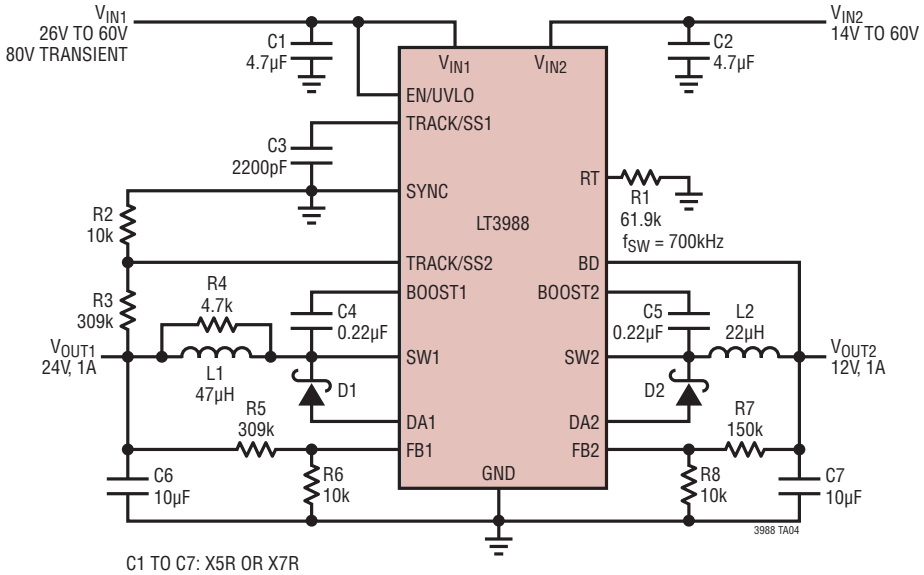
1MHz, Wide Input Range 5V and 1.8V Outputs



C1 TO C7: X5R OR X7R
D1: DIODES, INC. B160
D2: DIODES, INC. B120

TYPICAL APPLICATIONS

700kHz, 24V and 12V Outputs with Coincident Tracking

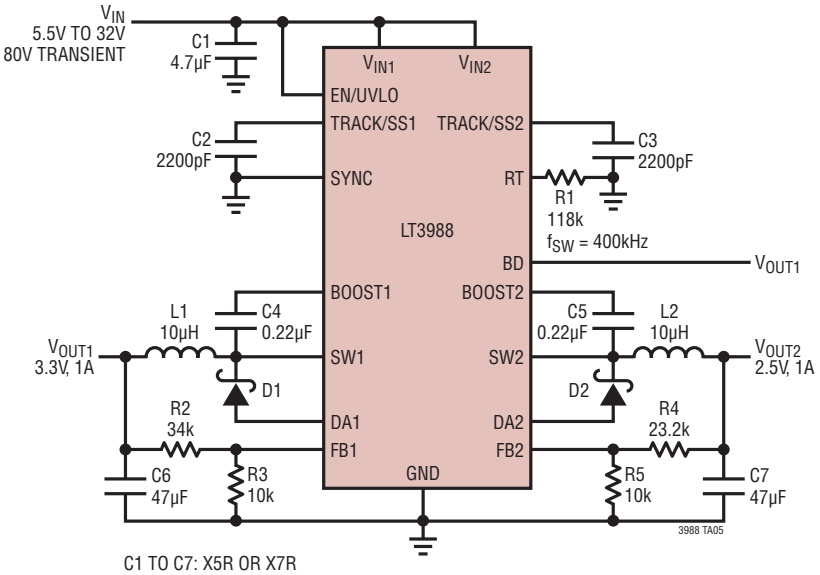


C1 TO C7: X5R OR X7R
D1, D2: DIODES, INC. B160
R4: USE 0.25W RESISTOR

DERATE OUTPUT CURRENT AT HIGHER AMBIENT TEMPERATURES AND INPUT VOLTAGES TO MAINTAIN JUNCTION TEMPERATURE BELOW THE ABSOLUTE MAXIMUM.

TYPICAL APPLICATIONS

400kHz, 3.3V and 2.5V Outputs

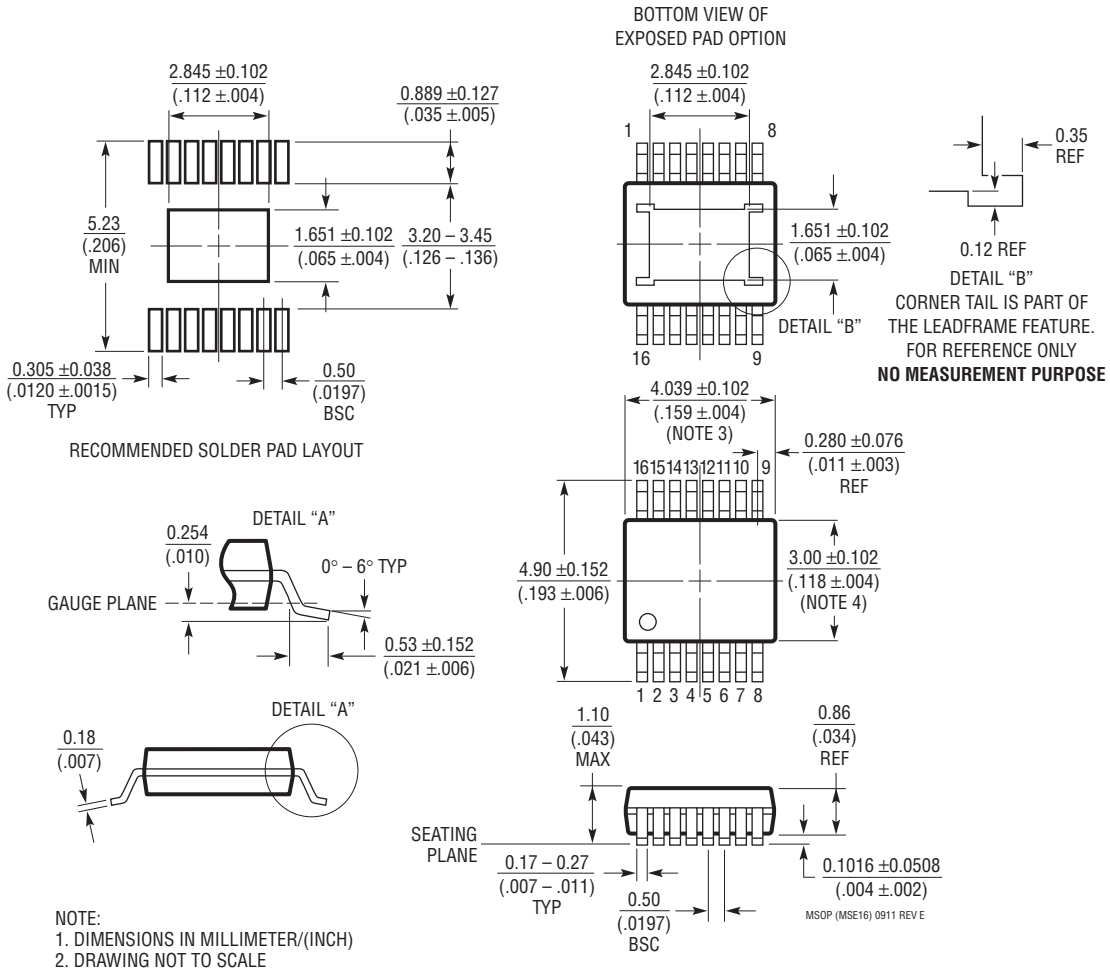


C1 TO C7: X5R OR X7R
D1, D2: DIODES, INC. B180

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

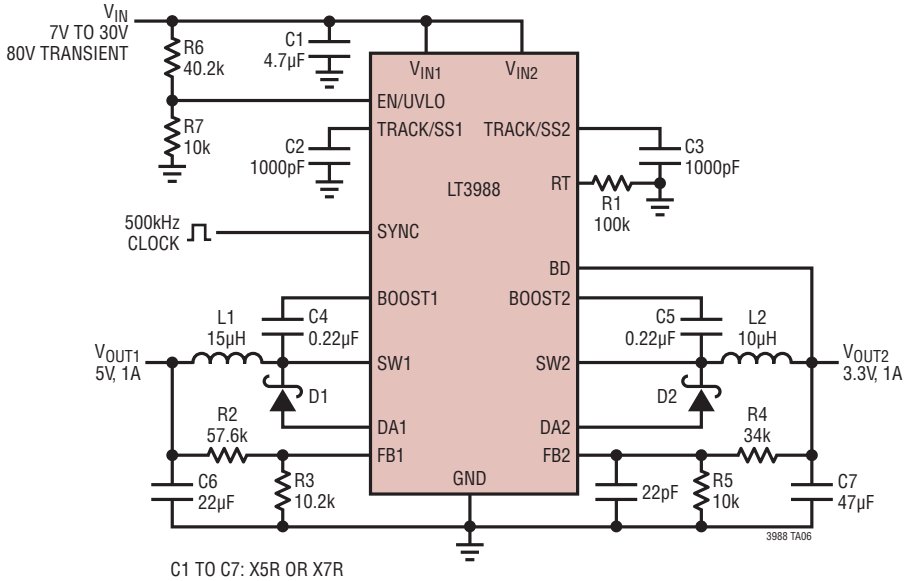
MSE Package
16-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1667 Rev E)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.

TYPICAL APPLICATION

500kHz External Sync, 5V and 3.3V Outputs with 6V UVLO



C1 TO C7: X5R OR X7R
D1, D2: DIODES, INC. B180
EN/UVLO THRESHOLD = 6.02V

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT3509	36V with Transient Protection to 60V, Dual 700mA (I_{OUT}), 2.2MHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 3.6V to 36V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 1.9mA, I_{SD} = 1µA, 3mm × 4mm DFN-14, MSOP-16E
LT3508	36V with Transient Protection to 40V, Dual 1.4A (I_{OUT}), 2.5MHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 3.7V to 36V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 4.6mA, I_{SD} = 1µA, 4mm × 4mm QFN-24, TSSOP-16E
LT3980	58V with Transient Protection to 80V, 2A (I_{OUT}), 2.4MHz, High Efficiency Step-Down DC/DC Converter with Burst Mode® Operation	V_{IN}: 3.6V to 58V, Transient to 80V, $V_{OUT(MIN)}$ = 0.79V, I_Q = 75µA, I_{SD} < 1µA, 3mm × 4mm DFN-16, MSOP-16E
LT3970	40V, 350mA (I_{OUT}), 2MHz, High Efficiency Step-Down DC/DC Converter with Only 2.5µA of Quiescent Current	V_{IN}: 4.2V to 40V, $V_{OUT(MIN)}$ = 1.2V, I_Q = 2.5µA, I_{SD} < 1µA, 2mm × 3mm DFN-10, MSOP-10
LT3990	60V, 350mA (I_{OUT}), 2MHz, High Efficiency Step-Down DC/DC Converter with only 2.5µA of Quiescent Current	V_{IN}: 4.2V to 60V, $V_{OUT(MIN)}$ = 1.2V, I_Q = 2.5µA, I_{SD} < 1µA, 3mm × 3mm DFN-10, MSOP-16E
LT3971	38V, 1.2A (I_{OUT}), 2MHz, High Efficiency Step-Down DC/DC Converter with Only 2.8µA of Quiescent Current	V_{IN}: 4.2V to 38V, $V_{OUT(MIN)}$ = 1.2V, I_Q = 2.8µA, I_{SD} < 1µA, 3mm × 3mm DFN-10, MSOP-10E
LT3991	55V, 1.2A (I_{OUT}), 2MHz, High Efficiency Step-Down DC/DC Converter with Only 2.8µA of Quiescent Current	V_{IN}: 4.2V to 55V, $V_{OUT(MIN)}$ = 1.2V, I_Q = 2.8µA, I_{SD} < 1µA, 3mm × 3mm DFN-10, MSOP-10E
LT3507/LT3507A	36V, Triple 2.4A,1.4A, and 1.4A (I_{OUT}), 2.5MHz, High Efficiency Step-Down DC/DC Converter with LDO Controller	V_{IN}: 4V to 36V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 7mA, I_{SD} = 1µA, 5mm × 7mm QFN-38
LT3680	36V, 3A, 2.4MHz High Efficiency MicroPower Step-Down DC/DC Converter	V_{IN}: 3.6V to 36V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 75µA, I_{SD} < 1µA, 3mm × 3mm DFN-10, MSOP-10E
LT3693	36V, 3A, 2.4MHz High Efficiency Step-Down DC/DC Converter	V_{IN}: 3.6V to 36V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 1.3mA, I_{SD} < 1µA, 3mm × 3mm DFN-10, MSOP-10E
LT3480	36V with Transient Protection to 60V, 2A (I_{OUT}), 2.4MHz, High Efficiency Step-Down DC/DC Converter with Burst Mode Operation	V_{IN}: 3.6V to 38V, Transient to 60V, $V_{OUT(MIN)}$ = 0.78V, I_Q = 70µA, I_{SD} < 1µA, 3mm × 3mm DFN-10, MSOP-10E

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