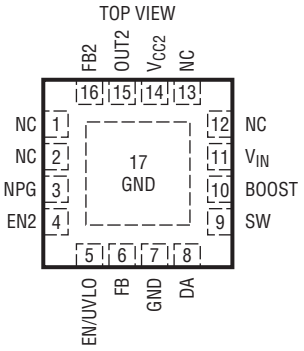
ABSOLUTE MAXIMUM RATINGS

(Note 1)

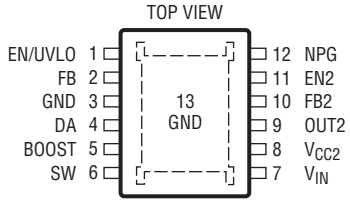
V_{IN}, EN/UVLO (Note 5)..... –0.3V to 55V
BOOST Voltage..... 55V
BOOST Above SW Voltage..... 25V
V_{CC2} Voltage..... –0.3V to 16V
V_{OUT2} Voltage..... –0.3V to 8V
FB, FB2 Voltages..... –0.3V to 6V
EN2, NPG Voltages..... –0.3V to 16V
Operating Junction Temperature Range (Note 2)
LT3645E..... –40°C to 125°C
LT3645I..... –40°C to 125°C
LT3645H..... –40°C to 150°C
Storage Temperature Range..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PIN CONFIGURATION



UD PACKAGE
16-LEAD (3mm × 3mm) PLASTIC QFN

θ_{JA} = 58.7°C/W, θ_{JC} = 7.1°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB



MSE PACKAGE
12-LEAD PLASTIC MSOP

θ_{JA} = 40°C/W, θ_{JC} = 5°C/W TO 10°C/W
EXPOSED PAD (PIN 13) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3645EUD#PBF	LT3645EUD#TRPBF	LFVS	16-Lead Plastic QFN	–40°C to 125°C
LT3645IUD#PBF	LT3645IUD#TRPBF	LFVS	16-Lead Plastic QFN	–40°C to 125°C
LT3645EMSE#PBF	LT3645EMSE#TRPBF	3645	12-Lead Plastic MSOP	–40°C to 125°C
LT3645IMSE#PBF	LT3645IMSE#TRPBF	3645	12-Lead Plastic MSOP	–40°C to 125°C
LT3645HMSE#PBF	LT3645HMSE#TRPBF	3645	12-Lead Plastic MSOP	–40°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, BOOST = 15.3V, V_{CC2} = 3.3V, OUT2 = 1.8V unless otherwise noted. (Notes 2, 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Undervoltage Lockout on V_{IN}	Rising	●	3	3.4	3.6	V
Overvoltage Lockout on V_{IN}	Rising	●	36	38.5	40	V
Overvoltage Lockout Hysteresis				1		V
Feedback Voltage FB		 ●	0.79 0.785	0.8 0.8	0.81 0.813	V
FB Pin Bias Current		●		20	300	nA
Feedback Voltage Line Regulation		●		0.015		%/V
V_{IN} Quiescent Current	Not Switching			1.4	3	mA
V_{IN} Quiescent Current in Shutdown	$V_{EN/UVLO}$ = 0.3V, V_{CC2} = 0V, V_{OUT2} = 0V			0.01	2	µA
Switching Frequency			675	750	825	kHz
Maximum Duty Cycle	100mA Load	●	83	87		%
Switch Current Limit	Rising (Note 4)		0.8	1	1.25	A
DA Pin Current to Stop Osc			0.6	1	1.25	A
Switch V_{CESAT}	I_{SW} = 500mA			400		mV
Switch Leakage Current					2	µA
Minimum Boost Voltage Above Switch	I_{SW} = 500mA			1.6	2.2	V
BOOST Pin Current	I_{SW} = 500mA			10	18	mA
BOOST Schottky Forward Drop	I_{OUT} = 50mA			0.7	0.9	V
EN/UVLO Threshold High	Rising		1.17	1.23	1.29	V
EN/UVLO Threshold Hysteresis				50		mV
EN/UVLO Input Current	$V_{EN/UVLO}$ = 5V $V_{EN/UVLO}$ = 0V			25	50 1	µA µA
Buck Soft-Start Time				0.9	1.8	ms
LDO Minimum Input Voltage V_{CC2}	I_{LOAD} = 200mA, V_{OUT2} = 0.8V, V_{IN} = 4.0V			1.1	1.38	V
LDO Feedback Voltage FB2		●	782	797	810	mV
LDO FB2 Bias Current		●		20	300	nA
LDO Line Regulation				0.020		%/V
LDO Load Regulation				–1		mV
LDO Dropout Voltage (V_{CC2} to V_{OUT2})	I_{LOAD} = 10mA I_{LOAD} = 10mA I_{LOAD} = 200mA	 ●		45 310	65 145 	mV mV mV
LDO Dropout Voltage (V_{IN} to V_{OUT2})	I_{LOAD} = 200mA I_{LOAD} = 200mA	 ●		1.1	1.4 1.7	V V
LDO Current Limit	 	 ●	 210	270 	 	mA mA
EN2 Pin Threshold	Rising Falling	● ●	 0.5	1.3 0.8	1.6 	V V
LDO Soft-Start Time				0.6	1.2	ms
NPG V_{CESAT}	I_{NPG} = 1mA, V_{FB} = V_{FB2} = 850mV				0.4	V
NPG Leakage	V_{NPG} = 16V, V_{FB} = V_{FB2} = 750mV				0.5	µA
FB2 NPG Threshold, % of Regulation Voltage	V_{FB} = 800mV, V_{FB2} Rising		88	90	92	%

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, BOOST = 15.3V, V_{CC2} = 3.3V, OUT2 = 1.8V unless otherwise noted. (Notes 2, 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
FB NPG Threshold, % of Regulation Voltage	V_{FB2} = 800mV, V_{FB} Rising		88	90	92	%
NPG Threshold Hysteresis				25		mV

Note1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3645E is guaranteed to meet performance specifications from 0°C to 125°C. Specifications over the –40°C to 125°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LT3645I is guaranteed over the full –40°C to 125°C operating temperature range. The LT3645H is guaranteed over the full –40°C to 150°C operating temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

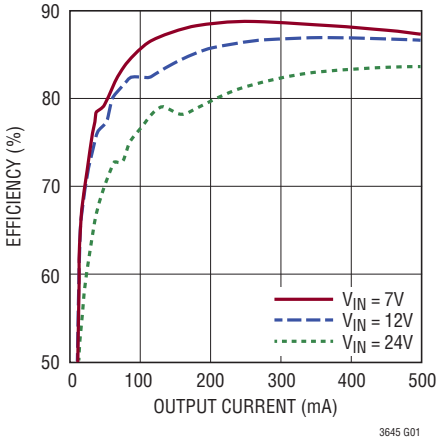
Note 3: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed the maximum junction operating temperature when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may result in device degradation or failure.

Note 4: Current Measurements are performed when the outputs are not switching. Slope compensation reduces current limit at high duty cycles.

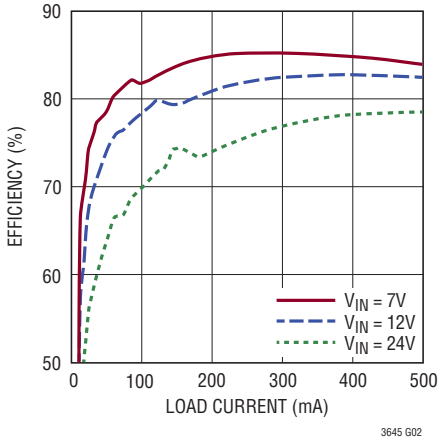
Note 5: Absolute Maximum Voltage at V_{IN} and EN/UVLO pins is 55V for nonrepetitive one second transients, and 36V for continuous operation.

TYPICAL PERFORMANCE CHARACTERISTICS

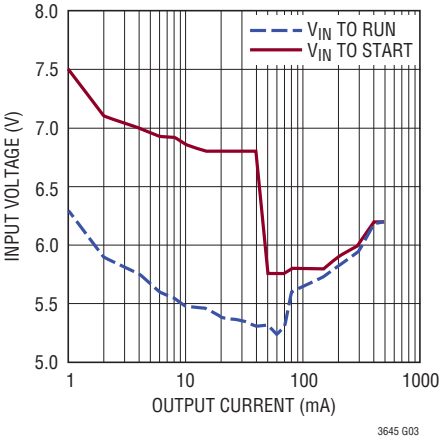
Efficiency V_{OUT} = 5V



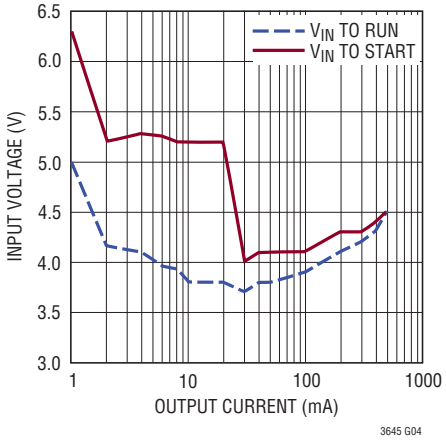
Efficiency V_{OUT} = 3.3V



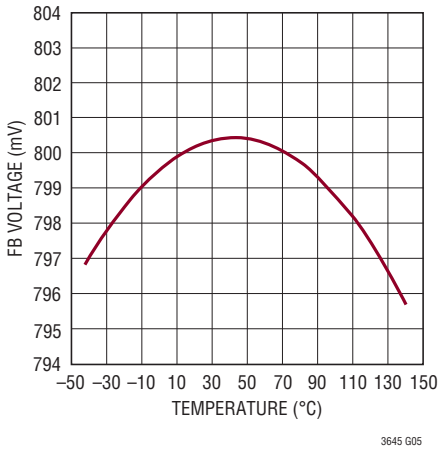
Buck Minimum Input Voltage, V_{OUT} = 5V



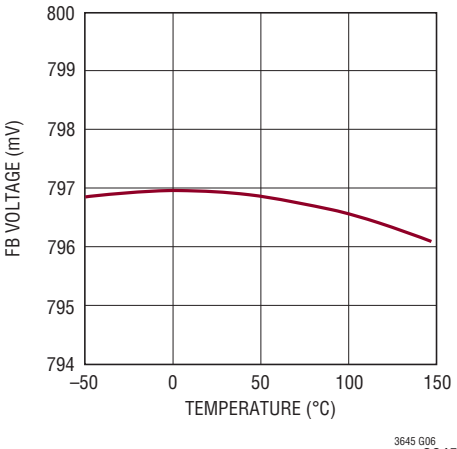
Buck Minimum Input Voltage, V_{OUT} = 3.3V



FB Voltage

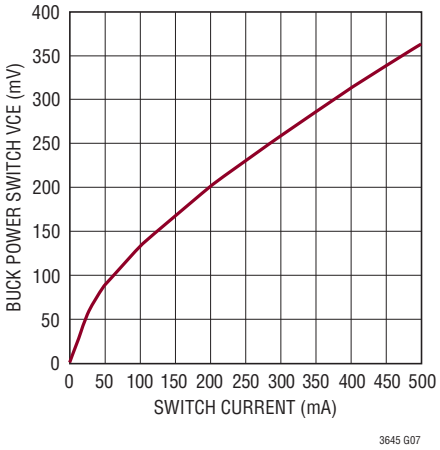


FB2 Voltage

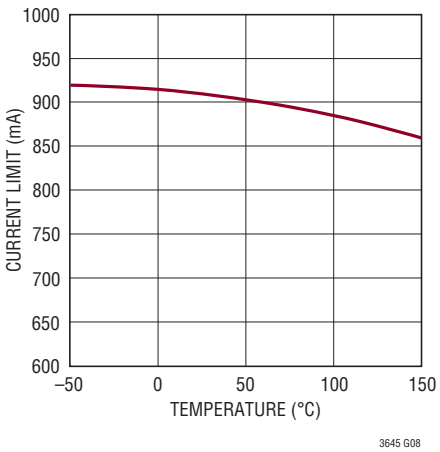


TYPICAL PERFORMANCE CHARACTERISTICS

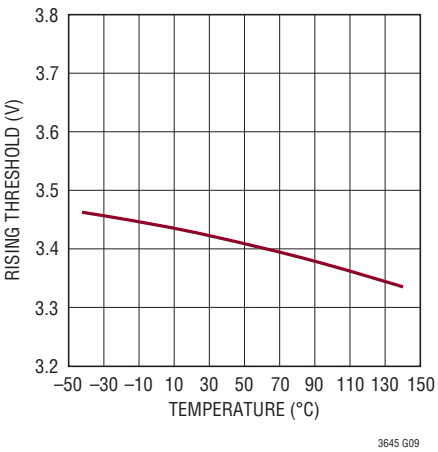
Buck Power Switch Voltage Drop



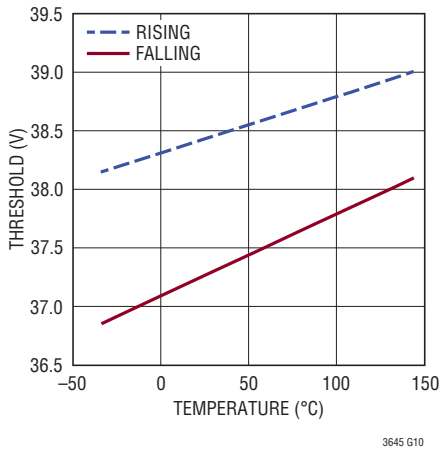
Buck Power Switch Current Limit



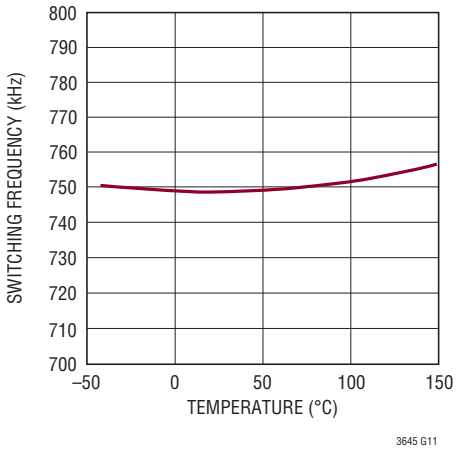
Undervoltage Lockout



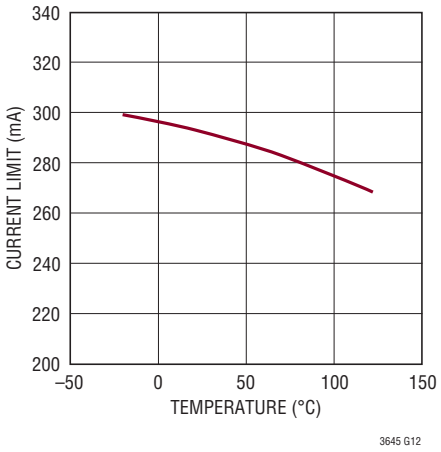
Overvoltage Lockout



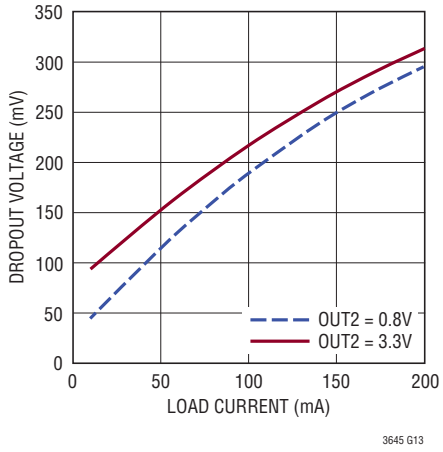
Switching Frequency



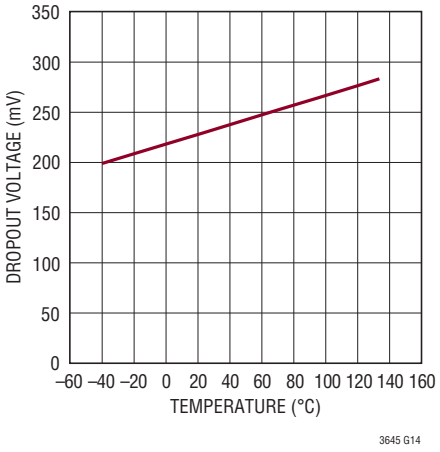
LDO Power Transistor Current Limit



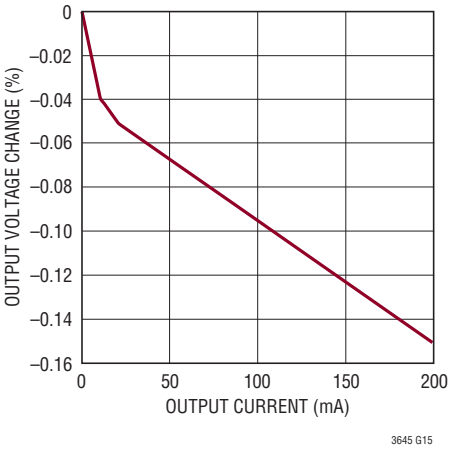
LDO Dropout Voltage to V_{CC2}



LDO Dropout Voltage

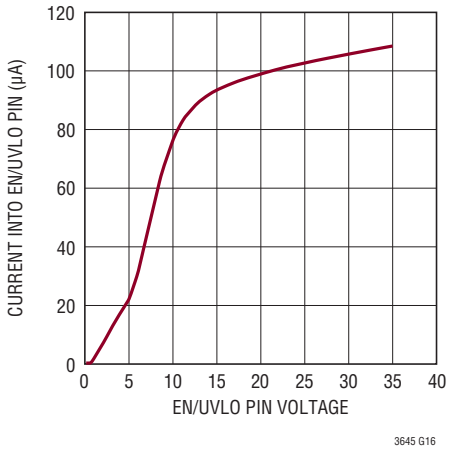


LDO Load Regulation

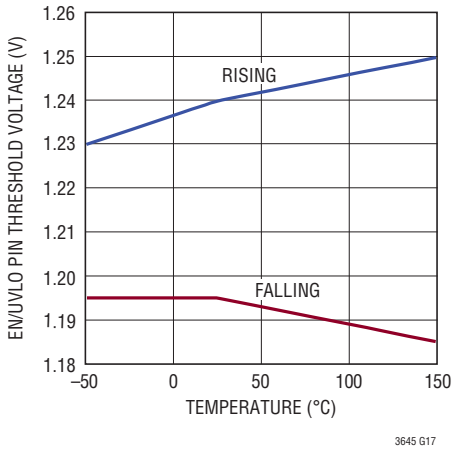


TYPICAL PERFORMANCE CHARACTERISTICS

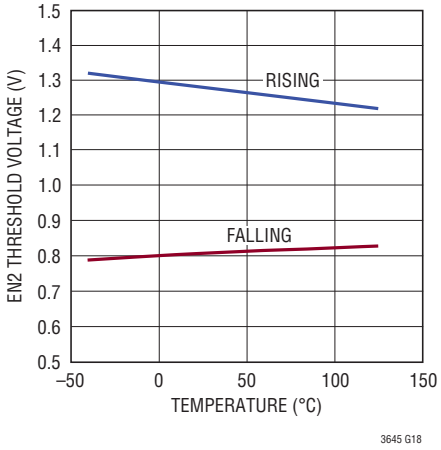
EN/UVLO Pin Current



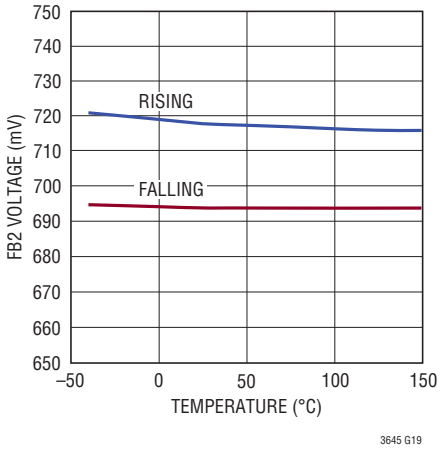
EN/UVLO PIN Threshold Voltage



EN2 Threshold Voltage



NPG Threshold Voltage, FB = 0.8V



PIN FUNCTIONS (MSOP/QFN)

EN/UVLO (Pin 1/Pin 5): The EN/UVLO pin is used to enable the buck switching regulator and the low dropout linear regulator (LDO). An accurate threshold of 1.23V allows the user to set the undervoltage lockout point with a simple resistor divider, see Precision Undervoltage Lockout section for more information. The EN/UVLO pin can be tied directly to V_{IN} if the UVLO or shutdown is not used.

FB (Pin 2/Pin 6): The FB pin programs the buck output voltage. The LT3645 regulates the FB pin to 0.8V. The feedback resistor divider tap should be connected to this pin. The output voltage is programmed according to the following equation:

$$R1 = R2 \bullet \left(\frac{V_{OUT}}{0.8} - 1 \right)$$

where R1 connects between OUT and FB and R2 connects between FB and GND. A good value for R2 is 10k.

GND (Pin 3, Exposed Pad Pin 13/Pin 7, Exposed Pad Pin 17): The GND pin should be tied to a local ground plane below the LT3645 and the circuit components. Return the feedback dividers from FB and FB2 to this pin. The exposed pad must be soldered to the PCB and electrically connected to ground. Use a large ground plane and thermal vias to optimize thermal performance.

DA (Pin 4/Pin 8): The DA pin senses the external catch diode current and prevents the buck regulator from switching if the sensed current is too high. Connect the anode of the external Schottky catch diode to this pin.

BOOST (Pin 5/Pin 10): The BOOST pin provides a drive voltage to the internal bipolar NPN power switch. Tie a 0.1µF capacitor between the BOOST and SW pins.

SW (Pin 6/Pin 9): The SW pin is the output of the internal buck power switch. Connect the inductor and the cathode of the external catch Schottky diode to this pin.

V_{IN} (Pin 7/ Pin 11): The V_{IN} pin supplies current to the LT3645's internal circuitry, to the internal buck power switch, and to the LDO. The V_{IN} pin must be locally bypassed.

V_{CC2} (Pin 8/Pin 14): The V_{CC2} pin supplies current to the linear regulator's output device. The V_{CC2} pin is also the anode of an internal Schottky diode used to generate the BOOST voltage. The V_{CC2} pin must be tied to a voltage source greater than 2.5V to utilize the internal Schottky boost diode. If the V_{CC2} pin is tied to a voltage lower than 2.5V, then an external Schottky diode must be connected between a power supply greater than 2.5V (anode) and the BOOST pin (cathode). Bypass this pin to ground with a 0.1µF capacitor close to the part.

OUT2 (Pin 9/Pin 15): The OUT2 pin is the output of the LDO. Connect a capacitor of at least 0.47µF from this pin to ground. See Frequency Compensation (LDO) section for more details.

FB2 (Pin 10/Pin 16): The FB2 pin programs the LDO output voltage. The LT3645 regulates the FB2 pin to 0.797V. The feedback resistor divider tap should be connected to this pin. The output voltage is programmed according to the following equation:

$$R3 = R4 \bullet \left(\frac{V_{OUT2}}{0.797} - 1 \right)$$

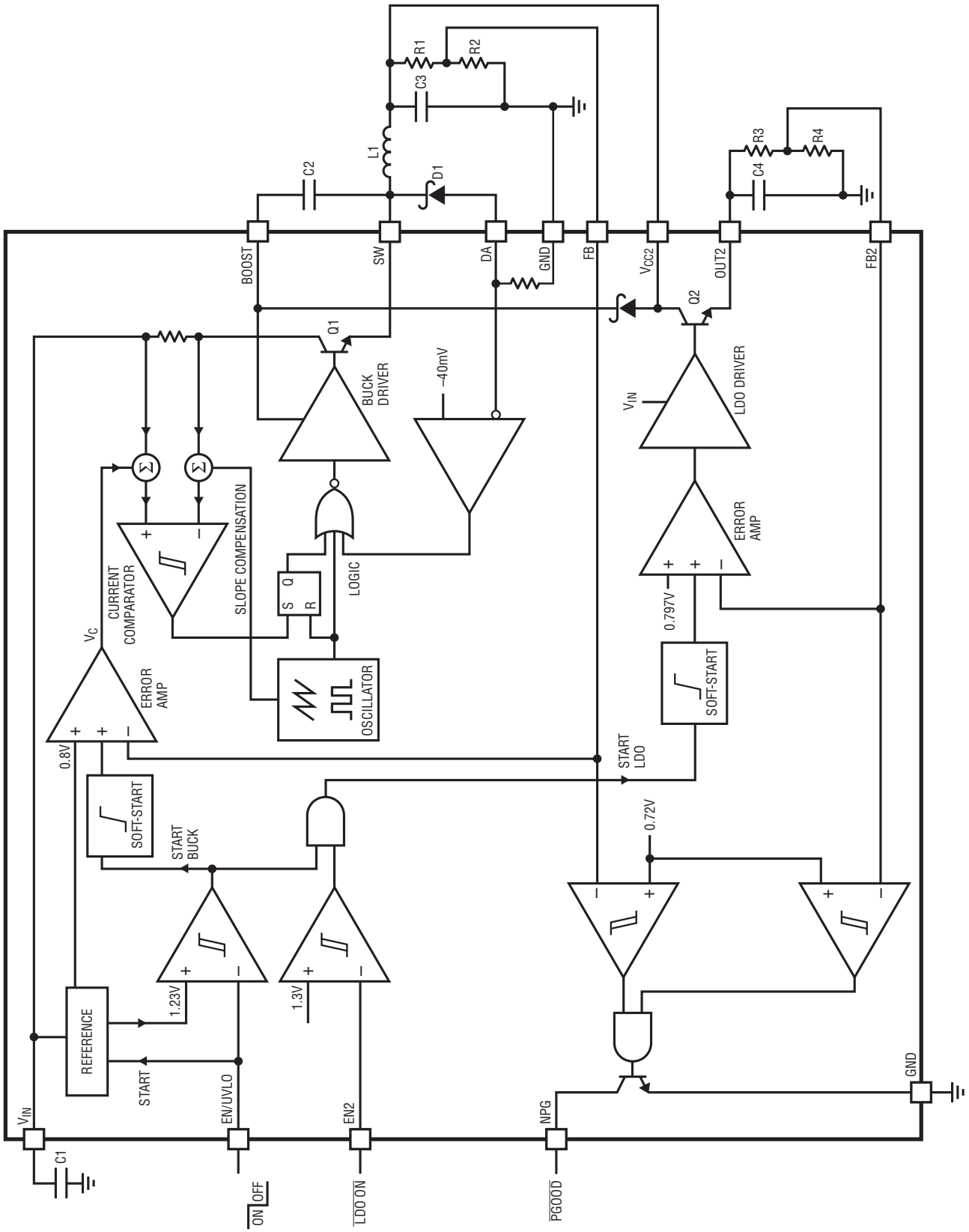
where R3 connects between OUT2 and FB2 and R4 connects between FB2 and GND. A good value for R4 is 10k.

EN2 (Pin 11/Pin 4): The EN2 pin is used to enable the linear regulator. Pull this pin above 1.6V to enable the LDO. Pull EN2 below 0.5V to disable the LDO.

NPG (Pin 12/Pin 3): The NPG pin is an open-collector output used to indicate that both buck and LDO output voltages are in regulation. The NPG pin pulls low when FB and FB2 both exceed 720mV.

NC (Pins 1, 2, 12, 13, QFN Only): No Connect Pins. Tie these to ground.

BLOCK DIAGRAM



OPERATION

The LT3645 includes a constant frequency, current mode step-down buck switching regulator together with a low-dropout regulator (LDO).

If EN/UVLO is less than ~0.7V, both the buck and LDO are off, the output is disconnected and the input current is less than 2µA. The buck turns on when EN/UVLO is greater than 1.23V. An undervoltage lockout (UVLO) turns the buck and LDO off when V_{IN} is less than 3.4V. An overvoltage lockout (OVLO) turns the buck and LDO off when V_{IN} is greater than 38.5V. The part will withstand nonrepetitive one second input voltage transients up to 55V. An internal thermal shutdown circuit monitors the die temperature and shuts both the buck and LDO off if the die temperature exceeds ~160°C. The thermal shutdown has 10 degrees of hysteresis.

An internal regulator provides power to the control circuitry and produces the 0.8V feedback voltage for the buck and LDO error amplifiers.

An internal, fixed-frequency oscillator in the step-down regulator enables an RS flip-flop, turning on the internal power switch Q1. A comparator monitors the current flowing between the V_{IN} and SW pins, turning the switch off when this current reaches a level determined by the voltage at V_C and the internal slope-compensation. An error amplifier servos the V_C node. The output of an external resistor divider between OUT and ground is tied to the V_{FB} pin and presented to the negative error amp input. The positive input to the error amp is a 0.8V reference, so the voltage loop forces the V_{FB} pin to 0.8V. The reference voltage of the buck error amplifier is ramped over 900µs during the soft-start period. When V_C rises, it results in an increase in output current, and when V_C falls, it results in less output current. Current limit is provided by an active clamp on the V_C node.

The buck power switch (Q1) is driven from the BOOST pin. An external capacitor and internal diode are used to generate a voltage at the BOOST pin that is higher than the input supply, which allows the driver to fully saturate the internal bipolar NPN power switch for efficient operation. An external diode can be used to make the BOOST drive more effective at low output voltages.

The oscillator reduces the LT3645's operating frequency during the soft-start period. This frequency foldback helps to control the output current during startup.

The current in the external catch diode (D1) is sensed through the DA pin. If the catch diode current exceeds 0.9A, the oscillator frequency is decreased. This prevents current runaway during startup or overload.

The LDO only operates if EN/UVLO is greater than 1.23V and EN2 is greater than 1.3V. If EN/UVLO is low and EN2 is high, the LDO will not start. When EN2 > 1.3V and EN/UVLO > 1.23V, the LDO power transistor will turn on and regulate the output at the OUT2 pin. An error amplifier driving Q2 has its positive input at the 0.797V reference. The output of an external resistor divider between OUT2 and ground is tied to the V_{FB2} pin and presented to the negative error amp input, forcing the V_{FB2} pin to 0.797V. The reference voltage of the LDO error amplifier is ramped over 600µs during the soft-start period. The LDO power transistor (Q2) is driven from the V_{IN} pin. Q2 is a bipolar NPN which draws its collector current from the V_{CC2} pin.

The NPG pin is an open-collector output that indicates when both buck and LDO outputs are in at least 90% in regulation. When FB and FB2 rise above 720mV, the NPG pin is pulled low.

APPLICATIONS INFORMATION

FB Resistor Networks

The output voltages are programmed with resistor dividers between the outputs and the V_{FB} and V_{FB2} pins. Choose the resistors according to

$$R1 = R2 \bullet \left(\frac{V_{OUT}}{0.8} - 1\right)$$

$$R3 = R4 \bullet \left(\frac{V_{OUT2}}{0.797} - 1\right)$$

R2 and R4 should be 20k or less to avoid bias current errors. In the step-down converter, an optional phase lead capacitor of 22pf between V_{OUT} and V_{FB} reduces light-load ripple.

Input Voltage Range

The maximum operating input voltage for the LT3645 is 36V. The minimum input voltage is determined by either the LT3645's minimum operating voltage of 3.6V or by its maximum duty cycle. The duty cycle is the fraction of time that the internal switch is on and is determined by the input and output voltages:

$$DC = (V_{OUT} + V_D)/(V_{IN} – V_{SW} + V_D)$$

where V_D is the forward voltage drop of the catch diode (~0.4V) and V_{SW} is the voltage drop of the internal switch (~0.4V at maximum load). This leads to a minimum input voltage of:

$$V_{IN(MIN)} = ((V_{OUT} + V_D)/DC_{MAX}) – V_D + V_{SW}$$

with DC_{MAX} = 0.83 for the LT3645.

The maximum input voltage is determined by the absolute maximum ratings of the V_{IN} and BOOST pins. For fixed frequency operation, the maximum input voltage is determined by the minimum duty cycle, which is:

$$V_{IN(MAX)} = ((V_{OUT} + V_D)/DC_{MIN}) – V_D + V_{SW}$$

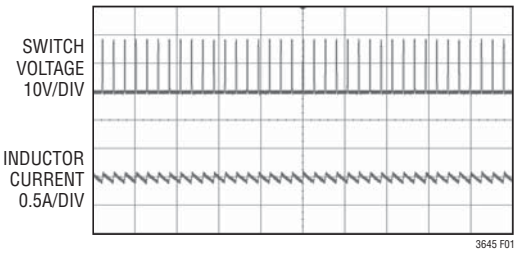
with DC_{MIN} = 0.075 for the LT3645.

Note that this is a restriction on the operating input voltage for continuous mode operation. The circuit will continue to regulate the output up until the overvoltage lockout input voltage (38.5V). The part will tolerate transient input voltages up to 55V, but once the input voltage exceeds 36V, the power switch will shut off and stop regulating the output voltage until the input voltage falls below 36V.

Minimum On Time

The LT3645 will operate at the correct frequency while the input voltage is below $V_{IN(MAX)}$. At input voltages that exceed $V_{IN(MAX)}$, the LT3645 will still regulate the output properly (up to 38.5V); however, the LT3645 will skip pulses to regulate the output voltage resulting in increased output voltage ripple.

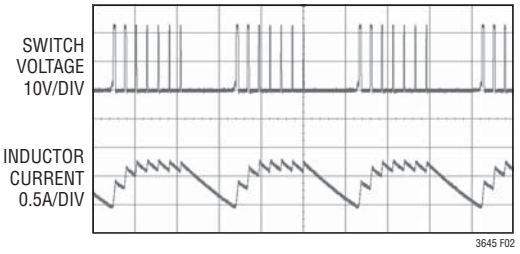
Figure 1 illustrates switching waveforms for a LT3645 application with V_{OUT} = 1.2V near $V_{IN(MAX)}$ = 21.3V.



V_{IN} = 18V
V_{OUT} = 1.2V
I_{OUT} = 500mA
C_{OUT} = 10µF
L = 10µH

Figure 1.

As the input voltage is increased, the part is required to switch for shorter periods of time. Delays associated with turning off the power switch dictate the minimum on time of the part. The minimum on time for the LT3645 is 100ns. Figure 2 illustrates the switching waveforms when the input voltage is increased to V_{IN} = 22V.



V_{IN} = 22V
V_{OUT} = 1.2V
I_{OUT} = 500mA
C_{OUT} = 10µF
L = 10µH

Figure 2.

APPLICATIONS INFORMATION

Table 1. Inductor Vendors

Vendor	URL	Part Series	Inductance Range (µH)	Size (mm)
Sumida	www.sumida.com	CDRH4D28 CDRH5D28 CDRH8D28	1.2 to 4.7 2.5 to 10 2.5 to 33	4.5 × 4.5 5.5 × 5.5 8.3 × 8.3
Toko	www.toko.com	A916CY D585LC	2 to 12 1.1 to 39	6.3 × 6.2 8.1 × 8.0
Würth Elektronik	www.we-online.com	WE-TPC(M) WE-PD2(M) WE-PD(S)	1 to 10 2.2 to 22 1 to 27	4.8 × 4.8 5.2 × 5.8 7.3 × 7.3

Now the required on time has decreased below the minimum on time of 100ns. Instead of the switch pulse width becoming narrower to accommodate the lower duty cycle requirement, the part skips a few pulses so that the average inductor current meets and does not exceed the load current requirement.

The LT3645 is robust enough to survive prolonged operation under these conditions as long as the peak inductor current does not exceed 1.2A. Inductor saturation due to high current may further limit performance in this operating region.

Inductor Selection and Maximum Output Current

Choose the inductor value according to:

$$L = 2.2 \bullet (V_{OUT} + V_D)/f$$

where V_D is the forward voltage drop of the catch diode (~0.4V), f is the switching frequency in MHz and L is in µH. With this value, there will be no subharmonic oscillation for applications with 50% or greater duty cycle. For robust operation in fault conditions, the saturation current should be above 1.5A. To keep efficiency high, the series resistance (DCR) should be less than 0.1Ω. Table 1 lists several inductor vendors. If the buck load current is less than 500mA, then a lower valued inductor can be used.

Catch Diode

Depending on load current, a 500mA to 1A Schottky diode is recommended for the catch diode, D1. The diode must have a reverse voltage rating equal to or greater than the overvoltage lockout voltage (38.5V). The ON Semiconductor MBRA140T3 and Central Semiconductor CMMSH1-40 are good choices, as they are rated for 1A continuous forward current and a maximum reverse voltage of 40V.

Input Filter Network

Bypass V_{IN} with a 1µF or higher ceramic capacitor of X7R or X5R type. Y5V types have poor performance over temperature and applied voltage and should not be used. A 1µF ceramic capacitor is adequate to bypass the LT3645 and will easily handle the ripple current. However, if the input power source has high impedance, or there is significant inductance due to long wires or cables, additional bulk capacitance might be necessary. This can be provided with a low performance (high ESR) electrolytic capacitor in parallel with the ceramic device. Step-down regulators draw current from the input supply in pulses with very fast rise and fall times. The input capacitor is required to reduce the resulting voltage ripple at the LT3645 input and to force this very high frequency switching current into a tight local loop, minimizing EMI. A 1µF capacitor is capable of this task, but only if it is placed close to the LT3645 and catch diode (see the PCB layout section). A second precaution regarding the ceramic input capacitor concerns the maximum input voltage rating of the LT3645. A ceramic input capacitor combined with trace or cable inductance forms a high quality (underdamped) tank circuit. If the LT3645 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT3645's voltage rating. This situation can easily be avoided. For more details, see Linear Technology Application Note 88.

APPLICATIONS INFORMATION

Output Capacitor

The output capacitor has two essential functions. Along with the inductor, it filters the square wave generated by the LT3645 to produce the DC output. In this role it determines the output ripple so low impedance at the switching frequency is important. The second function is to store energy in order to satisfy transient loads and stabilize the LT3645's control loop.

Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. A good value is:

$$C_{OUT} = 26.4/(V_{OUT} \bullet f)$$

where f is the switching frequency in MHz and C_{OUT} is in µF. This choice will provide low output ripple and good transient response. C_{OUT} = 10µF is a good choice for output voltages above 2.5V. For lower output voltages use 22µF or higher.

Transient performance can be improved with a high value capacitor, but a phase lead capacitor across the feedback resistor R1 may be required to get the full benefit (see the Compensation section). Using a small output capacitor results in an increased loop crossover frequency.

Use X5R or X7R types and keep in mind that a ceramic capacitor biased with V_{OUT} will have less than its nominal capacitance. High performance electrolytic capacitors can be used for the output capacitor. Low ESR is important, so choose one that is intended for use in switching regulators. The ESR should be specified by the supplier and should be 0.1Ω or less. Such a capacitor will be larger than a ceramic capacitor and will have a larger capacitance, because the capacitor must be large to achieve low ESR.

Table 2 lists several capacitor vendors.

Table 2. Capacitor Vendors

AVX	www.avxcorp.com
Murata	www.murata.com
Taiyo Yuden	www.t-yuden.com
Vishay Siliconix	www.vishay.com
TDK	www.tdk.com

BOOST Pin Considerations

The external capacitor C2 and an internal Schottky diode connected between the V_{CC2} and BOOST pins form a charge pump circuit which is used to generate a boost voltage that is higher than the input voltage (V_{IN}). In most application circuits where the duty cycle is less than 50%, use C2 = 0.1µF. If the duty cycle is higher than 50% then use C2 = 0.22µF.

The BOOST pin must be at least 2.2V above the SW pin to fully saturate the NPN power switch (Q1). The forward drop of the internal Schottky diode is 0.8V. This means that V_{CC2} must be tied to a supply greater than 2.6V.

V_{CC2} may be tied to a supply between 2.2V and 2.6V if an external Schottky diode (such as a BAS70) is connected from V_{CC2} (anode) to BOOST (cathode).

If no voltage supply greater than 2.6V is available, then an external boost Schottky diode can be tied from the V_{IN} pin (anode) to the BOOST pin (cathode) as shown in Figure 3. In this configuration, the BOOST capacitor will be charged to approximately the V_{IN} voltage, and will change if V_{IN} changes. In this configuration the maximum operating V_{IN} is 25V, because when V_{IN} = 25V, then when the power switch Q1 turns on, V_{SW} ~ 25V, and since the boost capacitor is charged to 25V, the BOOST pin will be at 50V. This connection is not as efficient as the others because the BOOST pin current comes from a higher voltage.

The minimum operating voltage of an LT3645 application is limited by the undervoltage lockout (~3.4V) and by the maximum duty cycle as outlined above. For proper startup, the minimum input voltage is also limited by the

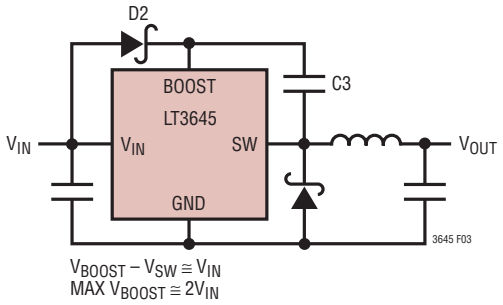


Figure 3.

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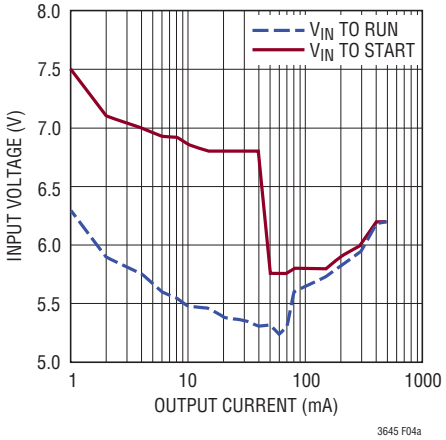
boost circuit. If the input voltage is ramped slowly, or if the LT3645 is turned on with the EN/UVLO pin when the output is already in regulation, then the boost capacitor might not be fully charged. Because the boost capacitor is charged with the energy stored in the inductor, the circuit will rely on some minimum load current to get the boost circuit running properly. This minimum load generally goes to zero once the circuit has started. The worst case situation is when V_{IN} is ramping very slowly. Figure 4a shows the minimum input voltage needed to start a 5V application versus output current. Figure 4b shows the minimum input voltage needed to start a 3.3V application versus output current.

Soft-Start

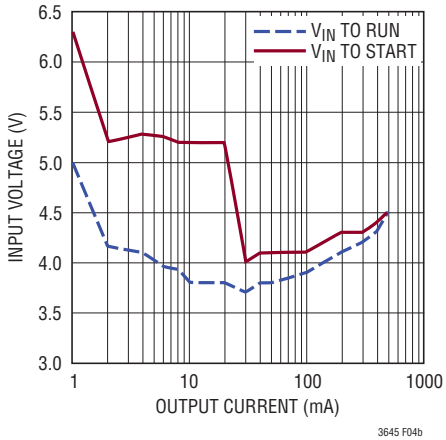
The LT3645 includes a 500µs internal soft-start for the buck converter and a 500µs soft-start for the LDO regulator. Both soft-starts are reset if the EN/UVLO pin is low, if V_{IN} drops below 3.4V (undervoltage), if V_{IN} exceeds 36V (overvoltage), or when the die temperature exceeds 160°C (thermal shutdown). The soft-start for the LDO can also be reset by pulling the EN2 pin low. The soft-start functions act to reduce the maximum input current during startup. Soft-start can not be disabled in the LT3645.

Reversed Input Protection

In some systems, the output will be held high when the input to the LT3645 is absent. This may occur in battery charging applications or in battery backup systems where a battery or some other supply is diode OR'd with the LT3645's output. If the V_{IN} pin is allowed to float and the EN/UVLO pin is held high (either by a logic signal or because it is tied to V_{IN}), then the LT3645's internal circuitry will draw its quiescent current through its SW pin. This is fine if the system can tolerate a few mA in this state. You can reduce this current by grounding the EN/UVLO pin, then the SW pin current will drop to essentially zero. However, if the V_{IN} pin is grounded while the output is held high, then parasitic diodes inside the LT3645 can



(4a) Typical Minimum Input Voltage, V_{OUT} = 5V



(4b) Typical Minimum Input Voltage, V_{OUT} = 3.3V

Figure 4.

APPLICATIONS INFORMATION

pull large currents from the output through the SW pin and the V_{IN} pin. Figure 5 shows a circuit that will run only when the input voltage is present and that protects against a shorted or reversed input.

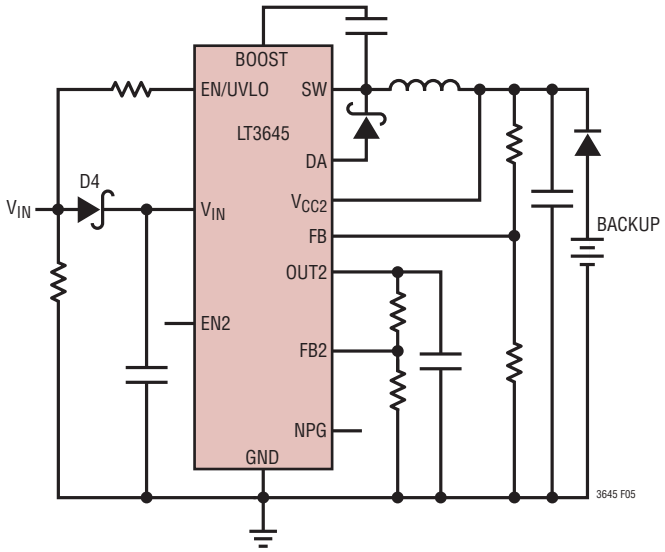


Figure 5. Diode D4 Prevents a Shorted Input from Discharging a Backup Battery Tied to the Output; It Also Protects the Circuit from a Reversed Input. The LT3645 Runs Only When the Input Is Present

Frequency Compensation (Buck)

The LT3645 uses current mode control to regulate the loop. This simplifies loop compensation. In particular, the LT3645 does not require the ESR of the output capacitor for stability, allowing the use of ceramic capacitors to achieve low output ripple and small circuit size. A low ESR output capacitor will typically provide for a greater margin of circuit stability than an otherwise equivalent capacitor with higher ESR, although the higher ESR will tend to provide a faster loop response. Figure 6 shows an equivalent circuit for the LT3645 control loop.

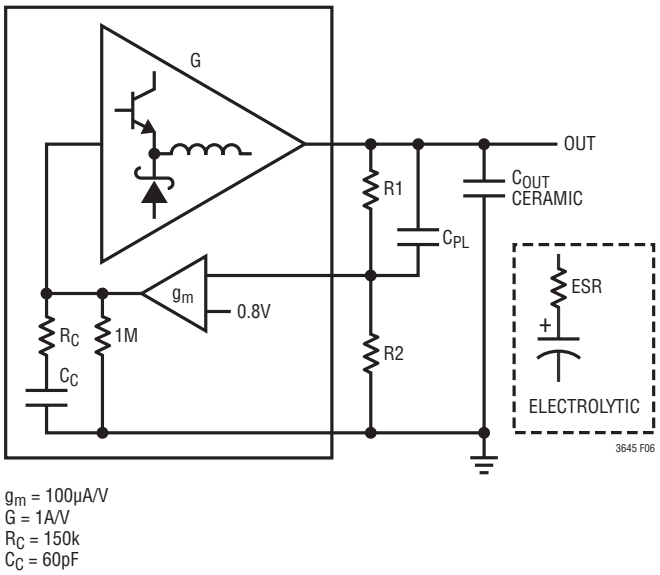


Figure 6. Model for Loop Response

The error amplifier (g_m) is a transconductance type with finite output impedance. The power section, consisting of the modulator, power switch, and inductor, is modeled as a transconductance amplifier (G) generating an output current proportional to the voltage at the V_C node. Note that the output capacitor integrates this current, and that the capacitor on the V_C node (C_C) integrates the error amplifier output current, resulting in two poles in the loop. R_C provides a zero. With the recommended output capacitor, the loop crossover occurs above the R_CC_C zero. This simple model works well as long as the value of the inductor is not too high and the loop crossover frequency is much lower than the switching frequency. With a larger ceramic capacitor that will have lower ESR, crossover may be lower and a phase lead capacitor connected across R1 in the feedback divider may improve the transient response. Large electrolytic capacitors may have an ESR

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large enough to create an additional zero, and the phase lead might not be necessary. If the output capacitor is different than the recommended capacitor, stability should be checked across all operating conditions, including input voltage and temperature.

Figure 7 shows the transient response of the LT3645 with a few output capacitor choices. The output is 3.3V. The load current is stepped from 0.25A to 0.5A and back to 0.25A, and the oscilloscope traces show the output voltage. The upper photo shows the recommended value. The second photo shows the improved response (faster recovery) resulting from a phase lead capacitor.

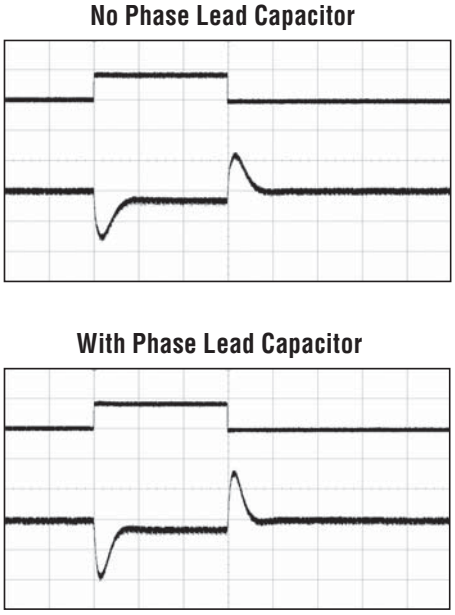


Figure 7.

Frequency Compensation (LDO)

The LT3645 LDO requires an output capacitor for stability. It is designed to be stable with most low ESR capacitors (typically ceramic, tantalum or low ESR electrolytic). A minimum output capacitor of 2.2µF with an ESR of 0.5Ω or less is recommended to prevent oscillations. Larger values of output capacitance decrease peak deviations and provide improved transient response for larger load current changes. Bypass capacitors, used to decouple individual components powered by the LT3645, increase the effective output capacitor value. For improvement in transient performance, place a capacitor across the OUT2 pin and the FB2 pin. Capacitors up to 1nF can be used. This bypass capacitor reduces system noise as well.

Extra consideration must be given to the use of ceramic capacitors. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior across temperature and applied voltage. The most common dielectrics used are specified with EIA temperature characteristic codes of Z5U, Y5V, X5R and X7R. The Z5U and Y5V dielectrics are good for providing high capacitances in a small package, but they tend to have strong voltage and temperature coefficients as shown in Figures 8 and 9.

When used with a 5V regulator, a 16V 10µF Y5V capacitor can exhibit an effective value as low as 1µF to 2µF for the DC bias voltage applied and over the operating

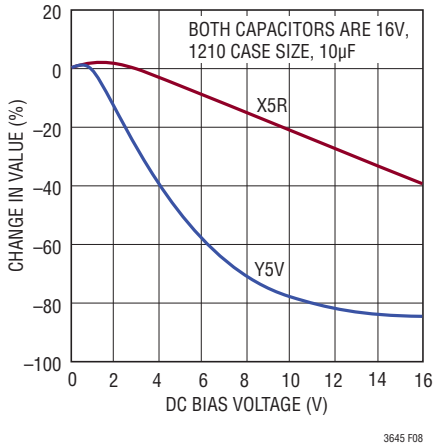


Figure 8. Ceramic Capacitor DC Bias Characteristics

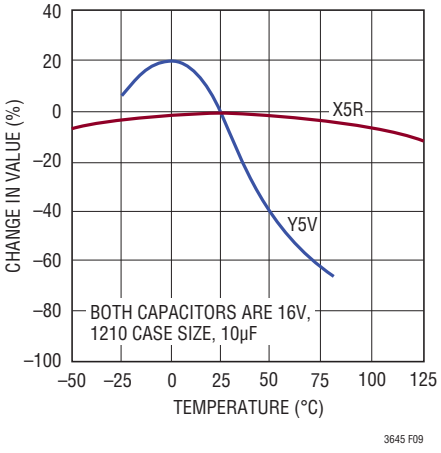


Figure 9. Ceramic Capacitor Temperature Characteristics

APPLICATIONS INFORMATION

temperature range. The X5R and X7R dielectrics result in more stable characteristics and are more suitable for use as the output capacitor. The X7R type has better stability across temperature, while the X5R is less expensive and is available in higher values. Care still must be exercised when using X5R and X7R capacitors; the X5R and X7R codes only specify operating temperature range and maximum capacitance change over temperature. Capacitance change due to DC bias with X5R and X7R capacitors is better than Y5V and Z5U capacitors, but can still be significant enough to drop capacitor values below appropriate levels. Capacitor DC bias characteristics tend to improve as component case size increases, but expected capacitance at operating voltage should be verified. Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress, similar to the way a piezoelectric microphone works. For a ceramic capacitor the stress can be induced by vibrations in the system or thermal transients.

Precision Undervoltage Lockout

The EN/UVLO pin has an accurate 1.23V threshold that can be used to shutdown the part when the input voltage drops below a specified level. To perform this function, a resistor divider between the EN/UVLO pin and the V_{IN} pin can be tied as shown in Figure 10. The resistor values can be determined from the following equation:

$$R7 = R8 \bullet \left(\frac{V_{IN(MIN)}}{1.23V} - 1 \right)$$

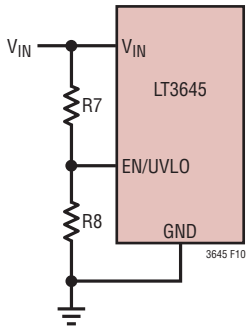


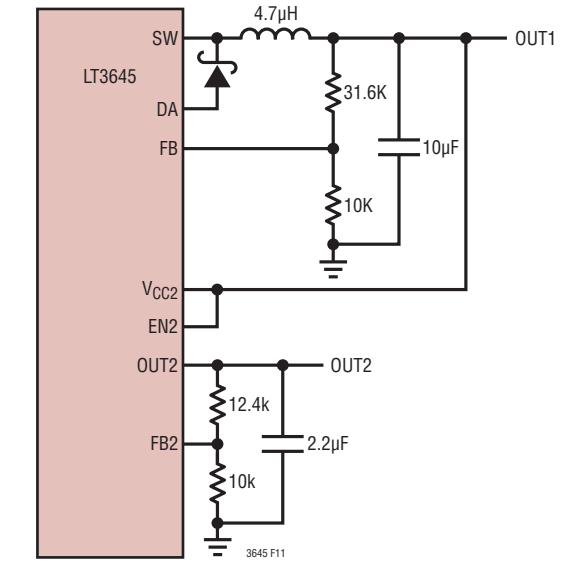
Figure 10. Precision UVLO Circuit

With the resistor divider connected, the part will only operate at input voltages greater than $V_{IN(MIN)}$. Note that the resistor divider will always draw current from V_{IN}. To reduce this current, the user might use large value resistors for R7 and R8. This is acceptable as long as R7 and R8 are selected such that they can supply 10µA to the EN/UVLO pin. A good value for R8 is 100k.

Output Voltage Sequencing

There are a few applications available for sequencing the buck and LDO output voltages. In Figures 11 and 12, the buck output (OUT1) is programmed to 3.3V, while the LDO output (OUT2) is programmed to 1.8V.

Figure 11 shows a standard configuration where OUT1 and OUT2 come up as soon as possible. In this configuration,



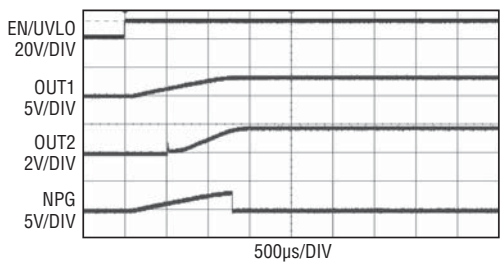


Figure 11. OUT1 and OUT2 Come Up as Soon as Possible

APPLICATIONS INFORMATION

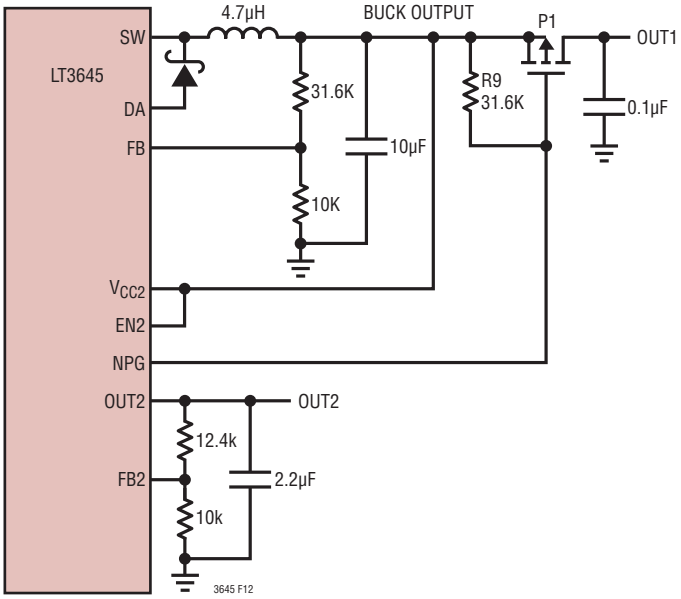
there is a small delay before OUT2 begins ramping up as OUT2 has to wait until V_{CC2} is above 2V before power can be supplied to OUT2.

Figure 12 utilizes the NPG pin to sequence the outputs such that OUT1 comes into regulation after OUT2 is already in regulation. When the part is off, the buck output, OUT1 and OUT2 will be 0V. The NPG pin will be high impedance, PFET P1 will be off and OUT1 will be disconnected from the buck output. When the part is turned on, first the buck output will come up to 3.3V. Once the Buck output is in regulation, the LDO output, OUT2 will come up to 1.8V. When both OUT2 and the buck output are in regulation, the NPG pin will pull low, turning on PFET P1 and supplying power to OUT1.

The NPG pin is capable of sinking 1mA and will pull the gate of P1 down to 300mV. Therefore R9 should be chosen such that:

$$R9 < (V_{OUT1} - 300mV)/1mA$$

Where R7 is in Ω. For a 3.3V buck output application, PFET P1 must be able to source 300mA to OUT1 from the buck output with ~3V of gate drive. Note that PFET



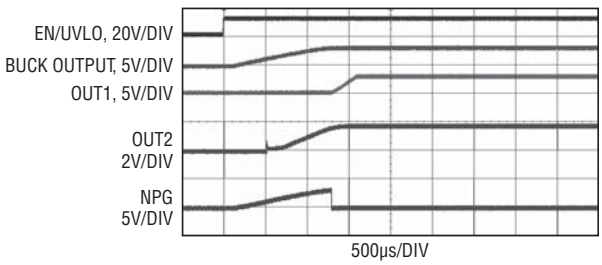


Figure 12. OUT2 Comes Up Before OUT1

APPLICATIONS INFORMATION

P1 has a finite on-resistance which will result in power dissipation and some loss in efficiency. For higher buck output voltage applications, a smaller PFET may be used since the gate drive will be higher.

PCB Layout

For proper operation and minimum EMI, care must be taken during printed circuit board layout. Figure 13 shows the recommended component placement with trace, ground plane, and via locations.

Note that large, switched currents flow in the LT3645's V_{IN} and SW pins, the catch diode (D1), and the input capacitor (C1). The loop formed by these components should be as small as possible and tied to system ground in only one place. These components, along with the inductor and output capacitor, should be placed on the same side of the circuit board, and their connections should be made on that layer. Place a local, unbroken ground system ground in only one place. These components, along with the inductor and output capacitor, should be placed on the same side of the circuit board, and their connections should be made on that layer. Place a local, unbroken ground plane below these components, and tie this ground plane to system ground at one location (ideally at the ground terminal of the output capacitor C1). The SW and BOOST nodes should be kept as small as possible. Finally, keep the FB nodes small so that the ground pin and ground traces will shield them from the SW and BOOST nodes. Include vias near the exposed GND pad of the LT3645 to help remove heat from the LT3645 to the ground plane.

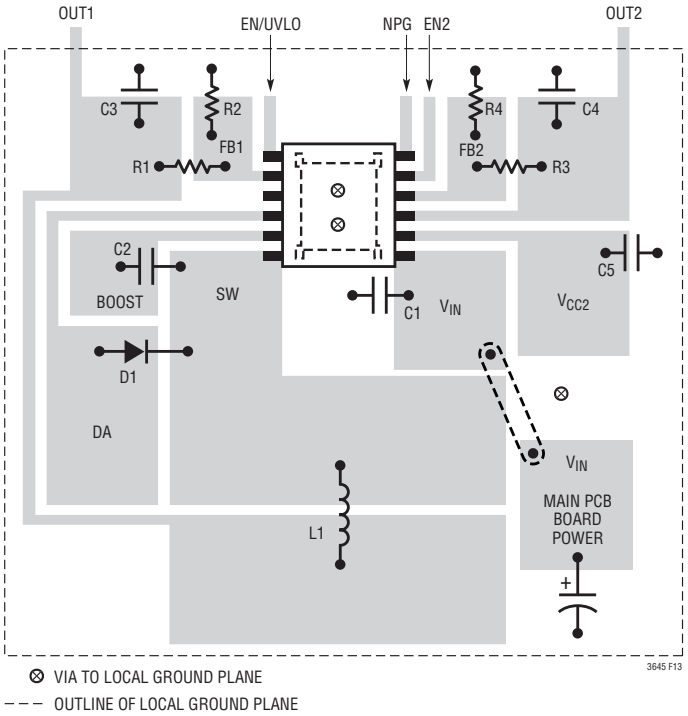


Figure 13.

High Temperature Considerations

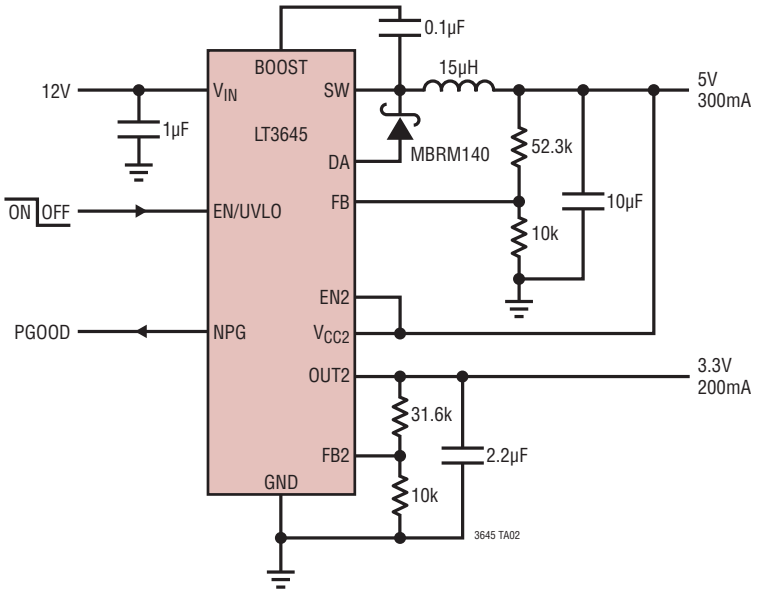
The die temperature of the LT3645 must be lower than the maximum rating of 125°C (150°C for H-grade). This is generally not a concern unless the ambient temperature is above 85°C. For higher temperatures, extra care should be taken in the layout of the circuit to ensure good heat sinking at the LT3645. The maximum load current should be derated as the ambient temperature approaches 125°C. The die temperature is calculated by multiplying the LT3645 power dissipation by the thermal resistance from junction to ambient. Power dissipation within the LT3645 can be estimated by calculating the total power loss from an efficiency measurement and subtracting the catch diode loss. The resulting temperature rise at full load is nearly independent of input voltage. Thermal resistance depends upon the layout of the circuit board, but 68°C/W is typical for the QFN (UD) package, and 40°C/W is typical for the MSE package. Thermal shutdown will turn off the Buck and LDO when the die temperature exceeds 160°C, but it is not a warrant to allow operation at die temperatures exceeding 125°C (150°C for H-grade).

Other Linear Technology Publications

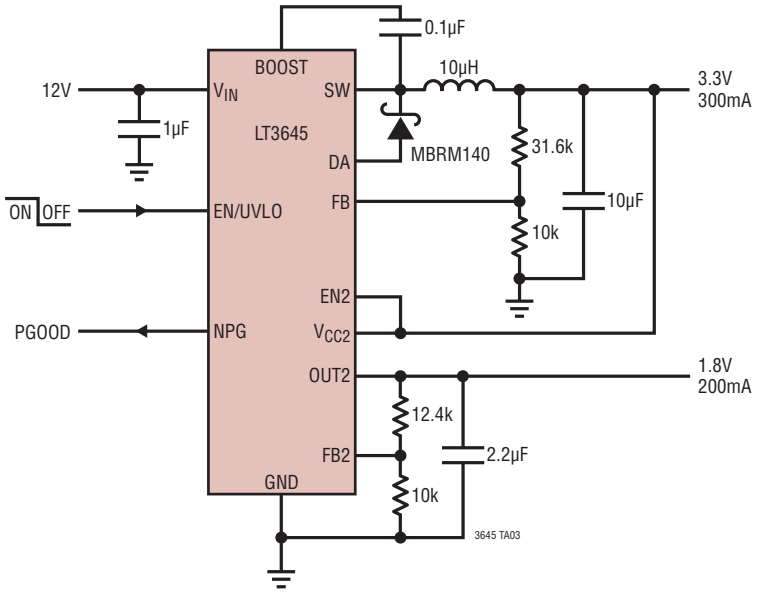
Application Notes 19, 35, and 44 contain more detailed descriptions and design information for step-down regulators and other switching regulators. The LT1376 data sheet has an extensive discussion of output ripple, loop compensation, and stability testing. Design Note 318 shows how to generate a bipolar output supply using a step-down regulator.

TYPICAL APPLICATIONS

5V Step-Down Converter with 3.3V Logic Rail

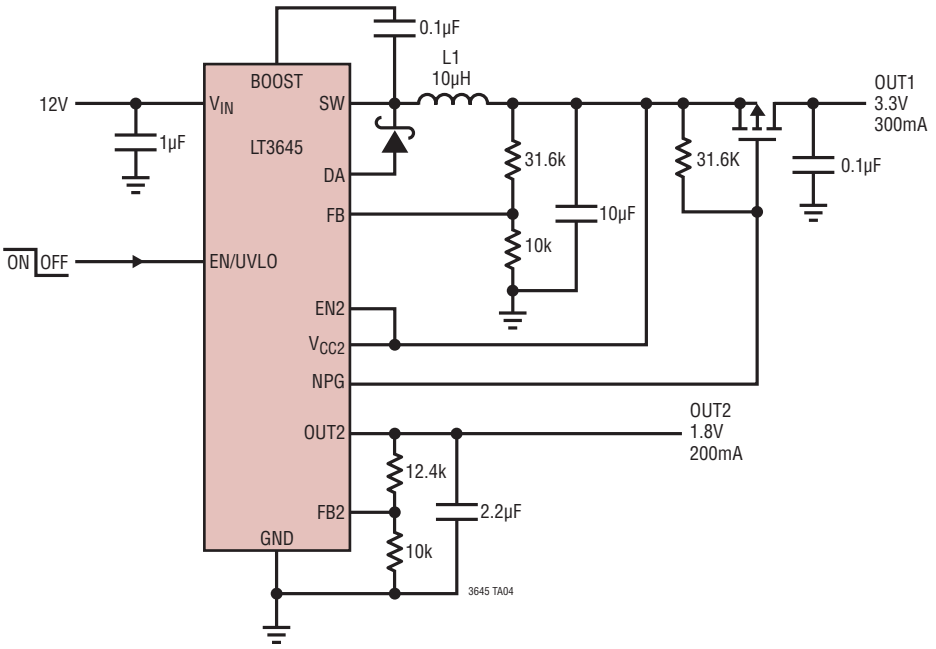


3.3V Step-Down Converter with 1.8V Logic Rail

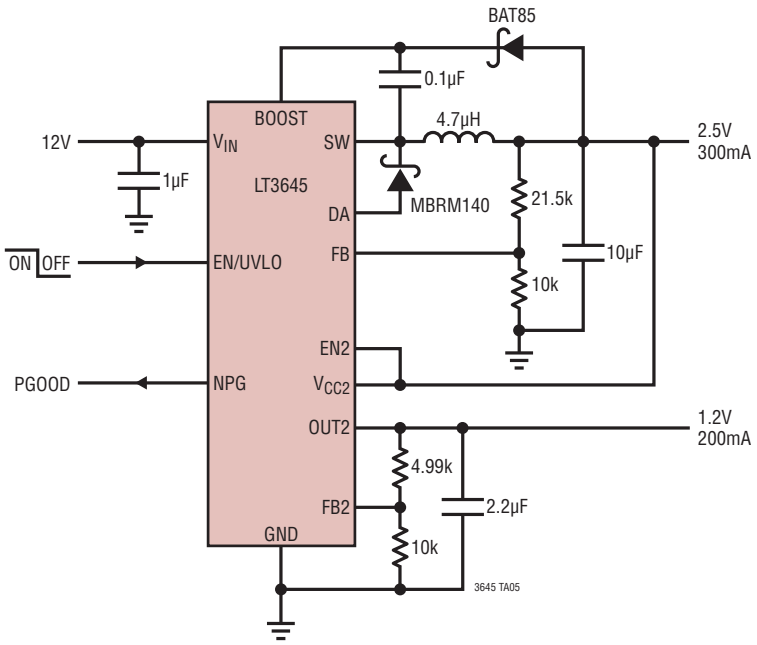


TYPICAL APPLICATIONS

3.3V Step-Down Converter with 1.8V Core Rail

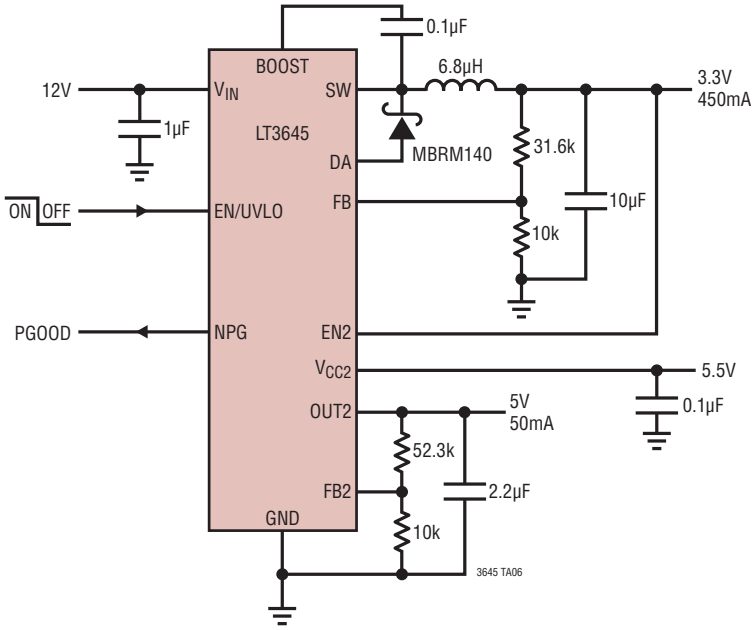


2.5V Step-Down Converter with 1.2V Logic Rail



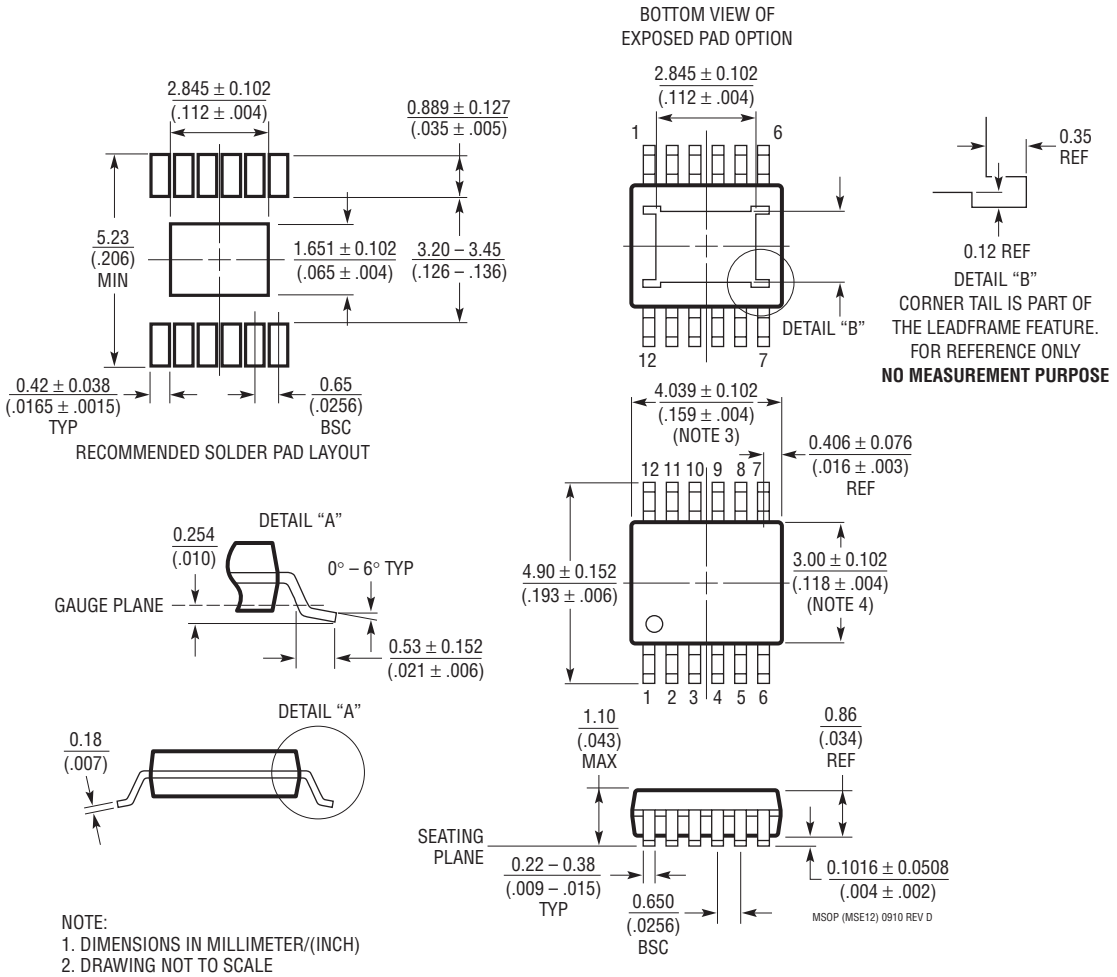
TYPICAL APPLICATIONS

3.3V Step-Down Converter with 5V Logic Rail



PACKAGE DESCRIPTION

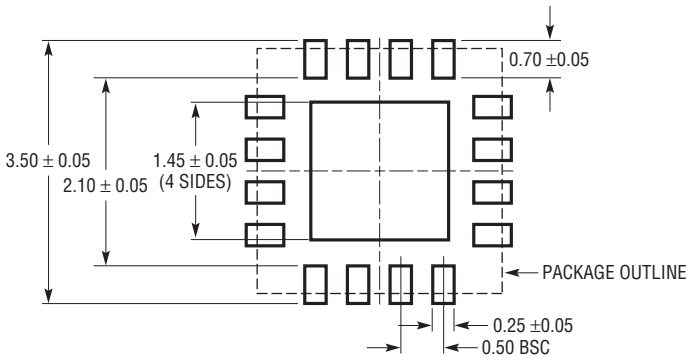
MSE Package
12-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1666 Rev D)



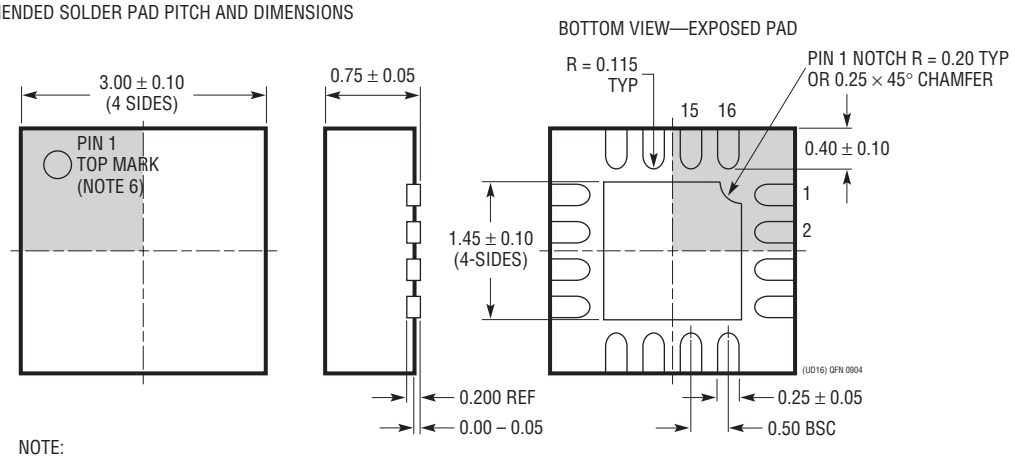
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

PACKAGE DESCRIPTION

UD Package
16-Lead Plastic QFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1691)



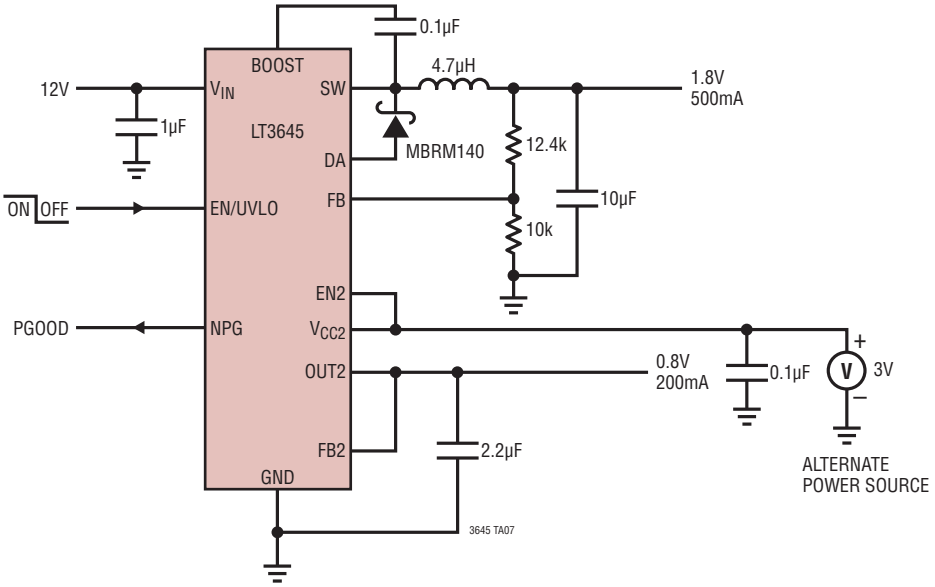
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WEED-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

1.8V Step-Down Converter with 0.8V Logic Rail



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT3694	36V, 70V Transient Protection, 2.6A, 2.5MHz High Efficiency Step-Down DC/DC Converter with Dual LDO Controllers	V_{IN}: 3.6V to 36V, Transient to 70V, $V_{OUT(MIN)}$ = 0.75V, I_Q = 1mA, I_{SD} < 1µA, 4mm × 5mm QFN-28, TSSOP-20E
LT3509	36V, 60V Transient Protection, Dual 700mA, 2.2MHz High Efficiency Step-Down DC/DC Converter	V_{IN}: 3.6V to 36V, Transient to 60V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 1.9mA, I_{SD} < 1µA, 3mm × 4mm DFN-14, MSOP-16E
LT3689	36V, 60V Transient Protection, 800mA, 2.2MHz High Efficiency MicroPower Step-Down DC/DC Converter with POR Reset and Watchdog Timer	V_{IN}: 3.6V to 36V, Transient to 60V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 75µA, I_{SD} < 1µA, 3mm × 3mm QFN-16
LT3682	36V, 60VMax, 1A, 2.2MHz High Efficiency Micropower Step-Down DC/DC Converter	V_{IN}: 3.6V to 36V, Transient to 60V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 75µA, I_{SD} < 1µA, 3mm × 3mm QFN-12
LT3970	40V, 350mA (I_{OUT}), 2.2MHz, High Efficiency Step-Down DC/DC Converter with Only 2.5µA of Quiescent Current	V_{IN}: 4.2V to 40V, $V_{OUT(MIN)}$ = 1.21V, I_Q = 2.5µA, I_{SD} < 1µA, 3mm × 3mm DFN-10, MSOP-10
LT3990	62V, 350mA (I_{OUT}), 2.2MHz, High Efficiency Step-Down DC/DC Converter with Only 2.5µA of Quiescent Current	V_{IN}: 4.2V to 40V, $V_{OUT(MIN)}$ = 1.21V, I_Q = 2.5µA, I_{SD} < 1µA, 3mm × 3mm DFN-10, MSOP-10
LT3791	38V, 1.2A, 2.2MHz High Efficiency MicroPower Step-Down DC/DC Converter with I_Q = 2.8µA	V_{IN}: 4.3V to 38V, $V_{OUT(MIN)}$ = 1.2V, I_Q = 2.8mA, I_{SD} < 1µA, 3mm × 3mm DFN-10, MSOP-10E
LT3991	55V, 1.2A, 2.2MHz High Efficiency MicroPower Step-Down DC/DC Converter with I_Q = 2.8µA	V_{IN}: 4.3V to 55V, $V_{OUT(MIN)}$ = 1.2V, I_Q = 2.8mA, I_{SD} < 1µA, 3mm × 3mm DFN-10, MSOP-10E
LT3480	36V with Transient Protection to 60V, 2A (I_{OUT}), 2.4MHz, High Efficiency Step-Down DC/DC Converter with Burst Mode® Operation	V_{IN}: 3.6V to 38V, $V_{OUT(MIN)}$ = 0.78V, I_Q = 70µA, I_{SD} < 1µA, 3mm × 3mm DFN-10, MSOP-10E
LT3685	36V with Transient Protection to 60V, 2A (I_{OUT}), 2.4MHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 3.6V to 38V, $V_{OUT(MIN)}$ = 0.78V, I_Q = 70µA, I_{SD} < 1µA, 3mm × 3mm DFN-10, MSOP-10E

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