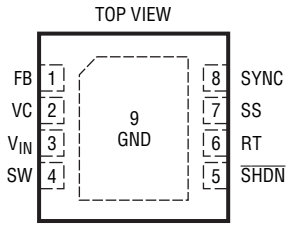
ABSOLUTE MAXIMUM RATINGS

(Note 1)

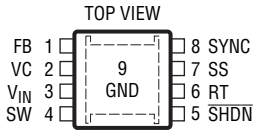
V_{IN} Voltage ..... –0.3V to 32V
SW Voltage ..... –0.4V to 42V
RT Voltage ..... –0.3V to 5V
SS and FB Voltage ..... –0.3V to 2.5V
VC Voltage ..... –0.3V to 2V
$\overline{SHDN}$ Voltage ..... –0.3V to 32V
SYNC Voltage ..... –0.3V to 5.5V

Operating Junction Temperature Range
LT3580E (Notes 2, 5) ..... –40°C to 125°C
LT3580I (Notes 2, 5) ..... –40°C to 125°C
LT3580H (Notes 2, 5) ..... –40°C to 150°C
LT3580MP (Notes 2, 5) ..... –55°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 9) IS GND, MUST BE SOLDERED TO PCB



MS8E PACKAGE
8-LEAD PLASTIC MSOP
θ_{JA} = 35°C/W TO 40°C/W
EXPOSED PAD (PIN 9) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3580EDD#PBF	LT3580EDD#TRPBF	LCXY	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT3580IDD#PBF	LT3580IDD#TRPBF	LCXY	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT3580EMS8E#PBF	LT3580EMS8E#TRPBF	LTDCJ	8-Lead Plastic MSOP	–40°C to 125°C
LT3580IMS8E#PBF	LT3580IMS8E#TRPBF	LTDCJ	8-Lead Plastic MSOP	–40°C to 125°C
LT3580HMS8E#PBF	LT3580HMS8E#TRPBF	LTDCJ	8-Lead Plastic MSOP	–40°C to 150°C
LT3580MPMS8E#PBF	LT3580MPMS8E#TRPBF	LTDCJ	8-Lead Plastic MSOP	–55°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 5V, $V_{\overline{SHDN}}$ = V_{IN} unless otherwise noted. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range		●	2.5		32	V
Positive Feedback Voltage		●	1.195	1.215	1.230	V
Negative Feedback Voltage		●	0	5	12	mV
Positive FB Pin Bias Current	V_{FB} = Positive Feedback Voltage, Current Into Pin	●	81	83.3	85	µA
Negative FB Pin Bias Current	V_{FB} = Negative Feedback Voltage, Current Out of Pin (LT3580E, LT3580I, LT3580MP) (LT3580H)	 ● ●	 81 81	 83.3 83.3	 85.5 86	 µA µA
Error Amplifier Transconductance				230		µmhos
Error Amplifier Voltage Gain				70		V/V
Quiescent Current	$V_{\overline{SHDN}}$ = 2.5V, Not Switching			1	1.5	mA
Quiescent Current in Shutdown	$V_{\overline{SHDN}}$ = 0V			0	1	µA
Reference Line Regulation	2.5V ≤ V_{IN} ≤ 32V			0.01	0.05	%/V
Switching Frequency, f_{OSC}	R_T = 45.3k (LT3580E, LT3580I, LT3580H) R_T = 45.3k (LT3580MP) R_T = 464k (LT3580E, LT3580I, LT3580H) R_T = 464k (LT3580MP)	● ● ● ●	1.8 1.8 180 180	2 2 200 200	2.2 2.25 220 225	MHz MHz kHz kHz
Switching Frequency in Foldback	Compared to Normal f_{OSC}			1/4		Ratio
Switching Frequency Set Range	SYNCing or Free Running	●	200		2500	kHz
SYNC High Level for Synchronization		●	1.3			V
SYNC Low Level for Synchronization		●			0.4	V
SYNC Clock Pulse Duty Cycle	V_{SYNC} = 0V to 2V		35		65	%
Recommended Minimum SYNC Ratio f_{SYNC}/f_{OSC}				3/4		
Minimum Off-Time				60		ns
Minimum On-Time				100		ns
Switch Current Limit	Minimum Duty Cycle (Note3) (LT3580E, LT3580I, LT3580H) Minimum Duty Cycle (Note3) (LT3580MP) Maximum Duty Cycle (Notes 3, 4) (LT3580E, LT3580I, LT3580MP) Maximum Duty Cycle (Notes 3, 4) (LT3580H)	● ● ● ●	2.2 2.15 1.6 1.55	2.5 2.2 1.9 1.9	2.8 2.8 2.6 2.6	A A A A
Switch V_{CESAT}	I_{SW} = 1.5A			300		mV
Switch Leakage Current	V_{SW} = 5V			0.01	1	µA
Soft-Start Charging Current	V_{SS} = 0.5V	●	4	6	8	µA
$\overline{SHDN}$ Minimum Input Voltage High	Active Mode, SHDN Rising (LT3580E, LT3580I) Active Mode, SHDN Rising (LT3580H, LT3580MP) Active Mode, SHDN Falling (LT3580E, LT3580I) Active Mode, SHDN Falling (LT3580H, LT3580MP)	● ● ● ●	1.27 1.25 1.24 1.22	1.32 1.32 1.29 1.29	1.38 1.4 1.33 1.35	V V V V
$\overline{SHDN}$ Input Voltage Low	Shutdown Mode	●			0.3	V
$\overline{SHDN}$ Pin Bias Current	$V_{\overline{SHDN}}$ = 3V $V_{\overline{SHDN}}$ = 1.3V $V_{\overline{SHDN}}$ = 0V	 	 9.7 	40 11.6 0	60 13.4 0.1	µA µA µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3580E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3580I is guaranteed over the full –40°C to 125°C operating junction temperature range. The LT3580H is guaranteed over the full –40°C to 150°C operating junction temperature range. The LT3580MP is guaranteed over the full –55°C to 125°C operating junction temperature range. Operating lifetime is derated at junction temperatures greater than 125°C.

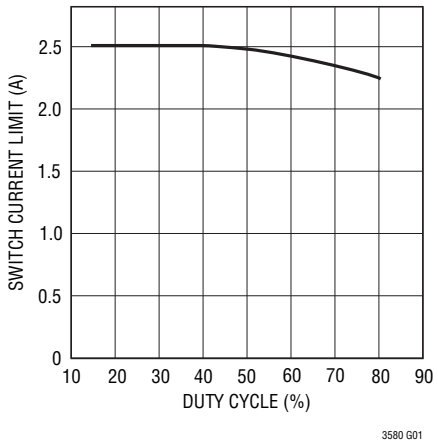
Note 3: Current limit guaranteed by design and/or correlation to static test.

Note 4: Current limit measured at equivalent switching frequency of 2.5MHz.

Note 5: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

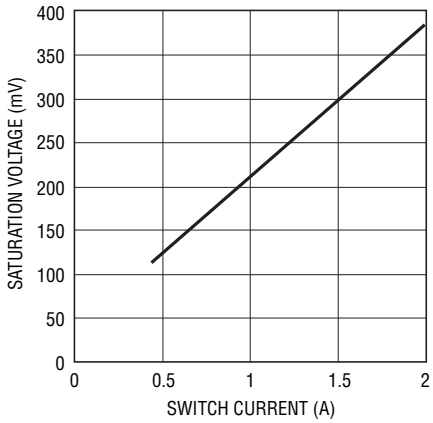
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise specified

Switch Current Limit at 1MHz



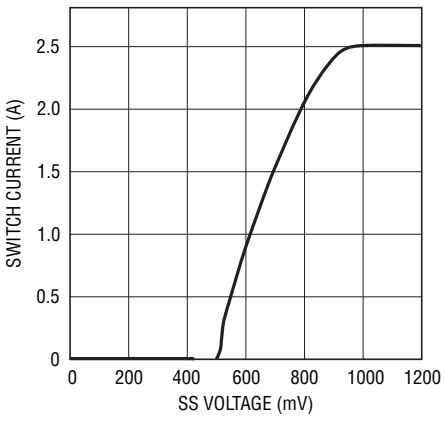
3580 G01

Switch Saturation Voltage



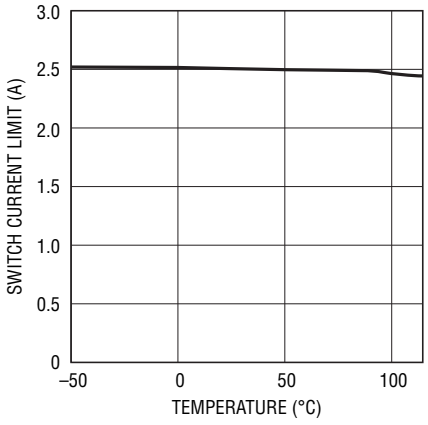
3580 G02

Switch Current Limit at Minimum Duty Cycle



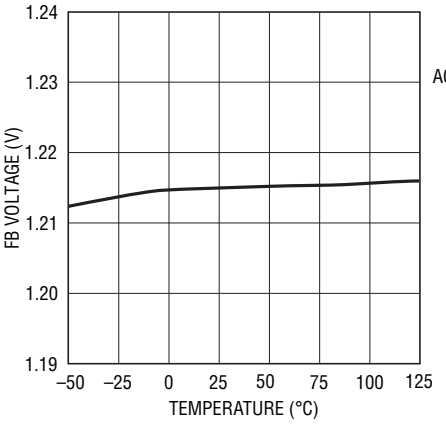
3580 G03

Switch Current Limit at Minimum Duty Cycle



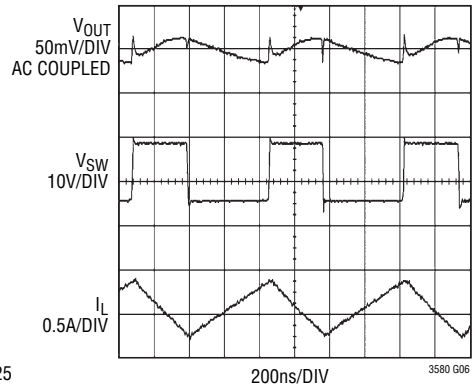
3580 G04

Positive Feedback Voltage



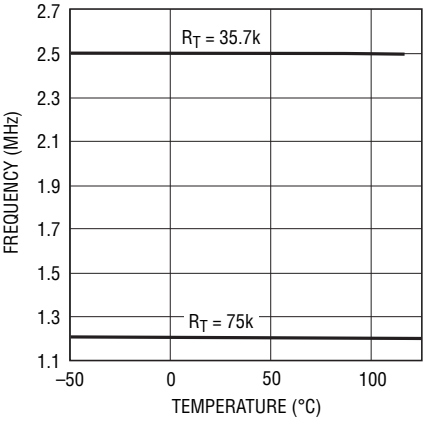
3580 G05

Switching Waveforms for Figure 14 Circuit



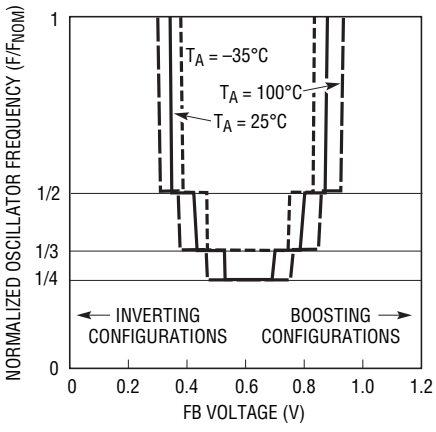
3580 G06

Oscillator Frequency



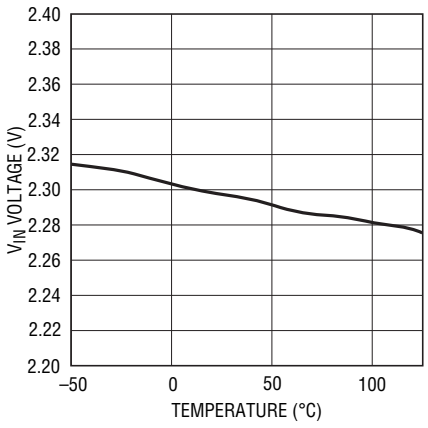
3580 G07

Oscillator Frequency During Soft-Start



3580 G08

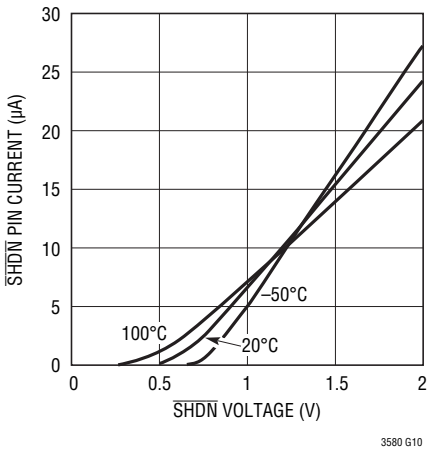
Internal UVLO



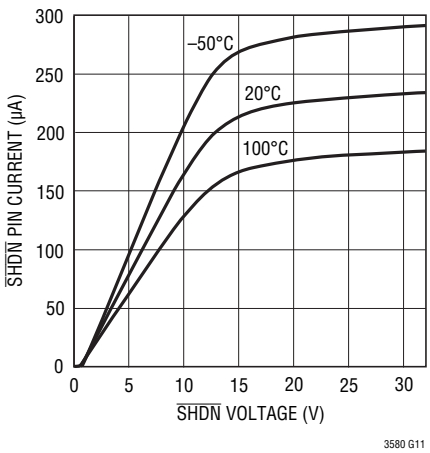
3580 G09

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise specified

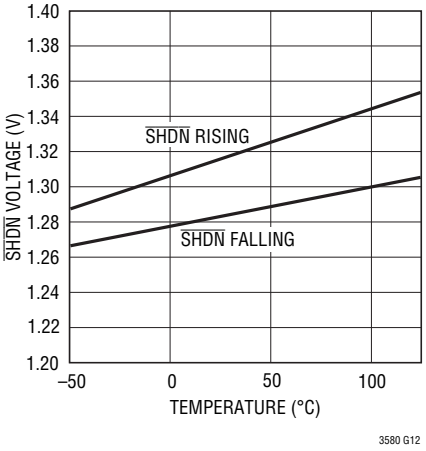
$\overline{SHDN}$ Pin Current



$\overline{SHDN}$ Pin Current



Active/Lockout Threshold



PIN FUNCTIONS

FB (Pin 1): Positive and Negative Feedback Pin. For a boost or inverting converter, tie a resistor from the FB pin to V_{OUT} according to the following equations:

$$R_{FB} = \frac{(V_{OUT} - 1.215)}{83.3 \bullet 10^{-6}};\ \text{Boost or SEPIC Converter}$$

$$R_{FB} = \frac{(|V_{OUT}| + 5mV)}{83.3 \bullet 10^{-6}};\ \text{Inverting Converter}$$

VC (Pin 2): Error Amplifier Output Pin. Tie external compensation network to this pin.

V_{IN} (Pin 3): Input Supply Pin. Must be locally bypassed.

SW (Pin 4): Switch Pin. This is the collector of the internal NPN Power switch. Minimize the metal trace area connected to this pin to minimize EMI.

$\overline{SHDN}$ (Pin 5): Shutdown Pin. In conjunction with the UVLO (undervoltage lockout) circuit, this pin is used to enable/disable the chip and restart the soft-start sequence. Drive below 1.24V (LT3580E, LT3580I) or 1.22V (LT3580H, LT3580MP) to disable the chip. Drive above 1.38V (LT3580E, LT3580I) or 1.40V (LT3580H, LT3580MP) to activate chip and restart the soft-start sequence. Do not float this pin.

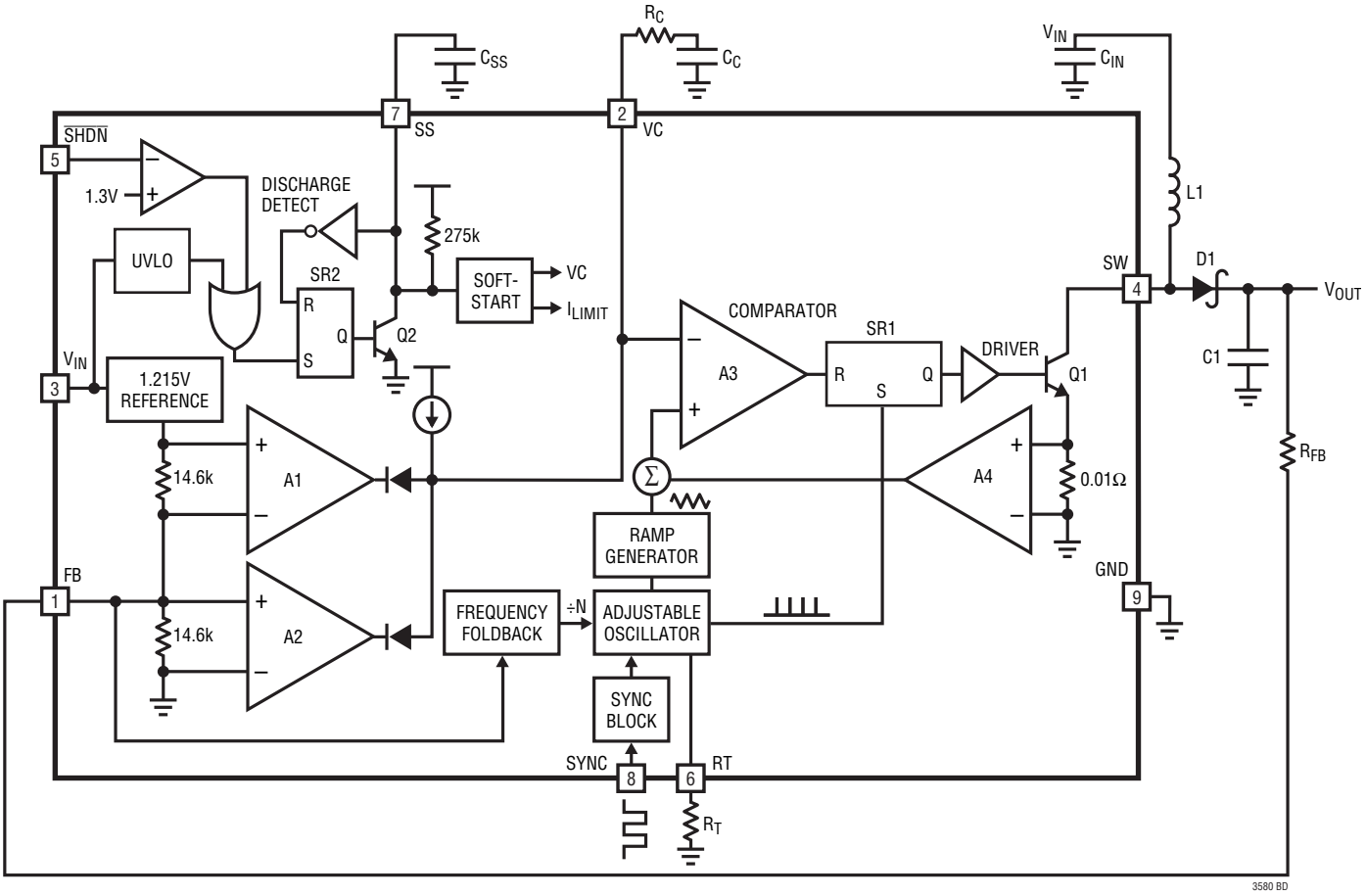
RT (Pin 6): Timing Resistor Pin. Adjusts the switching frequency. Place a resistor from this pin to ground to set the frequency to a fixed free running level. Do not float this pin.

SS (Pin 7): Soft-Start Pin. Place a soft-start capacitor here. Upon start-up, the SS pin will be charged by a (nominally) 275k resistor to about 2.2V.

SYNC (Pin 8): To synchronize the switching frequency to an outside clock, simply drive this pin with a clock. The high voltage level of the clock needs to exceed 1.3V, and the low level should be less 0.4V. Drive this pin to less than 0.4V to revert to the internal free running clock. See the Applications Information section for more information.

GND (Exposed Pad Pin 9): Ground. Exposed pad must be soldered directly to local ground plane.

BLOCK DIAGRAM



OPERATION

The LT3580 uses a constant-frequency, current mode control scheme to provide excellent line and load regulation. Refer to the Block Diagram which shows the LT3580 in a boost configuration. At the start of each oscillator cycle, the SR latch (SR1) is set, which turns on the power switch, Q1. The switch current flows through the internal current sense resistor generating a voltage proportional to the switch current. This voltage (amplified by A4) is added to a stabilizing ramp and the resulting sum is fed into the positive terminal of the PWM comparator A3. When this voltage exceeds the level at the negative input of A3, the SR latch is reset, turning off the power switch. The level at the negative input of A3 (VC pin) is set by the error amplifier A1 (or A2) and is simply an amplified version of the difference between the feedback voltage (FB pin) and the reference voltage (1.215V or 5mV depending on the configuration). In this manner, the error amplifier sets the correct peak current level to keep the output in regulation.

The LT3580 has a novel FB pin architecture that can be used for either boost or inverting configurations. When configured as a boost converter, the FB pin is pulled up to the internal bias voltage of 1.215V by the R_{FB} resistor connected from V_{OUT} to FB. Comparator A2 becomes inactive and comparator A1 performs the inverting amplification from FB to VC. When the LT3580 is in an inverting configuration, the FB pin is pulled down to 5mV by the R_{FB} resistor connected from V_{OUT} to FB. Comparator A1 becomes inactive and comparator A2 performs the noninverting amplification from FB to VC.

OPERATION

SEPIC Topology

The LT3580 can be configured as a SEPIC (single-ended primary inductance converter). This topology allows for the input to be higher, equal, or lower then the desired output voltage. Output disconnect is inherently built into the SEPIC topology, meaning no DC path exists between the input and output. This is useful for applications requiring the output to be disconnected from the input source when the circuit is in shutdown.

Inverting Topology

The LT3580 can also work in a dual inductor inverting topology. The part's unique feedback pin allows for the inverting topology to be built by simply changing the connection of external components. This solution results in very low output voltage ripple due to inductor L2 in series with the output. Abrupt changes in output capacitor current are eliminated because the output inductor delivers current to the output during both the off-time and the on-time of the LT3580 switch.

Start-Up Operation

Several functions are provided to enable a very clean start-up for the LT3580.

- First, the $\overline{SHDN}$ pin voltage is monitored by an internal voltage reference to give a precise turn-on voltage level. An external resistor (or resistor divider) can be connected from the input power supply to the $\overline{SHDN}$ pin to provide a user-programmable undervoltage lockout function.
- Second, the soft-start circuitry provides for a gradual ramp-up of the switch current. When the part is brought out of shutdown, the external SS capacitor is first discharged (providing protection against $\overline{SHDN}$ pin glitches and slow ramping), then an integrated 275k resistor pulls the SS pin up to ~2.2V. By connecting an external capacitor to the SS pin, the voltage ramp rate on the pin can be set. Typical values for the soft-start capacitor range from 100nF to 1µF.
- Finally, the frequency foldback circuit reduces the switching frequency when the FB pin is in a nominal range of 350mV to 900mV. This feature reduces the minimum duty cycle that the part can achieve thus allowing better control of the switch current during start-up. When the FB voltage is pulled outside of this range, the switching frequency returns to normal.

Current Limit and Thermal Shutdown Operation

The LT3580 has a current limit circuit not shown in the Block Diagram. The switch current is consistently monitored and not allowed to exceed the maximum switch current at a given duty cycle (see the Electrical Characteristics table). If the switch current reaches this value, the SR latch (SR1) is reset regardless of the state of the comparator (A1/A2). Also not shown in the Block Diagram is the thermal shutdown circuit. If the temperature of the part exceeds approximately 165°C, the SR2 latch is set regardless of the state of the comparator (A1/A2). A full soft-start cycle will then be initiated. The current limit and thermal shutdown circuits protect the power switch as well as the external components connected to the LT3580.

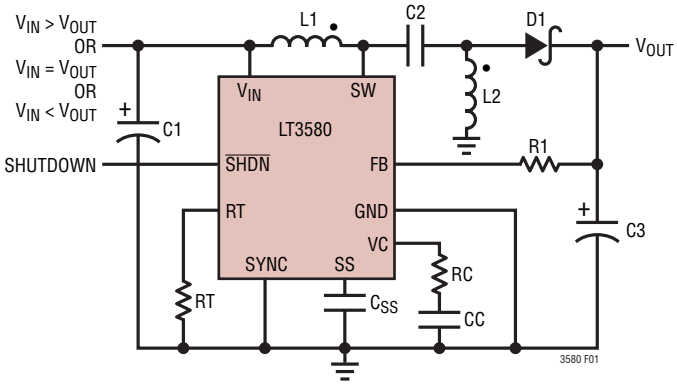


Figure 1. SEPIC Topology Allows for the Input to Span the Output Voltage. Coupled or Uncoupled Inductors Can Be Used. Follow Noted Phasing if Coupled

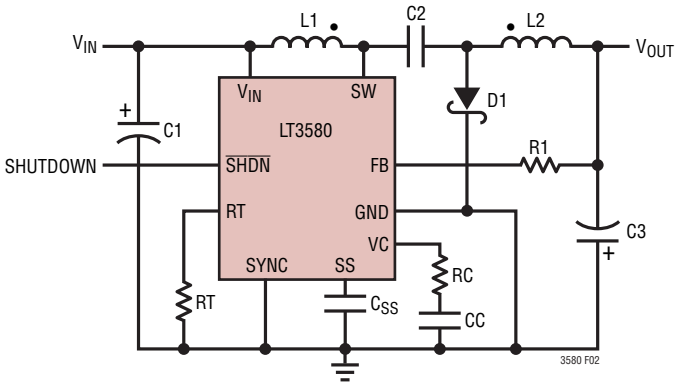


Figure 2. Dual Inductor Inverting Topology Results in Low Output Ripple. Coupled or Uncoupled Inductors Can Be Used. Follow Noted Phasing if Coupled

APPLICATIONS INFORMATION

Setting Output Voltage

The output voltage is set by connecting a resistor (R_{FB}) from V_{OUT} to the FB pin. R_{FB} is determined from the following equation:

$$R_{FB} = \frac{|V_{OUT} - V_{FB}|}{83.3\mu A}$$

where V_{FB} is 1.215V (typical) for non-inverting topologies (i.e., boost and SEPIC regulators) and 5mV (typical) for inverting topologies (see the Electrical Characteristics).

Power Switch Duty Cycle

In order to maintain loop stability and deliver adequate current to the load, the power NPN (Q1 in the Block Diagram) cannot remain "on" for 100% of each clock cycle. The maximum allowable duty cycle is given by:

$$DC_{MAX} = \frac{(T_P - \text{Min Off Time})}{T_P} \bullet 100\%$$

where T_P is the clock period and Min Off Time (found in the Electrical Characteristics) is typically 60ns.

The application should be designed so that the operating duty cycle does not exceed DC_{MAX}.

Duty cycle equations for several common topologies are given below, where V_D is the diode forward voltage drop and V_{CESAT} is typically 300mV at 1.5A.

For the boost topology:

$$DC \cong \frac{V_{OUT} - V_{IN} + V_D}{V_{OUT} + V_D - V_{CESAT}}$$

For the SEPIC or dual inductor inverting topology (see Figures 1 and 2):

$$DC \cong \frac{V_D + |V_{OUT}|}{V_{IN} + |V_{OUT}| + V_D - V_{CESAT}}$$

The LT3580 can be used in configurations where the duty cycle is higher than DC_{MAX}, but it must be operated in the discontinuous conduction mode so that the effective duty cycle is reduced.

Inductor Selection

General Guidelines: The high frequency operation of the LT3580 allows for the use of small surface mount inductors. For high efficiency, choose inductors with high frequency core material, such as ferrite, to reduce core losses. To improve efficiency, choose inductors with more volume for a given inductance. The inductor should have low DCR (copper wire resistance) to reduce I^2R losses, and must be able to handle the peak inductor current without saturating. Note that in some applications, the current handling requirements of the inductor can be lower, such as in the SEPIC topology, where each inductor only carries a fraction of the total switch current. Molded chokes or chip inductors usually do not have enough core area to support peak inductor currents in the 2A to 3A range. To minimize radiated noise, use a toroidal or shielded inductor. Note that the inductance of shielded types will drop more as current increases, and will saturate more easily. See Table 1 for a list of inductor manufacturers. Thorough lab evaluation is recommended to verify that the following guidelines properly suit the final application.

Table 1. Inductor Manufacturers

Coilcraft	DO3316P, MSS7341 and LPS4018 Series	www.coilcraft.com
Coiltronics	DR, LD and CD Series	www.coiltronics.com
Murata	LQH55D and LQH66S Series	www.murata.com
Sumida	CDRH5D18B/HP, CDR6D23MN, CDRH6D26/HP, CDRH6D28, CDR7D28MN and CDRH105R Series	www.sumida.com
TDK	RLF7030 and VLCF4020 Series	www.tdk.com
Würth	WE-PD and WE-PD2 Series	www.we-online.com

Minimum Inductance: Although there can be a tradeoff with efficiency, it is often desirable to minimize board space by choosing smaller inductors. When choosing an inductor, there are two conditions that limit the minimum inductance; (1) providing adequate load current, and (2) avoidance of subharmonic oscillation. Choose an inductance that is high enough to meet both of these requirements.

Adequate Load Current: Small value inductors result in increased ripple currents and thus, due to the limited peak switch current, decrease the average current that can be

APPLICATIONS INFORMATION

provided to a load (I_{OUT}). In order to provide adequate load current, L should be at least:

$$L > \frac{DC \bullet V_{IN}}{2(f)\left(I_{LIM} - \frac{|V_{OUT}| \bullet I_{OUT}}{V_{IN} \bullet \eta}\right)}$$

for boost, topologies, or:

$$L > \frac{DC \bullet V_{IN}}{2(f)\left(I_{LIM} - \frac{|V_{OUT}| \bullet I_{OUT}}{V_{IN} \bullet \eta} - I_{OUT}\right)}$$

for the SEPIC and inverting topologies.

where:

L = L1||L2 for uncoupled dual inductor topologies

DC = switch duty cycle (see previous section)

I_{LIM} = switch current limit, typically about 2.4A at 50% duty cycle (see the Typical Performance Characteristics section).

η = power conversion efficiency (typically 88% for boost and 75% for dual inductor topologies at high currents).

f = switching frequency

Negative values of L indicate that the output load current I_{OUT} exceeds the switch current limit capability of the LT3580.

Avoiding Subharmonic Oscillations: The LT3580's internal slope compensation circuit will prevent subharmonic oscillations that can occur when the duty cycle is greater than 50%, provided that the inductance exceeds a minimum value. In applications that operate with duty cycles greater than 50%, the inductance must be at least:

$$L > \frac{V_{IN} \bullet (2 \bullet DC - 1)}{(1 - DC) \bullet (f)}$$

for boost, coupled inductor SEPIC, and coupled inductor inverting topologies, or:

$$L1 \| L2 > \frac{V_{IN} \bullet (2 \bullet DC - 1)}{(1 - DC) \bullet (f)}$$

for the uncoupled inductor SEPIC and uncoupled inductor inverting topologies.

Maximum Inductance: Excessive inductance can reduce current ripple to levels that are difficult for the current comparator (A3 in the Block Diagram) to cleanly discriminate, thus causing duty cycle jitter and/or poor regulation. The maximum inductance can be calculated by:

$$L_{MAX} = \frac{V_{IN} - V_{CESAT}}{I_{MIN-RIPPLE}} \bullet \frac{DC}{f}$$

where L_{MAX} is L1||L2 for uncoupled dual inductor topologies and $I_{MIN-RIPPLE}$ is typically 95mA.

Current Rating: Finally, the inductor(s) must have a rating greater than its peak operating current to prevent inductor saturation resulting in efficiency loss. In steady state, the peak input inductor current (continuous conduction mode only) is given by:

$$I_{L1-PEAK} = \frac{|V_{OUT} \bullet I_{OUT}|}{V_{IN} \bullet \eta} + \frac{V_{IN} \bullet DC}{2 \bullet L1 \bullet f}$$

for the boost, uncoupled inductor SEPIC and uncoupled inductor inverting topologies.

For uncoupled dual inductor topologies, the peak output inductor current is given by:

$$I_{L2-PEAK} = I_{OUT} + \frac{|V_{OUT}| \bullet (1 - DC)}{2 \bullet L2 \bullet f}$$

For the coupled inductor topologies:

$$I_{OUT}\left[1 + \frac{V_{OUT}}{\eta \bullet V_{IN}}\right] + \frac{V_{IN} \bullet DC}{2 \bullet L \bullet f}$$

Note: Inductor current can be higher during load transients. It can also be higher during start-up if inadequate soft-start capacitance is used.

Capacitor Selection

Low ESR (equivalent series resistance) capacitors should be used at the output to minimize the output ripple voltage. Multilayer ceramic capacitors are an excellent choice, as they have an extremely low ESR and are available in very small packages. X5R or X7R dielectrics are preferred, as

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these materials retain their capacitance over wider voltage and temperature ranges. A 4.7µF to 20µF output capacitor is sufficient for most applications, but systems with very low output currents may need only a 1µF or 2.2µF output capacitor. Always use a capacitor with a sufficient voltage rating. Many capacitors rated at 2.2µF to 20µF, particularly 0805 or 0603 case sizes, have greatly reduced capacitance at the desired output voltage. Solid tantalum or OS-CON capacitors can be used, but they will occupy more board area than a ceramic and will have a higher ESR with greater output ripple.

Ceramic capacitors also make a good choice for the input decoupling capacitor, which should be placed as closely as possible to the LT3580. A 2.2µF to 4.7µF input capacitor is sufficient for most applications.

Table 2 shows a list of several ceramic capacitor manufacturers. Consult the manufacturers for detailed information on their entire selection of ceramic parts.

Table 2. Ceramic Capacitor Manufacturers

Kemet	www.kemet.com
Murata	www.murata.com
Taiyo Yuden	www.t-yuden.com

Compensation—Adjustment

To compensate the feedback loop of the LT3580, a series resistor-capacitor network in parallel with a single capacitor should be connected from the VC pin to GND. For most applications, the series capacitor should be in the range of 470pF to 2.2nF with 1nF being a good starting value. The parallel capacitor should range in value from 10pF to 100pF with 47pF a good starting value. The compensation resistor, R_C, is usually in the range of 5k to 50k. A good technique to compensate a new application is to use a 100kΩ potentiometer in place of series resistor R_C. With the series capacitor and parallel capacitor at 1nF and 47pF respectively, adjust the potentiometer while observing the transient response and the optimum value for R_C can be found. Figures 3a to 3c illustrate this process for the circuit of Figure 14 with a load current stepped between 400mA and 500mA. Figure 3a shows the transient response with R_C equal to 1k. The phase margin is poor, as evidenced by the excessive ringing in the output voltage and inductor current. In Figure 3b, the value of R_C is increased to 3k, which results in a more damped response. Figure 3c shows the results when R_C is increased further to 10k. The transient response is nicely damped and the compensation procedure is complete.

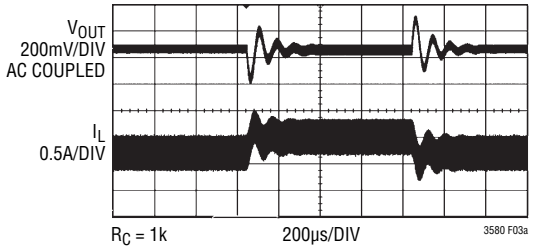

Figure 3a. Transient Response Shows Excessive Ringing

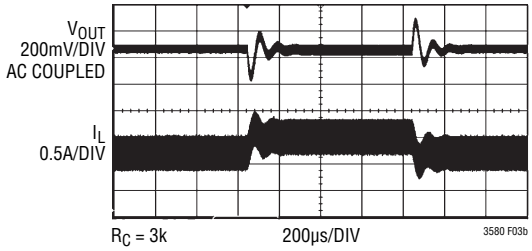

Figure 3b. Transient Response Is Better

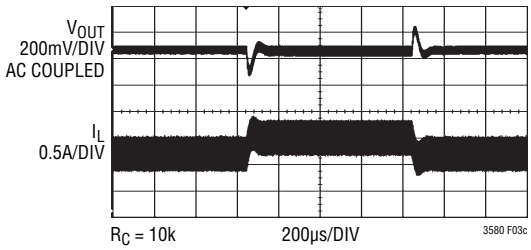

Figure 3c. Transient Response Is Well Damped

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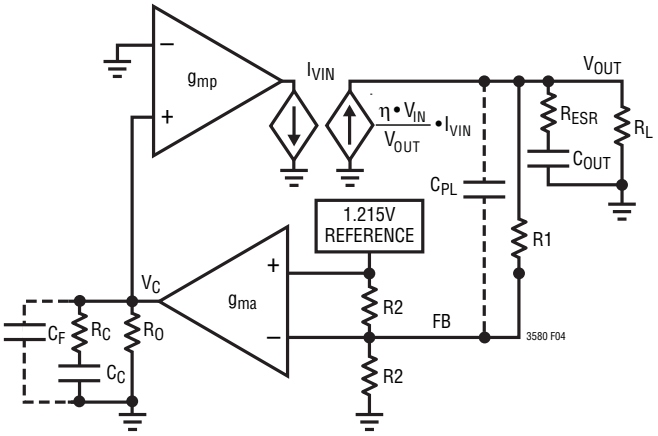
Compensation—Theory

Like all other current mode switching regulators, the LT3580 needs to be compensated for stable and efficient operation. Two feedback loops are used in the LT3580—a fast current loop which does not require compensation, and a slower voltage loop which does. Standard bode plot analysis can be used to understand and adjust the voltage feedback loop.

As with any feedback loop, identifying the gain and phase contribution of the various elements in the loop is critical. Figure 4 shows the key equivalent elements of a boost converter. Because of the fast current control loop, the power stage of the IC, inductor and diode have been replaced by a combination of the equivalent transconductance amplifier g_{mp} and the current controlled current source (which converts I_{VIN} to $\eta V_{IN}/V_{OUT} \bullet I_{VIN}$). g_{mp} acts as a current source where the peak input current, I_{VIN}, is proportional to the VC voltage. η is the efficiency of the switching regulator, and is typically about 88%.

Note that the maximum output currents of g_{mp} and g_{ma} are finite. The limits for g_{mp} are in the Electrical Characteristics section (switch current limit), and g_{ma} is nominally limited to about ±12µA.



C_C: COMPENSATION CAPACITOR
C_{OUT}: OUTPUT CAPACITOR
C_{PL}: PHASE LEAD CAPACITOR
C_F: HIGH FREQUENCY FILTER CAPACITOR
g_{ma}: TRANSCONDUCTANCE AMPLIFIER INSIDE IC
g_{mp}: POWER STAGE TRANSCONDUCTANCE AMPLIFIER
R_C: COMPENSATION RESISTOR
R_L: OUTPUT RESISTANCE DEFINED AS V_{OUT} DIVIDED BY $I_{LOAD(MAX)}$
R_O: OUTPUT RESISTANCE OF g_{ma}
R1, R2: FEEDBACK RESISTOR DIVIDER NETWORK
R_{ESR}: OUTPUT CAPACITOR ESR

Figure 4. Boost Converter Equivalent Model

From Figure 4, the DC gain, poles and zeros can be calculated as follows:

$$\text{Output Pole:}\quad P1 = \frac{2}{2 \bullet \pi \bullet R_L \bullet C_{OUT}}$$

$$\text{Error Amp Pole:}\quad P2 = \frac{1}{2 \bullet \pi \bullet \left[R_O + R_C\right] \bullet C_C}$$

$$\text{Error Amp Zero:}\quad Z1 = \frac{1}{2 \bullet \pi \bullet R_C \bullet C_C}$$

DC Gain:

(Breaking Loop at FB Pin)

$$A_{DC} = A_{OL}(0) = \frac{\partial V_C}{\partial V_{FB}} \bullet \frac{\partial I_{VIN}}{\partial V_C} \bullet \frac{\partial V_{OUT}}{\partial I_{VIN}} \bullet \frac{\partial V_{FB}}{\partial V_{OUT}} =$$

$$\left(g_{ma} \bullet R_0\right) \bullet g_{mp} \bullet \left(\eta \bullet \frac{V_{IN}}{V_{OUT}} \bullet \frac{R_L}{2}\right) \bullet \frac{0.5R2}{R1 + 0.5R2}$$

$$\text{ESR Zero:}\quad Z2 = \frac{1}{2 \bullet \pi \bullet R_{ESR} \bullet C_{OUT}}$$

$$\text{RHP Zero:}\quad Z3 = \frac{V_{IN}^2 \bullet R_L}{2 \bullet \pi \bullet V_{OUT}^2 \bullet L}$$

$$\text{High Frequency Pole:}\quad P3 > \frac{f_S}{3}$$

$$\text{Phase Lead Zero:}\quad Z4 = \frac{1}{2 \bullet \pi \bullet R1 \bullet C_{PL}}$$

$$\text{Phase Lead Pole:}\quad P4 = \frac{1}{2 \bullet \pi \bullet \frac{R1 \bullet \frac{R2}{2}}{R1 + \frac{R2}{2}} \bullet C_{PL}}$$

Error Amp Filter Pole:

$$P5 = \frac{1}{2 \bullet \pi \bullet \frac{R_C \bullet R_O}{R_C + R_O} \bullet C_F}, C_F < \frac{C_C}{10}$$

The current mode zero (Z3) is a right-half plane zero which can be an issue in feedback control design, but is manageable with proper external component selection.

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Using the circuit in Figure 14 as an example, Table 3 shows the parameters used to generate the bode plot shown in Figure 5.

Table 3. Bode Plot Parameters

PARAMETER	VALUE	UNITS	COMMENT
R_L	21.8	Ω	Application Specific
C_{OUT}	10	µF	Application Specific
R_{ESR}	10	mΩ	Application Specific
R_O	305	kΩ	Not Adjustable
C_C	1000	pF	Adjustable
C_F	0	pF	Optional/Adjustable
C_{PL}	0	pF	Optional/Adjustable
R_C	10	kΩ	Adjustable
R1	130	kΩ	Adjustable
R2	14.6	kΩ	Not Adjustable
V_{OUT}	12	V	Application Specific
V_{IN}	5	V	Application Specific
g_{ma}	230	µmho	Not Adjustable
g_{mp}	7	mho	Not Adjustable
L	4.2	µH	Application Specific
f_S	1.2	MHz	Adjustable

In Figure 5, the phase is –140° when the gain reaches 0dB giving a phase margin of 40°. The crossover frequency is 10kHz, which is more than three times lower than the frequency of the RHP zero to achieve adequate phase margin.

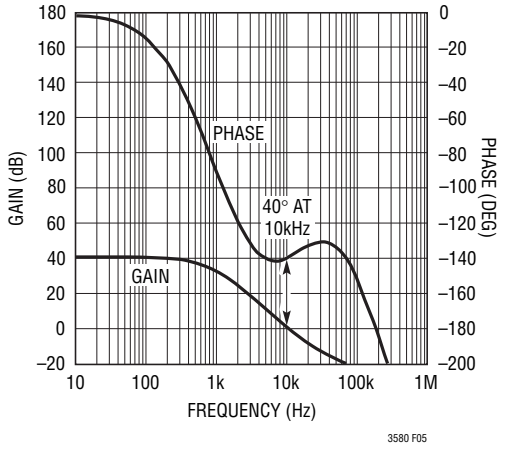

Figure 5. Bode Plot for Example Boost Converter

Diode Selection

Schottky diodes, with their low forward voltage drops and fast switching speeds, are recommended for use with the LT3580. The Microsemi UPS120 is a very good choice. Where the input-to-output voltage differential exceeds 20V, use the UPS140 (a 40V diode). These diodes are rated to handle an average forward current of 1A.

Oscillator

The operating frequency of the LT3580 can be set by the internal free-running oscillator. When the SYNC pin is driven low (< 0.4V), the frequency of operation is set by a resistor from R_T to ground. An internally trimmed timing capacitor resides inside the IC. The oscillator frequency is calculated using the following formula:

$$f_{OSC} = \frac{91.9}{(R_T + 1)}$$

where f_{OSC} is in MHz and R_T is in kΩ. Conversely, R_T (in kΩ) can be calculated from the desired frequency (in MHz) using:

$$R_T = \frac{91.9}{f_{OSC}} - 1$$

Clock Synchronization

The operating frequency of the LT3580 can be synchronized to an external clock source. To synchronize to the external source, simply provide a digital clock signal into the SYNC pin. The LT3580 will operate at the SYNC clock frequency. The LT3580 will revert to the internal free-running oscillator clock after SYNC is driven low for a few free-running clock periods.

Driving SYNC high for an extended period of time effectively stops the operating clock and prevents latch SR1 from becoming set (see the Block Diagram). As a result, the switching operation of the LT3580 will stop.

The duty cycle of the SYNC signal must be between 35% and 65% for proper operation. Also, the frequency of the SYNC signal must meet the following two criteria:

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(1) SYNC may not toggle outside the frequency range of 200kHz to 2.5MHz unless it is stopped low to enable the free-running oscillator.

(2) The SYNC frequency can always be higher than the free-running oscillator frequency, f_{OSC}, but should not be less than 25% below f_{OSC}.

Operating Frequency Selection

There are several considerations in selecting the operating frequency of the converter. The first is staying clear of sensitive frequency bands, which cannot tolerate any spectral noise. For example, in products incorporating RF communications, the 455kHz IF frequency is sensitive to any noise, therefore switching above 600kHz is desired. Some communications have sensitivity to 1.1MHz, and in that case, a 1.5MHz switching converter frequency may be employed. The second consideration is the physical size of the converter. As the operating frequency goes up, the inductor and filter capacitors go down in value and size. The tradeoff is efficiency, since the switching losses due to NPN base charge (see Thermal Calculations), Schottky diode charge, and other capacitive loss terms increase proportionally with frequency.

Soft-Start

The LT3580 contains a soft-start circuit to limit peak switch currents during start-up. High start-up current is inherent in switching regulators in general since the feedback loop is saturated due to V_{OUT} being far from its final value. The regulator tries to charge the output capacitor as quickly as possible, which results in large peak currents.

The start-up current can be limited by connecting an external capacitor (typically 100nF to 1µF) to the SS pin. This capacitor is slowly charged to ~2.2V by an internal 275k resistor once the part is activated. SS pin voltages below ~1.1V reduce the internal current limit. Thus, the gradual ramping of the SS voltage also gradually increases the current limit as the capacitor charges. This, in turn, allows the output capacitor to charge gradually toward its final value while limiting the start-up current.

In the event of a commanded shutdown or lockout ($\overline{SHDN}$ pin), internal undervoltage lockout (UVLO) or a thermal lockout, the soft-start capacitor is automatically discharged to ~200mV before charging resumes, thus assuring that the soft-start occurs after every reactivation of the chip.

Shutdown

The $\overline{SHDN}$ pin is used to enable or disable the chip. For most applications, $\overline{SHDN}$ can be driven by a digital logic source. Voltages above 1.38V enable normal active operation. Voltages below 300mV will shutdown the chip, resulting in extremely low quiescent current.

While the $\overline{SHDN}$ voltage transitions through the lockout voltage range (0.3V to 1.24V) the power switch is disabled and the SR2 latch is set (see the Block Diagram). This causes the soft-start capacitor to begin discharging, which continues until the capacitor is discharged and active operation is enabled. Although the power switch is disabled, $\overline{SHDN}$ voltages in the lockout range do not necessarily reduce quiescent current until the $\overline{SHDN}$ voltage is near or below the shutdown threshold.

Also note that $\overline{SHDN}$ can be driven above V_{IN} or V_{OUT} as long as the $\overline{SHDN}$ voltage is limited to less than 32V.

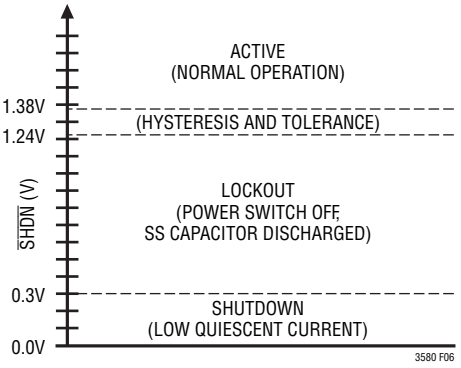

Figure 6. Chip States vs $\overline{SHDN}$ Voltage

Configurable Undervoltage Lockout

Figure 7 shows how to configure an undervoltage lockout (UVLO) for the LT3580. Typically, UVLO is used in situations where the input supply is current-limited, has a relatively high source resistance, or ramps up/down slowly. A switching regulator draws constant power from the source, so source current increases as source voltage drops. This looks like a negative resistance load to the source and can cause the source to current-limit or latch low under low

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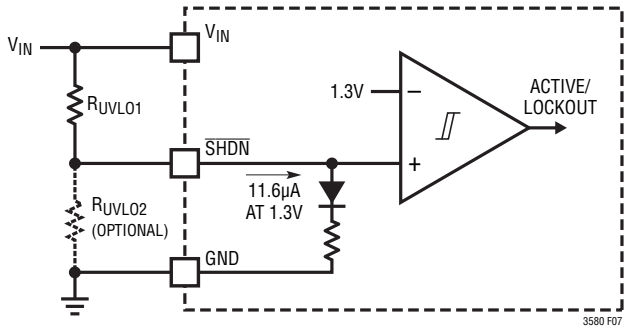

Figure 7. Configurable UVLO

source voltage conditions. UVLO prevents the regulator from operating at source voltages where these problems might occur.

The shutdown pin comparator has voltage hysteresis with typical thresholds of 1.32V (rising) and 1.29V (falling). Resistor R_{UVLO2} is optional. R_{UVLO2} can be included to reduce the overall UVLO voltage variation caused by variations in $\overline{SHDN}$ pin current (see the Electrical Characteristics). A good choice for R_{UVLO2} is ≤10k ±1%. After choosing a value for R_{UVLO2}, R_{UVLO1} can be determined from either of the following:

$$R_{UVLO1}=\frac{V_{IN}^{+}-1.32V}{\left(\frac{1.32V}{R_{UVLO2}}\right)+11.6\mu A}$$

or

$$R_{UVLO1}=\frac{V_{IN}^{-}-1.29V}{\left(\frac{1.29V}{R_{UVLO2}}\right)+11.6\mu A}$$

where V_{IN}^{+} and V_{IN}^{-} are the V_{IN} voltages when rising or falling respectively.

For example, to disable the LT3580 for V_{IN} voltages below 3.5V using the single resistor configuration, choose:

$$R_{UVLO1}=\frac{3.5V-1.29V}{\left(\frac{1.29V}{\infty}\right)+11.6\mu A}=190.5k$$

To activate the LT3580 for V_{IN} voltage greater than 4.5V using the double resistor configuration, choose R_{UVLO2} = 10k and:

$$R_{UVLO1}=\frac{4.5V-1.32V}{\left(\frac{1.32V}{10k}\right)+11.6\mu A}=22.1k$$

Internal Undervoltage Lockout

The LT3580 monitors the V_{IN} supply voltage in case V_{IN} drops below a minimum operating level (typically about 2.3V). When V_{IN} is detected low, the power switch is deactivated, and while sufficient V_{IN} voltage persists, the soft-start capacitor is discharged. After V_{IN} is detected high, the power switch will be reactivated and the soft-start capacitor will begin charging.

Thermal Considerations

For the LT3580 to deliver its full output power, it is imperative that a good thermal path be provided to dissipate the heat generated within the package. This is accomplished by taking advantage of the thermal pad on the underside of the IC. It is recommended that multiple vias in the printed circuit board be used to conduct heat away from the IC and into a copper plane with as much area as possible.

Thermal Lockout

If the die temperature reaches approximately 165°C, the part will go into thermal lockout, the power switch will be turned off and the soft-start capacitor will be discharged. The part will be enabled again when the die temperature has dropped by ~5°C (nominal).

Thermal Calculations

Power dissipation in the LT3580 chip comes from four primary sources: switch I^2R loss, NPN base drive (AC), NPN base drive (DC), and additional input current. The following formulas can be used to approximate the power losses. These formulas assume continuous mode operation,

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so they should not be used for calculating efficiency in discontinuous mode or at light load currents.

Average Input Current: $I_{IN} = \frac{V_{OUT} \bullet I_{OUT}}{V_{IN} \bullet \eta}$

Switch I^2R Loss: $P_{SW} = (DC)(I_{IN})^2(R_{SW})$

Base Drive Loss (AC): $P_{BAC} = 13n(I_{IN})(V_{OUT})(f)$

Base Drive Loss (DC): $P_{BDC} = \frac{(V_{IN})(I_{IN})(DC)}{50}$

Input Power Loss: $P_{INP} = 7mA(V_{IN})$

where:

R_{SW} = switch resistance (typically 200mΩ at 1.5A)

DC = duty cycle (see the Power Switch Duty Cycle section for formulas)

η = power conversion efficiency (typically 88% at high currents)

Example: boost configuration, V_{IN} = 5V, V_{OUT} = 12V, I_{OUT} = 0.5A, f = 1.25MHz, V_D = 0.5V:

I_{IN} = 1.36A

DC = 61.5%

P_{SW} = 228mW

P_{BAC} = 270mW

P_{BDC} = 84mW

P_{INP} = 35mW

Total LT3580 power dissipation (P_{TOT}) = 617mW

Thermal resistance for the LT3580 is influenced by the presence of internal, topside or backside planes. To calculate die temperature, use the appropriate thermal resistance number and add in worst-case ambient temperature:

$T_J = T_A + \theta_{JA} \bullet P_{TOT}$

where T_J = junction temperature, T_A = ambient temperature, θ_{JA} = 43°C/W for the 3mm × 3mm DFN package and 35°C/W to 40°C/W for the MSOP Exposed Pad package. P_{TOT} is calculated above.

V_{IN} Ramp Rate

While initially powering a switching converter application, the V_{IN} ramp rate should be limited. High V_{IN} ramp rates can cause excessive inrush currents in the passive components of the converter. This can lead to current and/or voltage overstress and may damage the passive components or the chip. Ramp rates less than 500mV/µs, depending on component parameters, will generally prevent these issues. Also, be careful to avoid hot-plugging. Hot-plugging occurs when an active voltage supply is "instantly" connected or switched to the input of the converter. Hot-plugging results in very fast input ramp rates and is not recommended. Finally, for more information, refer to Linear application note AN88, which discusses voltage overstress that can occur when an inductive source impedance is hot-plugged to an input pin bypassed by ceramic capacitors.

Layout Hints

As with all high frequency switchers, when considering layout, care must be taken to achieve optimal electrical, thermal and noise performance. One will not get advertised performance with a careless layout. For maximum efficiency, switch rise and fall times are typically in the 5ns to 10ns range. To prevent noise, both radiated and conducted, the high speed switching current path, shown in Figure 8, must be kept as short as possible. This is implemented in the suggested layout of a boost configuration in Figure 9. Shortening this path will also reduce the parasitic trace inductance. At switch-off, this parasitic inductance produces a flyback spike across the LT3580 switch. When operating at higher currents and output voltages, with poor layout, this spike can generate voltages across the LT3580 that may exceed its absolute maximum rating. A ground plane should also be used under the switcher circuitry to prevent interplane coupling and overall noise.

The VC and FB components should be kept as far away as practical from the switch node. The ground for these components should be separated from the switch current path. Failure to do so can result in poor stability or subharmonic oscillation.

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Board layout also has a significant effect on thermal resistance. The exposed package ground pad is the copper plate that runs under the LT3580 die. This is a good thermal path for heat out of the package. Soldering the pad onto the board reduces die temperature and increases the power capability of the LT3580. Provide as much copper area as possible around this pad. Adding multiple feedthroughs around the pad to the ground plane will also help. Figures 9 and 10 show the recommended component placement for the boost and SEPIC configurations, respectively.

Layout Hints for Inverting Topology

Figure 11 shows recommended component placement for the dual inductor inverting topology. Input bypass capacitor, C1, should be placed close to the LT3580, as shown. The load should connect directly to the output capacitor, C2, for best load regulation. You can tie the local ground into the system ground plane at the C3 ground terminal.

The cut ground copper at D1's cathode is essential to obtain low noise. This important layout issue arises due to the chopped nature of the currents flowing in Q1 and D1. If they are both tied directly to the ground plane before being combined, switching noise will be introduced into the ground plane. It is almost impossible to get rid of this noise, once present in the ground plane. The solution is to tie D1's cathode to the ground pin of the LT3580 before the combined currents are dumped in the ground plane as drawn in Figure 2, Figure 12 and Figure 13. This single layout technique can virtually eliminate high frequency "spike" noise, so often present on switching regulator outputs.

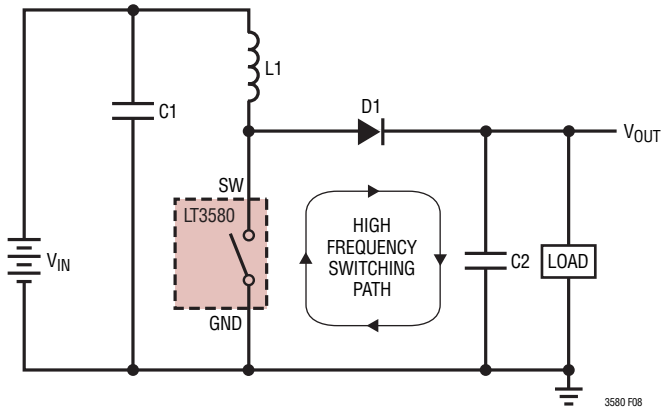

Figure 8. High Speed "Chopped" Switching Path for Boost Topology

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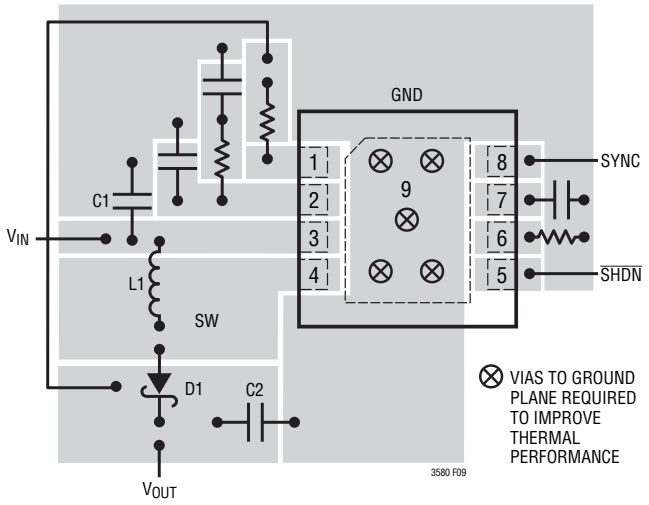


Figure 9. Suggested Component Placement for Boost Topology (Both DFN and MSOP Packages. Not to Scale). Pin 9 (Exposed Pad) Must Be Soldered Directly to the Local Ground Plane for Adequate Thermal Performance. Multiple Vias to Additional Ground Planes Will Improve Thermal Performance

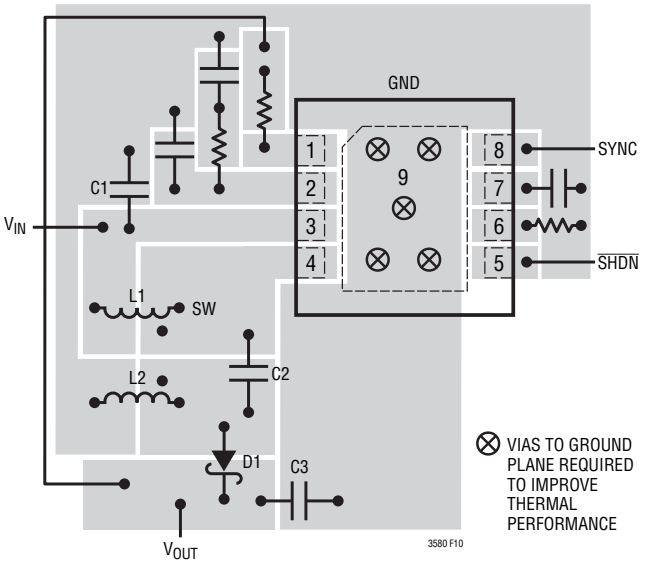


Figure 10. Suggested Component Placement for Sepic Topology (Both DFN And MSOP Packages. Not to Scale). Pin 9 (Exposed Pad) Must Be Soldered Directly to the Local Ground Plane for Adequate Thermal Performance. Multiple Vias to Additional Ground Planes Will Improve Thermal Performance

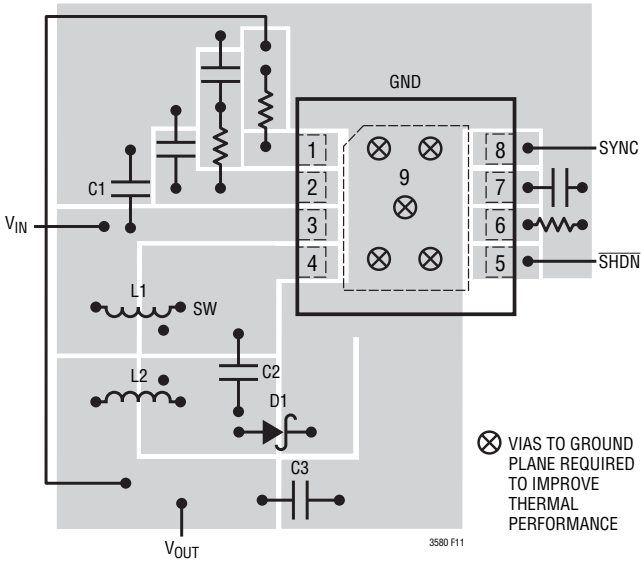


Figure 11. Suggested Component Placement for Inverting Topology (Both DFN and MSOP Packages. Not to Scale). Note Cut in Ground Copper at Diode's Cathode. Pin 9 (Exposed Pad) Must be Soldered Directly to Local Ground Plane for Adequate Thermal Performance. Multiple Vias to Additional Ground Planes Will Improve Thermal Performance

APPLICATIONS INFORMATION

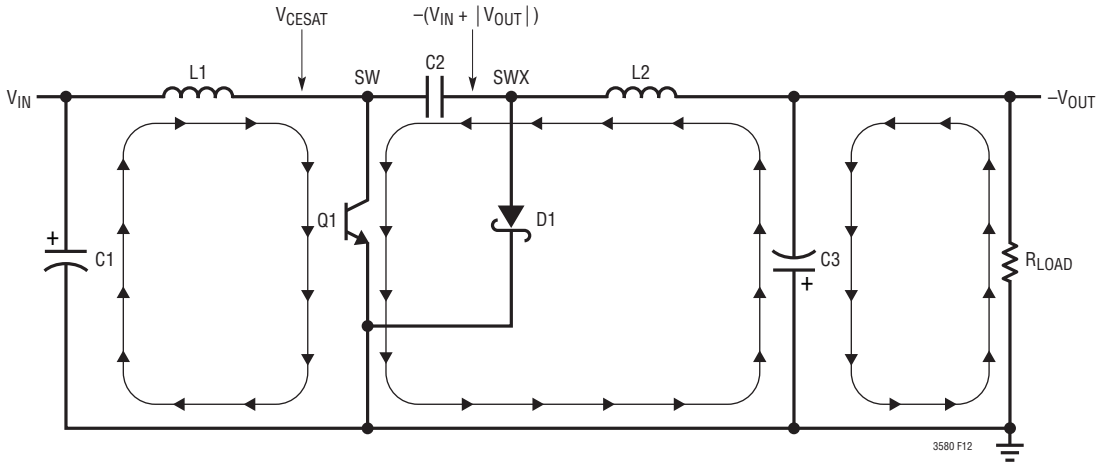


Figure 12. Switch-On Phase of an Inverting Converter. L1 and L2 Have Positive dI/dt

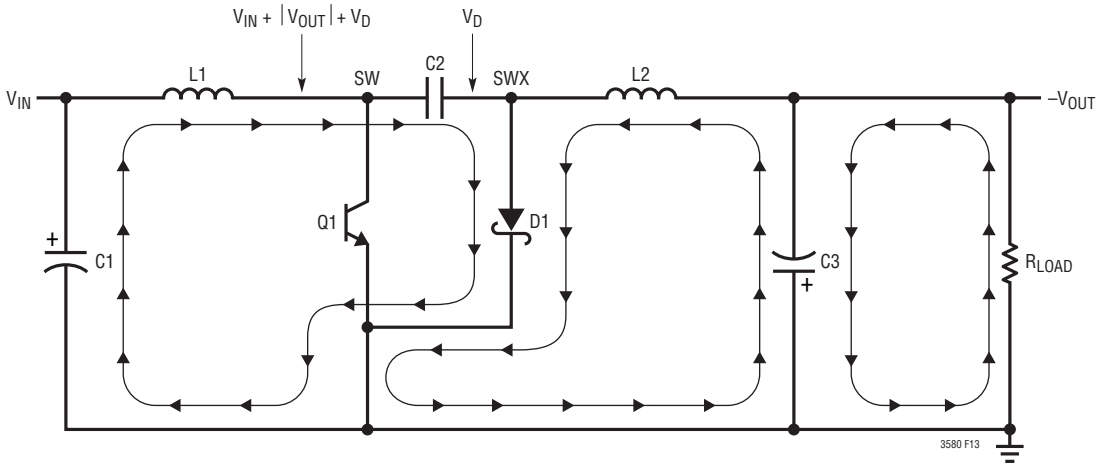


Figure 13. Switch-Off Phase of an Inverting Converter. L1 and L2 Currents Have Negative dI/dt

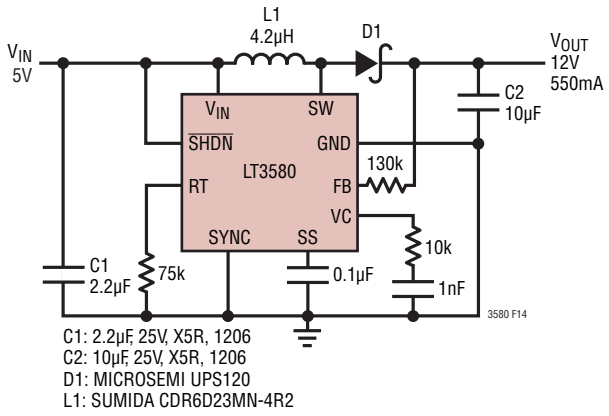
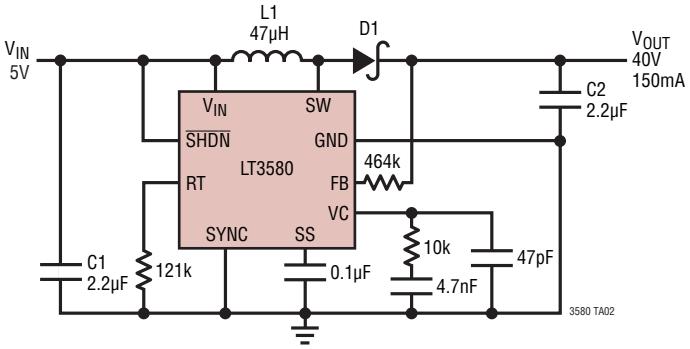


Figure 14. 1.2MHz, 5V to 12V Boost Converter

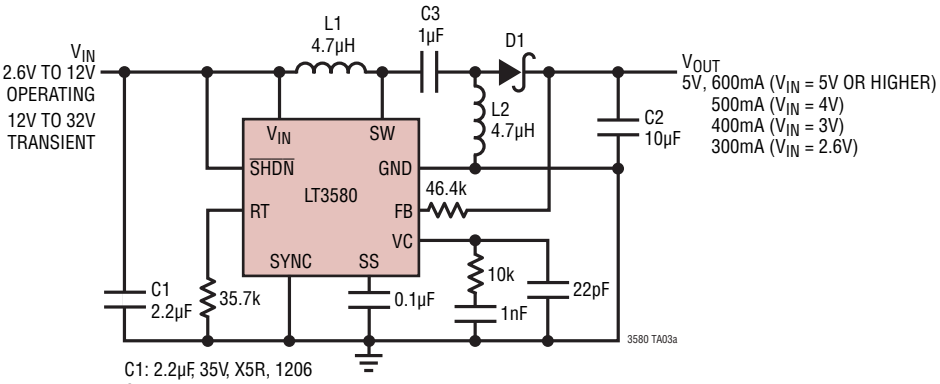
TYPICAL APPLICATIONS

750kHz, 5V to 40V, 150mA Boost Converter



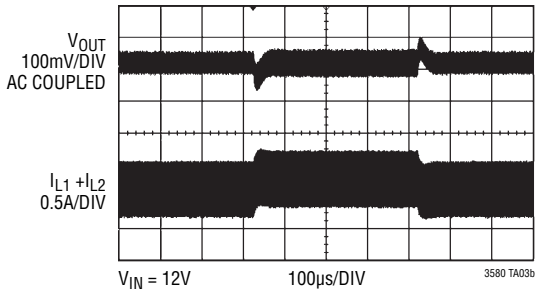
C1: 2.2µF, 25V, X5R, 1206
C2: 2.2µF, 50V, X5R, 1206
D1: MICROSEMI UPS140
L1: SUMIDA CDRH105R-470

Wide Input Range SEPIC Converter with 5V Output Switches at 2.5MHz



C1: 2.2µF, 35V, X5R, 1206
C2: 10µF, 10V, X5R, 1206
C3: 1µF, 50V, X5R, 0805
D1: MICROSEMI UPS140
L1, L2: TDK VLCF4020T-4R7N1R2

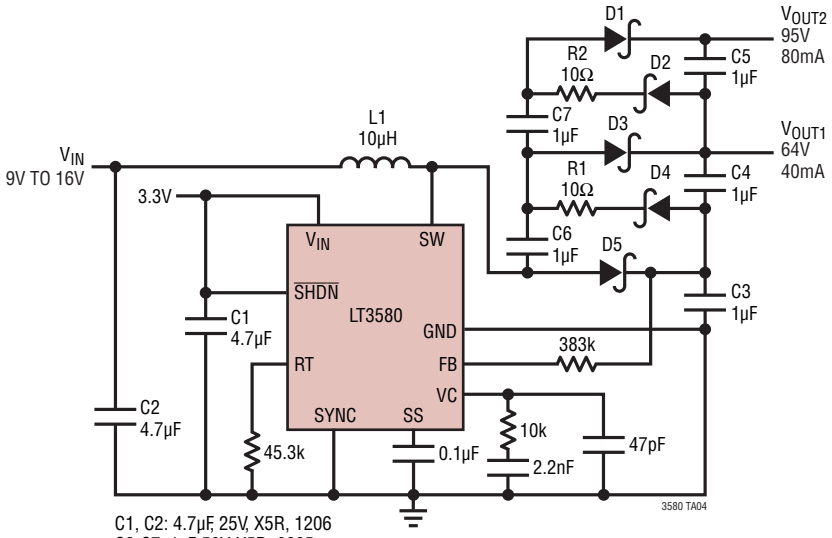
Transient Response with 400mA to 500mA Output Load Step



TYPICAL APPLICATIONS

VFD (Vacuum Flourescent Display) Power Supply Switches at 2MHz to Avoid AM Band

Danger High Voltage! Operation by High Voltage Trained Personnel Only

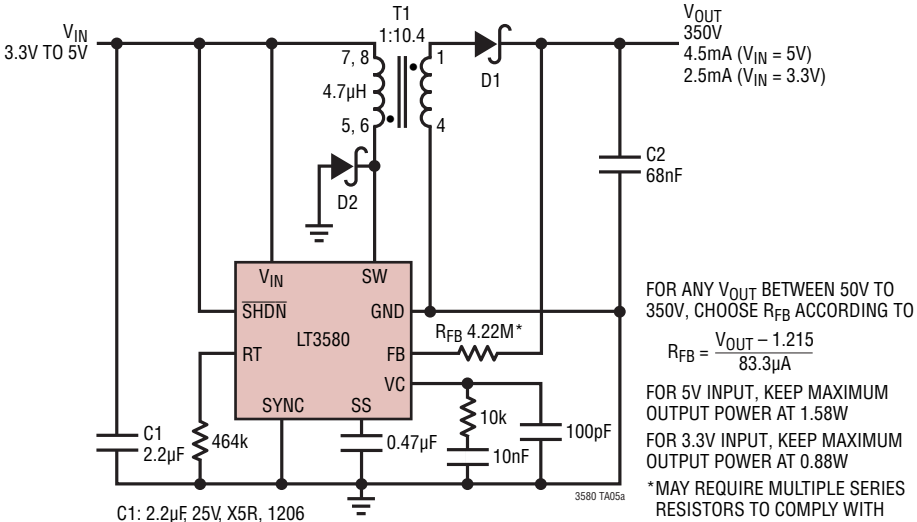


C1, C2: 4.7µF, 25V, X5R, 1206
C3-C7: 1µF, 50V, X5R, 0805
D1-D4: ON SEMICONDUCTOR MBR0540
D5: MICROSEMI UPS140
L1: SUMIDA CDR6D28MNNP-100
R1, R2: 0.5W

TYPICAL APPLICATIONS

High Voltage Positive Power Supply Uses Tiny 5.8mm × 5.8mm × 3mm Transformer and Switches at 200kHz

Danger High Voltage! Operation by High Voltage Trained Personnel Only



FOR ANY V_{OUT} BETWEEN 50V TO 350V, CHOOSE R_{FB} ACCORDING TO

$$R_{FB} = \frac{V_{OUT} - 1.215}{83.3\mu A}$$

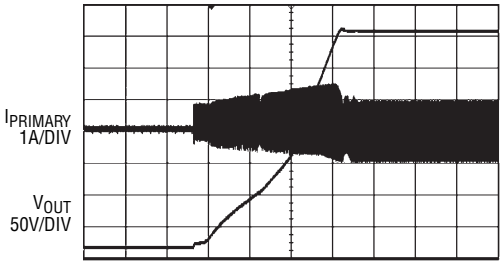
FOR 5V INPUT, KEEP MAXIMUM OUTPUT POWER AT 1.58W

FOR 3.3V INPUT, KEEP MAXIMUM OUTPUT POWER AT 0.88W

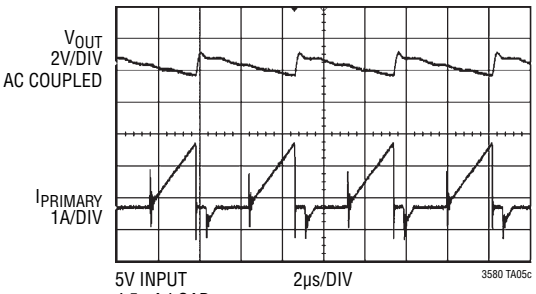
*MAY REQUIRE MULTIPLE SERIES RESISTORS TO COMPLY WITH MAXIMUM VOLTAGE RATINGS

C1: 2.2µF, 25V, X5R, 1206
C2: TDK C3225X7R2J683M
D1: VISHAY GSD2004S DUAL DIODE CONNECTED IN SERIES
D2: ON SEMICONDUCTOR MBR0540
T1: TDK LDT565630T-041

Start-Up Waveforms



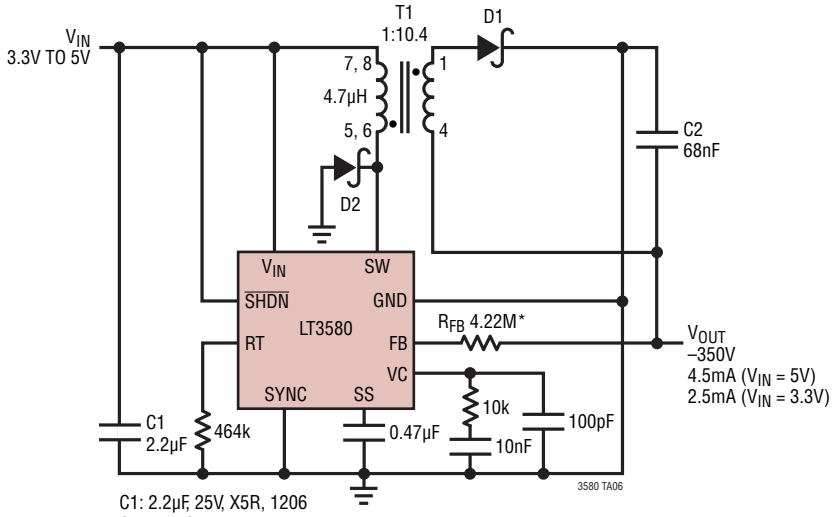
Switching Waveforms



TYPICAL APPLICATIONS

High Voltage Negative Power Supply Uses Tiny 5.8mm × 5.8mm × 3mm Transformer and Switches at 200kHz

Danger High Voltage! Operation by High Voltage Trained Personnel Only



C1: 2.2µF, 25V, X5R, 1206
C2: TDK C3225X7R2J683M
D1: VISHAY GSD2004S DUAL DIODE CONNECTED IN SERIES
D2: ON SEMICONDUCTOR MBR0540
T1: TDK LDT565630T-041

FOR ANY V_{OUT} BETWEEN –50V TO –350V, CHOOSE R_{FB} ACCORDING TO

$$R_{FB} = \frac{V_{OUT}}{83.3\mu A}$$

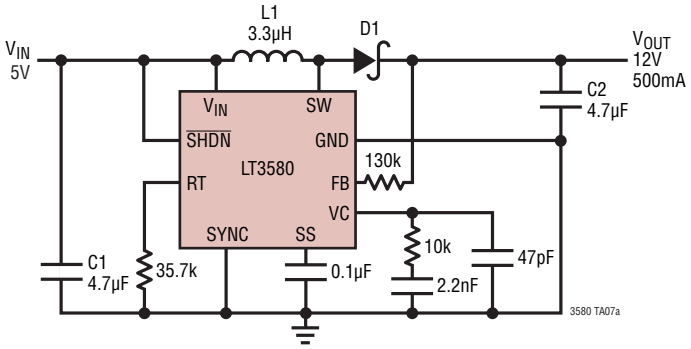
FOR 5V INPUT, KEEP MAXIMUM OUTPUT POWER AT 1.58W

FOR 3.3V INPUT, KEEP MAXIMUM OUTPUT POWER AT 0.88W

*MAY REQUIRE MULTIPLE SERIES RESISTORS TO COMPLY WITH MAXIMUM VOLTAGE RATINGS

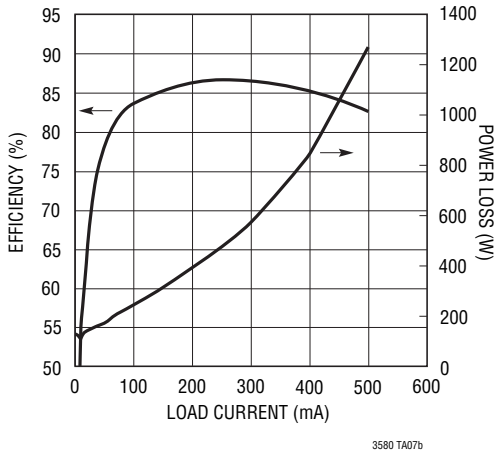
TYPICAL APPLICATIONS

5V to 12V Boost Converter Switches at 2.5MHz and Uses a Tiny 4mm × 4mm × 1.7mm Inductor

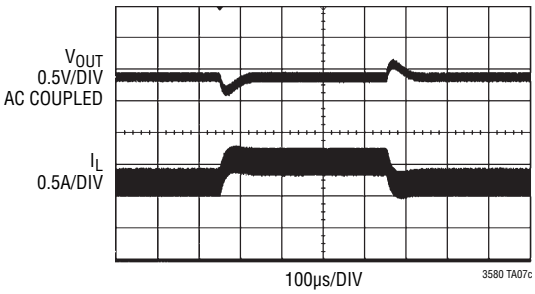


C1, C2: 4.7µF, 25V, X5R, 1206
D1: MICROSEMI UPS120
L1: COILCRAFT LPS4018-332ML

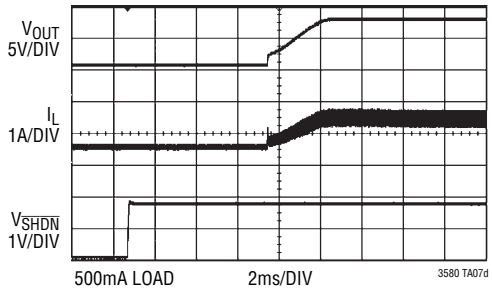
Efficiency and Power Loss vs Load Current



Transient Response with 400mA to 500mA to 400mA Output Load Step

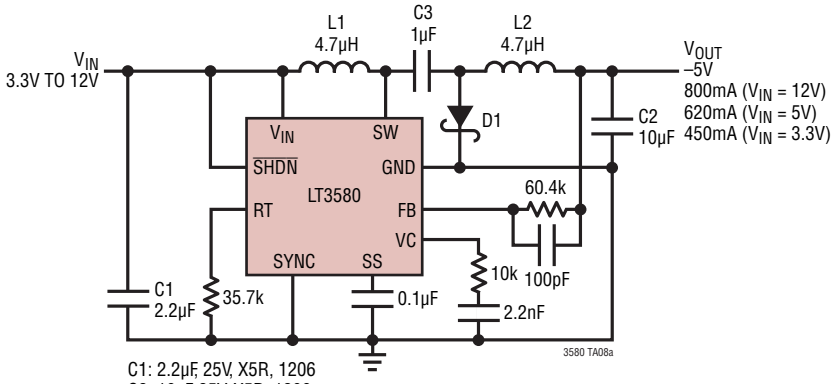


Start-Up Waveforms



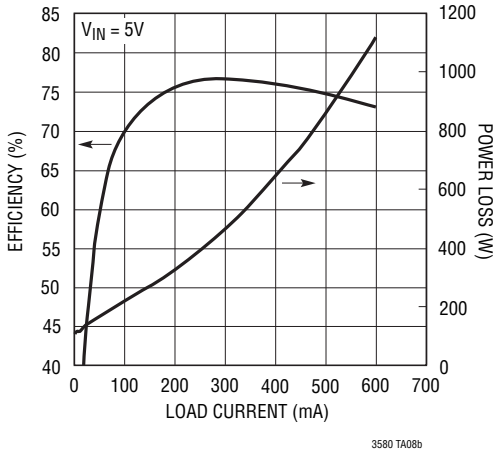
TYPICAL APPLICATIONS

–5V Output Inverting Converter Switches at 2.5MHz and Accepts Inputs Between 3.3V to 12V



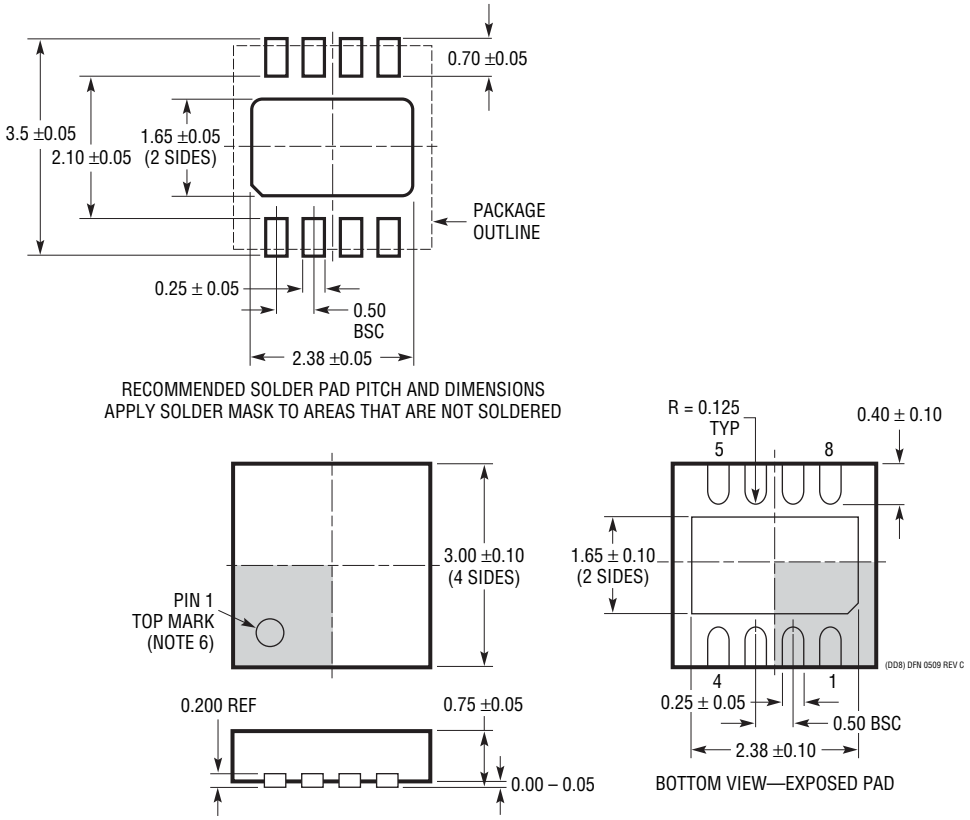
C1: 2.2µF, 25V, X5R, 1206
C2: 10µF, 25V, X5R, 1206
C3: 1µF, 50V, X5R, 0805
D1: CENTRAL SEMI CMMSH1-40
L1, L2: COILCRAFT LSP4018-472ML

Efficiency and Power Loss vs Load Current



PACKAGE DESCRIPTION

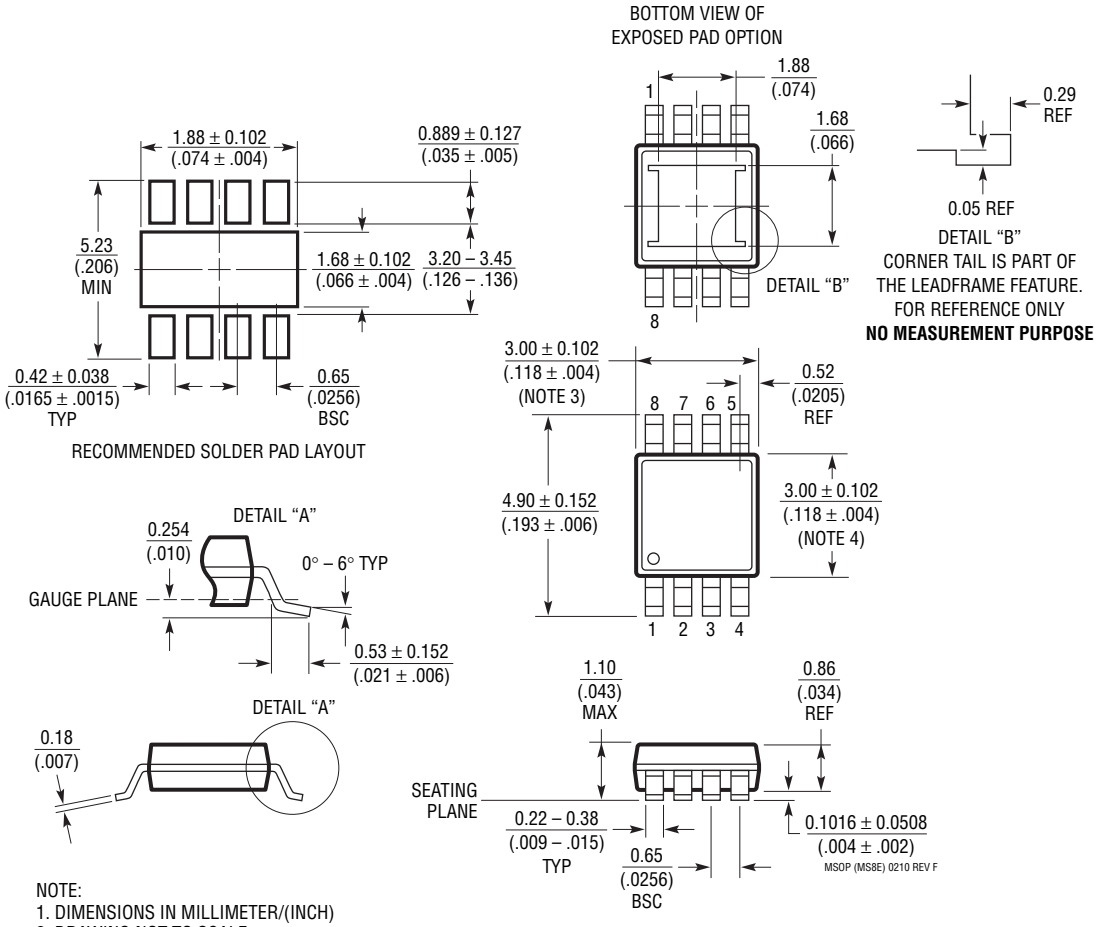
DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698 Rev C)



NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

MS8E Package
8-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1662 Rev F)



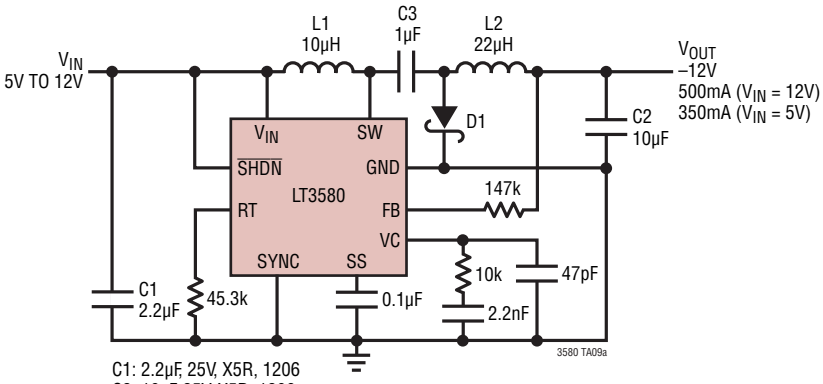
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD
   SHALL NOT EXCEED 0.254mm (.010") PER SIDE.

REVISION HISTORY (Revision history begins at Rev F)

REV	DATE	DESCRIPTION	PAGE NUMBER
F	06/10	Added GND to the Pin Configuration section.	2
		Revised Note 2 in the Electrical Characteristics section.	3
		Revised Graph G08 in the Typical Performance Characteristics section.	4
		Revised the Applications Information section.	10-11
		Revised Table 3 in the Applications Information section.	12
		Revised Figure 13 in the Applications Information section.	18
		Updated drawing TA01a in the Typical Applications section.	24
		Updated Related Parts table.	28
G	09/10	Added H- and MP-Grade information to Absolute Maximum Ratings, Order Information, Electrical Characteristics and Pin Functions sections. Added text at end of General Guidelines and revised equations under Avoiding Subharmonic Oscillations in Applications Information section.	2, 3, 5 8, 9

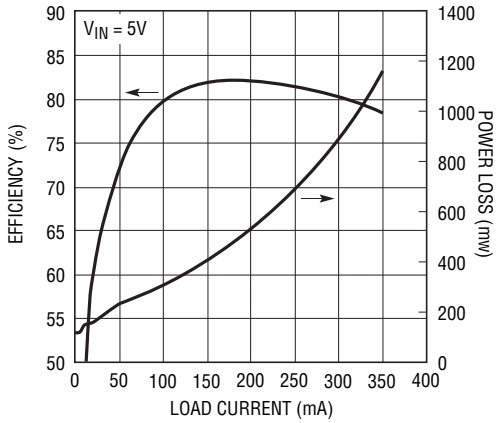
TYPICAL APPLICATION

2MHz Inverting Converter Generates –12V from a 5V to 12V Input



C1: 2.2µF, 25V, X5R, 1206
C2: 10µF, 25V, X5R, 1206
C3: 1µF, 50V, X5R, 0805
D1: CENTRAL SEMI CMMSH1-40
L1: SUMIDA CDRH6D28NP-100NC
L2: SUMIDA CDRH3D28NP-220NC

Efficiency and Power Loss vs Load Current



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1310	2A (I_{SW}), 40V, 1.2MHz High Efficiency Step-Up DC/DC Converter	V_{IN}: 2.3V to 16V, $V_{OUT(MAX)}$ = 40V, I_Q = 3mA, I_{SD} < 1µA, ThinSOT™ Package
LT1613	550mA (I_{SW}), 1.4MHz High Efficiency Step-Up DC/DC Converter	V_{IN}: 0.9V to 10V, $V_{OUT(MAX)}$ = 34V, I_Q = 3mA, I_{SD} < 1µA, ThinSOT Package
LT1618	1.5A (I_{SW}), 1.25MHz High Efficiency Step-Up DC/DC Converter	V_{IN}: 1.6V to 18V, $V_{OUT(MAX)}$ = 35V, I_Q = 1.8mA, I_{SD} < 1µA, MS10 Package
LT1930/LT1930A	1A (I_{SW}), 1.2MHz/2.2MHz High Efficiency Step-Up DC/DC Converter	V_{IN}: 2.6V to 16V, $V_{OUT(MAX)}$ = 34V, I_Q = 4.2mA/5.5mA, I_{SD} < 1µA, ThinSOT Package
LT1931/LT1931A	1A (I_{SW}), 1.2MHz/2.2MHz High Efficiency Inverting DC/DC Converter	V_{IN}: 2.6V to 16V, $V_{OUT(MAX)}$ = 34V, I_Q = 4.2mA/5.5mA, I_{SD} < 1µA, ThinSOT Package
LT1935	2A (I_{SW}), 40V, 1.2MHz High Efficiency Step-Up DC/DC Converter	V_{IN}: 2.3V to 16V, $V_{OUT(MAX)}$ = 40V, I_Q = 3mA, I_{SD} < 1µA, ThinSOT Package
LT1944/LT1944-1 (Dual)	Dual Output 350mA (I_{SW}), Constant Off-Time, High Efficiency Step-Up DC/DC Converter	V_{IN}: 1.2V to 15V, $V_{OUT(MAX)}$ = 34V, I_Q = 20µA, I_{SD} < 1µA, MS10 Package
LT1945 (Dual)	Dual Output Pos/Neg 350mA (I_{SW}), Constant Off-Time, High Efficiency Step-Up DC/DC Converter	V_{IN}: 1.2V to 15V, $V_{OUT(MAX)}$ = ±34V, I_Q = 20µA, I_{SD} < 1µA, MS10 Package
LT1946/LT1946A	1.5A (I_{SW}), 1.2MHz/2.7MHz High Efficiency Step-Up DC/DC Converter	V_{IN}: 2.6V to 16V, $V_{OUT(MAX)}$ = 34V, I_Q = 3.2mA, I_{SD} < 1µA, MS8E Package
LT1961	1.5A (I_{SW}), 1.25MHz High Efficiency Step-Up DC/DC Converter	V_{IN}: 3V to 25V, $V_{OUT(MAX)}$ = 35V, I_Q = 0.9mA, I_{SD} < 6µA, MS8E Package
LT3436	3A (I_{SW}), 800kHz, 34V Step-Up DC/DC Converter	V_{IN}: 3V to 25V, $V_{OUT(MAX)}$ = 34V, I_Q = 0.9mA, I_{SD} < 6µA, TSSOP16E Package
LT3467	1.1A (I_{SW}), 1.3MHz High Efficiency Step-Up DC/DC Converter	V_{IN}: 2.6V to 16V, $V_{OUT(MAX)}$ = 40V, I_Q = 1.2mA, I_{SD} < 1µA, ThinSOT, 2mm × 3mm DFN Packages
LT3477	42V, 3A, 3.5MHz Boost, Buck-Boost, Buck LED Driver	V_{IN}: 2.5V to 25V, $V_{OUT(MAX)}$ = 40V, Analog/PWM, I_{SD} < 1µA, QFN, TSSOP20E Packages
LT3479	3A Full-Featured DC/DC Converter with Soft-Start and Inrush Current Protection	V_{IN}: 2.5V to 24V, $V_{OUT(MAX)}$ = 40V, Analog/PWM, I_{SD} < 1µA, DFN, TSSOP Packages

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