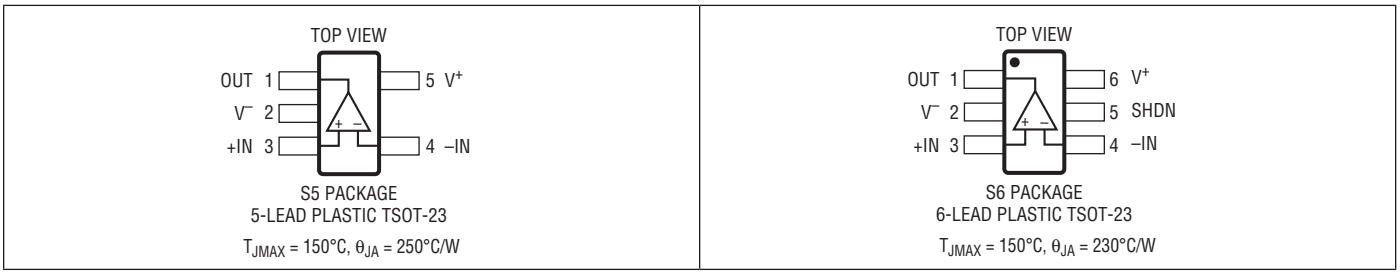
ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-) 18V
Input Differential Voltage 18V
Input Pin Voltage to V^- ..... +24V/–10V
Shutdown Pin Voltage Above V^- 18V
Shutdown Pin Current ..... ±10mA
Output Short-Circuit Duration (Note 2) ..... Indefinite

Operating Temperature Range (Note 10) .. –40°C to 85°C
Specified Temperature Range (Note 11) .. –40°C to 85°C
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LT1784CS5#PBF	LT1784CS5#TRPBF	LTJD	5-Lead Plastic TSOT-23	–40°C to 85°C
LT1784IS5#PBF	LT1784IS5#TRPBF	LTSN	5-Lead Plastic TSOT-23	–40°C to 85°C
LT1784CS6#PBF	LT1784CS6#TRPBF	LTIW	6-Lead Plastic TSOT-23	–40°C to 85°C
LT1784IS6#PBF	LT1784IS6#TRPBF	LTIX	6-Lead Plastic TSOT-23	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at T_A = 25°C. V_S = 3V, 0V; V_S = 5V, 0V, V_{CM} = V_{OUT} = half supply, for the 6-lead part V_{PIN5} = 0V, pulse power tested unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	T_A = 25°C			1.5	3.5	mV
		0°C ≤ T_A ≤ 70°C	●			4.2	mV
		–40°C ≤ T_A ≤ 85°C	●			4.5	mV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift (Note 7)	–40°C ≤ T_A ≤ 85°C	●		5	15	µV/°C
I_{OS}	Input Offset Current		●		25	50	nA
		V_{CM} = 18V (Note 3)	●			50	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at T_A = 25°C. V_S = 3V, 0V; V_S = 5V, 0V, V_{CM} = V_{OUT} = half supply, for the 6-lead part V_{PIN5} = 0V, pulse power tested unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_B	Input Bias Current		●		250	500	nA
		V_{CM} = 18V (Note 3)	●		225	400	µA
		SHDN or V_S = 0V, V_{CM} = 0V to 18V			0.1		nA
$\Delta I_B/\Delta T$	Input Bias Current Drift	–40°C ≤ T_A ≤ 85°C	●		0.4		nA/°C
	Input Noise Voltage	0.1Hz to 10Hz			1.5		μV_{P-P}
e_n	Input Noise Voltage Density	f = 10kHz			25		$nV/\sqrt{Hz}$
i_n	Input Noise Current Density	f = 10kHz			0.3		$pA/\sqrt{Hz}$
R_{IN}	Input Resistance	Differential		100	200		kΩ
		Common Mode, V_{CM} = 0V to (V_{CC} – 1.2V)			150		MΩ
		Common Mode, V_{CM} = 0V to 18V		45	80		kΩ
C_{IN}	Input Capacitance				5		pF
V_{CM}	Input Voltage Range		●	0		18	V
CMRR	Common Mode Rejection Ratio	V_{CM} = 0V to V_{CC} – 1.2V	●	84	95		dB
	(Note 3)	V_{CM} = 0V to 18V (Note 6)	●	60	70		dB
PSRR	Power Supply Rejection Ratio	V_S = 3V to 12.5V, V_{CM} = V_O = 1V	●	90	100		dB
A_{VOL}	Large-Signal Voltage Gain	V_S = 3V, V_O = 500mV to 2.5V, R_L = 10k		133	1000		V/mV
		V_S = 3V, 0°C ≤ T_A ≤ 70°C	●	90			V/mV
		V_S = 3V, –40°C ≤ T_A ≤ 85°C	●	60			V/mV
		V_S = 5V, V_O = 500mV to 4.5V, R_L = 10k		266	1000		V/mV
		V_S = 5V, 0°C ≤ T_A ≤ 70°C	●	180			V/mV
		V_S = 5V, –40°C ≤ T_A ≤ 85°C	●	120			V/mV
V_{OL}	Output Voltage Swing LOW	No Load	●		4	10	mV
		I_{SINK} = 5mA	●		200	400	mV
		V_S = 5V, I_{SINK} = 10mA	●		350	600	mV
V_{OH}	Output Voltage Swing HIGH	V_S = 3V, No Load	●	2.885	2.93		V
		V_S = 3V, I_{SOURCE} = 3mA	●	2.600	2.8		V
		V_S = 5V, No Load	●	4.885	4.93		V
		V_S = 5V, I_{SOURCE} = 10mA	●	4.400	4.7		V
I_{SC}	Short-Circuit Current (Note 2)	V_S = 3V, Short to GND		4	7.5		mA
		V_S = 3V, Short to V_{CC}		15	30		mA
		V_S = 5V, Short to GND		12.5	22		mA
		V_S = 5V, Short to V_{CC}		20.0	40		mA
	Minimum Supply Voltage		●		2.5	2.7	V
	Reverse Supply Voltage	I_S = –100µA	●	18			V
I_S	Supply Current				500	750	µA
	(Note 4)		●			900	µA
	Supply Current, Shutdown	V_{PIN5} = 2V, No Load (Note 8)	●		7	18	µA
I_{SHDN}	SHDN Pin Current	V_{PIN5} = 0.3V (On), No Load (Note 8)	●		0.5		nA
		V_{PIN5} = 2V (Shutdown), No Load (Note 8)	●		2.0	8	µA
		V_{PIN5} = 5V (Shutdown), No Load (Note 8)			5.0		µA
	Output Leakage Current, Shutdown	V_{PIN5} = 2V, No Load (Note 8)	●		0.05	1	µA
	Maximum SHDN Pin Current	V_{PIN5} = 18V, No Load (Note 8)	●		10	30	µA
V_{IL}	SHDN Pin Input Low Voltage	(Note 8)	●			0.3	V
V_{IH}	SHDN Pin Input High Voltage	(Note 8)	●	2			V
t_{ON}	Turn-On Time	V_{PIN5} = 5V to 0V, R_L = 10k (Note 8)			18		µs
t_{OFF}	Turn-Off Time	V_{PIN5} = 0V to 5V, R_L = 10k (Note 8)			2.2		µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at T_A = 25°C. V_S = 3V, 0V; V_S = 5V, 0V, V_{CM} = V_{OUT} = half supply, for the 6-lead part V_{PIN5} = 0V, pulse power tested unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
GBW	Gain Bandwidth Product (Note 4)	f = 5kHz 0°C ≤ T_A ≤ 70°C –40°C ≤ T_A ≤ 85°C	 ● ●	1.5 1.2 1.1	2.5		MHz MHz MHz
SR	Slew Rate (Note 5)	A_V = –1, R_L = ∞ 0°C ≤ T_A ≤ 70°C –40°C ≤ T_A ≤ 85°C	 ● ●	1.2 1.1 1.0	2.1		V/µs V/µs V/µs
FPBW	Full-Power Bandwidth (Note 9)	V_{OUT} = $2V_{P-P}$			350		kHz
t_S	Settling Time	V_S = 5V, ΔV_{OUT} = 2V to 0.1%, A_V = –1			3.7		µs
THD	Distortion	V_S = 3V, V_O = $1.8V_{P-P}$, A_V = 1, R_L = 10k, f = 1kHz			0.001		%

The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at T_A = 25°C. V_S = ±5V, V_{CM} = 0V, V_{OUT} = 0V, for the 6-lead part V_{PIN5} = V^-, pulse power tested unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	T_A = 25°C 0°C ≤ T_A ≤ 70°C –40°C ≤ T_A ≤ 85°C	 ● ●		1.6	3.75 4.50 4.80	mV mV mV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift (Note 7)	–40°C ≤ T_A ≤ 85°C	●		5	15	µV/°C
I_{OS}	Input Offset Current		●		25	50	nA
I_B	Input Bias Current		●		250	500	nA
$\Delta I_B/\Delta T$	Input Bias Current Drift	0°C ≤ T_A ≤ 70°C	●		0.4		nA/°C
	Input Noise Voltage	0.1Hz to 10Hz			1.5		μV_{P-P}
e_n	Input Noise Voltage Density	f = 1kHz			25		$nV/\sqrt{Hz}$
i_n	Input Noise Current Density	f = 1kHz			0.3		$pA/\sqrt{Hz}$
R_{IN}	Input Resistance	Differential Common Mode, V_{CM} = –5V to 13V	● ●	100 45	200 80		kΩ kΩ
C_{IN}	Input Capacitance				5		pF
V_{CM}	Input Voltage Range		●	–5		13	V
CMRR	Common Mode Rejection Ratio	V_{CM} = –5V to 13V	●	60	70		dB
A_{VOL}	Large-Signal Voltage Gain	V_O = ±4V, R_L = 10k 0°C ≤ T_A ≤ 70°C	 ●	50 35	100		V/mV V/mV
V_{OL}	Output Voltage Swing LOW	No Load I_{SINK} = 5mA I_{SINK} = 10mA	● ● ●		–4.996 –4.800 –4.650	–4.99 –4.60 –4.40	V V V
V_{OH}	Output Voltage Swing HIGH	No Load I_{SOURCE} = 5mA I_{SOURCE} = 10mA	● ● ●	4.885 4.550 4.400	4.92 4.75 4.65		V V V
I_{SC}	Short-Circuit Current (Note 2)	Short to GND 0°C ≤ T_A ≤ 70°C	 ●	15 10	27		mA mA
PSRR	Power Supply Rejection Ratio	V_S = ±1.5V to ±9V	●	90	100		dB
I_S	Supply Current		 ●		540	800 975	µA µA
	Supply Current, Shutdown	V_{PIN5} = –3V, V_S = ±5V, No Load (Note 8)	●		8	20	µA
I_{SHDN}	SHDN Pin Current	V_{PIN5} = –4.7V (On), V_S = ±5V, No Load (Note 8) V_{PIN5} = –3V (Shutdown), V_S = ±5V, No Load (Note 8)	● ●		0.5 2.0	 8	nA µA
	Maximum SHDN Pin Current	V_{PIN5} = 9V, V_S = ±9V (Note 8)	●		10	30	µA
	Output Leakage Current, Shutdown	V_{PIN5} = –7V, V_S = ±9V, No Load (Note 8)	●		0.05	1	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at T_A = 25°C. V_S = ±5V, V_{CM} = 0V, V_{OUT} = 0V, for the 6-lead part V_{PIN5} = V^-, pulse power tested unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IL}	SHDN Pin Input Low Voltage	V_S = ±5V (Note 8)	●			–4.7	V
V_{IH}	SHDN Pin Input High Voltage	V_S = ±5V (Note 8)	●	–3			V
t_{ON}	Turn-On Time	V_{PIN5} = 0V to –5V, R_L = 10k (Note 8)	●		18		µs
t_{OFF}	Turn-Off Time	V_{PIN5} = –5V to 0V, R_L = 10k (Note 8)	●		2.2		µs
GBW	Gain Bandwidth Product	f = 5kHz		1.55	2.6		MHz
		0°C ≤ T_A ≤ 70°C	●	1.30			MHz
		–40°C ≤ T_A ≤ 85°C	●	1.20			MHz
SR	Slew Rate	A_V = –1, R_L = ∞, V_O = ±4V, Measured at V_O = ±2V		1.3	2.2		V/µs
		0°C ≤ T_A ≤ 70°C	●	1.2			V/µs
		–40°C ≤ T_A ≤ 85°C	●	1.1			V/µs
FPBW	Full-Power Bandwidth (Note 9)	V_{OUT} = $8V_{P-P}$			94		kHz
t_S	Settling Time	V_S = 5V, ΔV_{OUT} = 4V to 0.1%, A_V = 1			3.4		µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: A heat sink may be required to keep the junction temperature below absolute maximum.

Note 3: V_S = 5V limits are guaranteed by correlation to V_S = 3V and V_S = ±5V or V_S = ±9V tests.

Note 4: V_S = 3V limits are guaranteed by correlation to V_S = 5V and V_S = ±5V or V_S = ±9V tests.

Note 5: Guaranteed by correlation to slew rate at V_S = ±5V, and GBW at V_S = 5V and V_S = ±5V tests.

Note 6: This specification implies a typical input offset voltage of 5.7mV at V_{CM} = 18V and a maximum input offset voltage of 18mV at V_{CM} = 18V.

Note 7: This parameter is not 100% tested.

Note 8: Specifications apply to 6-lead SOT-23 with shutdown.

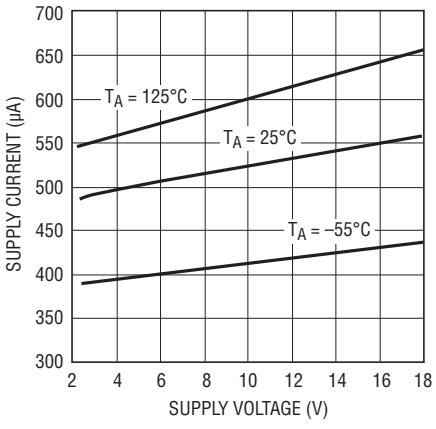
Note 9: Full-power bandwidth is calculated from the slew rate. FPBW = $SR/2\pi V_P$.

Note 10: The LT1784C is guaranteed functional over the operating temperature range –40°C to 85°C.

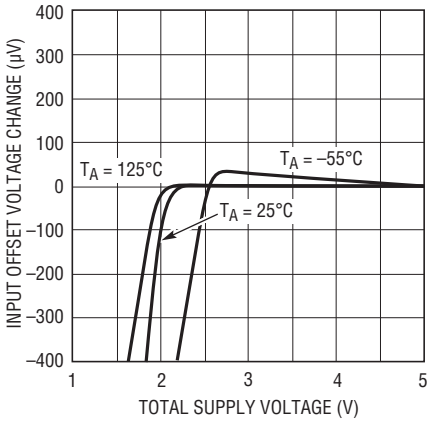
Note 11: The LT1784C is guaranteed to meet specified performance from 0°C to 70°C. The LT1784C is designed, characterized and expected to meet specified performance from –40°C to 85°C but is not tested or QA sampled at these temperatures. LT1784I is guaranteed to meet specified performance from –40°C to 85°C.

TYPICAL PERFORMANCE CHARACTERISTICS

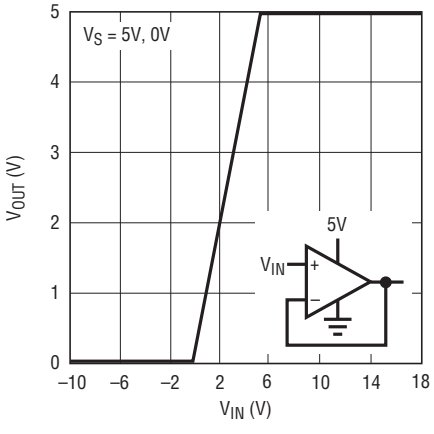
Supply Current vs Supply Voltage



Minimum Supply Voltage

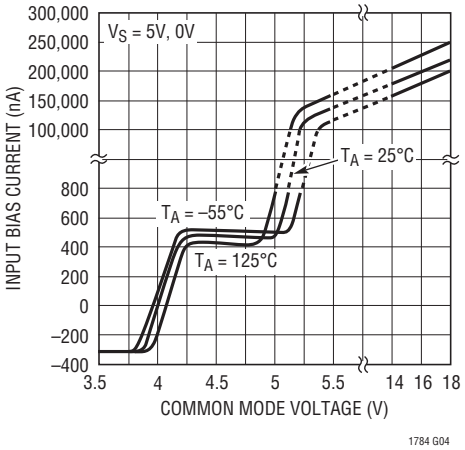


Output Voltage vs Large Input Voltage



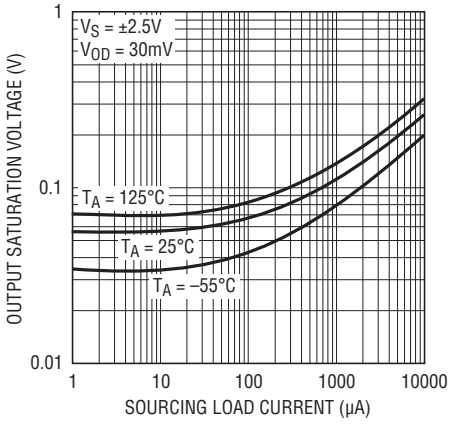
TYPICAL PERFORMANCE CHARACTERISTICS

Input Bias Current vs Common Mode Voltage



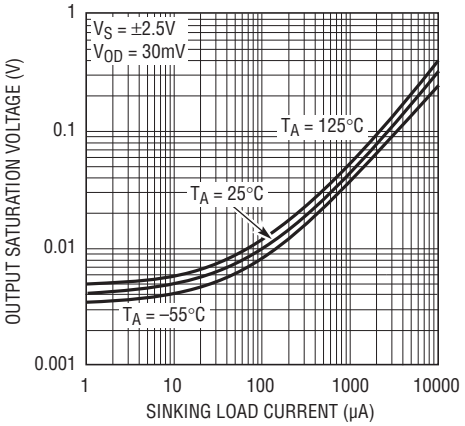
1784 G04

Output Saturation Voltage vs Load Current (Output High)



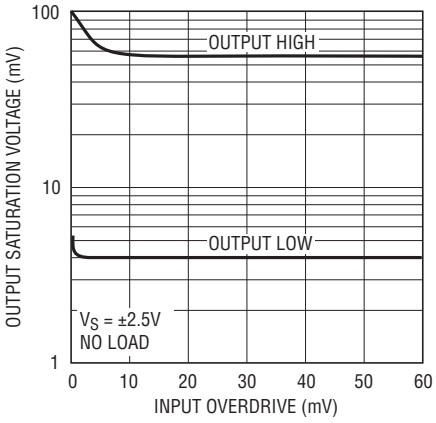
1784 G05

Output Saturation Voltage vs Load Current (Output Low)



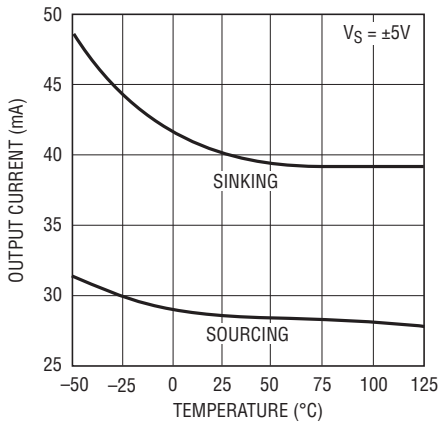
1784 G06

Output Saturation Voltage vs Input Overdrive



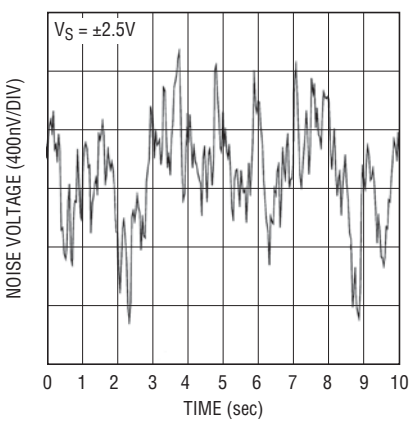
1784 G07

Output Short-Circuit Current vs Temperature



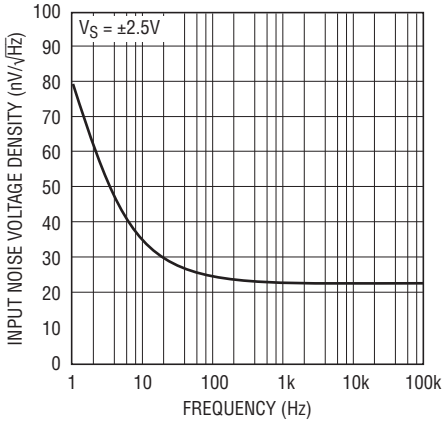
1784 G08

0.1Hz to 10Hz Noise Voltage



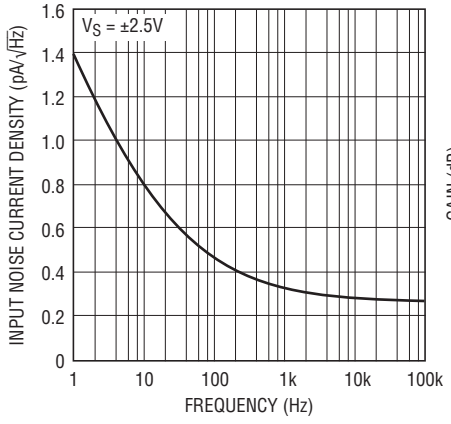
1784 G09

Noise Voltage Density vs Frequency



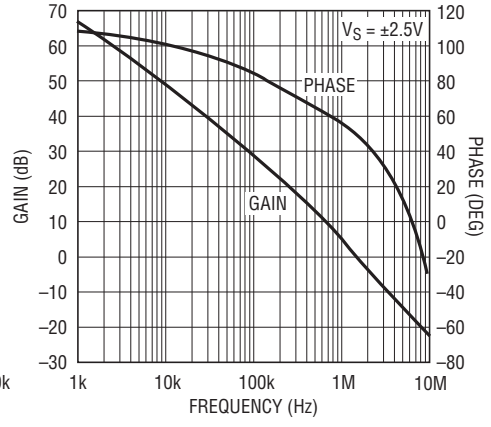
1784 G10

Input Noise Current vs Frequency



1784 G11

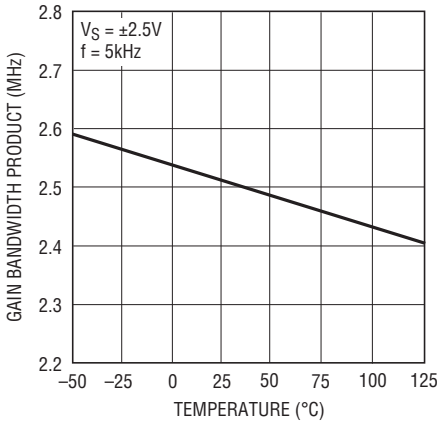
Gain and Phase Shift vs Frequency



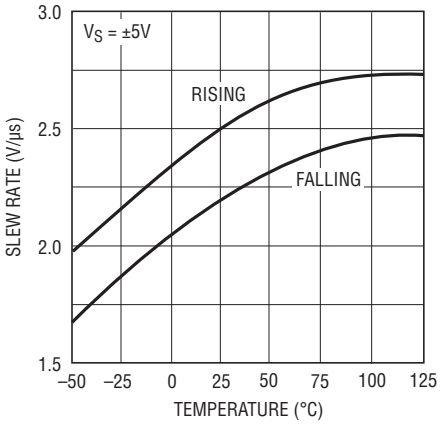
1784 G12

TYPICAL PERFORMANCE CHARACTERISTICS

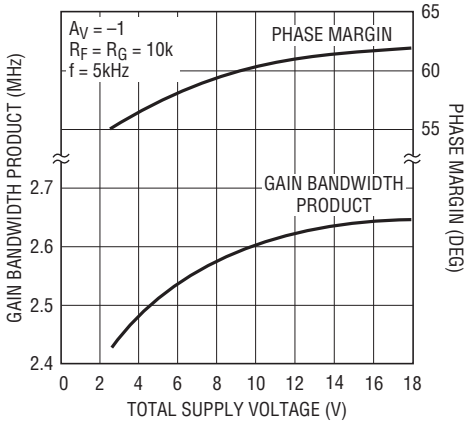
Gain Bandwidth Product vs Temperature



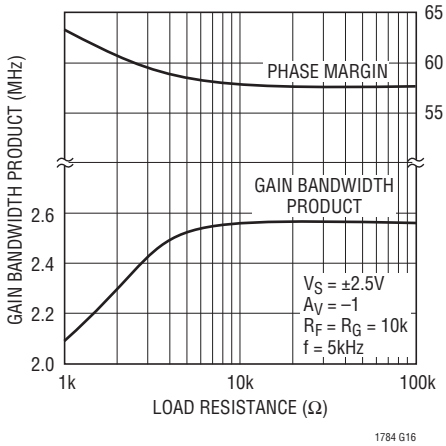
Slew Rate vs Temperature



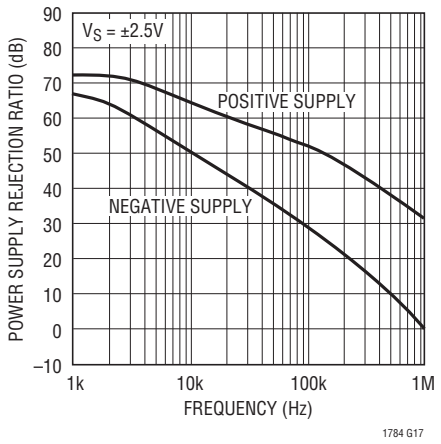
Gain Bandwidth Product and Phase Margin vs Supply Voltage



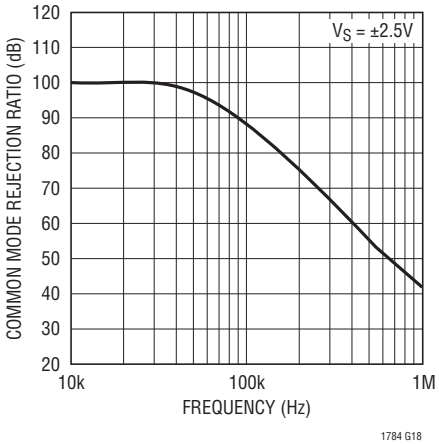
Gain Bandwidth and Phase Margin vs Load Resistance



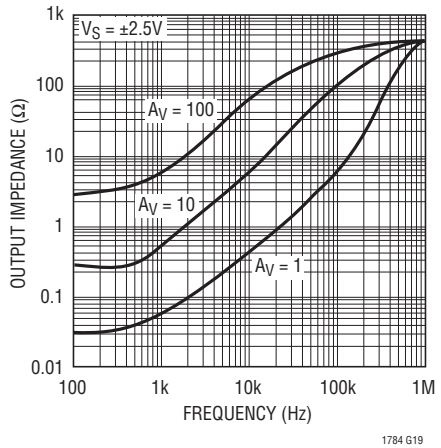
PSRR vs Frequency



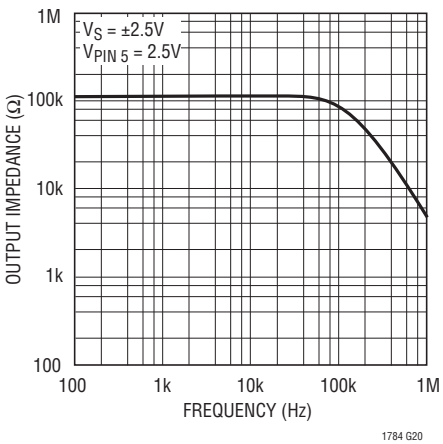
CMRR vs Frequency



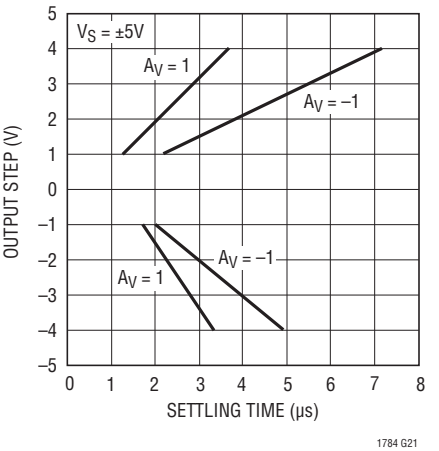
Output Impedance vs Frequency



Disabled Output Impedance vs Frequency

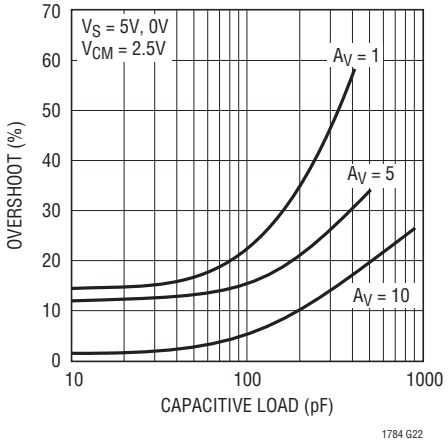


Settling Time to 0.1% vs Output Step



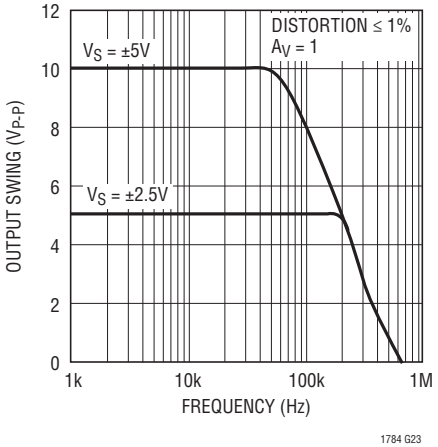
TYPICAL PERFORMANCE CHARACTERISTICS

Capacitive Load Handling Overshoot vs Capacitive Load



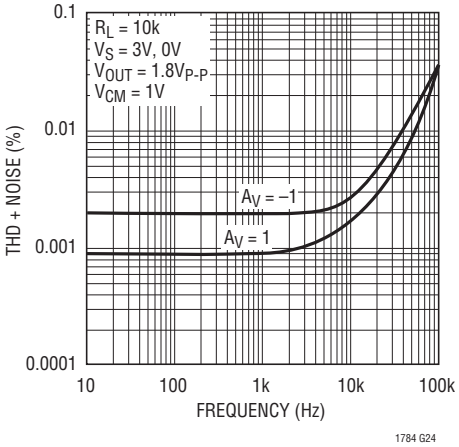
1784 G22

Undistorted Output Swing vs Frequency



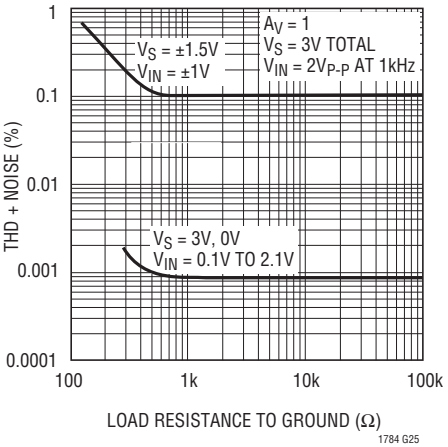
1784 G23

Total Harmonic Distortion + Noise vs Frequency



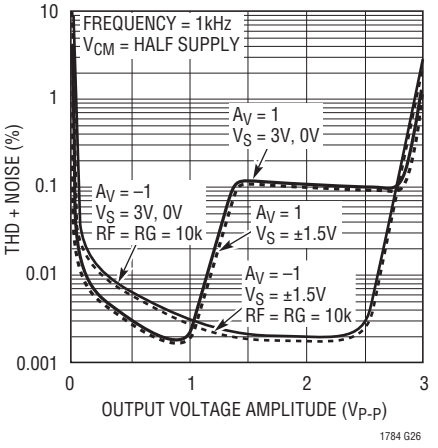
1784 G24

Total Harmonic Distortion + Noise vs Load Resistance



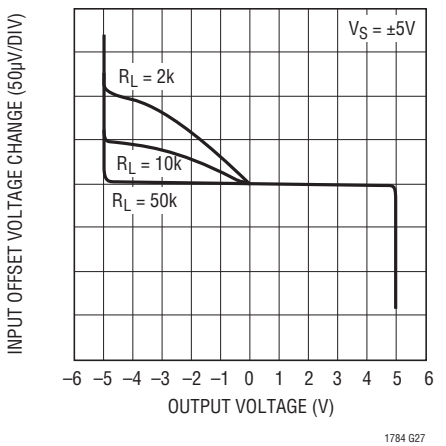
1784 G25

Total Harmonic Distortion + Noise vs Output Voltage Amplitude



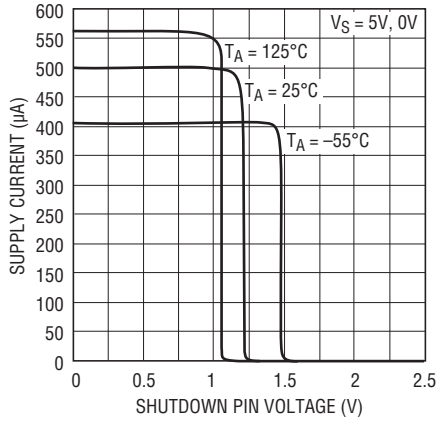
1784 G26

Open-Loop Gain



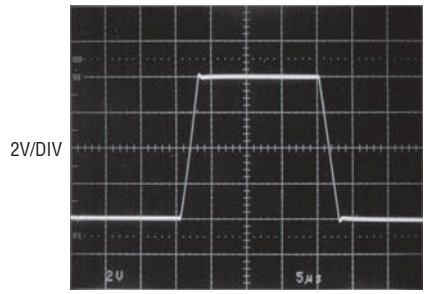
1784 G27

Supply Current vs SHDN Pin Voltage



1784 G28

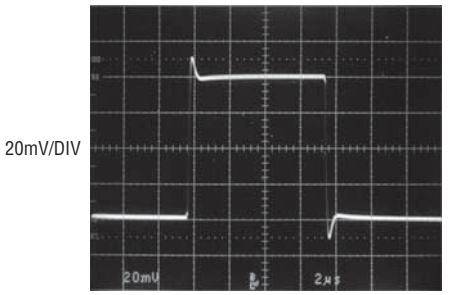
Large Signal Response



V_S = ±5V
A_V = 1
C_L = 15pF
5μs/DIV

1784 G29

Small Signal Response



V_S = ±5V
A_V = 1
C_L = 15pF
2μs/DIV

1784 G30

APPLICATIONS INFORMATION

Supply Voltage

The positive supply pin of the LT1784 should be bypassed with a small capacitor (typically 0.1µF) within an inch of the pin. When driving heavy loads, and additional 4.7µF electrolytic capacitor should be used. When using split supplies the same is true for the negative supply pin.

The LT1784 is protected against reverse battery voltages up to 18V. In the event a reverse battery condition occurs the supply current is less than 1nA.

Inputs

The LT1784 has two input stages, NPN and PNP (see the Simplified Schematic), resulting in three distinct operating regions as shown in the "Input Bias Current vs Common Mode" Typical Performance Characteristic curve.

For input voltages about 1V or more below V^+, the PNP input stage is active and the input bias current is typically –250nA. When the input common mode voltage is within 0.6V of the positive rail, the NPN stage is operating and the input bias current is typically 500nA. Increases in temperature will cause the voltage at which operation switches from the PNP input stage to the NPN input stage to move towards V^+. The input offset voltage of the NPN stage is untrimmed and is typically 3mV.

A Schottky diode in the collector of the input transistors, along with special geometries for these NPN transistors, allow the LT1784 to operate with either or both of its inputs above V^+. At about 0.3V above V^+, the NPN input transistors is fully saturated and the input bias current is typically 200µA at room temperature. The input offset voltage is typically 3mV when operating above V^+. The LT1784 will operate with inputs 18V above $V^–$ regardless of V^+.

The inputs are protected against excursions as much as 10V below $V^–$ by an internal 1k resistor in series with each input and a diode from the input to the negative supply. The input stage of the LT1784 incorporates phase reversal protection to prevent the output from phase reversing for inputs up to 9V below $V^–$. There are no clamping diodes between the inputs and the maximum differential input voltage is 18V.

Output

The output of the LT1784 can swing to within 80mV of the positive rail and within 4mV of the negative rail with no load. When monitoring input voltages within 80mV of the positive rail or within 4mV of the negative rail, gain should be taken to keep the output from clipping. The LT1784 can typically sink and source over 25mA at ±5V supplies, sourcing current is reduced to 7.5mA at 3V total supplies as noted in the Electrical Characteristics section.

The LT1784 is internally compensated to drive at least 400pF of capacitance under any output loading conditions. A 0.22µF capacitor in series with a 150Ω resistor between the output and ground will compensate these amplifiers for larger capacitive loads, up to 10,000pF at all output currents.

Distortion

There are two main contributors to distortion in op amps: output crossover distortion as the output transitions from sourcing to sinking current, and distortion caused by nonlinear common mode rejection. If the op amp is operating inverting, there is no common mode induced distortion. If the op amp is operating in the PNP input stage (input not within 1V of V^+), the CMRR is very good, typically 95dB. When the LT1784 switches between input stages, there is significant nonlinearity in the CMRR. Lower load resistance increases the output crossover distortion but has no effect on the input stage transition distortion. For lowest distortion, the LT1784 should be operated single supply, with the output always sourcing current and with the input voltage swing between ground and (V^+ – 1V). See Typical Performance Characteristics curve, "Total Harmonic Distortion + Noise vs Output Voltage Amplitude."

Gain

The open-loop gain is almost independent of load when the output is sourcing current. This optimizes performance in single supply applications where the load is returned to ground. The Typical Performance Characteric curve "Open-Loop Gain" for various loads shows the details.

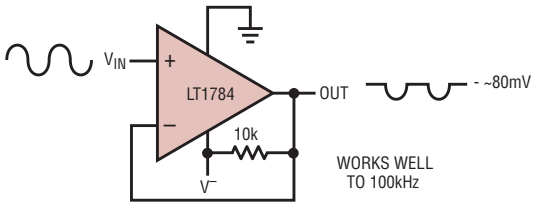
APPLICATIONS INFORMATION

Shutdown

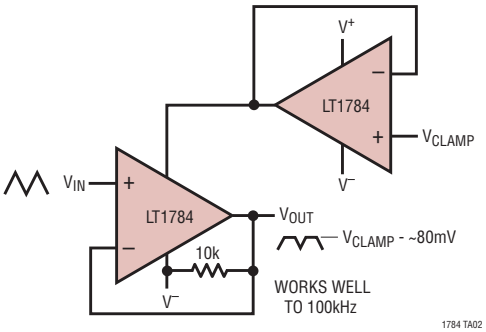
The 6-lead part includes a shutdown feature that disables the part, reducing quiescent current and making the output high impedance. The part can be shut down by bringing the SHDN pin 1.2V or more above V^-. When shut down, the supply current is less than 1µA ($V^- \leq V_{OUT} \leq V^+$). In normal operation, the SHDN pin can be tied to V^- or left floating. See Typical Performance Characteristics curve, "Supply Current vs SHDN pin Voltage."

TYPICAL APPLICATIONS

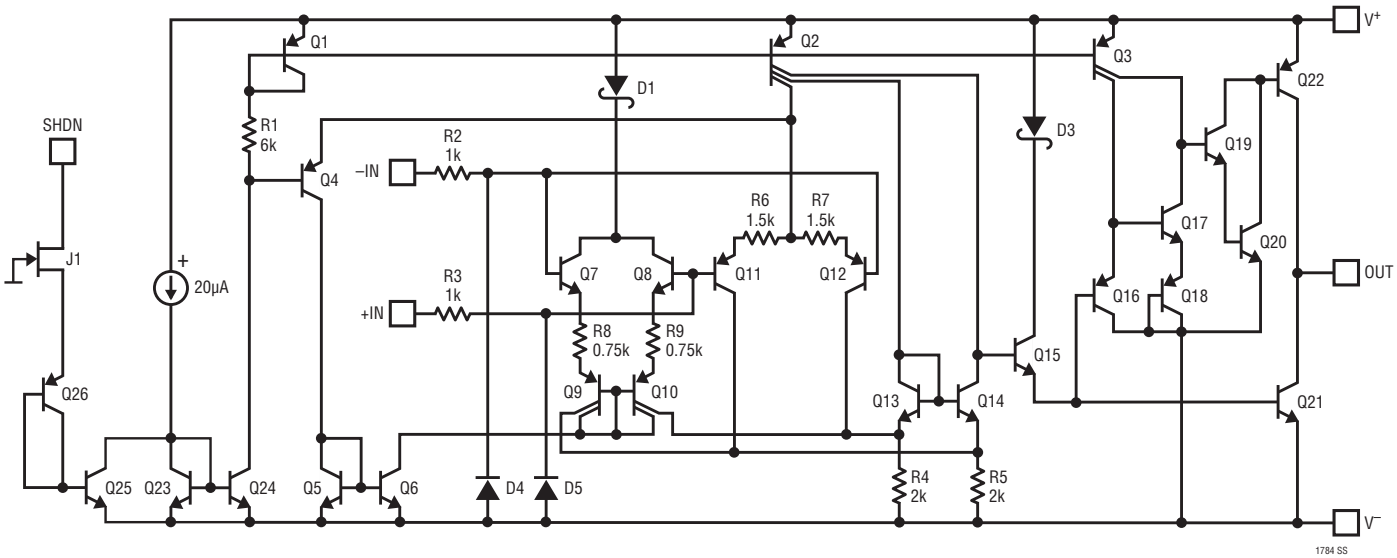
Negative Rectifier



Adjustable Clamp

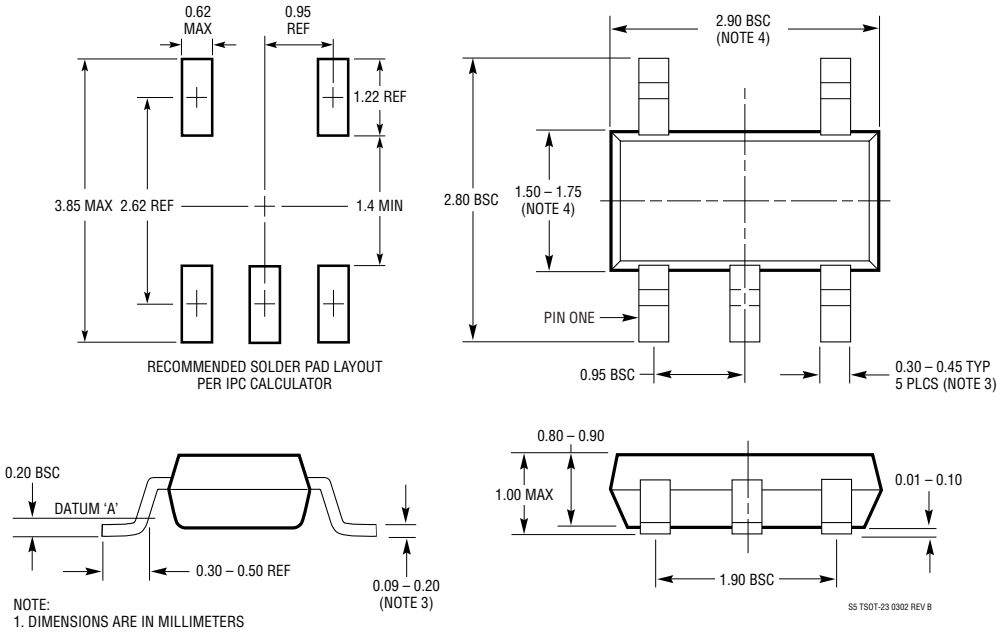


SIMPLIFIED SCHEMATIC



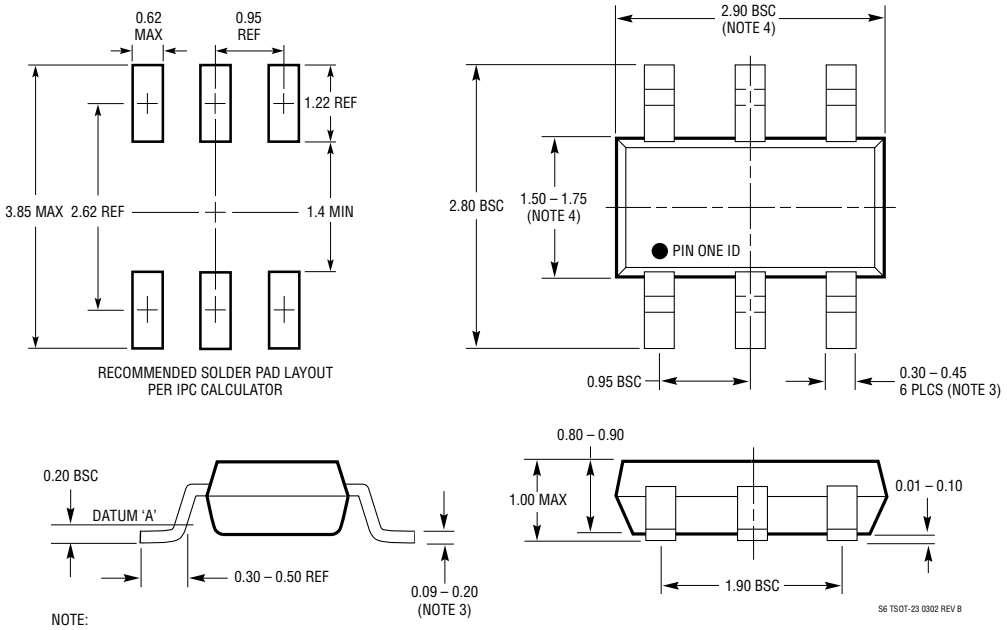
PACKAGE DESCRIPTION

S5 Package
5-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1635 Rev B)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

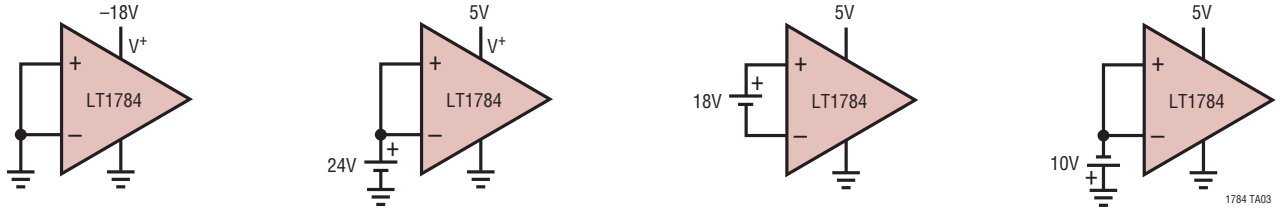
S6 Package
6-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1636 Rev B)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

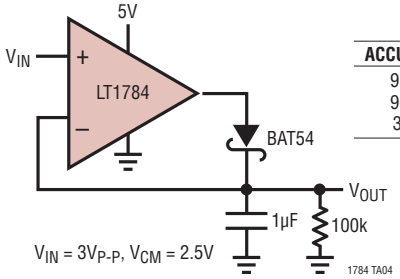
TYPICAL APPLICATIONS

Protected Fault Conditions



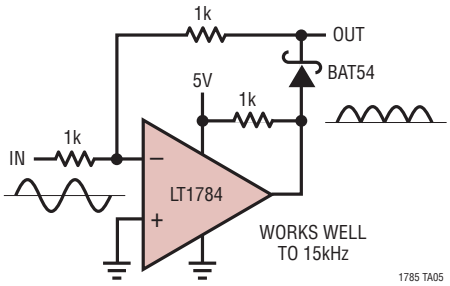
REVERSE BATTERY | INPUT OVERVOLTAGE | INPUT DIFFERENTIAL VOLTAGE | INPUTS BELOW GROUND

Simple Peak Detector

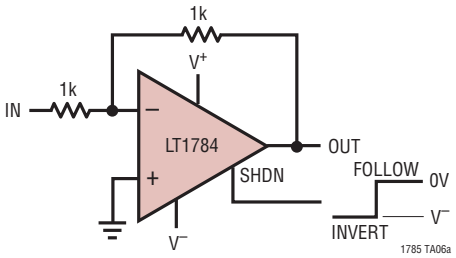


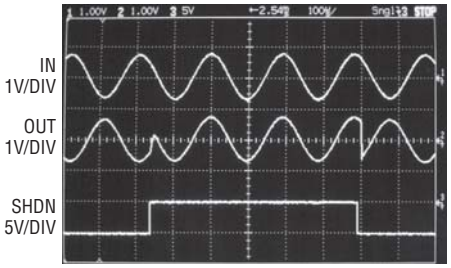
ACCURACY	BANDWIDTH
98%	3kHz TO 5.7kHz
90%	116Hz TO 47kHz
3dB	34Hz TO 96kHz

Simple Supply Full Wave Rectifier



Simple Polarity Selector





VS = ±5V 100µs/DIV
VIN = 3VP-P AT 5kHz

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1782	Micropower Over-The-Top Rail-to-Rail In/Out Op Amp in SOT-23	55µA Max Supply Current, 800µV Max Offset Voltage
LT1783	1.25MHz Over-The-Top Rail-to-Rail In/Out Op Amp in SOT-23	300µA Max Supply Current, 800µV Max Offset Voltage
LT1797	10MHz Rail-to-Rail In/Out Op Amp in SOT-23	Unity-Gain Stable, 2.25µV/µs Slew Rate
LT1637	1.1MHz Over-The-Top Rail-to-Rail In/Out Op Amp	Micropower, 0.4V/µs Slew Rate
LT1638/LT1639	Dual/Quad 1.2MHz Over-The-Top Rail-to-Rail In/Out Op Amp	Micropower 230µA Max, 0.4V/µs Slew Rate
LT1880	SOT-23 Pico Amp Input, Precision, Rail-to-Rail Output Op Amp	150µV Offset, 900pA Bias Current

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