FAIRCHILD SEMICONDUCTOR®

December 2012

LM336Z25
Programmable Shunt Regulator

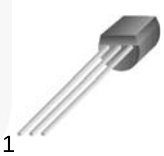
Features

- Low-Temperature Coefficient
- Guaranteed Temperature Stability: 4 mV (Typical)
- 0.2 Ω Dynamic Impedance
- 1.0% Initial Tolerance Available
- Easily Trimmed for Minimum Temperature Drift

Description

The LM336Z25 integrated circuit is a precision 2.5 V shunt regulator. The monolithic I_C voltage reference operates as a low temperature coefficient 2.5 V Zener with 0.2 Ω dynamic impedance. A third terminal on the LM336Z25 allows the reference voltage and temperature coefficient to be trimmed. LM336Z25 is useful as a precision 2.5 V low-voltage reference for digital voltmeters, power supplies, or OP-AMP circuitry. The 2.5 V makes it convenient to obtain a stable reference from low-voltage supplies. Further, since the LM336Z25 operates as a shunt regulator, it can be used as either a positive or negative voltage reference.

TO-92



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Ordering Information

Part Number	Operating Temperature Range	Top Mark	Package	Packing Method
LM336Z25	0 ~ +70°C	LM336Z25	TO-92	Bulk
LM336Z25X		LM336Z25	TO-92	Tape and Reel

Block Diagram

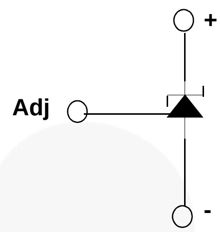


Figure1. Block Diagram

Schematic Diagram

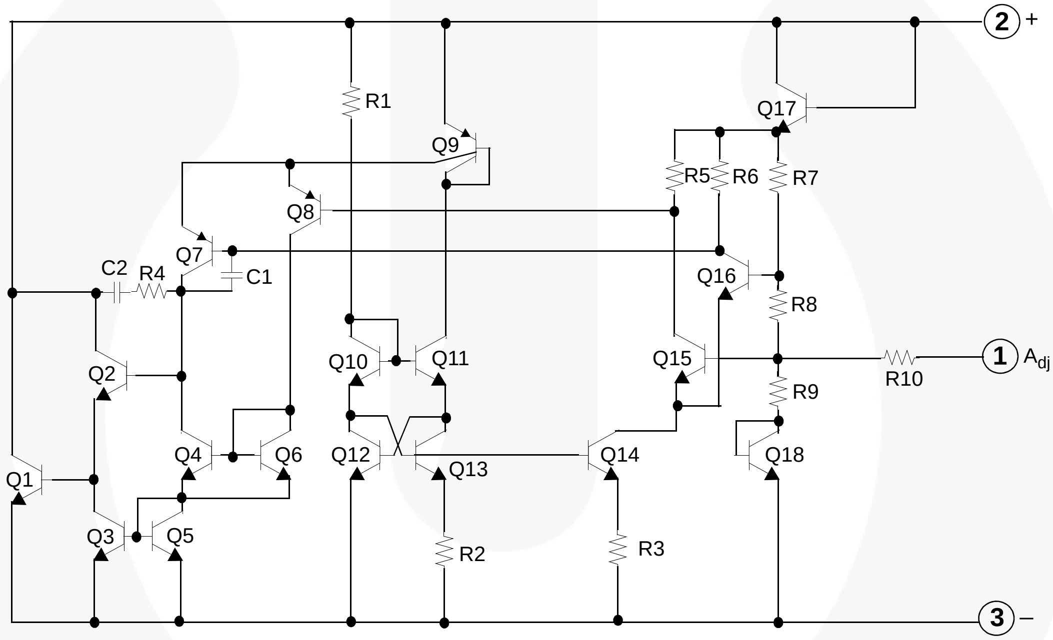


Figure 2. Schematic Diagram

Absolute Maximum Ratings[1]

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Value	Unit
I_R	Reverse Current	15	mA
I_F	Forward current	10	mA
T_{OPR}	Operating Temperature Range	0 ~ +70	°C
T_{STG}	Storage Temperature Range	-60 ~ +150	°C

Note:

1. The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating.

Electrical Characteristics

Values are at 0°C ≤ T_A ≤ +70°C unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_R	Reverse Breakdown Voltage	T_A = 25°C, I_R = 1 mA	2.44	2.49	2.54	V
$\Delta V_R / \Delta I_R$	Reverse Breakdown Change with Current	T_A = 25°C, 600µA ≤ I_R ≤ 10 mA		2.6	10.0	mV
Z_D	Reverse Dynamic Impedance	T_A = 25°C, I_R = 1 mA		0.2	1.0	Ω
ST_T	Temperature Stability	I_R = 1mA		1.8	6.0	mV
$\Delta V_R / \Delta I_R$	Reverse Breakdown Change with Current	600 µA ≤ I_R ≤ 10 mA		3.0	12.0	mV
Z_D	Reverse Dynamic Impedance	I_R = 1 mA		0.4	1.4	Ω
ST	Long Term Stability In Reference Voltage	I_R = 1 mA		20.0		ppm/ Khr

Typical Performance Characteristics

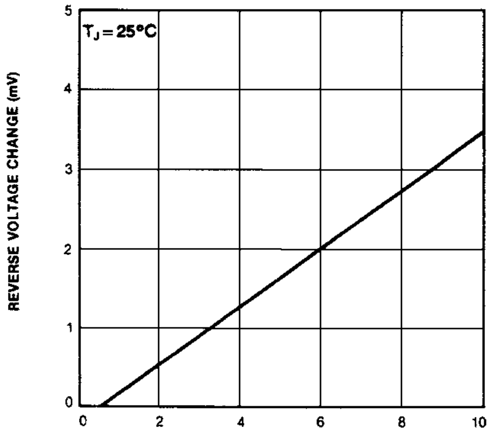


Figure 3. Reverse Voltage Change

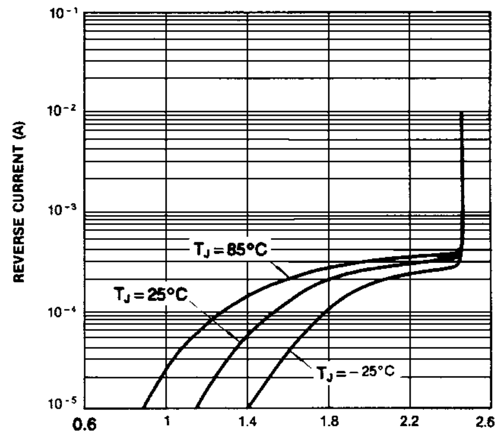


Figure 4. Reverse Characteristics

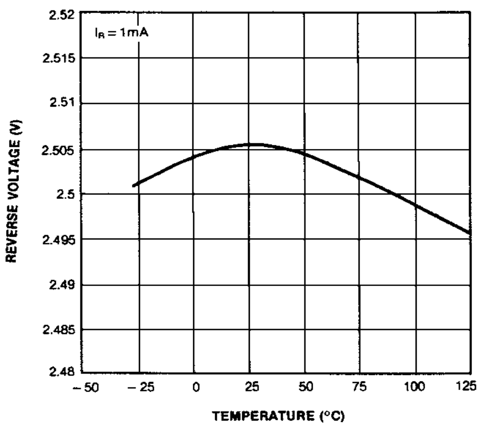


Figure 5. Temperature (°C)

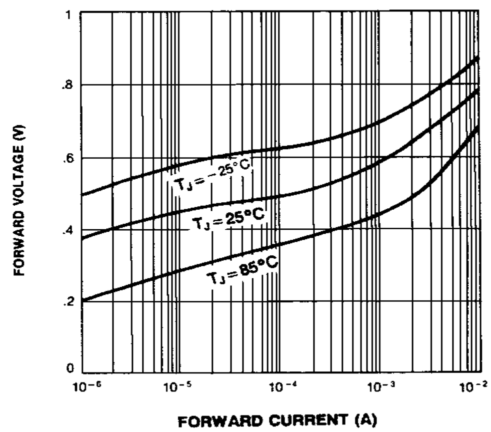
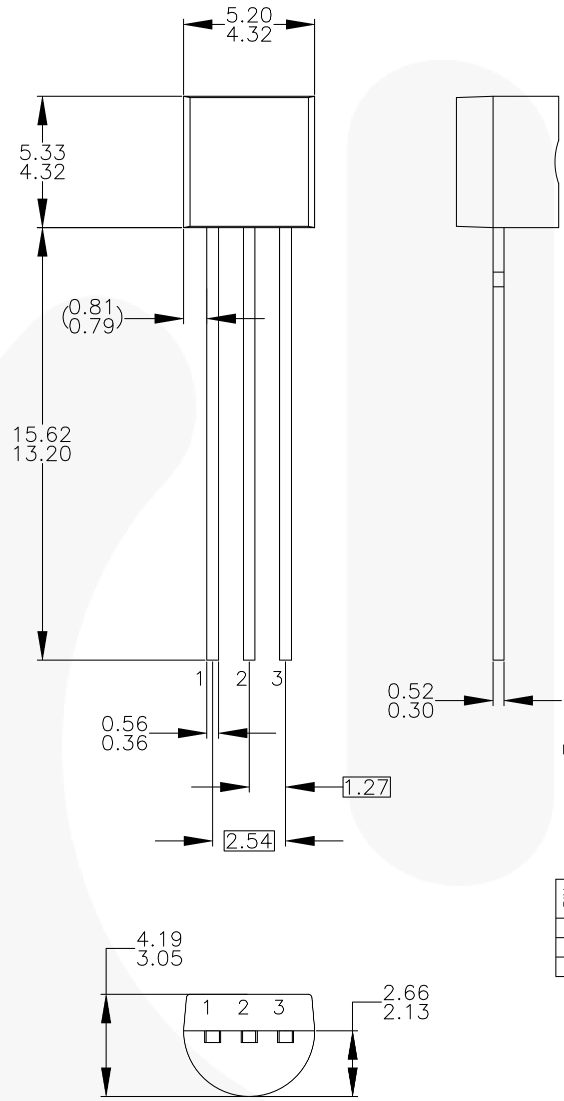


Figure 6. Forward Characteristics

Physical Dimensions

TO-92 Bulk Type



NOTES: UNLESS OTHERWISE SPECIFIED

A) DRAWING WITH REFERENCE TO JEDEC TO−92 RECOMMENDATIONS.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DRAWING CONFORMS TO ASME Y14.5M−1994.
D) TO−92 (92,94,96,97,98) PIN CONFIGURATION:

PIN	92			94			96			97			98		
	P	F	M	P	F	M	B	F	M	P	F	M	P	F	M
1	E	S	S	E	S	S	B	D	G	C	G	D	C	G	D
2	B	D	G	C	G	D	E	S	S	B	D	G	E	S	S
3	C	G	D	B	D	G	C	G	D	E	S	S	B	D	G

LEGEND:
P − BIPOLAR E − EMITTER D − DRAIN
F − JFET B − BASE S − SOURCE
M − DMOS C − COLLECTOR G − GATE

E) FOR PACKAGE 92, 94, 96, 97 AND 98: PIN CONFIGURATION DRAIN "D" AND SOURCE "S" ARE INTERCHANGEAGLE AT JFET "F" OPTION.
F) DRAWING FILENAME: MKT−ZA03DREV3.

Figure 17. 3-Lead, TO-92, Molded, Standard Straight Lead

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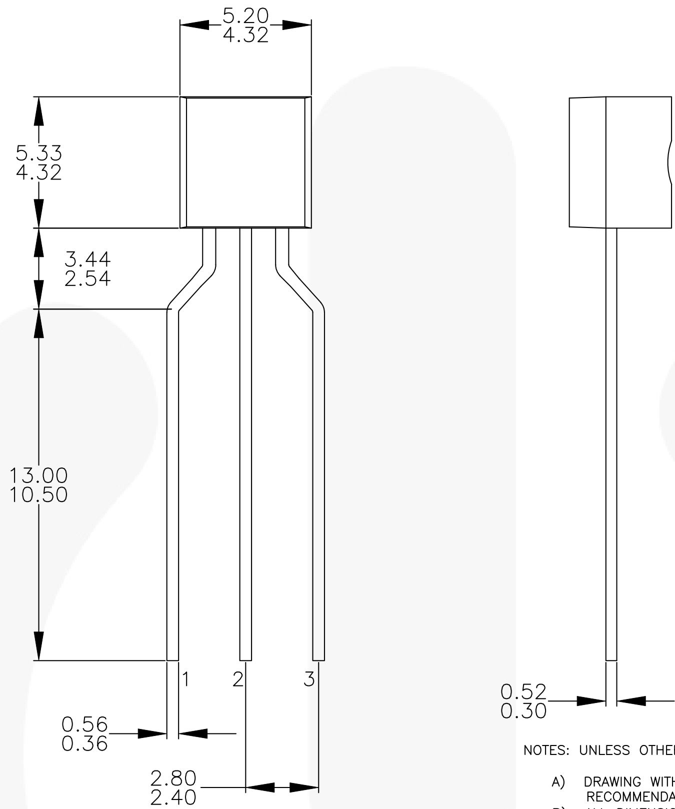
Physical Dimensions (Continued)

TO-92 Tape and Reel Type

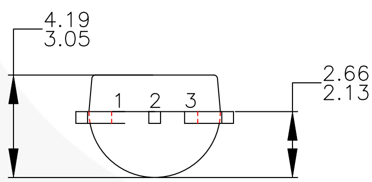


NOTES: UNLESS OTHERWISE SPECIFIED

A) DRAWING WITH REFERENCE TO JEDEC TO−92 RECOMMENDATIONS.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DRAWING CONFORMS TO ASME Y14.5M−1994.
D) TO−92 (92,94,96,97,98) PIN CONFIGURATION:

PIN	92			94			96			97			98		
	P	F	M	P	F	M	B	F	M	P	F	M	P	F	M
1	E	S	S	E	S	S	B	D	G	C	G	D	C	G	D
2	B	D	G	C	G	D	E	S	S	B	D	G	E	S	S
3	C	G	D	B	D	G	C	G	D	E	S	S	B	D	G

LEGEND:
P − BIPOLAR   E − EMITTER   D − DRAIN
F − JFET   B − BASE   S − SOURCE
M − DMOS   C − COLLECTOR   G − GATE



E) FOR PACKAGE 92, 94, 96, 97 AND 98:
PIN CONFIGURATION DRAIN "D" AND SOURCE "S"
ARE INTERCHANGEAGLE AT JFET "F" OPTION.
F) DRAWING FILENAME: MKT−ZA03FREV2.

Figure 18. 3-Lead, TO-92, Molded, 0.200 in Line Spacing Lead Form

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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