Order Information

Model Name	Order Number	Package	Transport Media, Quantity	Marking Information
LM2904	LM2904-SR	8-Pin SOP	Tape and Reel, 4,000	LM2904
	LM2904-VR	8-Pin MSOP	Tape and Reel, 3,000	LM2904
LM2902	LM2902-SR	14-Pin SOP	Tape and Reel, 2,500	LM2902
	LM2902-TR	14-Pin TSSOP	Tape and Reel, 3,000	LM2902

Absolute Maximum Ratings Note 1

Supply Voltage: $V^+ - V^-$ Note 2 ..... 42V
Input Voltage..... V^- – 0.3 to V^+ + 0.3
Input Current: +IN, –IN Note 3..... ±20mA
Differential Input Voltage..... ±42V
Output Short-Circuit Duration Note 4..... Infinite

Current at Supply Pins..... ±60mA
Operating Temperature Range.....–40°C to 125°C
Maximum Junction Temperature..... 150°C
Storage Temperature Range..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 260°C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The op amp supplies must be established simultaneously, with, or before, the application of any input signals.

Note 3: The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 500mV beyond the power supply, the input current should be limited to less than 10mA.

Note 4: A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	MIL-STD-883H Method 3015.8	2	kV
CDM	Charged Device Model ESD	JEDEC-EIA/JESD22-C101E	2	kV

Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Pin SOP	158	43	°C/W
8-Pin MSOP	210	45	°C/W
14-Pin SOP	120	36	°C/W
14-Pin TSSOP	180	35	°C/W

Electrical Characteristics

The specifications are at T_A = 27°C. V_S = 5V, V_{CM} = V_{OUT} =2.5V, R_L = 2kΩ, C_L =100pF, unless otherwise noted.

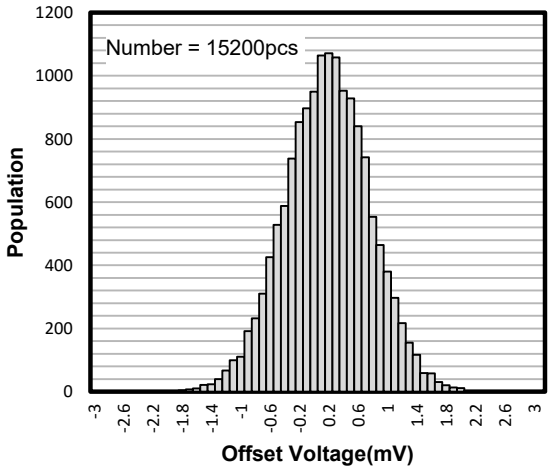
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_S = 5 V, V_{CM} = 2.5V and V_{CM} = 0V	-3	±1	3	mV
		V_S = 30 V, V_{CM} = 15V and V_{CM} = 0V	-3	±1	3	mV
V_{OS} TC	Input Offset Voltage Drift	-40°C to 125°C		1		μV/°C
I_B	Input Bias Current	T_A = 27 °C		60		pA
		T_A = 85 °C		200		pA
I_{OS}	Input Offset Current			0.001		pA
V_n	Input Voltage Noise	f = 0.1Hz to 10Hz		10		μV_{PP}
e_n	Input Voltage Noise Density	f = 1kHz		48		nV/√Hz
i_n	Input Current Noise	f = 1kHz		2		fA/√Hz
C_{IN}	Input Capacitance	Differential Common Mode		2.5 5		pF
CMRR	Common Mode Rejection Ratio	DC, V_S = 30V, V_{CM} = 0V to 28V	80	120		dB
V_{CM}	Common-mode Input Voltage Range	V_S = 5 V to 30V	V^-		V^+-2	V
PSRR	Power Supply Rejection Ratio	V_S = 5 V to 30V	90	120		dB
A_{VOL}	Open-Loop Large Signal Gain	V_S = 15 V, V_O = 1 V to 11 V, R_L = 2 kΩ	98	110		dB
V_{OH}	Output Swing from Supply Rail	R_{LOAD} = 10kΩ, V_S = ±15 V	14.70	14.75		V
		R_{LOAD} = 2kΩ, V_S = ±15 V	13.70	13.90		V
V_{OL}	Output Swing from Supply Rail	R_{LOAD} = 10kΩ , V_S = ±15 V		-14.85	-14.70	V
		R_{LOAD} = 2kΩ, V_S = ±15 V		-14.25	-14.10	V
		R_{LOAD} ≥ 10 kΩ, V_S = 15 V		5		mV
R_{OUT}	Closed-Loop Output Impedance	A_V = 1, f =1kHz, I_{OUT} = 0		0.002		Ω
R_O	Open-Loop Output Impedance	f = 1kHz, I_{OUT} = 0		120		Ω
I_{SC}	Output Short-Circuit Current	Sink or source current, V_S = 30V	20	35		mA
V_S	Supply Voltage		3		36	V
I_Q	Quiescent Current per Amplifier	V_S = 5V, No load		100	150	μA
		V_S = 30V, No load		110	200	μA
PM	Phase Margin	R_{LOAD} = 1kΩ, C_{LOAD} = 100pF		62		°
GM	Gain Margin	R_{LOAD} = 1kΩ, C_{LOAD} = 60pF		18		dB
GBWP	Gain-Bandwidth Product	f = 1kHz		1.2		MHz
SR	Slew Rate at unity gain	A_V = 1, V_S = ±15V, V_{OUT} = -10V to 10V, C_{LOAD} =60pF, R_{LOAD} = 10kΩ		0.55		V/μs
FPBW	Full Power Bandwidth Note 1			17.5		kHz
t_S	Settling Time, 0.1% Settling Time, 0.01%	A_V = -1, V_{OUT} = 1V Step		2.8 3.1		μs
THD+N	Total Harmonic Distortion and Noise	f = 1kHz, A_V =1, R_L = 2kΩ, V_{OUT} = 1Vp-p		0.001		%
X_{talk}	Channel Separation	f = 1 kHz to 20 kHz		80		dB

Note 1: Full power bandwidth is calculated from the slew rate FPBW = SR/π • V_{P-P}

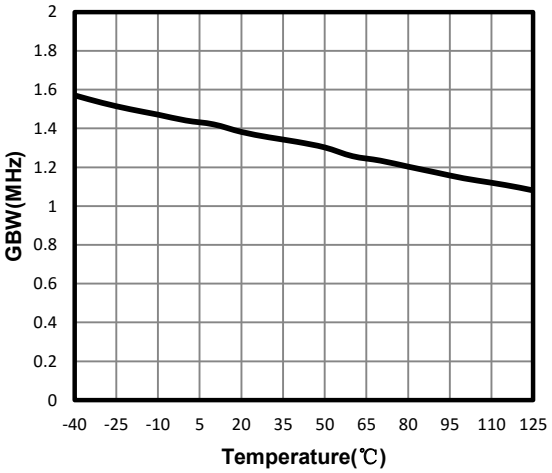
Typical Performance Characteristics

V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified.

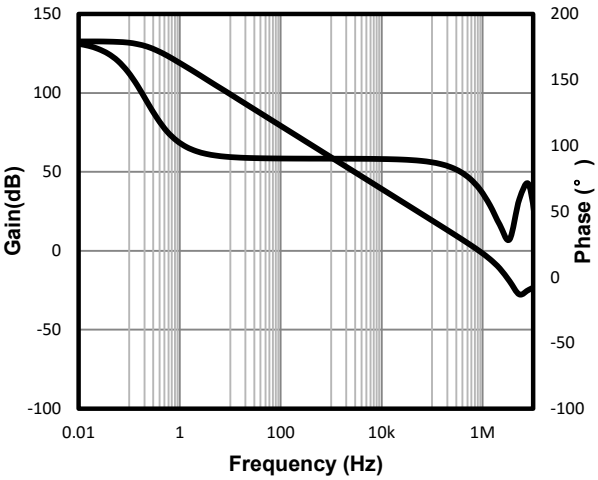
Offset Voltage Production Distribution



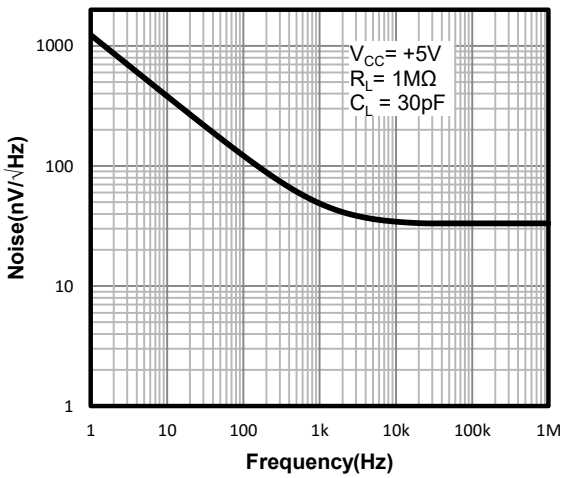
Unity Gain Bandwidth vs. Temperature



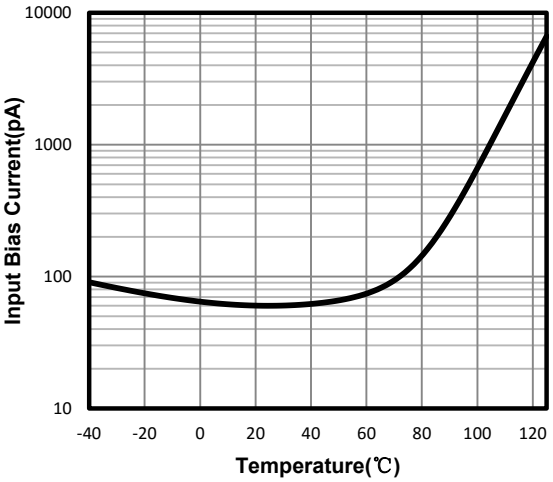
Open-Loop Gain and Phase



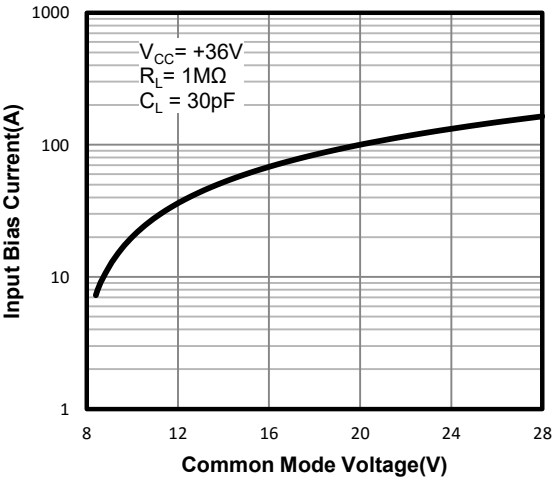
Input Voltage Noise Spectral Density



Input Bias Current vs. Temperature



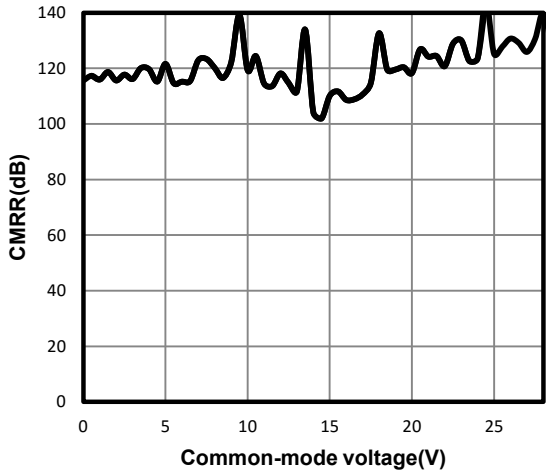
Input Bias Current vs. Input Common Mode Voltage



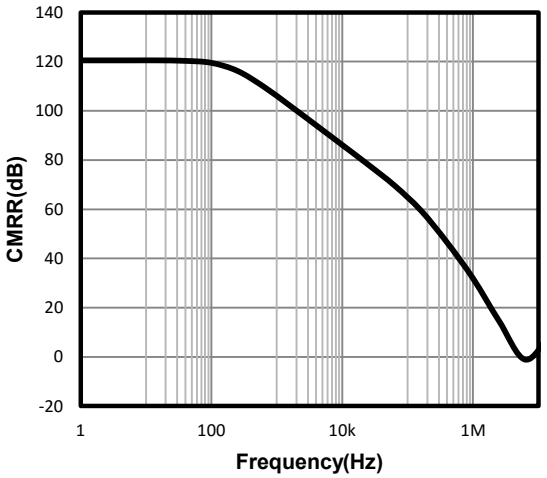
Typical Performance Characteristics

V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. (Continued)

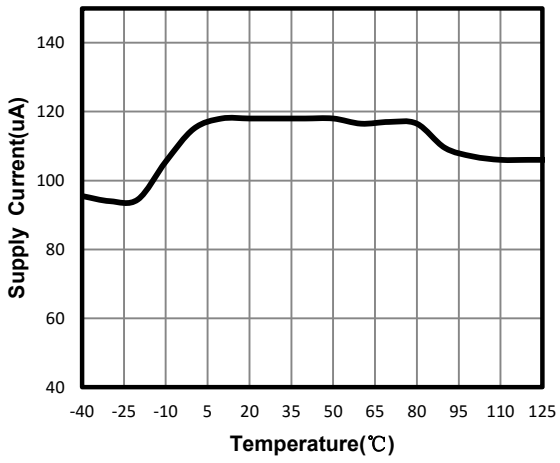
Common Mode Rejection Ratio



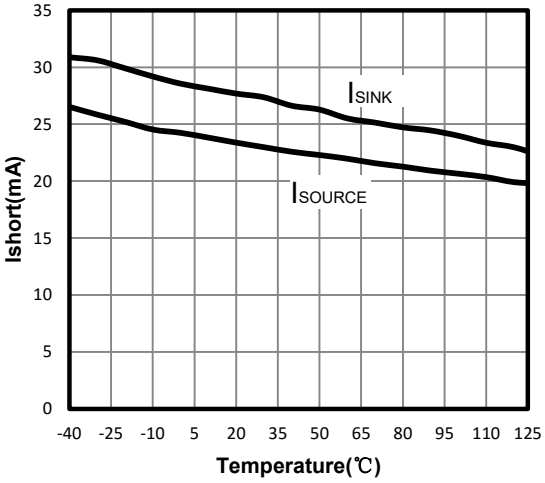
CMRR vs. Frequency



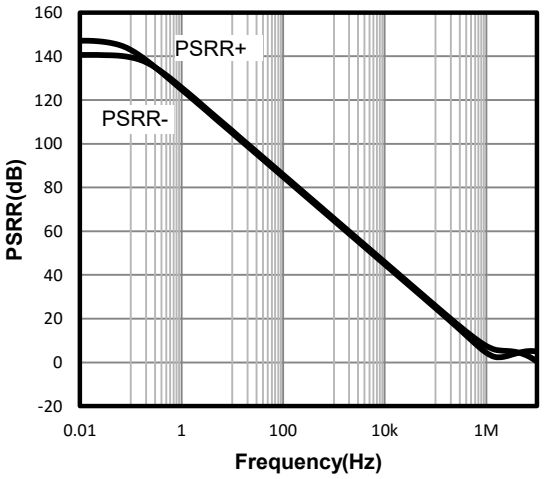
Quiescent Current vs. Temperature



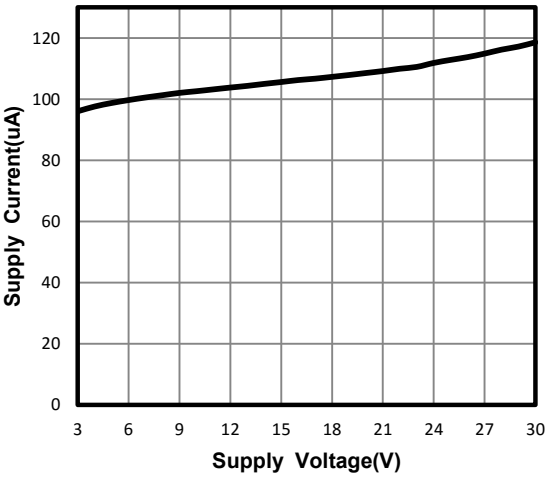
Short Circuit Current vs. Temperature



Power-Supply Rejection Ratio



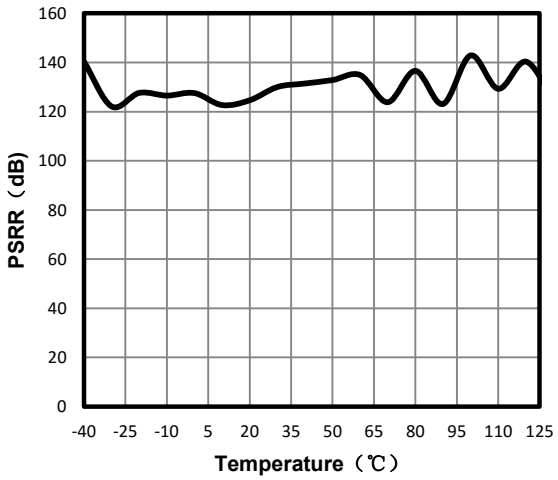
Quiescent Current vs. Supply Voltage



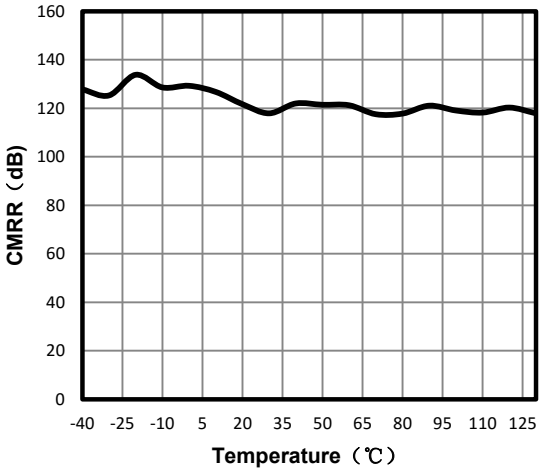
Typical Performance Characteristics

V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. (Continued)

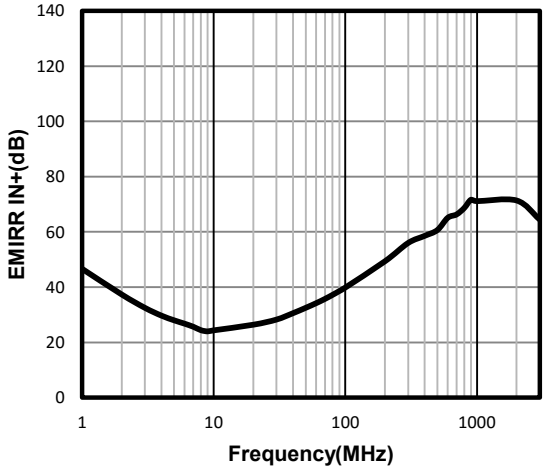
Power-Supply Rejection Ratio vs. Temperature



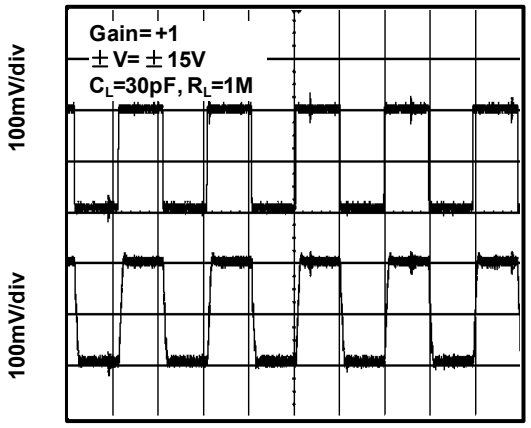
CMRR vs. Temperature



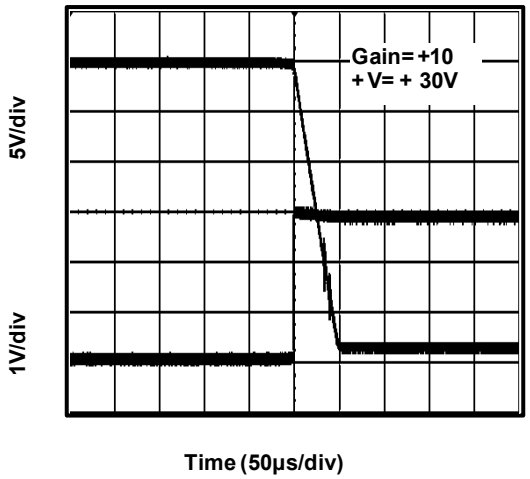
EMIRR IN+ vs. Frequency



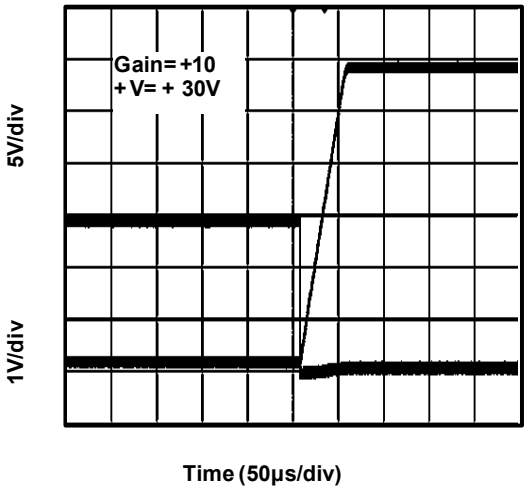
Small-Scale Step Response



Negative Over-Voltage Recovery



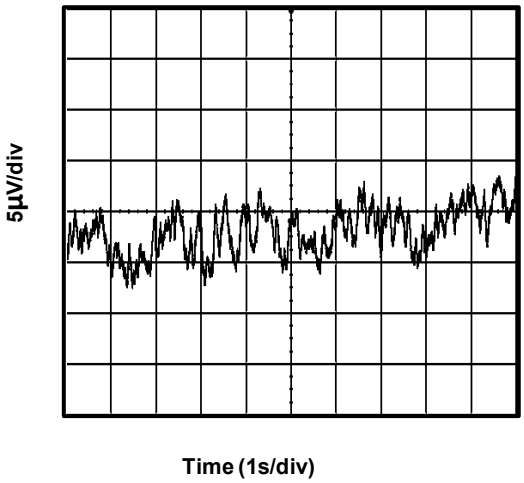
Positive Over-Voltage Recovery



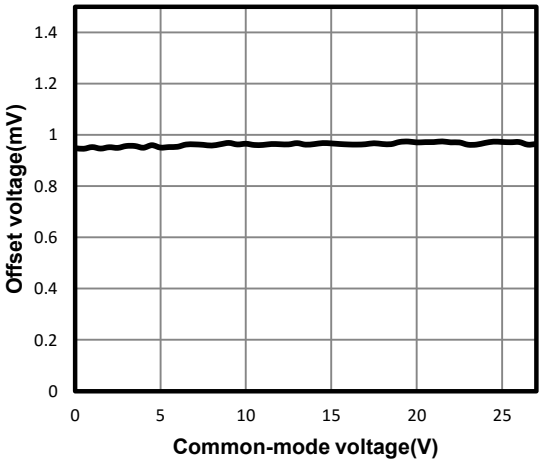
Typical Performance Characteristics

V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. (Continued)

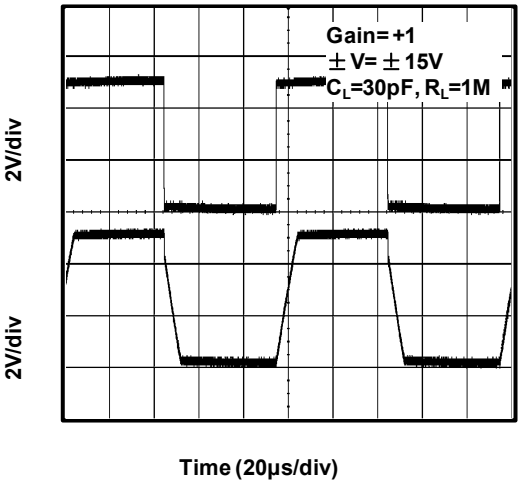
0.1 Hz TO 10 Hz Input Voltage Noise



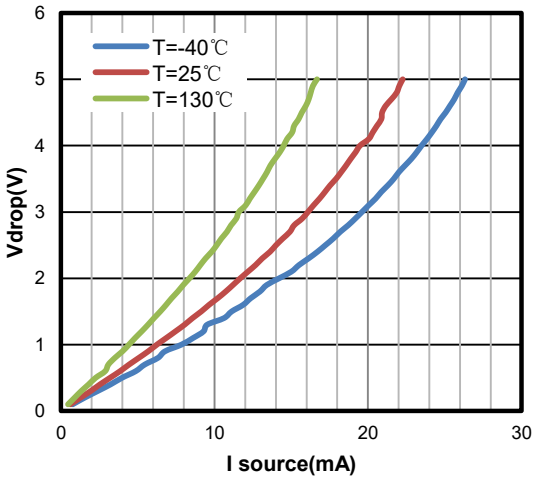
Offset Voltage vs Common-Mode Voltage



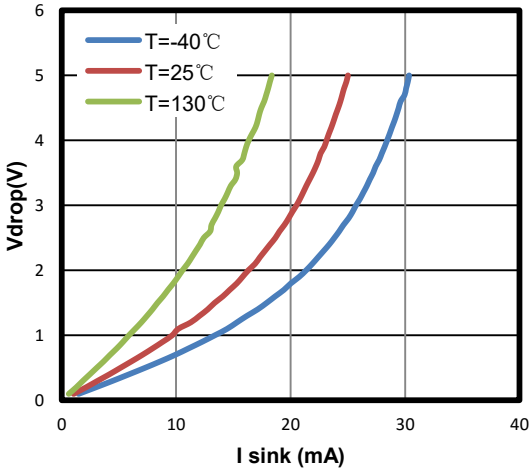
Large-Scale Step Response



Positive Output Swing vs. Load Current



Negative Output Swing vs. Load Current



Pin Functions

-IN: Inverting Input of the Amplifier.

+IN: Non-Inverting Input of Amplifier.

OUT: Amplifier Output. The voltage range extends to within mV of each supply rail.

V+ or +V_S: Positive Power Supply. Typically the voltage is from 3V to 36V. Split supplies are possible as long as the voltage between V+ and V– is between 3V and 36V. A bypass capacitor of 0.1μF as close to the part as possible should be used between power supply pins or between supply pins and ground.

V- or -V_S: Negative Power Supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between V_+ and $V_–$ is from 3V to 36V. If it is not connected to ground, bypass it with a capacitor of 0.1μF as close to the part as possible.

Operation

The LM2904/2902 input signal range extends beyond the negative and positive power supplies. The output can even extend all the way to the negative supply. The input stage is comprised of two CMOS differential amplifiers, a PMOS stage and NMOS stage that are active over different ranges of common mode input voltage. The Class-AB control buffer and output bias stage uses a proprietary compensation technique to take full advantage of the process technology to drive very high capacitive loads. This is evident from the transient over shoot measurement plots in the Typical Performance Characteristics.

Applications Information

High Supply Voltage and Low Power Consumption

The LM2904/2902 of operational amplifiers can operate with power supply voltages from 3V to 36V. Each amplifier draws only 100μA quiescent current. The low supply voltage capability and low supply current are ideal for portable applications demanding HIGH CAPACITIVE LOAD DRIVING CAPABILITY and WIDE BANDWIDTH. The LM2904/2902 is optimized for wide bandwidth low power applications. They have an industry leading high GBWP to power ratio and are unity gain stable for 10nf CAPACITIVE load. When the load capacitance increases, the increased capacitance at the output pushed the non-dominant pole to lower frequency in the open loop frequency response, lowering the phase and gain margin. Higher gain configurations tend to have better capacitive drive capability than lower gain configurations due to lower closed loop bandwidth and hence higher phase margin.

Low Input Referred Noise

The LM2904/2902 provides a low input referred noise density of 48nV/ √Hz at 1kHz. The voltage noise will grow slowly with the frequency in wideband range, and the input voltage noise is typically 10μV_{P-P} at the frequency of 0.1Hz to 10Hz.

Low Input Offset Voltage

The LM2904/2902 has a low offset voltage tolerance of 3mV maximum which is essential for precision applications. The offset voltage is trimmed with a proprietary trim algorithm to ensure low offset voltage for precision signal processing requirement.

Low Input Bias Current

The LM2904/2902 is a CMOS OPA family and features very low input bias current in pA range. The low input bias current allows the amplifiers to be used in applications with high resistance sources. Care must be taken to minimize PCB Surface Leakage. See below section on “PCB Surface Leakage” for more details.

PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5pA of current to flow, which is greater than the LM2904/2902 OPA's input bias current at +27°C (±1pA, typical). It is recommended to use multi-layer PCB layout and route the OPA's -IN and +IN signal under the PCB surface.

The effective way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 1 for Inverting Gain application.

1. For Non-Inverting Gain and Unity-Gain Buffer:
   a) Connect the non-inverting pin (V_{IN}+) to the input with a wire that does not touch the PCB surface.
   b) Connect the guard ring to the inverting input pin (V_{IN}–). This biases the guard ring to the Common Mode input voltage.
2. For Inverting Gain and Trans-impedance Gain Amplifiers (convert current to voltage, such as photo detectors):
   a) Connect the guard ring to the non-inverting input pin (V_{IN}+). This biases the guard ring to the same reference voltage as the op-amp (e.g., V_{DD}/2 or ground).
   b) Connect the inverting pin (V_{IN}–) to the input with a wire that does not touch the PCB surface.

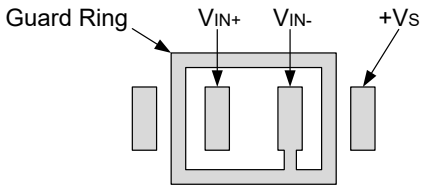


Figure 1

Ground Sensing and Rail to Rail Output

The LM2904/2902 has excellent output drive capability, delivering over 35mA of output drive current. The output stage is a rail-to-rail topology that is capable of swinging to within 5mV of either rail. Since the inputs can go 100mV beyond either rail, the op-amp can easily perform 'True Ground Sensing'.

The maximum output current is a function of total supply voltage. As the supply voltage to the amplifier increases, the output current capability also increases. Attention must be paid to keep the junction temperature of the IC below 150°C when the output is in continuous short-circuit. The output of the amplifier has reverse-biased ESD diodes connected to each supply. The output should not be forced more than 0.5V beyond either supply, otherwise current will flow through these diodes.

ESD

The LM2904/2902 has reverse-biased ESD protection diodes on all inputs and output. Input and out pins cannot be biased more than 200mV beyond either supply rail.

Feedback Components and Suppression of Ringing

Care should be taken to ensure that the pole formed by the feedback resistors and the parasitic capacitance at the inverting input does not degrade stability. For example, in a gain of +2 configuration with gain and feedback resistors of 10k, a poorly designed circuit board layout with parasitic capacitance of 5pF (part +PC board) at the amplifier's inverting input will cause the amplifier to ring due to a pole formed at 1.2MHz. An additional capacitor of 5pF across the feedback resistor as shown in Figure 2 will eliminate any ringing.

Careful layout is extremely important because low power signal conditioning applications demand high-impedance circuits. The layout should also minimize stray capacitance at the OPA's inputs. However some stray capacitance may be unavoidable and it may be necessary to add a 2pF to 10pF capacitor across the feedback resistor. Select the smallest capacitor value that ensures stability.

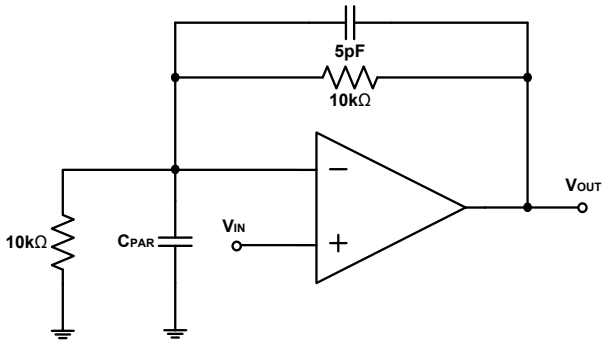


Figure 2

Driving Large Capacitive Load

The LM2904/2902 of OPA is designed to drive large capacitive loads. Refer to Typical Performance Characteristics for "Phase Margin vs. Load Capacitance". As always, larger load capacitance decreases overall phase margin in a feedback system where internal frequency compensation is utilized. As the load capacitance increases, the feedback loop's phase margin decreases, and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in output step response. The unity-gain buffer (G = +1V/V) is the most sensitive to large capacitive loads.

When driving large capacitive loads with the LM2904/2902 (e.g., > 200 pF when G = +1V/V), a small series resistor at the output (R_{ISO} in Figure 3) improves the feedback loop's phase margin and stability by making the output load resistive at higher frequencies.

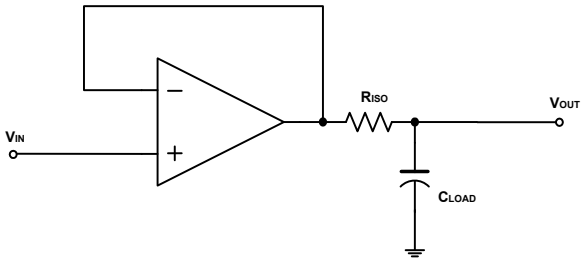


Figure 3

Power Supply Layout and Bypass

The LM2904/2902 OPA's power supply pin (V_{DD} for single-supply) should have a local bypass capacitor (i.e., 0.01μF to 0.1μF) within 2mm for good high frequency performance. It can also use a bulk capacitor (i.e., 1μF or larger) within 100mm to provide large, slow currents. This bulk capacitor can be shared with other analog parts.

Ground layout improves performance by decreasing the amount of stray capacitance and noise at the OPA's inputs and outputs. To decrease stray capacitance, minimize PC board lengths and resistor leads, and place external components as close to the op amps' pins as possible.

Proper Board Layout

To ensure optimum performance at the PCB level, care must be taken in the design of the board layout. To avoid leakage currents, the surface of the board should be kept clean and free of moisture. Coating the surface creates a barrier to moisture accumulation and helps reduce parasitic resistance on the board.

Keeping supply traces short and properly bypassing the power supplies minimizes power supply disturbances due to output current variation, such as when driving an ac signal into a heavy load. Bypass capacitors should be connected as closely as possible to the device supply pins. Stray capacitances are a concern at the outputs and the inputs of the amplifier. It is recommended that signal traces be kept at least 5mm from supply lines to minimize coupling.

A variation in temperature across the PCB can cause a mismatch in the Seebeck voltages at solder joints and other points where dissimilar metals are in contact, resulting in thermal voltage errors. To minimize these thermocouple effects, orient resistors so heat sources warm both ends equally. Input signal paths should contain matching numbers

and types of components, where possible to match the number and type of thermocouple junctions. For example, dummy components such as zero value resistors can be used to match real resistors in the opposite input path. Matching components should be located in close proximity and should be oriented in the same manner. Ensure leads are of equal length so that thermal conduction is in equilibrium. Keep heat sources on the PCB as far away from amplifier input circuitry as is practical.

The use of a ground plane is highly recommended. A ground plane reduces EMI noise and also helps to maintain a constant temperature across the circuit board.

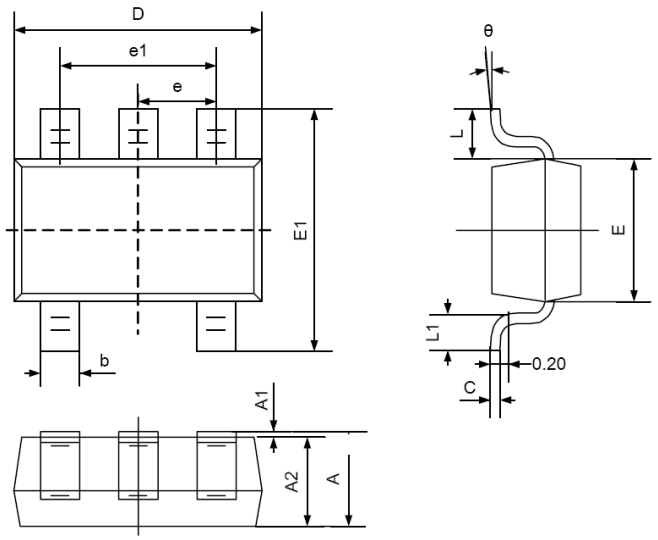
Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

Revision	Change
Rev. A	Initial Release

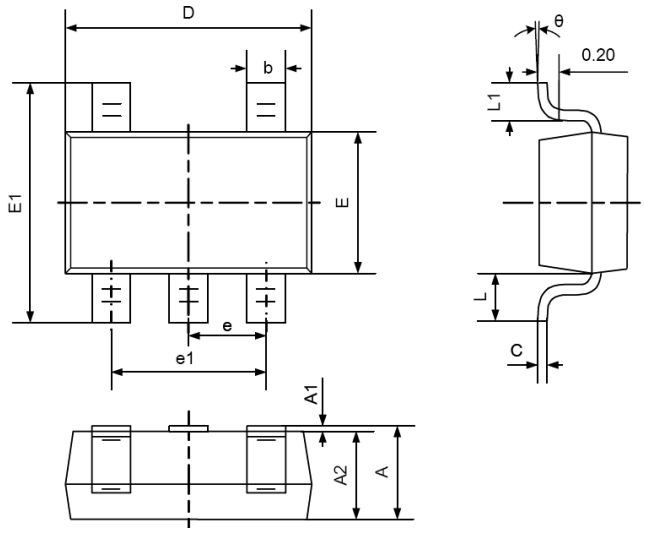
Package Outline Dimensions

SC70-5 /SOT-353



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.150	0.350	0.006	0.014
C	0.080	0.150	0.003	0.006
D	2.000	2.200	0.079	0.087
E	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650TYP		0.026TYP	
e1	1.200	1.400	0.047	0.055
L	0.525REF		0.021REF	
L1	0.260	0.460	0.010	0.018
θ	0°	8°	0°	8°

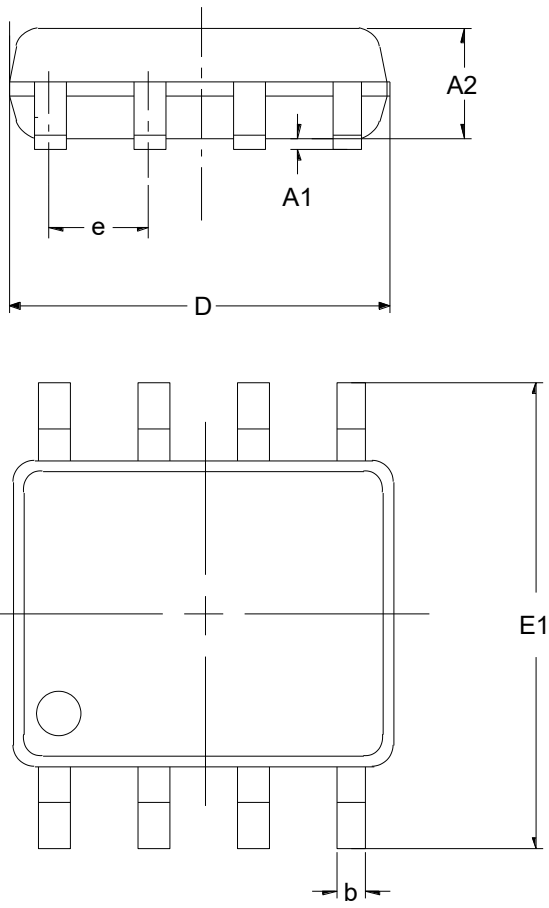
SOT23-5



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
C	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.460	0.012	0.024
θ	0°	8°	0°	8°

Package Outline Dimensions

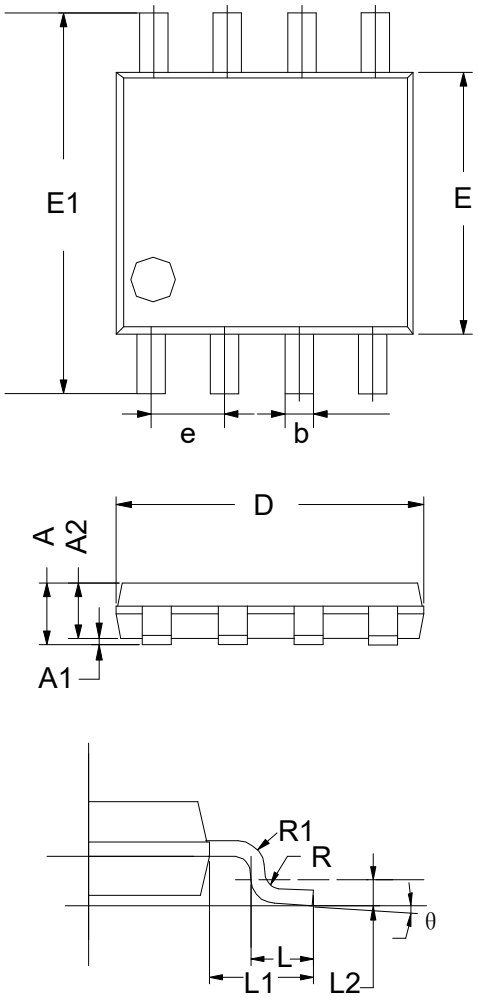
SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270 TYP		0.050 TYP	
L1	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package Outline Dimensions

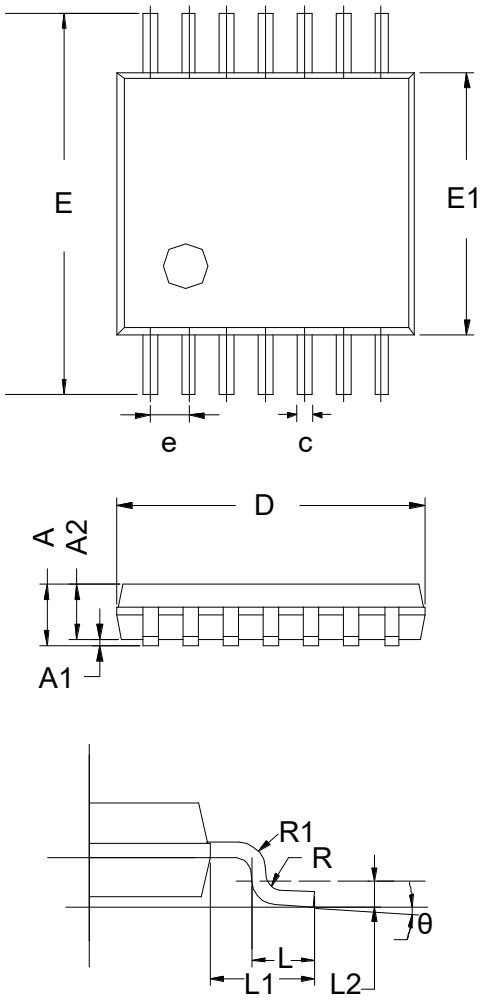
MSOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.200	0.031	0.047
A1	0.000	0.200	0.000	0.008
A2	0.760	0.970	0.030	0.038
b	0.30 TYP		0.012 TYP	
C	0.15 TYP		0.006 TYP	
D	2.900	3.100	0.114	0.122
e	0.65 TYP		0.026	
E	2.900	3.100	0.114	0.122
E1	4.700	5.100	0.185	0.201
L1	0.410	0.650	0.016	0.026
θ	0°	6°	0°	6°

Package Outline Dimensions

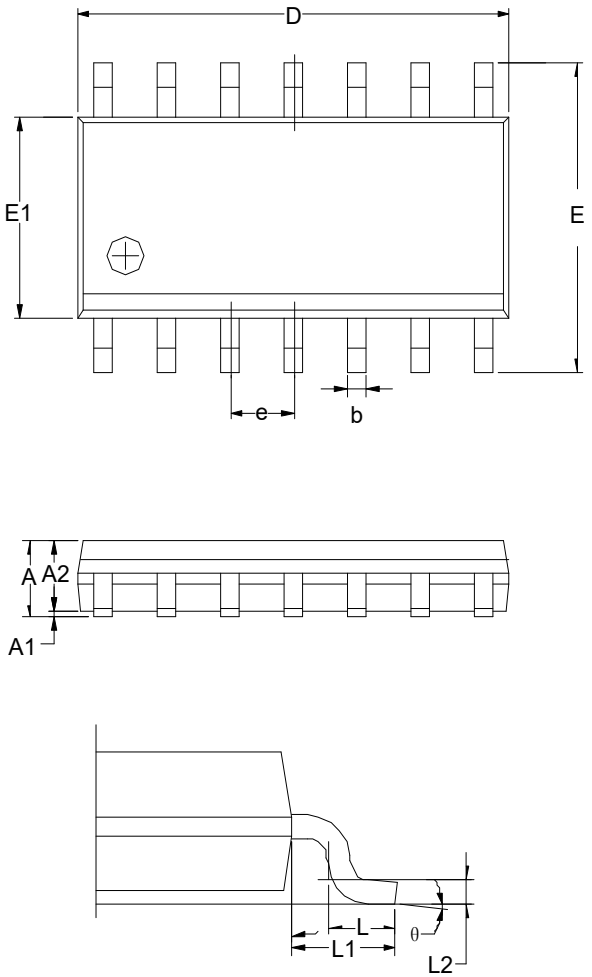
TSSOP-14



Symbol	Dimensions In Millimeters		
	MIN	TYP	MAX
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00	1.05
b	0.20	-	0.28
c	0.10	-	0.19
D	4.86	4.96	5.06
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
L2	0.25 BSC		
R	0.09	-	-
θ	0°	-	8°

Package Outline Dimensions

SOP-14



Symbol	Dimensions In Millimeters		
	MIN	TYP	MAX
A	1.35	1.60	1.75
A1	0.10	0.15	0.25
A2	1.25	1.45	1.65
b	0.36		0.49
D	8.53	8.63	8.73
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
L	0.45	0.60	0.80
L1	1.04 REF		
L2	0.25 BSC		
θ	0°		8°