Table 2. Pin Description

N°	Pin	Function
1 to 3	NC	Internally not connected
4	GND	0V supply
5	Vdd	Power supply
6	Vouty	Output Voltage
7	ST	Self Test (Logic 0: normal mode; Logic 1: Self-test)
8	Voutx	Output Voltage
9-13	NC	Internally not connected
14	PD	Power Down (Logic 0: normal mode; Logic 1: Power-Down mode)
15	Voutz	Output Voltage
16	FS	Full Scale selection (Logic 0: 2g Full-scale; Logic 1: 6g Full-scale)
17-18	Reserved	Leave unconnected
19	NC	Internally not connected
20	Reserved	Leave unconnected
21	NC	Internally not connected
22-23	Reserved	Leave unconnected
24-25	NC	Internally not connected
26	Reserved	Connect to Vdd or GND
27	Reserved	Leave unconnected or connect to Vdd
28	Reserved	Leave unconnected or connect to GND
29-44	NC	Internally not connected

Figure 3. Pin Connection (Top view)

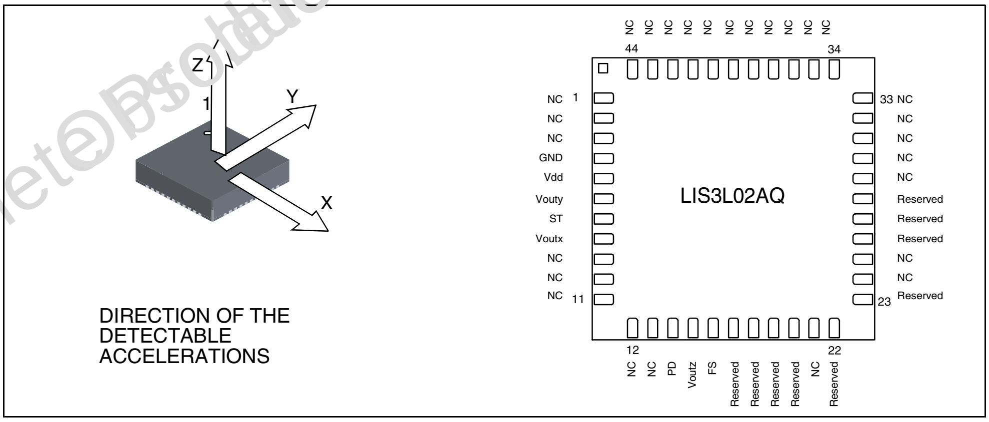

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Table 3. Electrical Characteristics

(Temperature range -40°C to +85°C) All the parameters are specified @ Vdd =3.3V, T=25°C unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Typ.[1]	Max.	Unit
Vdd	Supply voltage		2.4	3.3	3.6	V
Idd	Supply current	mean value PD pin connected to GND		0.85	1.5	mA
IddPdn	Supply current in Power Down Mode	rms value PD pin connected to Vdd		2	5	µA
Voff	Zero-g level[2]	T = 25°C	Vdd/2-10%	Vdd/2	Vdd/2+10%	V
OffDr	Zero-g level Vs temperature	Delta from +25°C		±1.5		mg/°C
Ar	Acceleration range[3]	FS pin connected to GND	±1.8	±2.0		g
		FS pin connected to Vdd	±5.4	±6.0		g
So	Sensitivity[2]	Full-scale = 2g	Vdd/5–10%	Vdd/5	Vdd/5+10%	V/g
		Full-scale = 6g	Vdd/15–10%	Vdd/15	Vdd/15+10%	V/g
SoDr	Sensitivity drift Vs temperature	Delta from +25°C		±0.01		%/°C
NL	Non Linearity[4]	Best fit straight line Full-scale = 2g X, Y axis		±0.3	±1.5	% FS
		Best fit straight line; Full-scale = 2g Z axis		±0.6	±2	% FS
CrossAx	Cross-Axis[5]			±2	±4	%
fuc	Sensing Element Resonant Frequency[6]	X, Y axis	3.2	4.0	4.8	KHz
		Z axis	1.8	2.5	3.2	KHz
an	Acceleration noise density	Vdd=3.3V; Full-scale = 2g		50		$\mu g/\sqrt{Hz}$
Vt	Self test output voltage delta change[7,8,9]	T = 25°C Vdd=3.3V Full-scale = 2g X axis	-20	-40		mV
		T = 25°C Vdd=3.3V Full-scale = 2g Y axis	20	40		mV
		T = 25°C Vdd=3.3V Full-scale = 2g Z axis	20	50		mV

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Table 3. Electrical Characteristics (continued)
(Temperature range -40°C to +85°C) All the parameters are specified @ Vdd =3.3V, T=25°C unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Typ.[1]	Max.	Unit
Vst	Self test input	Logic 0 level	0		0.8	V
		Logic 1 level	2.2		Vdd	V
Rout	Output impedance		80	110	140	kΩ
Cload	Capacitive load drive[10]		320			pF
Ton	Turn-On Time at exit from Power Down mode	Cload in µF		550*Cload +0.3		ms

Notes: 1. Typical specifications are not guaranteed
2. Offset and sensitivity are essentially ratiometric to supply voltage
3. Guaranteed by wafer level test and measurement of initial offset and sensitivity
4. Guaranteed by design through measurements done up to 1g
5. Contribution to the measuring output of the inclination/acceleration along the perpendicular axis
6. Guaranteed by design
7. Self test "output voltage delta change" is defined as $Vout_{(Vst=Logic1)}-Vout_{(Vst=Logic0)}$
8. Self test "output voltage delta change" varies cubically with supply voltage
9. When full-scale is set to 6g, self-test "output delta change" is one third of the specified value
10. Bandwidth=1/(2*π*110KΩ*Cload)

ABSOLUTE MAXIMUM RATING

Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 4. Absolute Maximum Rating

Symbol	Ratings	Maximum Value	Unit
Vdd	Supply voltage	-0.3 to 7	V
Vin	Input voltage on any control pin (FS, PD, ST)	-0.3 to Vdd +0.3	V
A_{POW}	Acceleration (Any axis, Powered, Vdd=3.3V)	3000g for 0.5 ms	
		10000g for 0.1 ms	
A_{UNP}	Acceleration (Any axis, Unpowered)	3000g for 0.5 ms	
		10000g for 0.1 ms	
T_{OP}	Operating Temperature Range	-40 to +85	°C
T_{STG}	Storage Temperature Range	-40 to +105	°C
ESD	Electrostatic discharge protection	2KV HBM	

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3 FUNCTIONALITY

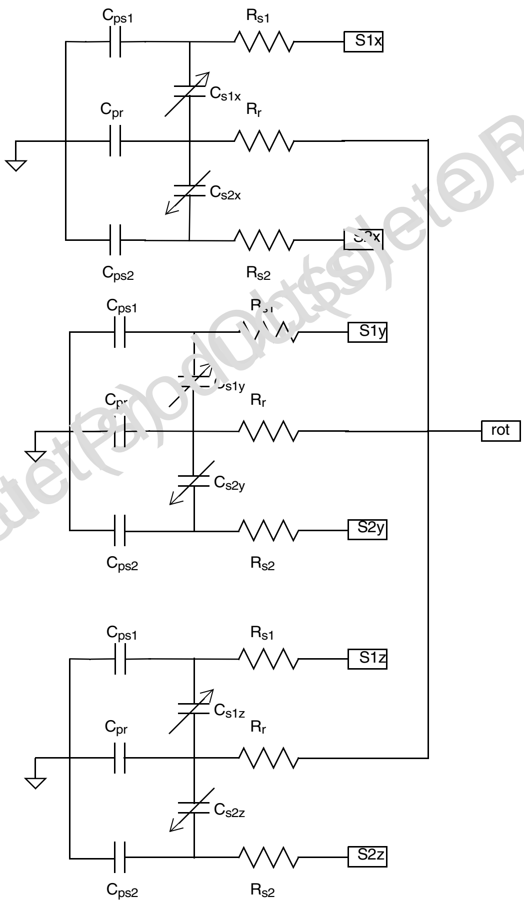
The LIS3L02AQ is a low-cost, low-power, analog output three-axis linear accelerometer packaged in QFN package. The complete device includes a sensing element and an IC interface able to take the information from the sensing element and to provide an analog signal to the external world.

3.1 Sensing element

The THELMA process is utilized to create a surface micro-machined accelerometer. The technology allows to carry out suspended silicon structures which are attached to the substrate in a few points called anchors and free to move on a plane parallel to the substrate itself. To be compatible with the traditional packaging techniques a cap is placed on top of the sensing element to avoid blocking the moving parts during the molding phase.

The equivalent circuit for the sensing element is shown in the figure below; when a linear acceleration is applied, the proof mass displaces from its nominal position, causing an imbalance in the capacitive half-bridge. This imbalance is measured using charge integration in response to a voltage pulse applied to the sense capacitor.

Figure 4. Equivalent electrical circuit



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The nominal value of the capacitors, at steady state, is few pF and when an acceleration is applied the maximum variation of the capacitive load is few hundredths of pF.

3.2 IC Interface

The complete signal processing uses a fully differential structure, while the final stage converts the differential signal into a single-ended one to be compatible with the external world.

The first stage is a low-noise capacitive amplifier that implements a Correlated Double Sampling (CDS) at its output to cancel the offset and the 1/f noise. The produced signal is then sent to three different S&Hs, one for each channel, and made available to the outside.

The low noise input amplifier operates at 200 kHz while the three S&Hs operate at a sampling frequency of 66 kHz. This allows a large oversampling ratio, which leads to in-band noise reduction and to an accurate output waveform.

All the analog parameters (output offset voltage and sensitivity) are ratiometric to the voltage supply. Increasing or decreasing the voltage supply, the sensitivity and the offset will increase or decrease linearly. The feature provides the cancellation of the error related to the voltage supply along an analog to digital conversion chain.

3.3 Factory calibration

The IC interface is factory calibrated to provide to the final user a device ready to operate.

The trimming values are stored inside the device by a non volatile structure. Any time the device is turned on, the trimming parameters are downloaded into the registers to be employed during the normal operation thus allowing the final user to employ the device without any need for further calibration.

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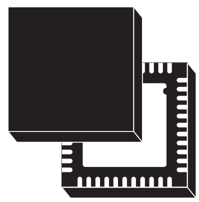
4 PACKAGE INFORMATION

Figure 5. QFN-44 Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	1.70	1.80	1.90	0.067	0.071	0.075
A1	0.19		0.21	0.007		0.008
b	0.20	0.25	0.30	0.008	0.01	0.012
D		7.0			0.276	
E		7.0			0.276	
e		0.50			0.020	
J	5.04		5.24	0.198		0.206
K	5.04		5.24	0.198		0.206
L	0.38	0.48	0.58	0.015	0.019	0.023
P		45 REF			45 REF	

OUTLINE AND MECHANICAL DATA



QFN-44 (7x7x1.8mm)
Quad **F**lat **P**ackage **N**o lead

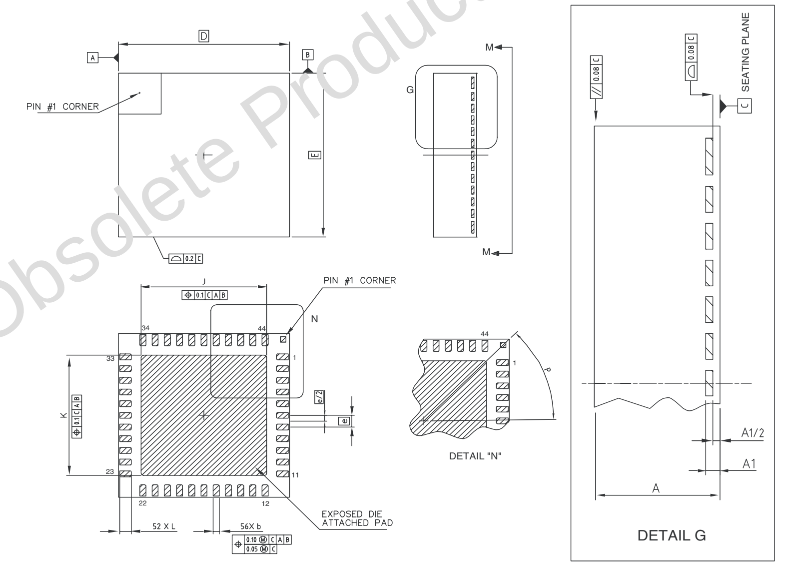


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Table 5. Revision History

Date	Revision	Description of Changes
January 2004	1	First Issue
February 2004	2	Values of some parameters has been changed in Electrical characteristics table.
November 2004	3	Modified/added some values in the table 2 Electrical characteristics.
November 2004	4	Corrected few typo errors.

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